18V Input, 40A Continuous, 45A Peak Output, Asynchronous Step-Down DC/DC Converter

FEATURES

- 4V to 18V Operating Input Range
- RM91500A：40A Continuous, 45A Peak Output Current
- Default Internal Voltage Reference：0.600V
- Default Frequency：600kHz
- Default Soft-start Time：2ms
- Power Good Indicator
- UVLO/OTP/OCP Protections
- RoHS Compliant and Halogen Free
- Compact Package: LGA5×6-30

APPLICATIONS

- Telecom
- Base Stations
- Servers

DESCRIPTION

The RM91500A achieves 40A of continuous, 45A peak output current from 4V to 18V input voltage. The device integrates main switch and synchronous switch with very low $R_{DS(ON)}$ to minimize the conduction loss. It provides accurate regulation for a variety of loads with an accurate ±1% voltage reference (V_{REF}) over T_J= -40℃ to 125℃. The DC/DC regulator adopts the COT architecture to achieve fast transient responses for high step-down applications. Cycle-by-cycle current limit, hiccup/latch-off over current protection and thermal shutdown protect the device during an over current condition.

The RM91500A device is also guarantees robustness with output short protection, thermal protection and input under voltage lockout.

TYPICAL APPLICATION

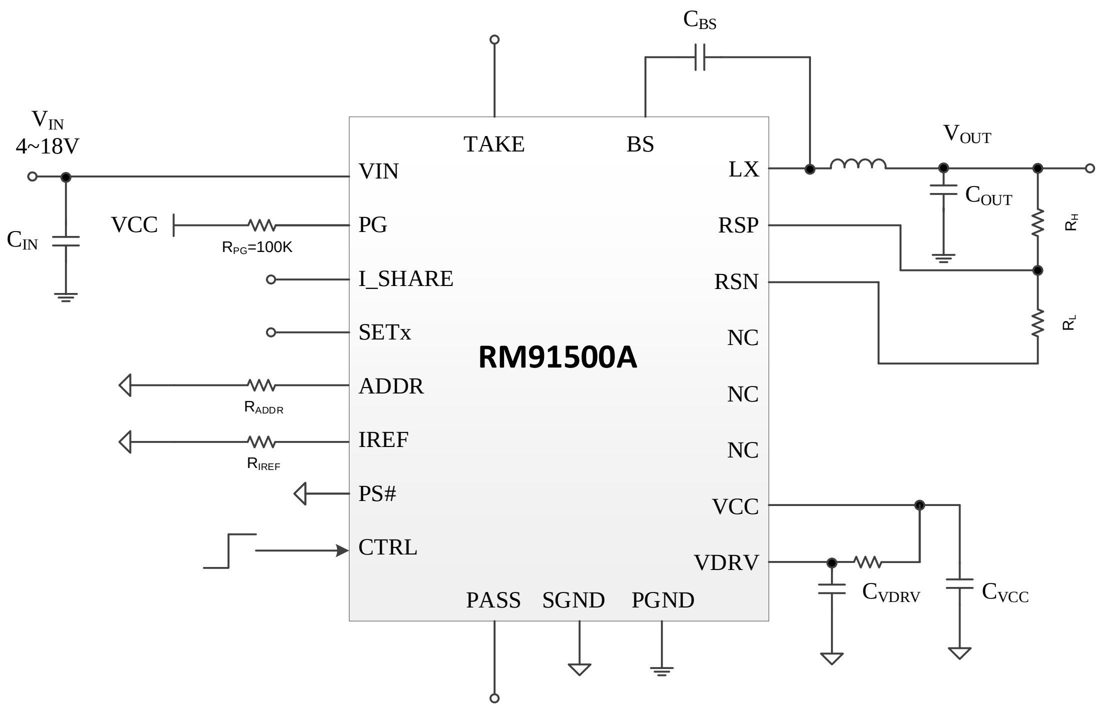

Figure 1. Schematic Diagram

18V Input, 40A Continuous, 45A Peak Output, Asynchronous Step-Down DC/DC Converter

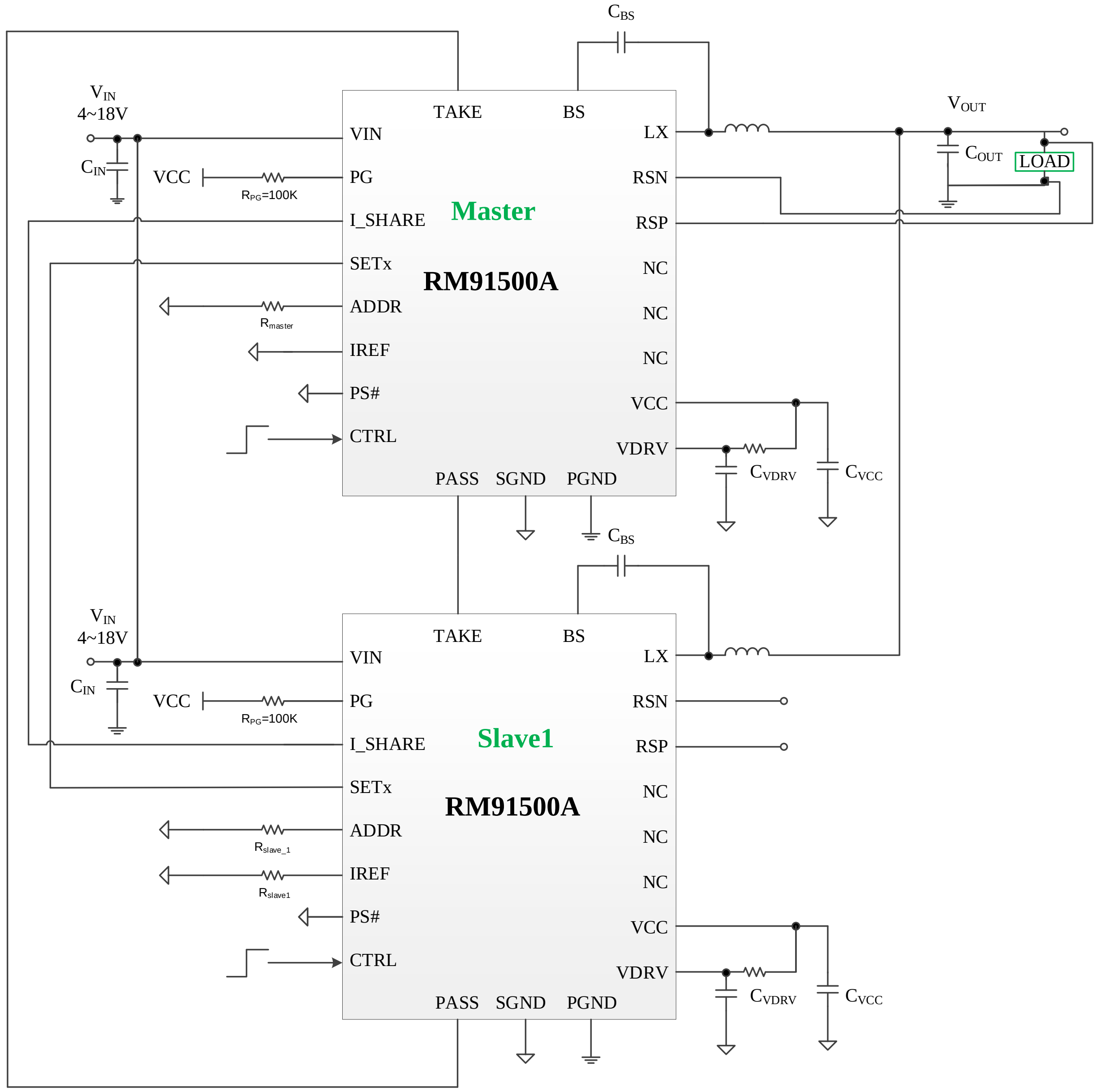

Figure 2. Two Phases Operation Schemati

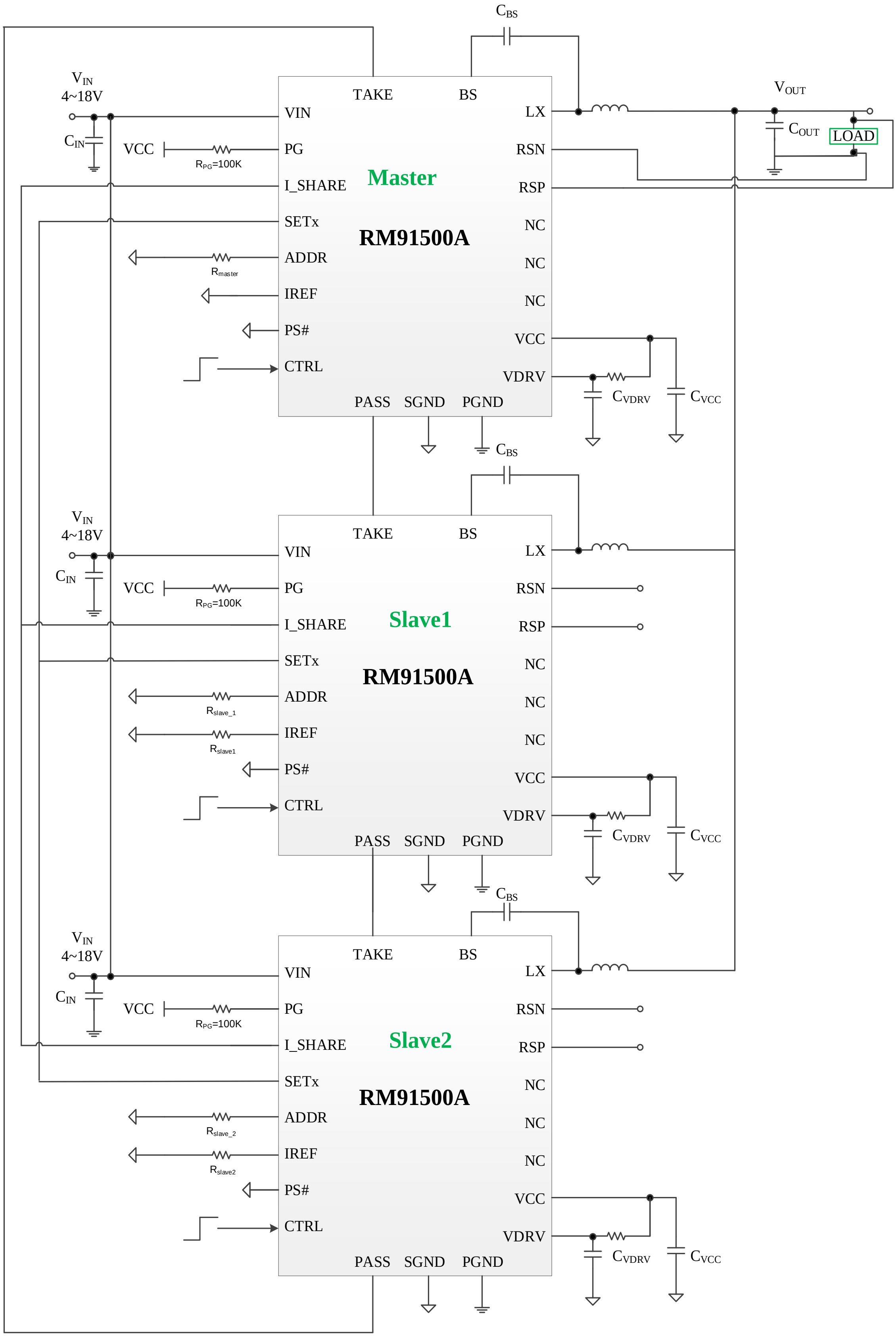

Figure 3. Three Phases Operation Schematic

Package and Pin Description

Pinout Diagram(top view)

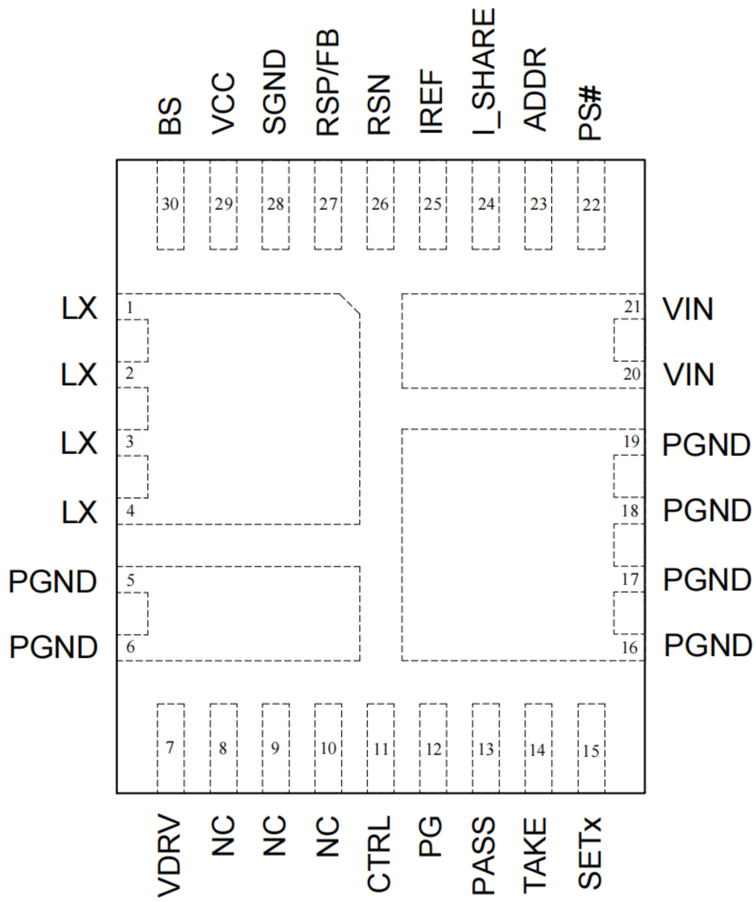

Figure 4. LGA5×6-30 Pin Definition Diagram

Pin Definition

Pin Name	Pin Number	Pin Description
LX	1,2,3,4	Inductor pin. Connect this pin to the switching node of inductor.
PGND	5,6,16,17,18,19	Power Ground pin.
VDRV	7	Decoupling input pin for 3.3V driver power supply. Decouple VDRV with a minimum 1uF ceramic capacitor as close to VDRV as possible. VDRV accepts an external 3.3V bias. If no external 3.3V bias is provided, connect VDRV to VCC through 2-10Ω resistor.
NC	8	NC, this pin can be floating.
NC	9	NC, this pin can be floating.
NC	10	NC, this pin can be floating.
CTRL	11	CTRL is a digital input that turns the regulator on and off. When CTRL is high, turn on the regulator, when CTRL is low, turn off the regulator. Do not leave it floating.
PG	12	Power good output. The output of PG is an open-drain signal.

PASS	13	Passes the set signal to the next phase.
TAKE	14	Receives set signal from the previous phase.
SETx	15	Set signal pin. When used for stand-alone device, this pin can be floating. For multi-phase application, SETx is an output pin for master, and input pin for slaver.
VIN	20, 21	Input pin. Decouple this pin to GND pin with at least 3pcs 22µF ceramic capacitors.
PS#	22	Phase shedding. With proper setting, pull PS# high to enable a slave phase, pull PS# low to disable a slave phase. Connect PS# of the master phase to AGND.
ADDR	23	Device slave address configure pin.
I_SHARE	24	Current sharing signal for multi-phase operation. For a stand-alone device, the I_SHARE pin can be left floating.
IREF	25	Reference current generator amplifier output.
RSN	26	The negative input of the remote sense amplifier.
RSP/FB	27	The positive input of the remote sense amplifier. Feedback.An external resistor divider from the output to RSN (tapped to FB) sets the output voltage. It is recommended to place the resistor divider as close to FB as possible.
SGND	28	Analog ground should be electrically connected to GND close to the device
VCC	29	Internal 3.3V LDO output. Power supply for internal analog circuits and driving circuit. Decouple this pin to GND with a minimum 1µF ceramic capacitor.
BS	30	Boot-strap pin. Supply high side gate driver. Connect this pin to the LX pin with a 100nF ceramic capacitor.

Order Information

Part No.	**Model**	**Description**	**Package**
70902014	RM91500A	RM91500A, 40A Continuous, 45A Peak Buck Asynchronous Step-Down DC/DC Converter, 4-18V, V_{FB} 0.600V, LGA5×6-30	LGA5×6-30

Absolute Maximum Ratings (Note 1)

Item	Min	Max	Units
V_{IN}	-0.3	19	V
LX	-0.3V (-5V for 10ns)	V_{IN} +0.3 (V_{IN} +5V for 10ns)	V
V_{IN}-LX	-5V for 10ns	V_{IN} +5V for 10ns	V
BS-LX	-0.3	4	V
RSP/FB, I_SHARE, SETx,	-0.3	V_{IN} +0.3	V
CTRL,PG	-0.3	3.6	V
VCC, VDRV	-0.3	4.5	V
All Other Pin	-0.3	4.3	V
Junction Temperature	-40	150	ºC
Lead Temperature (Soldering, 10 sec.)	——	260	ºC
Storage Temperature Range	-65	150	ºC

Recommended Operating Conditions (Note 2)

Item	Min	Max	Units
V_{IN}	4	18	V
T_J (Junction Temperature Range)	-40	125	ºC
T_A (Operating Ambient Temperature）	-40	85	ºC

Thermal Resistance (Note 3)

Item	θ_{JA}	θ_{JC_TOP}	Units
LGA (5mmx6mm)	TBD	TBD	ºC/W
EVQ-RM91500A	13.33	3.47	ºC/W

Note 1: Stresses beyond the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 2: The device is not guaranteed to function outside its operating conditions.

Note3: θ_{JA} is the Thermal resistance from junction to ambient. θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.Measured on EVQ-RM91500A 4-layer PCB, 8cmx8cm.

Electrical Characteristics (4)

(V_{IN} =4V to 16V, T_J= -40~125°C, typical value is tested at T_J = 25° C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Specifications						
Input Voltage Range	V_{IN}		4		18	V
Input UVLO Threshold (rising)	$V_{UVLO,rising\_default}$	V_{CC}=3.3V		2.75		V
Input UVLO Threshold (falling)	$V_{UVLO,falling\_default}$			2.5		V
Shutdown Supply Current	I_{SD}	V_{CTRL}=0V, Tj=+25°C		2.5		mA
Output Specifications						
Reference Voltage	$V_{REF\_DEFAULT}$	4V≤V_{IN}≤18V -40°C≤T_J≤125°C	591	600	609	mV
Top Switch Resistance	$R_{DS(ON)1}$			3.0		mΩ
Bottom Switch Resistance	$R_{DS(ON)2}$			0.9		mΩ
Soft- start Time	$t_{SS\_DEFAULT}$			2		ms
Turn On Delay Time	$t_{ON\_DELY\_DEFAULT}$			4		ms
Minimum On Time[5]	T_{ON_MIN}	f_{SW}=1MHz, V_{OUT}=0.6		50		ns
Minimum Off-Time	T_{OFF_MIN}	V_{FB}=580mV		220		ns
Signal Specifications						
CTRL Rising Threshold	V_{CTRL_H}		1.35			V
CTRL Falling Threshold	V_{CTRL_L}				0.8	V
Power Good Threshold	V_{PG_H}	V_{FB} Falling, PG from low to high.		80%V_{REF}		V
	V_{PG_L}/V_{UVP}	V_{FB} Falling (Fault), PG from high to low.		85%V_{REF}		V
	V_{PG_L}/V_{OVP}	V_{FB} Rising (Fault), PG from high to low.		115%V_{REF}		V
Power Good from Low to High Delay When Soft-start	T_{PG_DLY}			2		mS
Power Good Leakage Current	$I_{PG,LKG}$	V_{PG}=3V		1.5		µA
Power Good Low-level Output Voltage	$V_{OL,100}$	V_{IN}=0V, pull PG up to 3.3V through a 100kΩ resistor, T_J=25°C		600		mV
	$V_{OL,10}$	V_{IN}=0V, pull PG up to 3.3V through a 10kΩ resistor, T_J=25°C		700		mV
General Specifications						
Switching Frequency	f_{SW}			600		kHz
Top FET Current Limit	$I_{LIM,TOP}$			60		A
Bottom FET Current Limit	$I_{LIM,BOT}$			36		A

(inductor valley)						
Low Side Negative Current Limit	$I_{LIM, NEG}$			-20		A
Over Temperature Fault Limit	$T_{OT,FAULT}$			145		℃

Note 4: MOSFET on-resistance specifications are guaranteed by correlation to wafer level measurements.

Note 5: Guaranteed by design.

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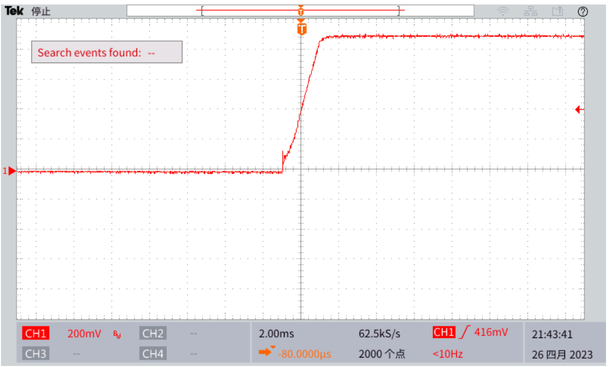
Typical Performance Characteristics (6)(7)

Note (6): Performance waveforms are tested on the evaluation board.

Note (7): V_{IN} =12V, V_{OUT}=0.9V, T_A = +25°C, unless otherwise noted.

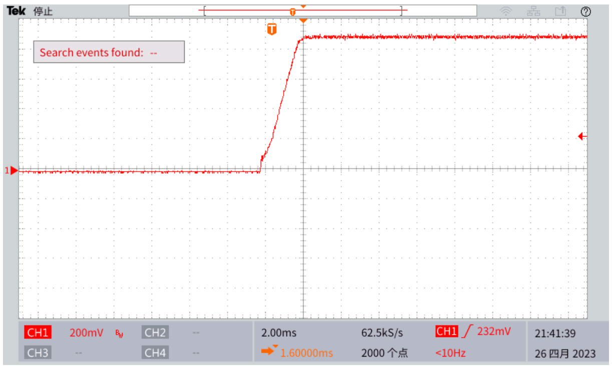
Power Up at No Load

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=0A



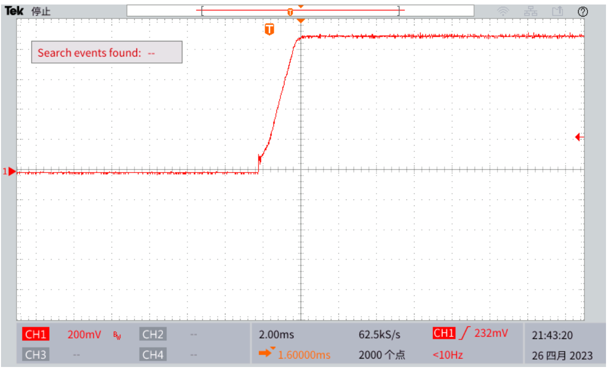
Power Up at Full Load

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=30A



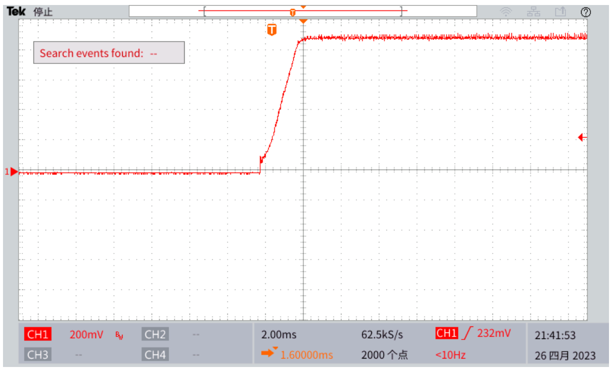
Power Up at No Load

V_{IN}=12V, V_{OUT}=0.9V, I_{OUT}=0A



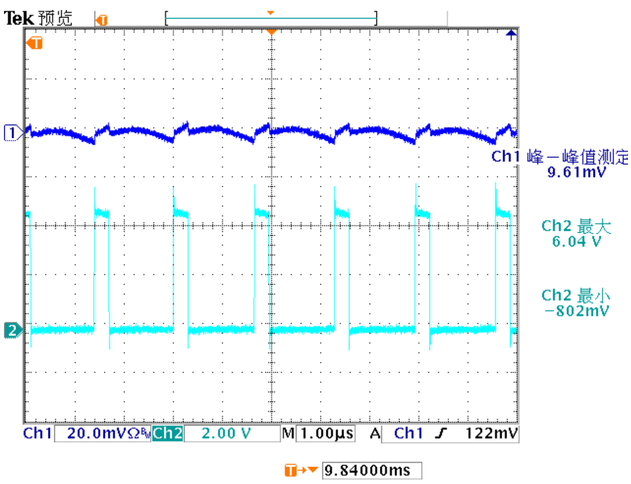
Power Up at Full Load

V_{IN}=12V, V_{OUT}=0.9V, I_{OUT}=30A



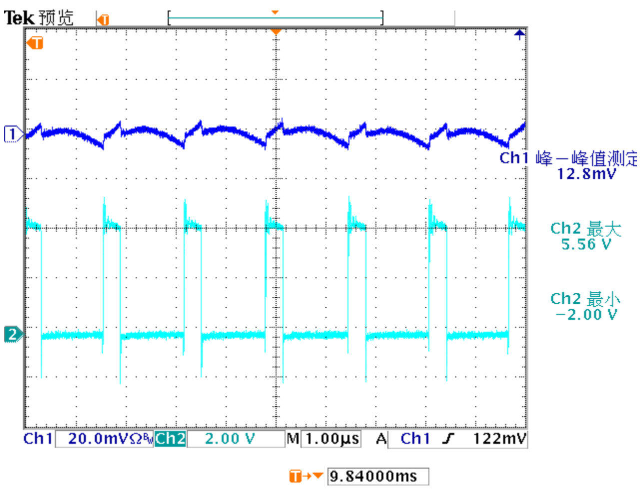
Output Ripple Voltage

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=0A, C_{out}=7*47uF+0.1uF;



Output Ripple Voltage

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=30A, C_{out}=7*47uF+0.1uF;



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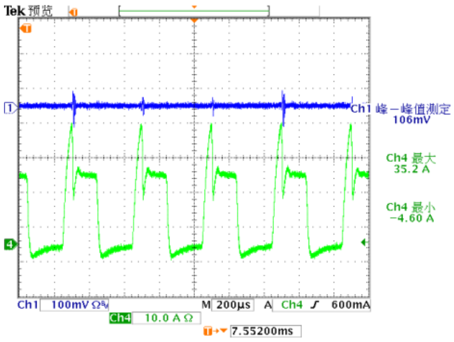
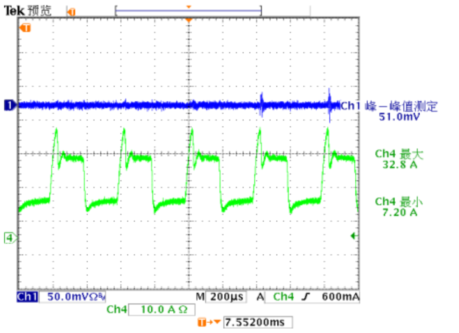
Loop Response

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=0A~25A, C_{out}=7*47uF+0.1uF;



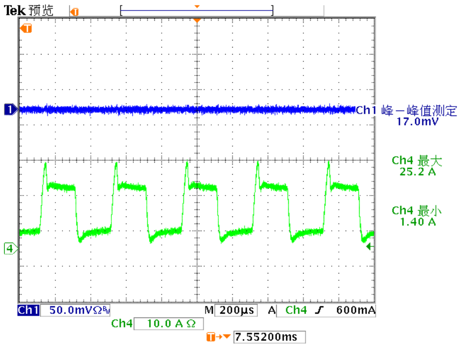
Loop Response

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=15A~30A, C_{out}=7*47uF+0.1uF;



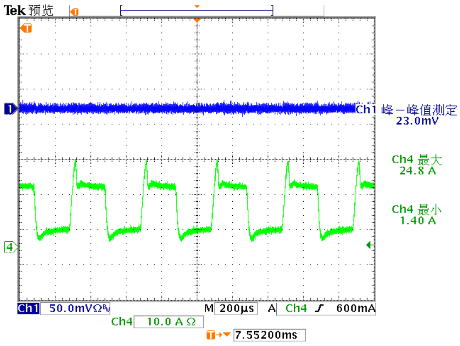
Loop Response

V_{IN}=5V, V_{OUT}=0.9V, I_{OUT}=7.5A~22.5A, C_{out}=7*47uF+0.1uF;



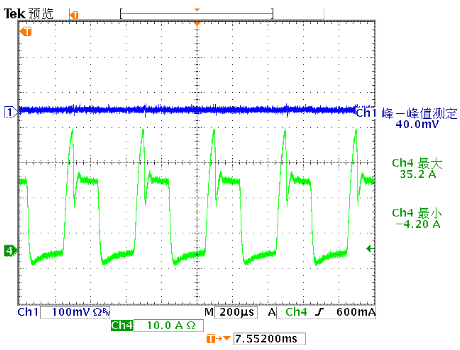
Loop Response

V_{IN}=12V, V_{OUT}=0.9V, I_{OUT}=7.5A~22.5A, C_{out}=7*47uF+0.1uF;



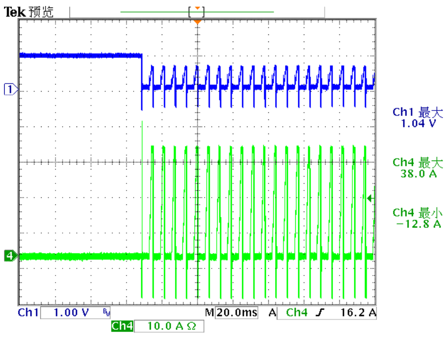
Loop Response

V_{IN}=12V, V_{OUT}=0.9V, I_{OUT}=0A~15A, C_{out}=7*47uF+0.1uF;



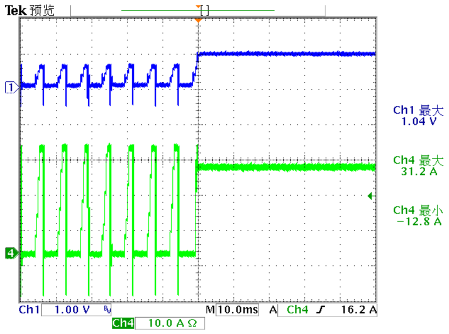
Short Circuit Entry

V_{IN}=12V, V_{OUT}=0.9V, I_{OUT}=0A to short



Short Circuit Recovery

V_{IN}=12V, V_{OUT}=0.9V, I_{OUT}= short to 25A


Tek 预览
Ch1 最大
1.04 V
Ch4 最大
31.2 A
Ch4 最小
−12.8 A
Ch1 1.00 V
M 10.0ms A Ch4 16.2 A
Ch4 10.0 A Ω

Functional Block Diagram

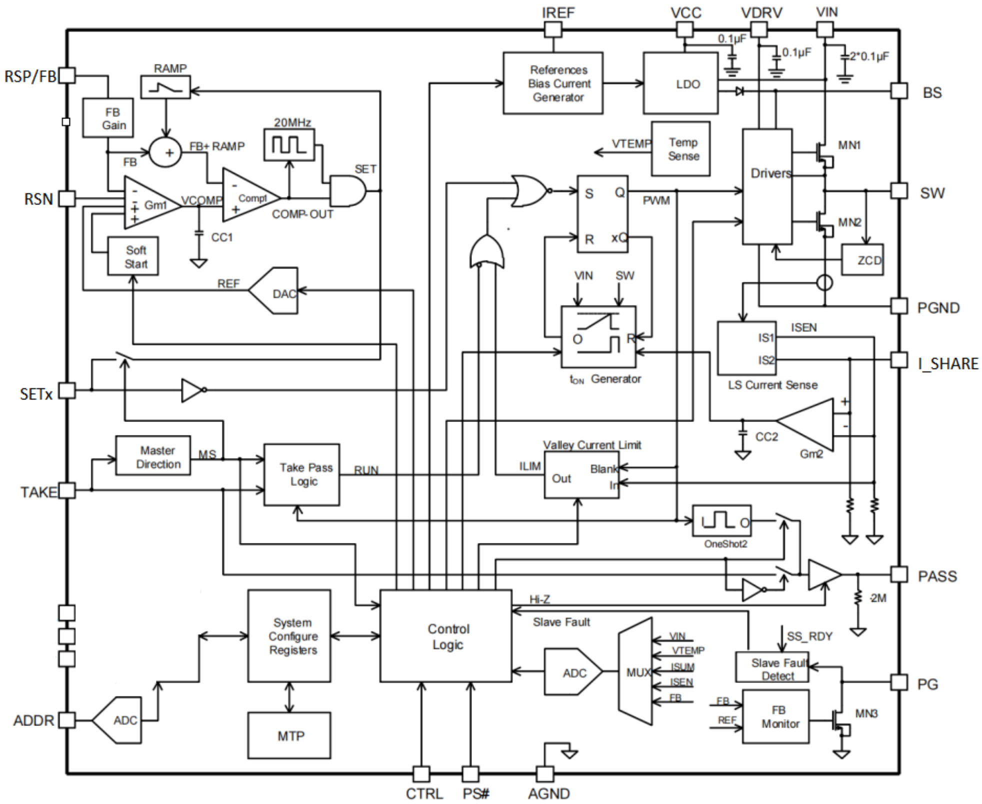


Figure 5. Functional Block Diagram

Functional Description

The RM91500A is an synchronous, step-down regulator that uses multi-phase constant-on-time (MCOT) control to provide fast transient response. It achieves 30A of continuous output current from 4.8V to 16V input voltage.

Multiphase Parallel Design

The RY91X00A supports up to three-phase parallel operation. When operating in parallel, the following configurations must be followed:

1 The PASS output of the preceding phase should be connected to the TAKE input of the following phase, and the PASS output of the last phase should be connected back to the TAKE input of the first phase.

2 The SET, ISII, and CTRL signals should be connected together respectively for all phases.

3 Only the PG signal from the Master phase should be used, and it should be pulled up appropriately.

4 The IREF pin's grounding resistor should be set as follows: 60.4kΩ for the Master phase, 180kΩ for the second phase, and 0Ω (short to ground) for the third phase.

5 The ADDR pin is reserved and can be connected to ground through resistors of 4.99kΩ, 15kΩ, or 24.9kΩ, depending on the configuration.

6 For voltage feedback, only the RSP and RSN of the Master phase should be used; the RSP and RSN of the Slave phases should be left unconnected (floating).

7 The PS pin of the Master phase should be connected to GND, while the PS pins of the Slave phases should be pulled up to their respective VCC through a 10kΩ resistor.

Applications Information

Output Voltage Set

The output voltage is determined by the resistor divider connected at the RSP/FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} \cdot \frac{R_L}{R_L + R_H}$$

Choose R_H and R_L to program the proper output voltage. To minimize the power consumption under light loads, it is desirable to choose large resistance values for both R_H and R_L. If R_H =100kΩ is chosen, then RL can be calculated by the calculation formula as follows:

$$R_L = \frac{0.600V \times R_H}{(V_{OUT} - 0.600V)}$$

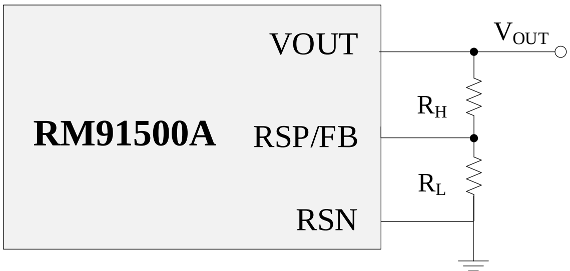


Figure 6. Output voltage setting

Input Capacitor C_{IN}

The purpose of the input capacitor is to stabilize the input voltage and provide the AC input current for the synchronous step-down DC/DC regulator. The RMS value of the input capacitor ripple current can be estimated using the following formula:

$$I_{CIN} = I_{OUT} * \sqrt{D * (1 - D)} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})}$$

Where I_{OUT} is the load current; V_{OUT} is the output voltage;; V_{IN} is the input voltage;

When the input ripple voltage is determined, the input capacitor can be selected by:

$$C_{IN} = \frac{I_{OUT}}{f_{sw} * \Delta V_{IN}} * D * (1 - D) = \frac{I_{OUT}}{f_{sw} * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * (1 - \frac{V_{OUT}}{V_{IN}})$$

To minimize the potential noise problem, place 4.7uF*3/100V capacitors in typical application as close to the VIN and GND pins as possible.

Output Capacitor C_{OUT}

The output capacitor is selected to handle the output ripple noise requirements. Both steady state ripple and transient requirements must be taken into consideration when selecting this capacitor.

By choosing the appropriate output capacitor to meet the output voltage ripple, noise requirements. When selecting capacitors, both steady-state ripple and transient requirements must be considered, and the output ripple can be calculated by the following formula:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_{sw} * L} * (1 - \frac{V_{OUT}}{V_{IN}}) * (R_{ESR} + \frac{1}{8 * f_{sw} * C_{OUT}})$$

where C_{OUT} is the output capacitor value; R_{ESR} is the equivalent series resistance value of the output capacitor.

For the best performance, it is recommended to use X7R or better grade ceramic capacitor with greater than 50µF capacitance. Place this ceramic capacitor really close to the VOUT and GND pins to minimize the loop area formed by C_{OUT}, and the VOUT/GND pins.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{f_{sw} * \Delta I_L} * (1 - \frac{V_{OUT}}{V_{IN}})$$

Where ΔI_L is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

N-Channel MOSFET switch is integrated in the RM91500A to convert the input voltage to the regulated output voltage. Since the top MOSFET needs a gate voltage greater than the input voltage, a boost capacitor connected between BST and SW pins is required to drive the gate of the top switch. The boost capacitor is charged by the internal rail when SW is low. Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.

Slave Address

To support the use of multiple RM91500A devices, use the ADDR pin to program the slave address for each RM91500A device.

Table 3: Address vs. ADDR Resistor

R_{ADDR} (kΩ)	Slave Address ($R_{\_IREF}$=60.4kΩ)
4.99k	30h

15k	31h
24.9k	32h
499k+499k	3Fh

Over-Current Protection (OCP)

When the LS-FET is on, the SW current (inductor current) is sensed and monitored cycle by cycle.When V_{FB} drops below the reference, the HSFET is only allowed to turn on if no over-current (OC) condition is detected while the LS-FET is on. Therefore, the inductor current is limited cycle by cycle.If the over current condition that OCP signal is high level when RM91500A detects inductor current, lasts for 128 continuous clock cycles, OCP is triggered.

Over-Temperature Protection (OTP)

The IC monitors the junction temperature internally. If the junction temperature exceeds the threshold value 145℃, the device enters hiccup mode.

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Recommand Schematic parameters

V_{IN}	V_{OUT}	C_{IN}	L	C_{OUT_min}	C_{VCC}	C_{DRV}+R_{DRV}	R_{BS}+C_{BS}	RCC	R_H	R_L
12V	0.9V	270uF+10uF*4+0.1uF	190nH	47uF*10	1uF	1uF+2.2Ω	0Ω+0.22uF	Rr=100k、Cr=1000pF、Cd=220pF	7.5k	2.4k+12.1k
12V	1.2V	270uF+10uF*4+0.1uF	190nH	47uF*10	1uF	1uF+2.2Ω	0Ω+0.22uF	Rr=100k、Cr=1000pF、Cd=220pF	15k	4.75k+10k
12V	1.8V	270uF+10uF*4+0.1uF	190nH	47uF*10	1uF	1uF+2.2Ω	0Ω+0.22uF	Rr=100k、Cr=1000pF、Cd=220pF	30.1k	3.01k+11.8k
12V	3.3V	270uF+10uF*4+0.1uF	330nH or 470nH	47uF*10	1uF	1uF+2.2Ω	0Ω+0.22uF	Rr=51.1k、Cr=1000pF、Cd=220pF	19.1k	4.02k+0.24k

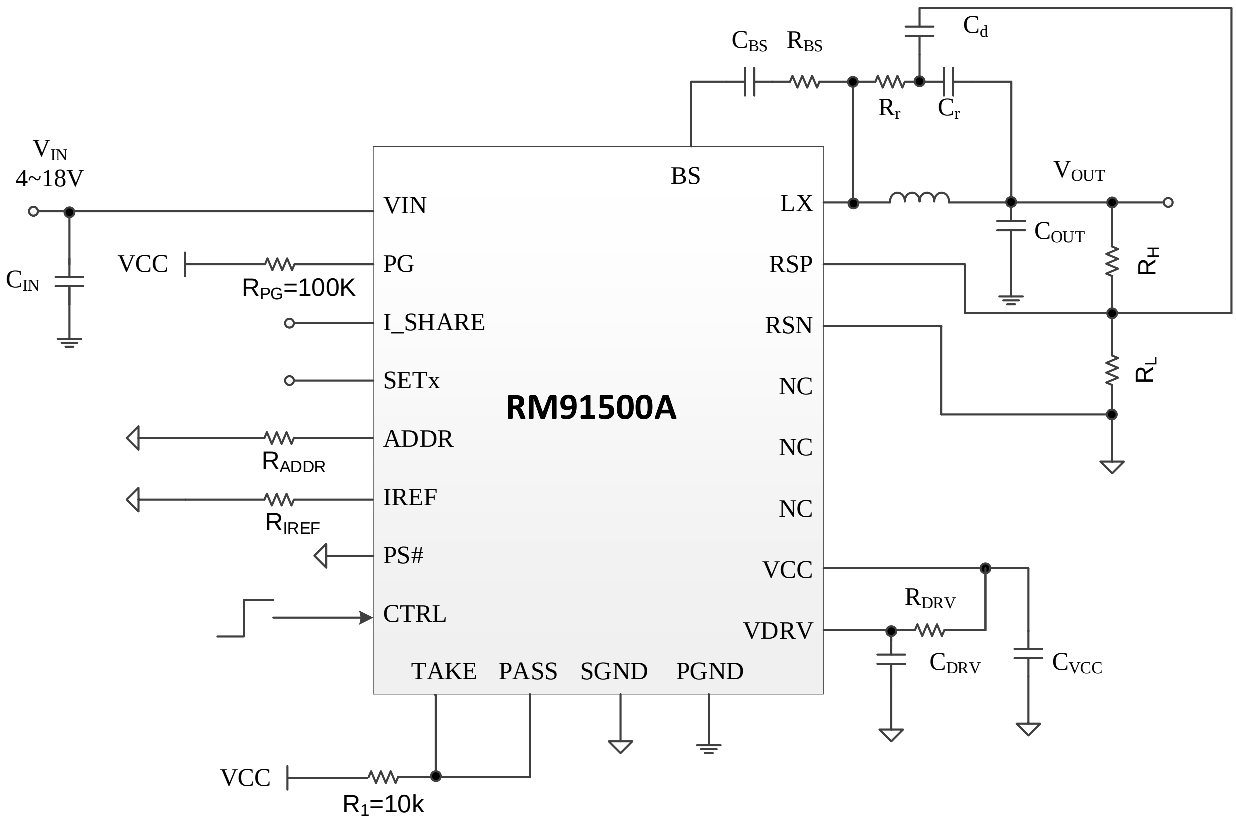


Figure 7. Schematic diagram of RCC ripple injection circuit.

Recommand PCB Layout

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 6 and follow the guidelines below:

1. Place the input MLCC capacitors as close to the IN and PGND pins as possible.
2. Place the major MLCC capacitors on the same layer of IC.
3. Maximize the VIN and PGND copper plane to minimize the parasitic impedance.
4. Place as many PGND vias as possible close to the pin to minimize parasitic impedance and thermal resistance.
5. Place a VCC decoupling capacitor close to the device.
6. Connect AGND and PGND at the point of the VCC capacitor’s ground connection.
7. Place the BST capacitor as close to BST and SW as possible.

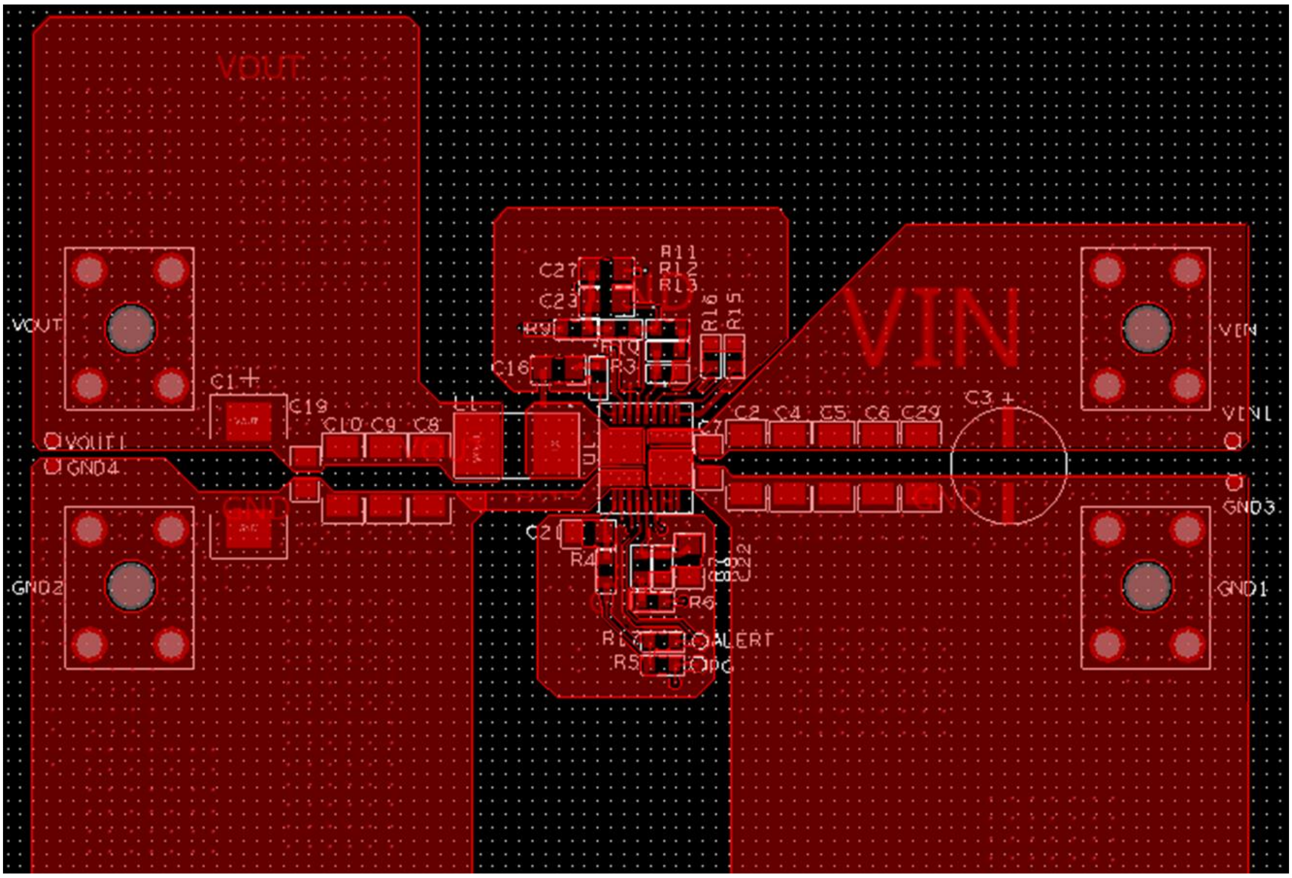
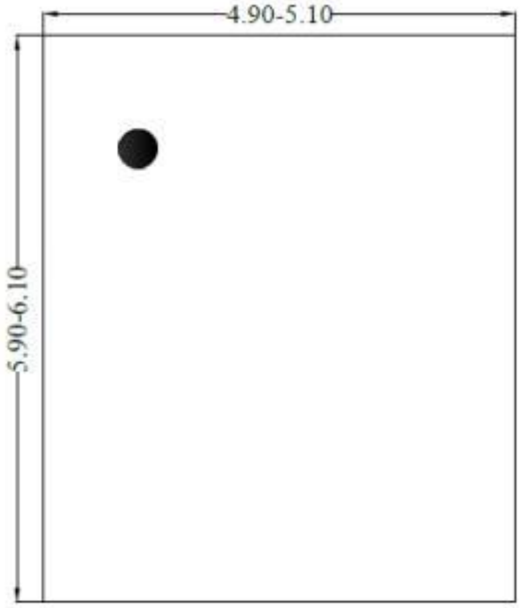
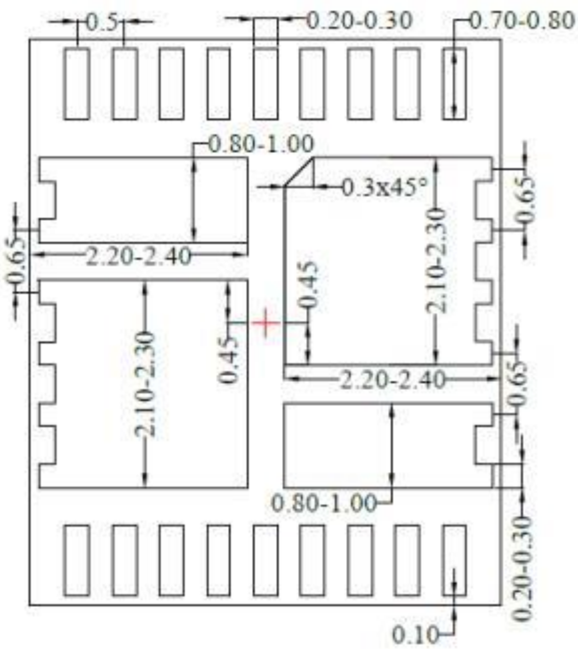


Figure 8. Recommended PCB Layout (Placement and Top Layer PCB)

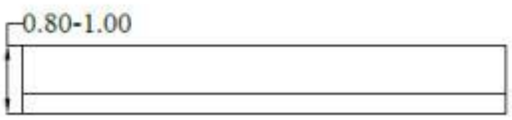
LGA5x6-30 Package Outline Drawing



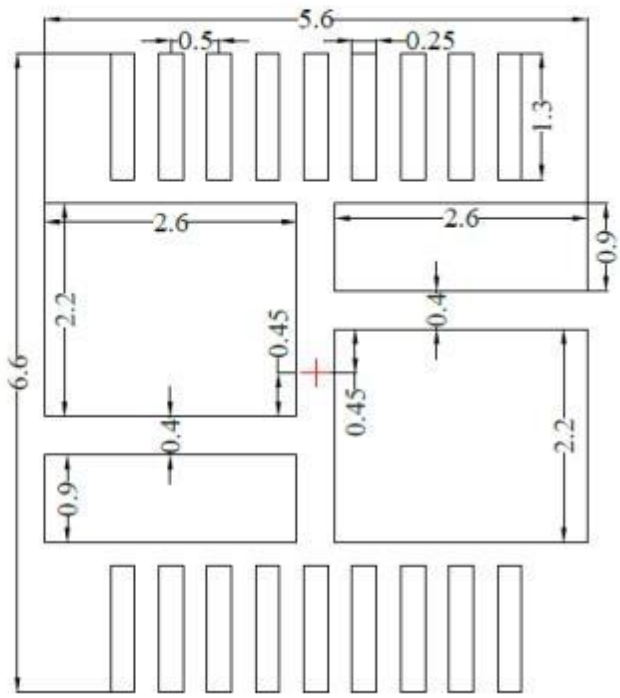
Top View



Bottom view



Front View



Recommended PCB layout

(only for reference)