

Product Overview

NSE34050Q-Q1 is a quad channel 50mΩ high-side switch with protection and diagnostics for 12V automotive system applications. It's designed for driving all types automotive resistive, inductive or capacitive loads.

This device provides advanced protective functions in fault conditions, such as overvoltage clamp, current limitation, thermal shutdown and off-state diagnosis.

A FaultRST pin can be used to latch or retry the output in case of fault.

A sense enable pin allows lower power dissipation when it is disabled.

Key Features

- AEC-Q100 qualified
 - Temperature grade 1: -40°C to 125°C
- Protections
 - Current limitation: 27A
 - 48V overvoltage clamp
 - Thermal shutdown protection
 - Thermal swing protection when ΔT exceeds 60°C
 - Loss of ground and loss of Vcc protection
 - Undervoltage shutdown
 - Reverse battery protection with turning the power MOS on
 - ESD protection
- Fault diagnostic block
 - Thermal shutdown diagnosis
 - Off-state open-load diagnosis
 - Output short to Vcc diagnosis
 - Current limitation or output short to ground diagnosis
- Very low standby current
- Very low electromagnetic susceptibility

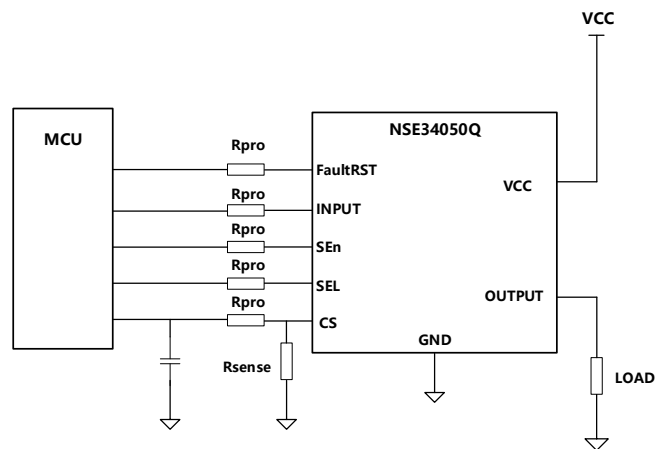
Applications

- All types automotive resistive, inductive or capacitive loads
- Driving high inrush current loads

Device Information

Part Number	Package	Body Size
NSE34050Q-Q1	PowerSSO-16	4.9mm x 3.9mm

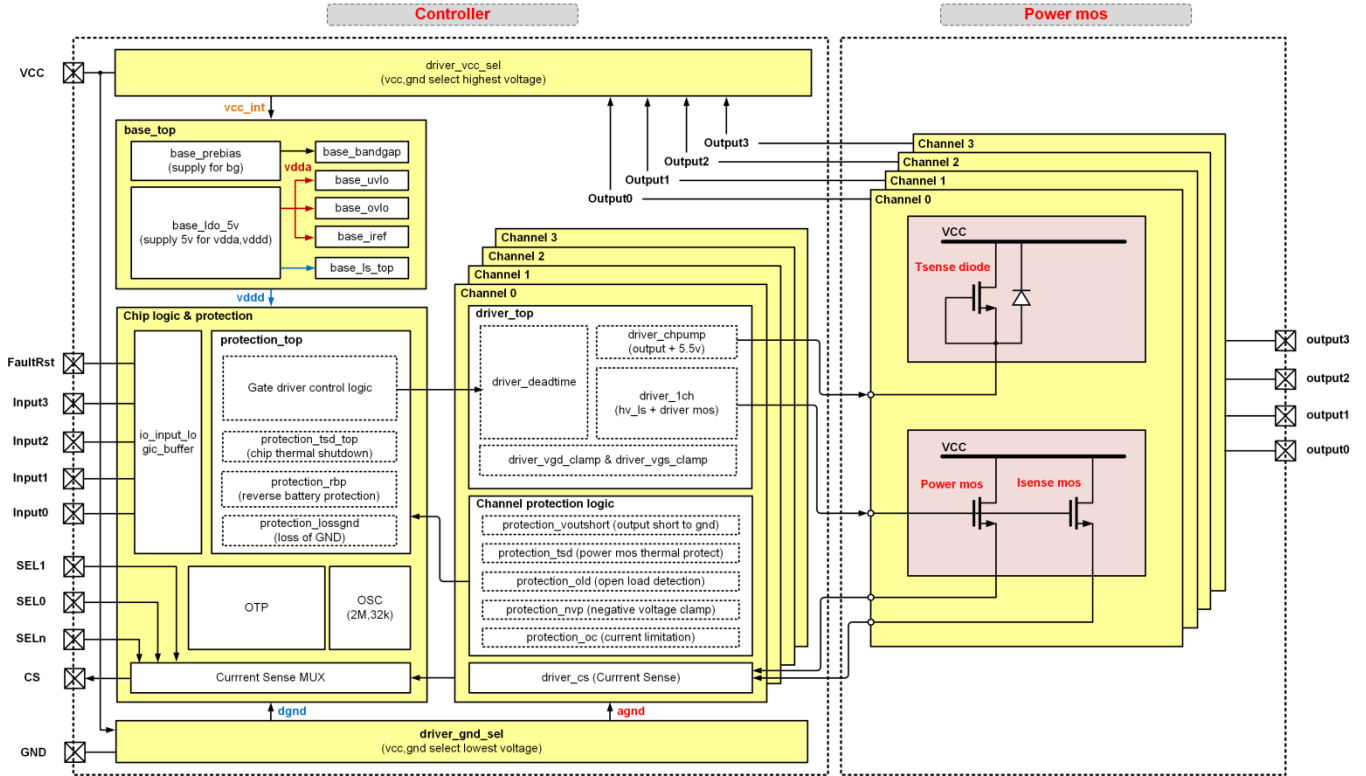
Typical Application



Index

1. BLOCK DIAGRAM	3
2. PIN CONFIGURATION AND FUNCTIONS	3
3. RECOMMENDED CONNECTIONS FOR UNUSED PINS	4
4. ABSOLUTE MAXIMUM RATINGS	4
5. THERMAL INFORMATION	5
NOTES:	5
1). ONE CHANNEL ON	5
2). FOUR LAYERS 2S2P PCB JEDEC JESD 51-7	5
3). TWO LAYERS 2S0P PCB JEDEC JESD 51-5	5
6. SPECIFICATIONS	5
6.1. ELECTRICAL CHARACTERISTICS.....	5
6.2. TYPICAL PERFORMANCE CHARACTERISTICS	13
6.2.1. <i>True table</i>	13
6.2.2. <i>Current sense MUX address</i>	14
7. PROTECTIONS	14
7.1. CURRENT LIMITATION	14
7.1.1. <i>Retry strategy</i>	15
7.2. THERMAL SHUTDOWN AND THERMAL SWING	17
7.3. INDUCTIVE LOAD VOLTAGE CLAMP.....	18
7.4. REVERSE POLARITY PROTECTION	18
7.5. LOSS OF BATTERY AND LOSS OF GROUND PROTECTION	18
8. APPLICATION INFORMATION	19
9. ELECTRICAL CHARACTERISTICS CURVES	19
10. IMMUNITY AGAINST TRANSIENT ELECTRICAL DISTURBANCES	19
11. PACKAGE AND PCB THERMAL DATA	19
12. PACKAGE INFORMATION	20
12.1. POWERSSO-16.....	20
13. REVISION HISTORY	21

1. Block diagram



2. Pin Configuration and Functions

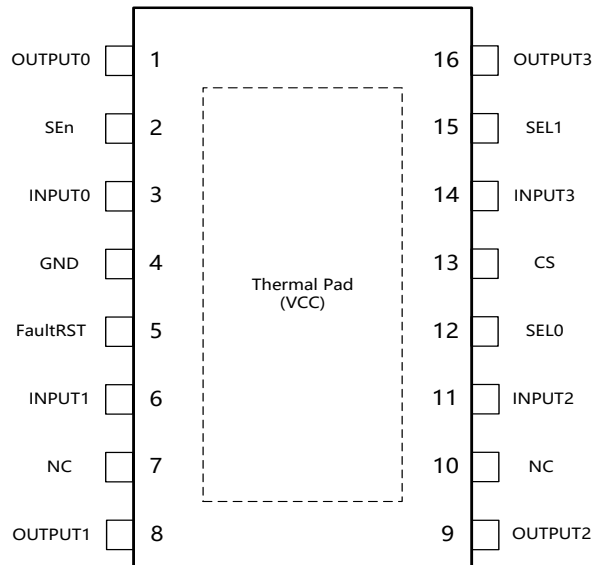


Table 1 PowersSO-16 Pin Configuration and Description

PIN NO.	SYMBOL	FUNCTION
1, 8, 9, 16	OUTPUT _{0,1,2,3}	Power output.
2	SEn	Digital signal enables the CS diagnostic pin, active high.
3, 6, 11, 14	INPUT _{0,1,2,3}	Digital signal to control the channel n on/off, active high.
4	GND	Ground connection.
5	FaultRST	Digital signal to control the device auto-retry or latch-off in case of fault. The device works in auto-retry mode when it keeps low.
7, 10	N.C.	Not connect.
12, 15	SEL _{0,1}	Current sense channel select.
13	CS	Current sense output.

3. Recommended Connections for Unused Pins

Table 2 Recommended connections for unused pins

PIN NAME	CONNECTIONS FOR UNUSED PINS	IMPACT IF NOT USED
OUTPUT _{0,1,2,3}	Floating	No output.
SEn	Floating or ground through 15kΩ resistor	Current sense is not available.
INPUT _{0,1,2,3}	Floating or ground through 15kΩ resistor	All channel is off.
FaultRST	Floating or ground through 15kΩ resistor	Default auto-retry mode.
SEL _{0,1}	Floating or ground through 15kΩ resistor	Can not select current sense channel.
CS	To ground through 1kΩ resistor, floating is not allowed	Current sense is not available.

4. Absolute Maximum Ratings

Parameters	Symbol	Min	Typ	Max	Unit
DC supply voltage	V _{cc}			40	V
Reverse DC supply voltage	-V _{cc}	-0.3			V
Maximum jump start voltage	V _{ccjs}			28	V

Parameters	Symbol	Min	Typ	Max	Unit
Reverse ground pin current	$-I_{GND}$	-200			mA
OUTPUT DC current	I_{out}			Internally limited	A
Reverse OUTPUT DC current	$-I_{out}$	Load limited			A
INPUT DC input current	I_{IN}	-1		10	mA
SEn DC input current	I_{SEn}				
SEL DC input current	I_{SEL}				
FaultRST DC input current	I_{FR}				
FaultRST DC input voltage	V_{FR}			7.5	V
CS pin DC output current	I_{snese}	-20		10	mA
Single pulse avalanche energy(L = 1mH, T _j = 150°C)	E_{AS}			24	mJ
Electrostatic discharge, Human-body model	HBM	-4000		4000	V
Electrostatic discharge, Charged-device model	CDM	-750		750	V
Junction Temperature	T_j	-40		150	°C
Storage Temperature	T_{stg}	-55		150	°C

5. Thermal Information

Parameters	Symbol	Value	Unit
IC Junction-to-ambient Thermal Resistance ^{1),3)}	θ_{JA}	57.3	°C/W
IC Junction-to-ambient Thermal Resistance ^{1),2)}	θ_{JA}	23.5	°C/W
IC Junction-to-board Thermal Resistance ^{1),2)}	θ_{JB}	6.3	°C/W

Notes:

- 1). One channel ON.
- 2). Four layers 2s2p PCB JEDEC JESD 51-7
- 3). Two layers 2s0p PCB JEDEC JESD 51-5

6. Specifications

6.1. Electrical Characteristics

(VCC = 7 V to 28 V, T_j = -40°C to 150°C, unless otherwise noted, All typical value refer to VCC = 13 V, T_j = 25°C, unless otherwise noted.)

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Power Section						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Operating supply voltage	V_{CC}	4	13	28	V	
Undervoltage lockdown falling voltage	V_{UVLOF}		3.3		V	
Undervoltage lockdown rising voltage	V_{UVLOR}		3.6		V	
Undervoltage lockdown hysteresis	V_{UVhys}		300		mV	
ON-state resistance	R_{ON}		50		m Ω	$I_{out} = 2\text{ A}$; $T_j = 25^\circ\text{C}$
				100	m Ω	$I_{out} = 2\text{ A}$; $T_j = 150^\circ\text{C}$
				75	m Ω	$I_{out} = 2\text{ A}$; $T_j = 25^\circ\text{C}$; $V_{CC} = 4\text{ V}$
Vcc-output clamp voltage	V_{CLAMP}	41	46	52	V	$I_s = 20\text{ mA}$; $T_j = -40^\circ\text{C}$ to 150°C
Supply current in standby mode	I_{SB}			0.5	μA	$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{FR} = V_{SEN} = V_{SELO,1} = 0\text{ V}$; $T_j = 25^\circ\text{C}$
				3	μA	$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{FR} = V_{SEN} = V_{SELO,1} = 0\text{ V}$; $T_j = 125^\circ\text{C}$
Standby mode blanking time	t_{D_SB}	60	300	550	μs	$V_{CC} = 13\text{ V}$; $V_{IN} = V_{OUT} = V_{FR} = V_{SELO,1} = 0\text{ V}$; $V_{SEN} = 5\text{ V}$ to 0 V
Supply current in onstate mode without Iout	$I_{S(ON)}$		10	16	mA	$V_{CC} = 13\text{ V}$; $V_{OUT} = V_{FR} = V_{SEN} = V_{SELO,1} = 0\text{ V}$; $V_{IN0,1,2,3} = 5\text{ V}$; $I_{OUT0,1,2,3} = 0\text{ A}$
GND current in onstate mode with Iout	$I_{GND(ON)}$			20	mA	$V_{CC} = 13\text{ V}$; $V_{OUT} = V_{FR} = V_{SELO,1} = 0\text{ V}$; $V_{IN0,1,2,3} = V_{SEN} = 5\text{ V}$; $I_{OUT0,1,2,3} = 1\text{ A}$
Bode diode forward voltage	V_{BD}			0.7	V	$I_{out} = -2\text{ A}$; $T_j = 150^\circ\text{C}$
Input_{0,1,2,3} section						
Low-level input voltage	V_{IL}			0.9	V	
Low-level input current	I_{IL}	1			μA	$V_{IN} = 0.9\text{ V}$
High-level input voltage	V_{IH}	2.1			V	
High-level input current	I_{IH}			10	μA	$V_{IN} = 2.1\text{ V}$
Input hysteresis voltage	$V_{I(hyst)}$	0.2			V	
Input clamp voltage	V_{ICL}	5.3		7.5	V	$I_{IN} = 1\text{ mA}$
			-0.7			$I_{IN} = -1\text{ mA}$
FaultRST section						

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Low-level input voltage	V_{FRL}			0.9	V	
Low-level input current	I_{FRL}	1			μA	$V_{IN} = 0.9\text{V}$
High-level input voltage	V_{FRH}	2.1			V	
High-level input current	I_{FRH}			10	μA	$V_{IN} = 2.1\text{V}$
Input hysteresis voltage	$V_{FR(hyst)}$	0.13			V	
Input clamp voltage	V_{FRCL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
SEL_{0,1} section						
Low-level input voltage	V_{SELL}			0.9	V	
Low-level input current	I_{SELL}	1			μA	$V_{IN} = 0.9\text{V}$
High-level input voltage	V_{SELH}	2.1			V	
High-level input current	I_{SELH}			10	μA	$V_{IN} = 2.1\text{V}$
Input hysteresis voltage	$V_{SEL(hyst)}$	0.13			V	
Input clamp voltage	V_{SELCL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
SEn section						
Low-level input voltage	V_{SEnL}			0.9	V	
Low-level input current	I_{SEnL}	1			μA	$V_{IN} = 0.9\text{V}$
High-level input voltage	V_{SEnH}	2.1			V	
High-level input current	I_{SEnH}			10	μA	$V_{IN} = 2.1\text{V}$
Input hysteresis voltage	$V_{SEn(hyst)}$	0.13			V	
Input clamp voltage	V_{SEnCL}	5.3		7.5	V	IIN = 1 mA
			-0.7			IIN = -1 mA
Switching characteristics (VCC = 13V, Tj = -40°C to 150°C)						
Turn-on delay time	$t_{d(ON)}$	10	25	70	μs	$R_L = 6.5 \Omega$, $V_{CC} = 13 \text{V}$, $T_j = 25^\circ\text{C}$
Turn-off delay time	$t_{d(OFF)}$	10	25	70	μs	$R_L = 6.5 \Omega$, $V_{CC} = 13 \text{V}$, $T_j = 25^\circ\text{C}$
Turn-on slew rate	dv/dt_{on}	0.2	0.25	0.65	$\text{V}/\mu\text{s}$	$R_L = 6.5 \Omega$, $V_{CC} = 13 \text{V}$, $T_j = 25^\circ\text{C}$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Turn-off slew rate	dv/dt_{off}	0.2	0.35	0.65	V/ μ s	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$, $T_j = 25^\circ C$
Switching energy losses at turn-on	W_{ON}	0.1	0.2	0.3	mJ	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$
Switching energy losses at turn-off	W_{OFF}	0.1	0.2	0.3	mJ	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$
Pulse skew time ($t_{PHL} - t_{PLH}$)	t_{SKEW}	-30	10	40	μ s	$R_L = 6.5 \Omega$, $V_{CC} = 13 V$
Protections						
DC short-circuit current	I_{limit}	21	27	38	A	$V_{CC} = 13 V$, $V_{IN} = 5 V$
Deglitch time			3		μ s	
Auto-retry times in case of fault after the Counter reset	$n_{RETRY(CR)}$	-	5	-		See Figure
Auto-retry times in case of fault after the first t_{RETRY} activation	$n_{RETRY(NT)}$	-	1	-		
Retry cycles allowed before channel latch off	$n_{RETRY(CYC)}$	-	2	-		
Auto-retry time after fault condition	t_{RETRY}	40	70	100	ms	
Counter reset delay time after fault condition	$t_{DELAY(CR)}$	40	70	100	ms	
	$t_{DEN(CR)}$	50	100	150	μ s	
Shutdown temperature	T_{TSD}	150	175	200	$^\circ C$	
Reset temperature	T_R	$T_{RS} + 1$	$T_{RS} + 7$			
Thermal reset of diagnostic indication	T_{RS}	135				$V_{FR} = 0V$, $V_{SEN} = 5V$
Thermal hysteresis ($T_{TSD} - T_R$)	T_{HYST}		7			
Dynamic temperature	ΔT_j		60		K	$T_j = -40^\circ C$, $V_{CC} = 13V$
Dynamic temperature hysteresis	$\Delta T_j(HYS)$		20?		K	
Fault reset time for output unlatch	t_{LATCH_RST}	3	10	20	μ s	$V_{FR} = 5V$ to $0V$, $V_{SEN} = 5V$
Turn off output voltage clamp	V_{DEMAG}	$V_{CC}-41$	$V_{CC}-46$	$V_{CC}-52$	V	$T_j = -40^\circ C$ to $150^\circ C$
CS pin to ground clamp voltage	V_{CSG_CL}		7		V	$I_{SENSE} = -1mA$, $V_{CC} = 13V$
Current Sense						
K_0		-30%	1200	30%		$I_{OUT} = 0.01A$ to $0.05A$, $V_{sense} = 0.5V$

Parameters	Symbol	Min	Typ	Max	Unit	Comments
K ₁	I _{OUT} /I _{SEN}	-25%	1200	25%		I _{OUT} = 0.2A, V _{SENSE} = 0.5V
K ₂		-20%	1200	20%		I _{OUT} = 0.4A, V _{SENSE} = 4V
K ₃		-15%	1200	15%		I _{OUT} = 1.5A, V _{SENSE} = 4V
K ₄		-10%	1200	10%		I _{OUT} = 4.5A, V _{SENSE} = 4V
CS pin leakage current	I _{SENSE0}			0.5	μA	V _{SEN} = 0V
		-0.5		0.5		V _{SEN} = 0V, -1V < V _{SENSE} < 5V
				2		V _{SEN} = 5V, I _{OUTX} = 0A, V _{INPUT0,1,2,3} = 5V, channel diagnostic selected
				2		V _{SEN} = 5V, I _{OUTX} = 0A, V _{INPUT0,1,2,3} = 0V, channel diagnostic selected
Output voltage for CS shutdown	V _{OUT_MSD}		5		V	V _{SEN} = 5V, R _{SENSE} = 2.7kΩ, I _{OUT} = 2A
CS saturation voltage	V _{SENSE_SAT}		5.5		V	VCC = 7V, V _{SEN} = 5V, R _{SENSE} = 2.7kΩ, I _{OUT} = 4.5A
CS saturation current	I _{SENSE_SAT}	4			mA	VCC = 7V, V _{SEN} = 5V, V _{SENSE} = 4V, V _{INPUT} = 5V, T _j = 150°C
Output saturation current	I _{OUT_SAT}	4.8			A	VCC = 7V, V _{SEN} = 5V, V _{SENSE} = 4V, V _{INPUT} = 5V, T _j = 150°C
Off-state diagnostic						
Off-state open-load voltage detection threshold	V _{OL}	2	3	4	V	V _{SEN} = 5V, V _{INPUT} = 0V
Off-state output sink current	I _{L(off)}	-100		-15	μA	V _{INPUT} = 0V, V _{OUT} = V _{OL}
Off-state diagnostic delay time from falling edge of INPUT	t _{DSTKON}	100	350	700	μs	V _{SEN} = 5V, V _{INPUT} = 5V to 0V
Setting time for valid Off-state open-load diagnostic indication from rising edge of SEn	t _{D_OL_V}			60	μs	V _{SEN} = 0V to 5V
Off-state diagnostic delay time from rising edge of V _{OUT}	t _{D_VOL}		5	30	μs	V _{SEN} = 5V, V _{INPUT} = 0V, V _{OUT} = 0V to 4V
Fault diagnostic						
CS pin output voltage in fault condition	V _{SENSEH}	5		6.6	V	
CS pin output current in fault condition	I _{SENSEH}	7	20	30	mA	

Parameters	Symbol	Min	Typ	Max	Unit	Comments
Current sense timings						
CS setting time from rising edge of SEn	t_{DSENSE1H}			60	μs	$V_{\text{SEn}} = 0\text{V to } 5\text{V}, V_{\text{INPUT}} = 5\text{V}, R_{\text{SENSE}} = 1\text{k}\Omega, R_{\text{L}} = 6.5\Omega$
CS disable time delay from falling edge of SEn	t_{DSENSE1L}		5	20	μs	$V_{\text{SEn}} = 5\text{V to } 0\text{V}, R_{\text{SENSE}} = 1\text{k}\Omega, R_{\text{L}} = 6.5\Omega$
CS setting time from rising edge of INPUT	t_{DSENSE2H}		100	250	μs	$V_{\text{SEn}} = 5\text{V}, V_{\text{INPUT}} = 0\text{V to } 5\text{V}, R_{\text{SENSE}} = 1\text{k}\Omega, R_{\text{L}} = 6.5\Omega$
CS setting time from rising edge of I_{OUT} (dynamic response to a step change of I_{OUT})	$\Delta t_{\text{DSENSE2H}}$			100	μs	$V_{\text{SEn}} = 5\text{V}, V_{\text{INPUT}} = 5\text{V}, R_{\text{SENSE}} = 1\text{k}\Omega, R_{\text{L}} = 6.5\Omega$
CS turn off delay time from falling edge of INPUT	t_{DSENSE2L}		50	250	μs	$V_{\text{SEn}} = 5\text{V}, V_{\text{INPUT}} = 5\text{V to } 0\text{V}, R_{\text{SENSE}} = 1\text{k}\Omega, R_{\text{L}} = 6.5\Omega$

Figure 1 Switching times and switching loss

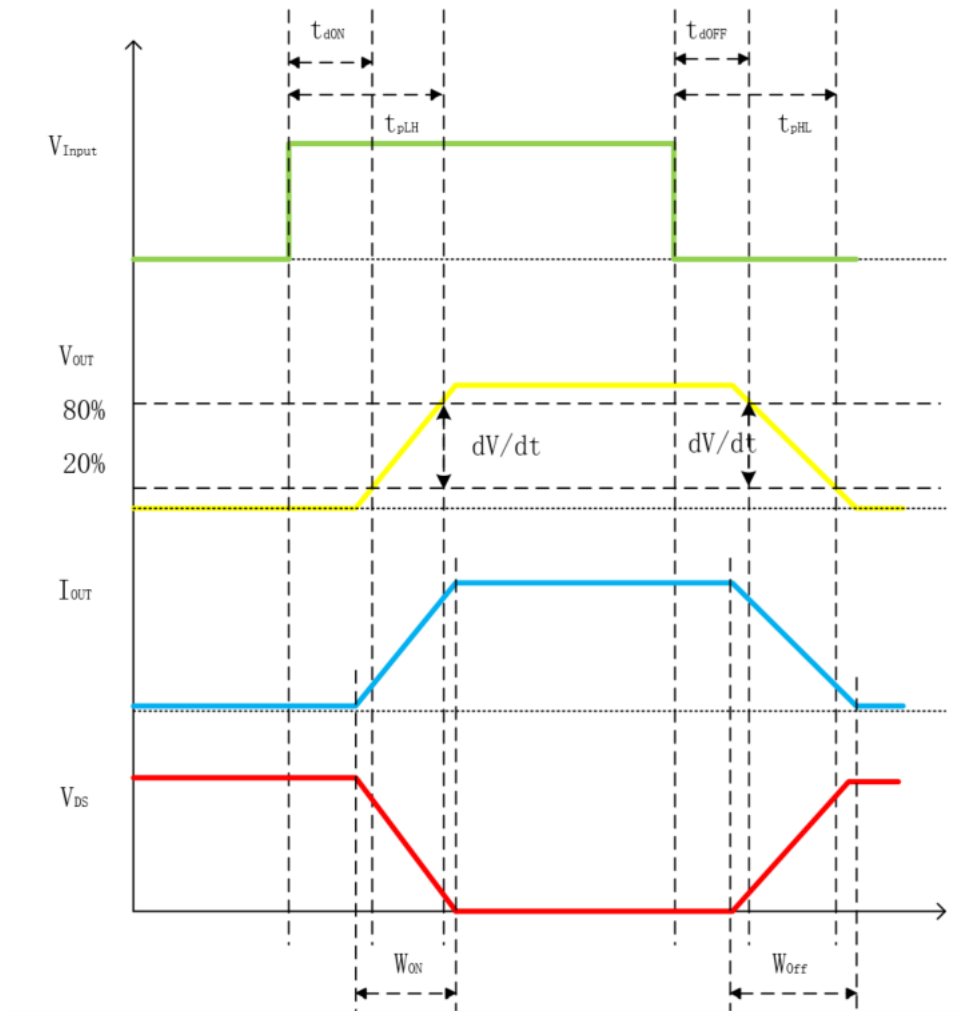


Figure 2 Off-state diagnostic delay time from falling edge of INPUT

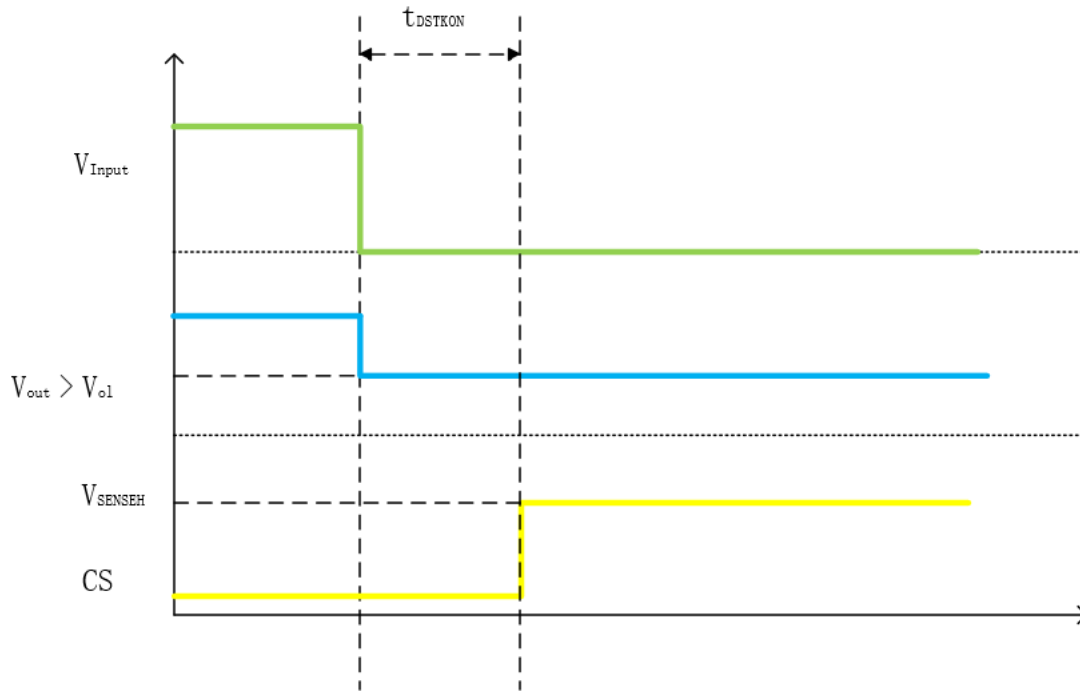


Figure 3 Off-state diagnostic delay time from rising edge of VOUT

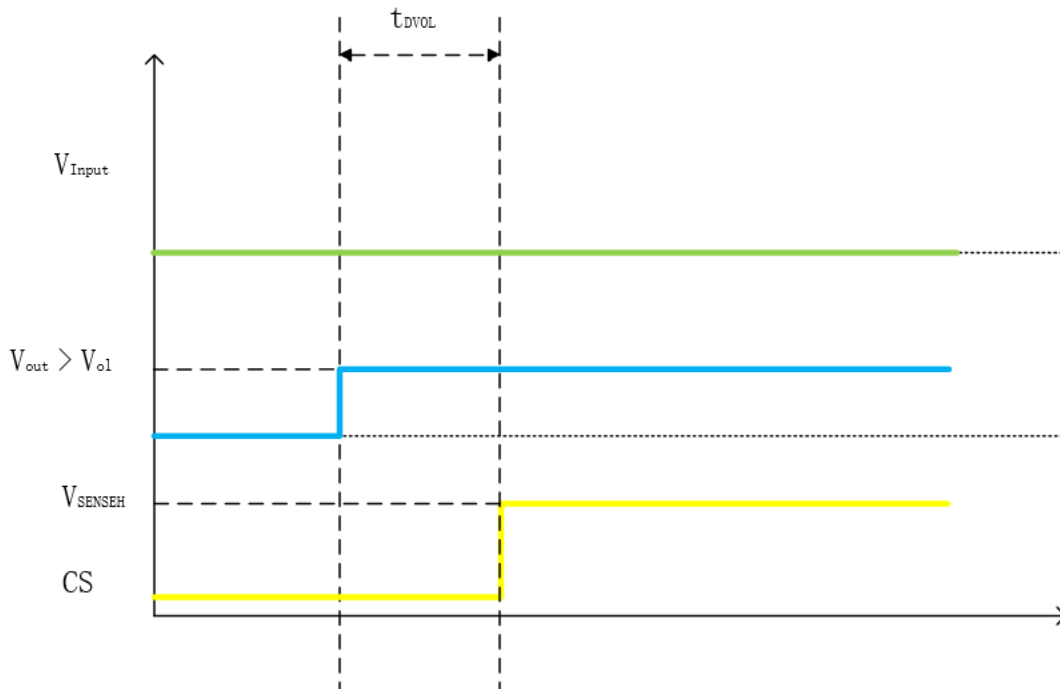
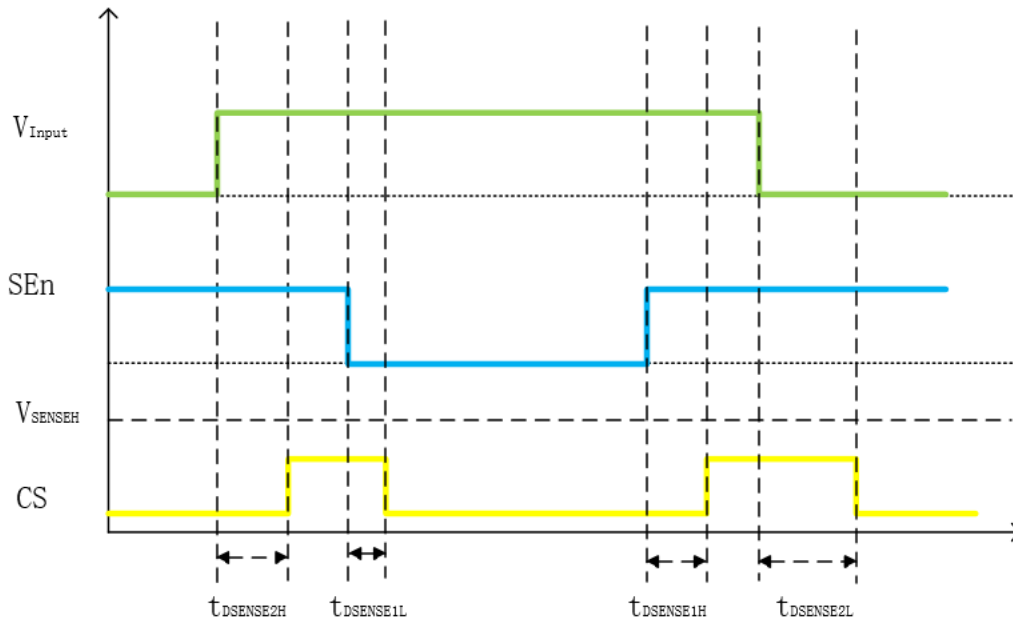


Figure 4 Current sense timing



6.2. Typical Performance Characteristics

6.2.1. True table

Mode	Conditions	IN_x	FR	SEn	SEL_x	OUT_x	CS	Comments
Standby	All logic inputs low	L	L	L	L	L	Hi-Z	
Normal	Nominal load connected, $T_j < 150^\circ C$	L	X	Refer to CS address	Refer to CS address	L	Refer to CS address	
		H	L			H	Refer to CS address	Outputs for auto-retry
		H	H			H	Refer to CS address	Outputs for latch-off
Overload	Overload or short to GND, $T_j > 175^\circ C$ or $\Delta T_j > 60k$	L	X	Refer to CS address	Refer to CS address	L	Refer to CS address	
		H	L			H	Refer to CS address	
		H	H			L	Refer to CS address	
Under voltage	$VCC < UVLO$ (falling)	X	X	X	X	L	Hi-Z	
Off-state diagnostics	Short to VCC	L	X	Refer to CS address	Refer to CS address	H	Refer to CS address	

Mode	Conditions	IN _x	FR	SEn	SEL _x	OUT _x	CS	Comments
	Open-load	L	X			H	Refer to CS address	External pull-up
Negative output voltage	Inductive load turn off	L	X	Refer to CS address		< 0V	Refer to CS address	

6.2.2. Current sense MUX address

SEn	SELO	SEL1	MUX channel	Normal mode	Overload	Off-state diag	Negative output
L	X	X		Hi-Z			
H	L	L	Channel 0	$I_{SENSE} = 1/K * I_{OUT0}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	L	H	Channel 1	$I_{SENSE} = 1/K * I_{OUT1}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	L	Channel 2	$I_{SENSE} = 1/K * I_{OUT2}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z
H	H	H	Channel 3	$I_{SENSE} = 1/K * I_{OUT3}$	$V_{SENSE} = V_{SENSEH}$	$V_{SENSE} = V_{SENSEH}$	Hi-Z

7. Protections

7.1. Current limitation

NSE34050Q-Q1 has current limitation to protect the silicon and bonding wire in case of overload or short circuit to ground. In order to allow a higher load inrush at low ambient temperature, Overload threshold is related with VDS and temperature.

Figure 5 Overload current threshold VS VDS

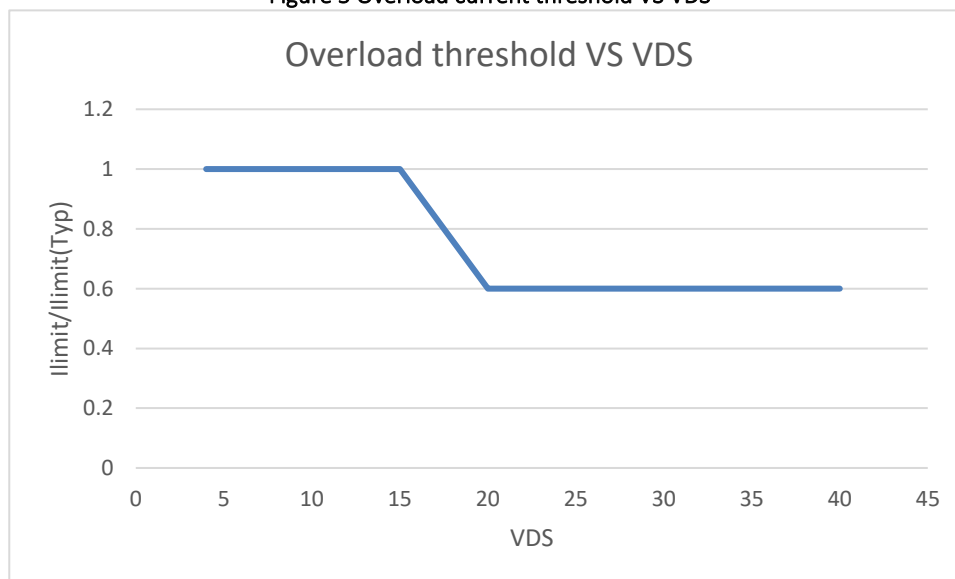
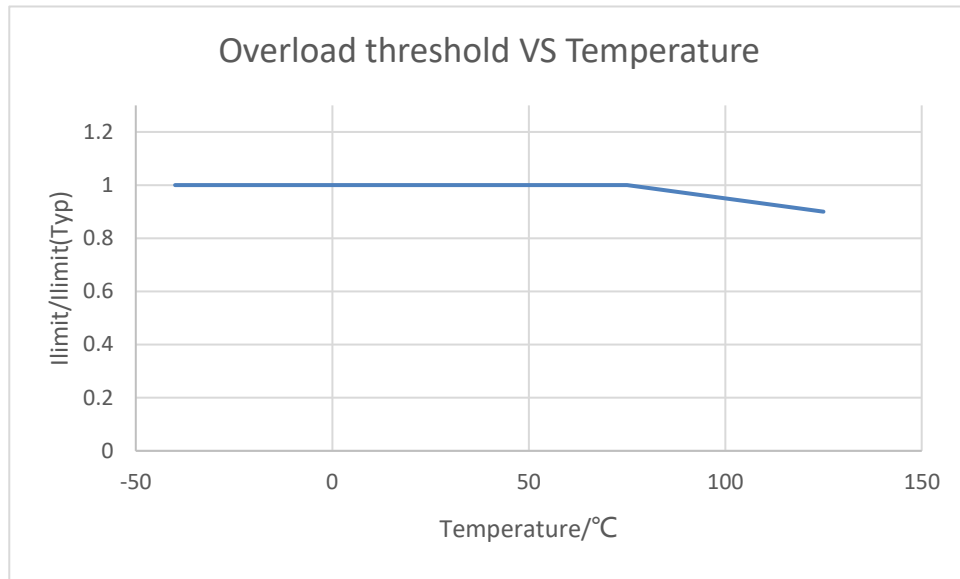


Figure 6 Overload current threshold VS temperature



7.1.1. Retry strategy

While the FaultRST pin is set to low, NSE34050 works in auto-retry mode. Then the channel can be allowed to restart only if all retry conditions have been fulfilled in case of fault condition.

In the fault condition, the channel will switched on for $n_{RETRY(CR)}$ times then switch off, after a time t_{RETRY} , the channel will switch on for $n_{RETRY(CYC)}$ retry cycles then latch off. It is necessary to set the input pin to low for a time longer than $t_{DELAY(CR)}$ to reset the internal counter to unlatch the channel. The auto-retry timing is shown in Figure 7 and the latch-up timing is shown in Figure 8.

Figure 7 Auto-retry timing

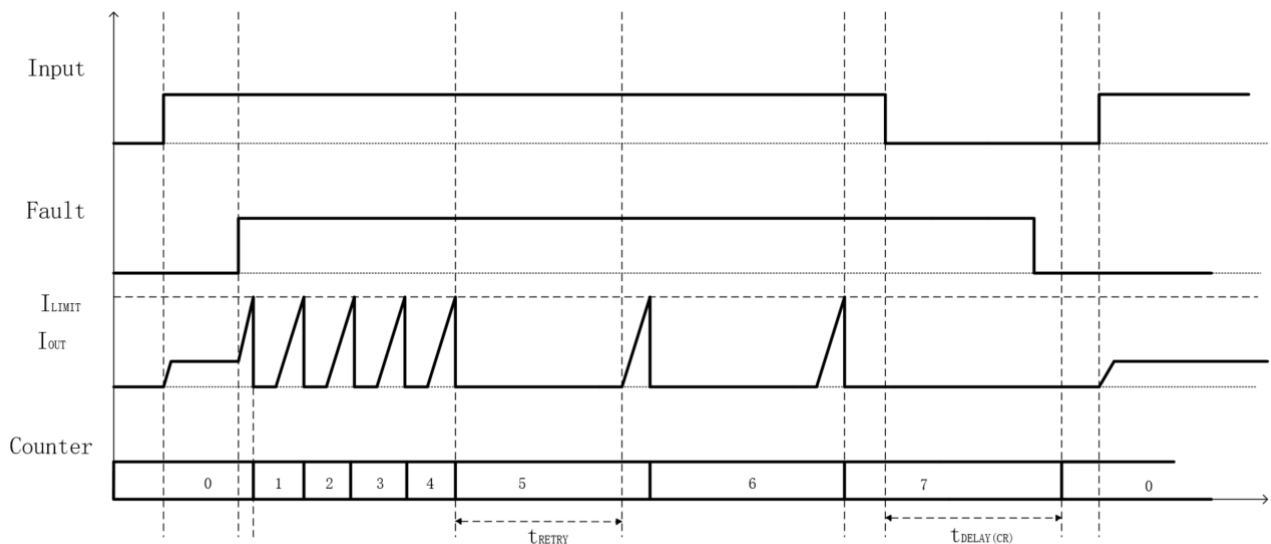


Figure 8 Latch-up timing

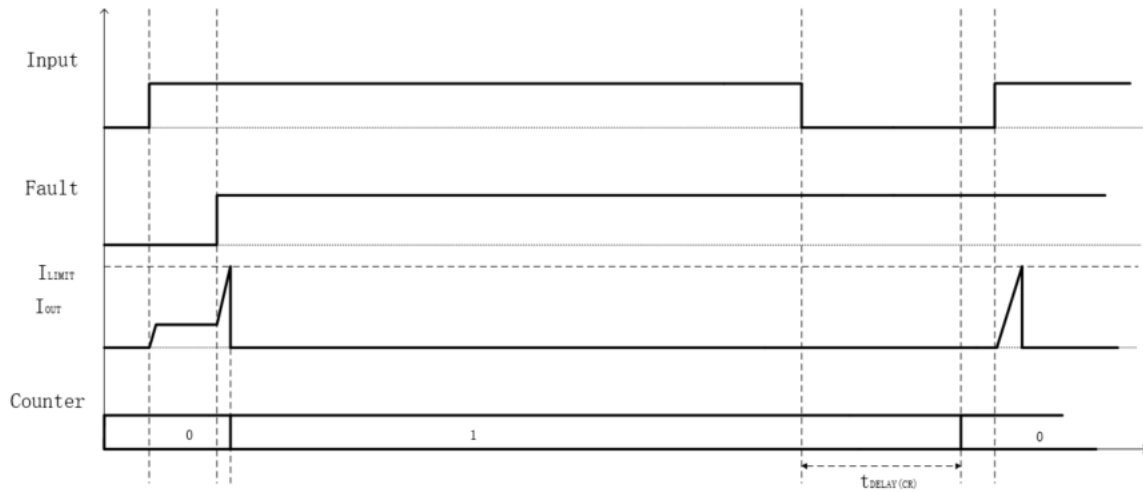
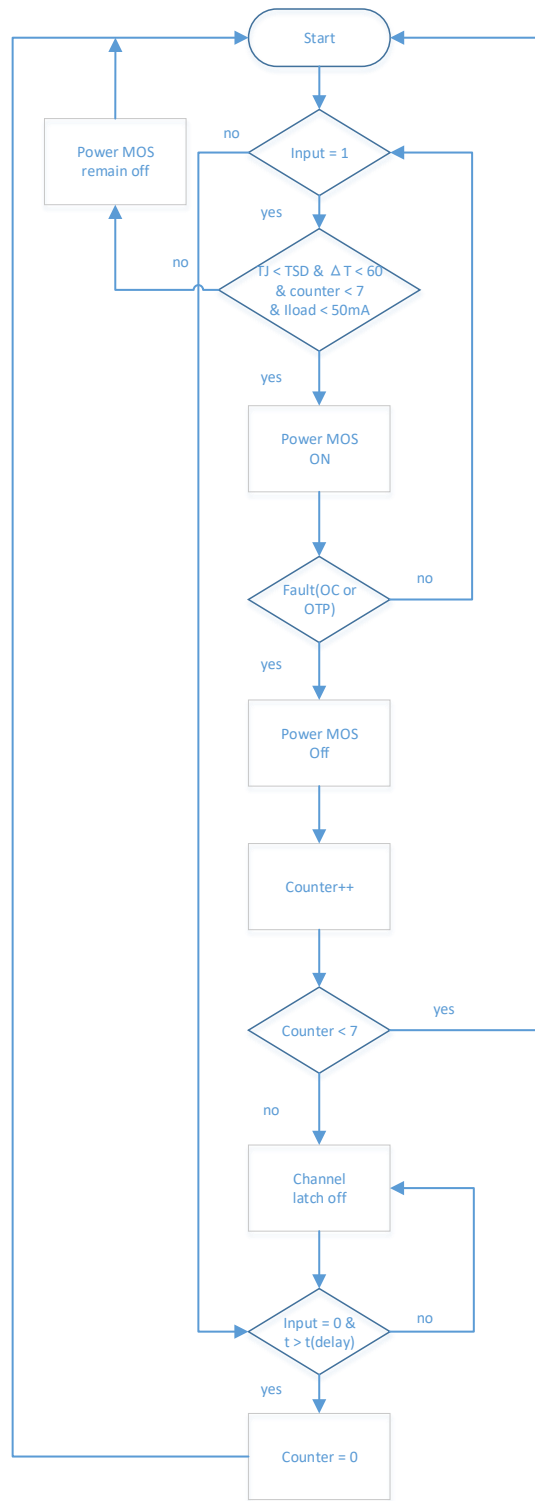


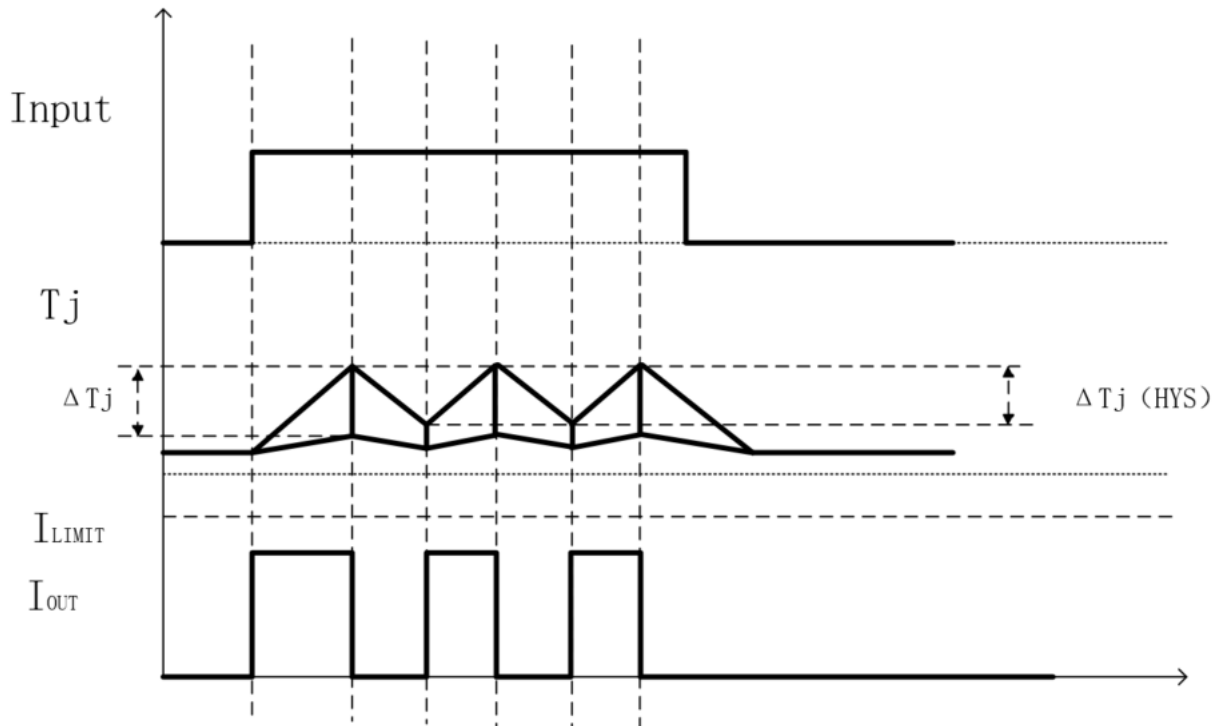
Figure 9 Retry strategy



7.2. Thermal shutdown and thermal swing

This device has both absolute and dynamic temperature protection. There are two thermal sensors on the controller and the MOSFET, the one on the MOSFET is the hottest and the one on the controller is the coldest. The absolute temperature protection is to shutdown the MOSFET when the hottest junction temperature exceeds the T_{TSD} , and the dynamic temperature protection is also to shutdown the MOSFET when the temperature difference between the hottest and the coldest exceeds ΔT_j .

Figure 9 Thermal swing



7.3. Inductive load voltage clamp

In the case device turns off when driving inductive load, the voltage between VCC and output will exceed VCC. VDS should be clamped to limit the voltage to protect the power MOSFET from breakdown. The clamp voltage is lower than BVDSS of the MOSFET, the energy of inductor is dissipated without damaging the device.

7.4. Reverse polarity protection

In reverse polarity condition, the device will switch on the power MOSFET, so that to reduce the power dissipation on the power MOSFET, which is limited by the load. If power MOSFET is off, reverse current will pass through body diode and cause more power dissipation which may damage the device. What's more, the device integrate a diode in the GND, so that it is not necessary to place a diode outside the GND pin to avoid the reverse current.

7.5. Loss of battery and loss of ground protection

When the load is inductive, then battery is loss of connection, it is recommended to place an external diode to handle the energy of inductor when loss of battery.

In case of loss ground, the power MOSFET will be ensured to switch off to avoid MOSFET on by mistake.

8. Application information

9. Electrical characteristics curves

10. Immunity against transient electrical disturbances

11. Package and PCB thermal data

12. Package Information

12.1. PowerSSO-16

13. Revision history

Revision	Description	Date
0V1	Initial version	2021/08
0V2	Some updates and add true table	2021/09
0V3	Add application information	2021/12
0V5	Market pre-release	2022/04