Zbit 32Gb SD NAND Datasheet

ZBSD32GBYIGY

Rev 1.2

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Contents

1. Overview

1.1 Product Description

Zbit SD NAND are highly integrated flash memories with serial and random access capability. Can be use in the device which can support SD2.0/6.0 standard. It is accessible via a dedicated serial interface optimized for fast and reliable data transmission. It has been developed to provide an inexpensive, mechanically robust storage medium in card form for multimedia consumer applications. Zbit SD NAND card allows the design of inexpensive players and drivers without moving parts. A low power consumption and a wide supply voltage range favors mobile, battery-powered application such as audio players, organizers, palmtops, electronic books, encyclopedia and dictionaries. Using very effective data compression schemes such as MPEG, the SD card will deliver enough capacity for all kinds of multimedia data.

1.2 Features Summary

- Capacity: 32Gb
- Complies to SD Specification V2.0/6.0
- Voltage range for communication: 2.7~3.6V
- Variable clock rate 0-25 MHz (standard), 0-50 MHz (high performance)
- Up to 25 MB/sec data transfer rate (using four parallel data lines)
- Operating Temperature: -25°C to +85°C
- Storage Temperature: -40°C to +105°C
- Standby Current：< 250uA
- Password protection (CMD42-LOCK_UNLOCK)
- Sophisticated system for error recovery including a powerful ECC
- Global Wear Leveling
- Power management for low power operation

2. Pin Assignment

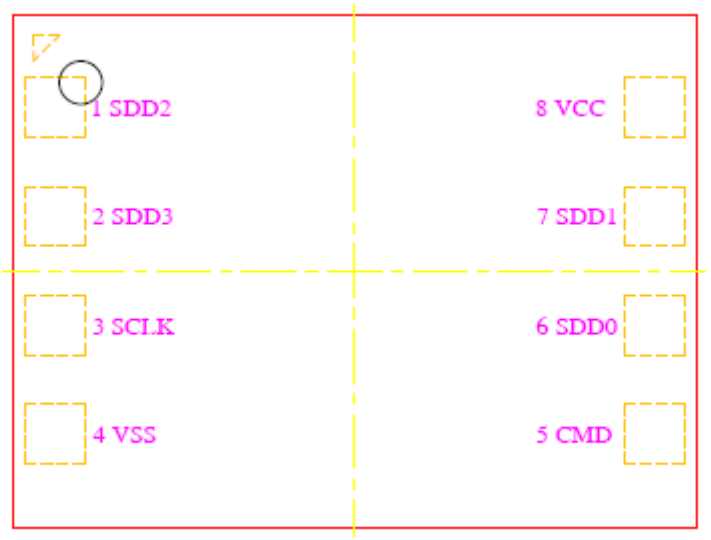


Figure 1:Top View

Pin No.	SD Mode		
	Name	Type	Description
1	SDD2	I/O/PP	Data Line [Bit 2]
2	SDD3	I/O/PP	Data Line [Bit 3]
3	SCLK	I	Clock
4	VSS	S	Supply voltage ground
5	CMD	PP	Command/Response
6	SDD0	I/O/PP	Data Line [Bit 0]
7	SDD1	I/O/PP	Data Line [Bit 1]
8	VCC	S	Supply voltage

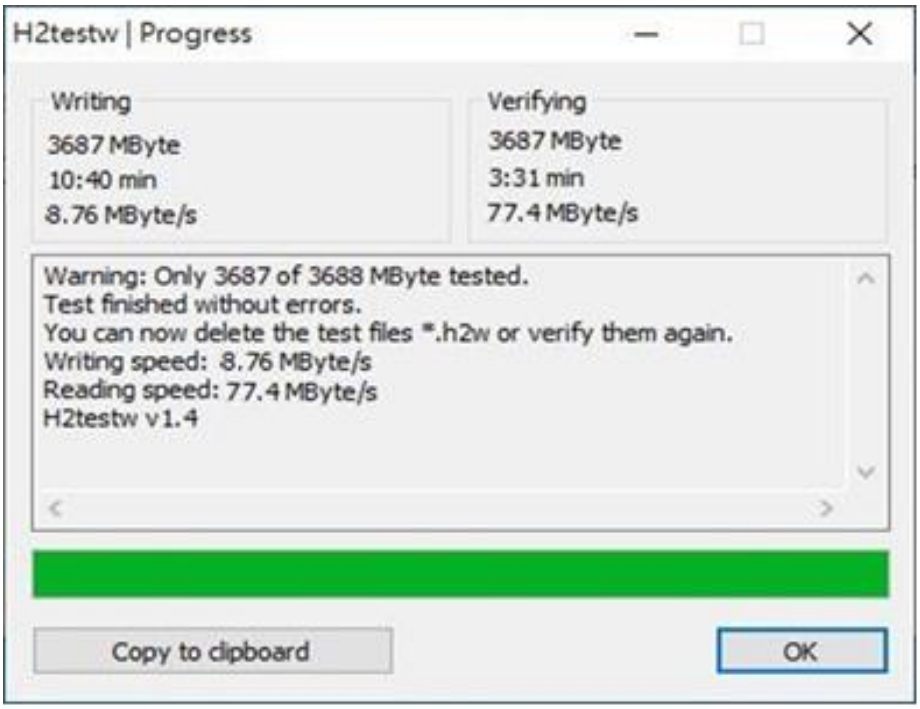
Table 1: Pin Assignment

1) S: power supply.
2) I: input; O: output using push-pull drivers.
3) PP: I/O using push-pull drivers.
4) The extended SDD lines (SDD1-SDD3) are input on power up. They start to operate as SDD lines after SET_BUS_WIDTH command. The Host shall keep its own SDD1-SDD3 lines in input mode, as well, while they are not used. It is defined so, in order to keep compatibility to SD NAND.
5) After power up this line is input with 50KOhm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

3. Product List

Part Number	Density	User Density	Sequential R/W	Package
ZBSD32GBQIGY	32Gb	3687MB	77/9 MB/s	6.6*8 (mm)

Table 2: Product List



Note: Measurement based on AU6437 card reader, H2Test V1.4 software, Win10 OS

4. Current Consumption

Symbol	Parameter	Conditions	Min	Typ	Max	Units
VIL	Input low voltage		VSS-0.3		0.25VCC	V
VIH	Input high voltage		0.635VCC		VCC+0.3	V
VOL	Output low voltage	IOL=100uA@VCC_min				V
VOH	Output high voltage	IOH=100uA@VCC_min	0.75VCC			V
IIN	Input leakage	VIN=VCC or 0	-10	±1	10	μA
IOUT	Tri-state output leakage current	/	-10	±1	10	μA
ISTBY	Standby current	Clock stop		0.1	0.2	mA

IOP	Operation current	3.3V@50MHz Write		15	25	mA
		3.3V@50MHz Read		10	20	mA
Vrs	Input Voltage Setup Time	From 0V to VDD min			250	ms

Note：Test condition: RTS5308 card reader (Voltage 3.3V), Fluke289c multi-meter.

Peak Voltage and Leak Current

Parameter	Conditions	Min	Max	Units
Peak voltage on all line	/	-0.3	VDD+0.3	V
Input Leakage Current	/	-10	10	uA
Output low voltage	/	-10	10	uA

Signal Capacitance

Symbol	Parameter	Min	Max	Units
RCMD RDAT	Pullup Resistance	10	100	KΩ
CL	Total bus capacitance for each signal line	/	40	pF
CCARD	Card capacitance for signal pin	/	10	pF
RDAT3	Pull up Resistance inside card (pin1)	10	90	KΩ
CC	Capacity Connected to Powerline	/	5	uF

5. Operational Environment

Parameter	Range	
Temperature	Operating	-25℃~85℃
	Non-Operating	-40℃~105℃
Humidity	Operating	25% to 85%, non-condensing
	Non-Operating	25% to 85%, non-condensing
Electrostatic Discharge (ESD)	IEC 61000-4-2 contact discharge: +/- 2[kV] and +/- 4[kV] 150[pF],330[Ohm] air discharge: up to +/- 15[kV] 150[pF], 330[Ohm]	

Table 3: Operational Environment

6. Bus Timing

6.1 Default Mode

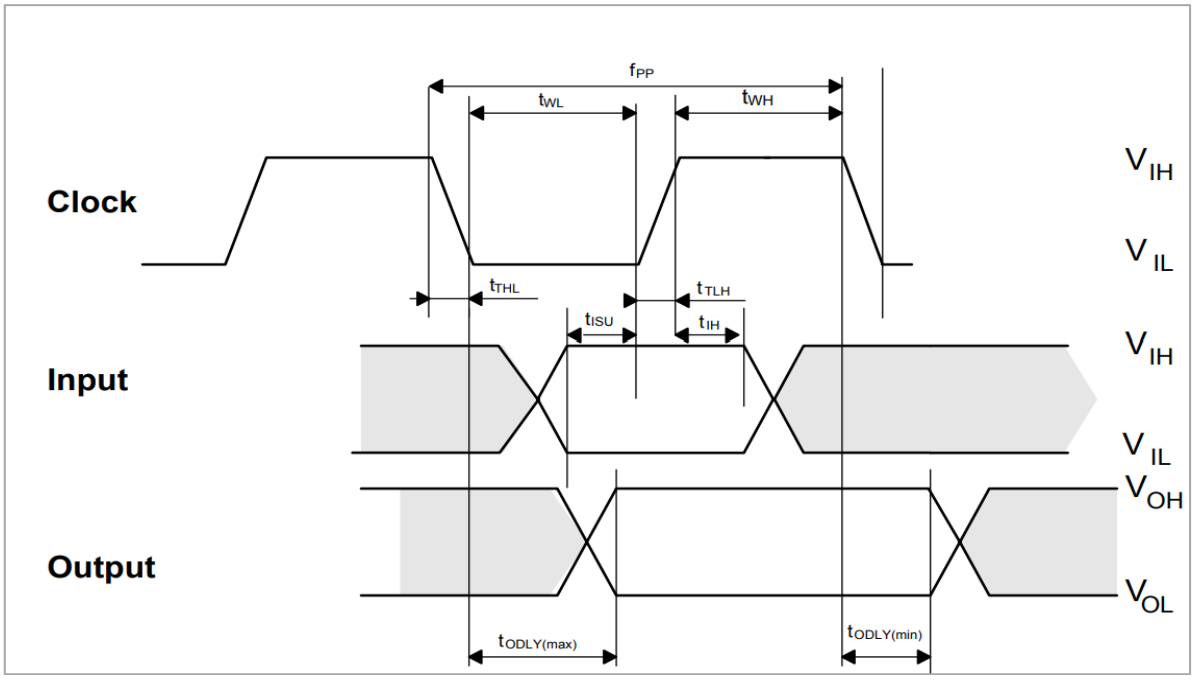


Figure 2: Timing Diagram Data Input/Output Referenced to Clock (Default)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min（VIH）and max（VIL））					
Clock frequency data transfer Mode	fpp	0	25	MHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	10		ns	
Clock high time	t_{WH}	10		ns	
Clock rise time	t_{TLH}		10	ns	
Clock fall time	t_{THL}		10	ns	
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	5		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH}	5		ns	
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	0	14	ns	CL ≤ 40pF (1 card)
Output Hold time	t_{OH}	0	50	ns	

Note: 0 Hz means to stop the clock.The given minimum frequency range is for cases were continues clock is required.

Table 4: Bus Timing-Parameters Values (Default Speed)

6.2 High Speed Mode

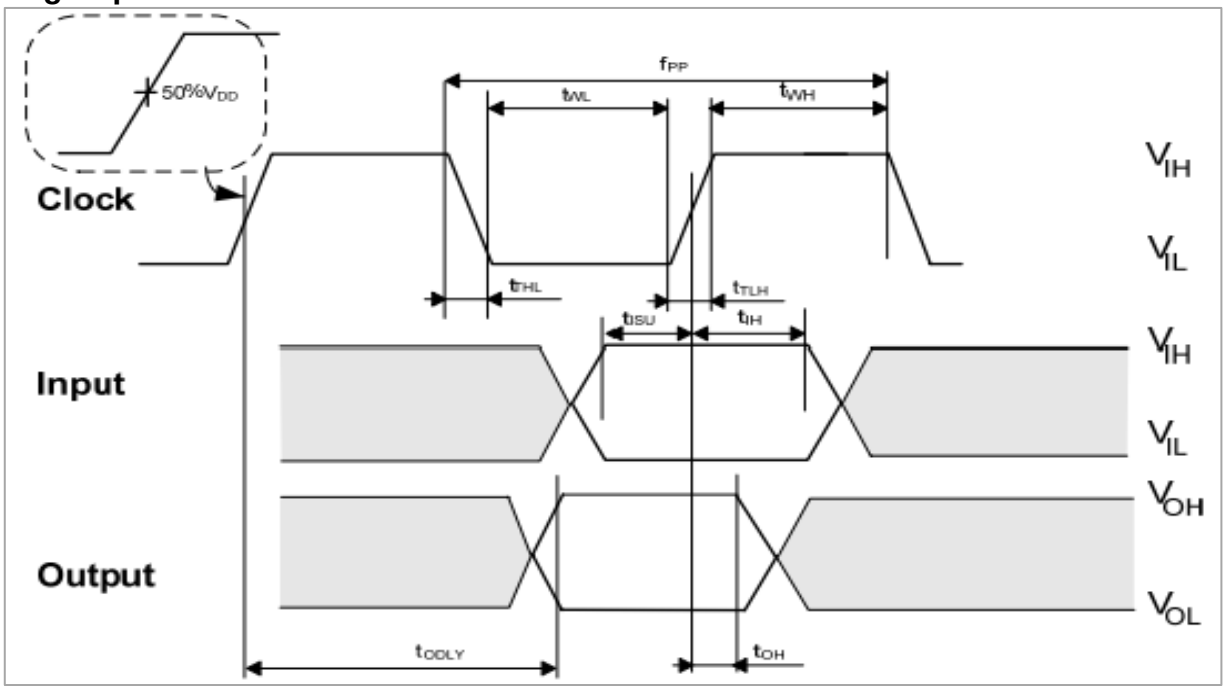


Figure 3: Timing Diagram Data Input/Output Referenced to Clock (High-Speed)

Parameter	Symbol	Min.	Max	Unit	Remark
Clock CLK （All values are referred to min（VIH）and max（VIL））					
Clock frequency data transfer Mode	fpp	0	50	MHz	C_{CARD} ≤ 10pF (1 card)
Clock low time	t_{WL}	7		ns	
Clock high time	t_{WH}	7		ns	
Clock rise time	t_{TLH}		3	ns	
Clock fall time	t_{THL}		3	ns	
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	6		ns	C_{CARD} ≤ 10pF (1 card)
Input hold time	t_{IH}	2		ns	
Outputs CMD, DAT (referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}		14	ns	CL ≤ 40pF (1 card)
Output Hold time	t_{OH}	2.5		ns	CL ≥ 15pF (1 card)
Total System capacitance for each line[1]	CL		40	pF	1 card

Note: In order to satisfy sever timing, the host shall drive only one card.

Table 5: Bus Timing – Parameters Values (High Speed)

7. Power Up

7.1 Power Up Diagram

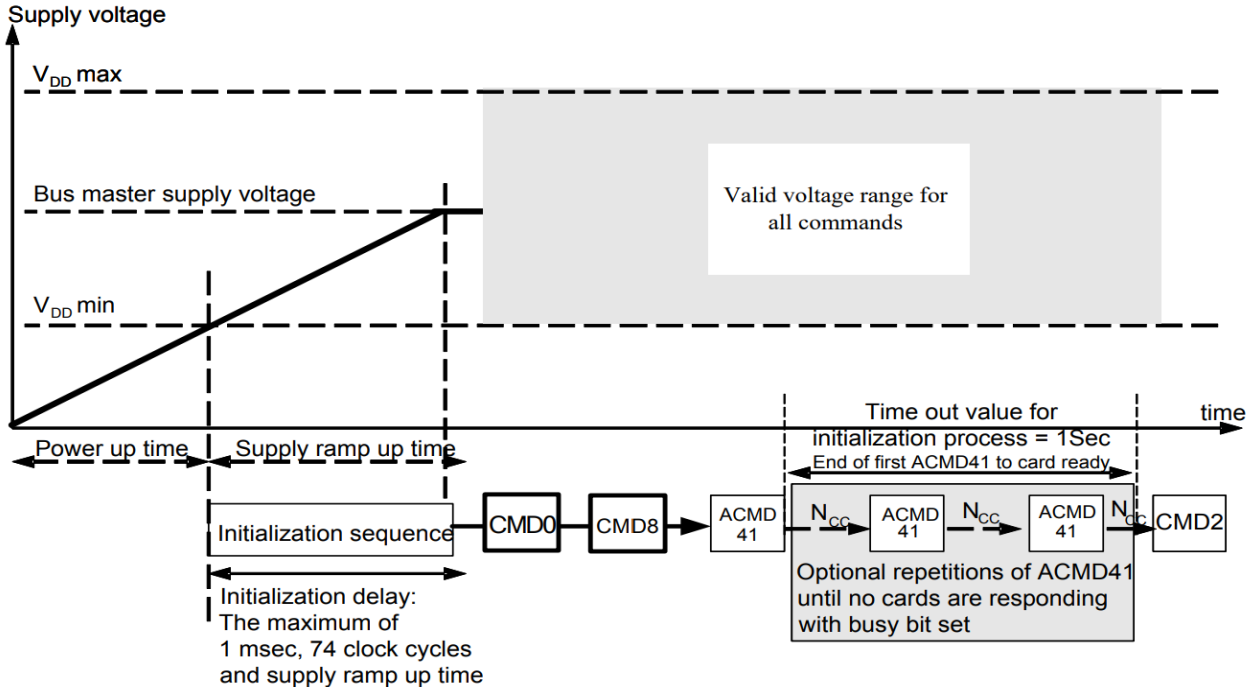


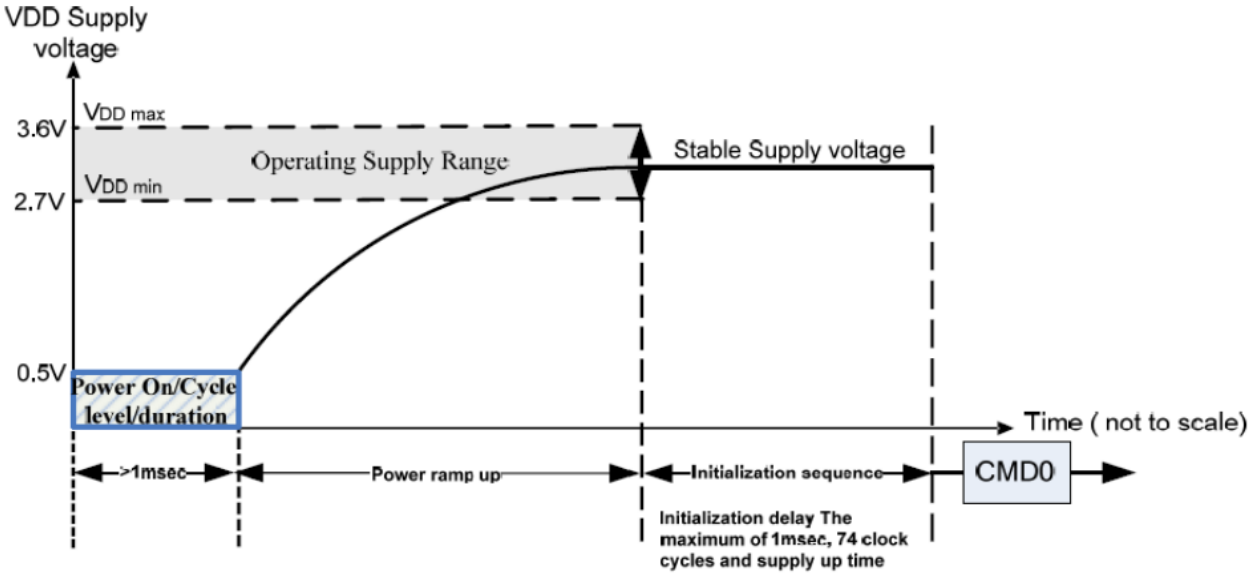
Figure 4: Power-up Diagram

Note:

1) Power up time' is defined as voltage rising time from 0 volt to VCC min.
2) Supply ramp up time' provides the time that the power is built up to the operating level (Host Supply Voltage) and the time to wait until the SDNAND can accept the first command.
3) The host shall supply power to the SDNAND so that the voltage is reached to Vcc_min within 250ms and start to supply at least 74 SD clocks to the SD NAND with keeping CMD line to high.

7.2 Power Up Time

Host needs to keep power line level less than 0.5V and more than 1ms before power ramp up.



1) Followings are requirements for Power on and Power cycle to assure a reliable SD NAND hard reset.

- Voltage level shall be below 0.5V
- Duration shall be at least 1ms

2) The power ramp up time is defined from 0.5V threshold level up to the operating supply voltage which is stable between VCC (min.) and VCC (max.) and host can supply SDCLK. Followings are recommendation of Power ramp up:

- Voltage of power ramp up should be monotonic as much as possible.
- The minimum ramp up time should be 0.2ms.
- The maximum ramp up time should be 50ms for 2.7-3.6V power supply.

3) When the host shuts down the power, the VCC shall be lowered to less than 0.5Volt for a minimum period of 1ms. During power down, DAT, CMD, and CLK should be disconnected or driven to logical 0 by the host to avoid a situation that the operating current is drawn through the signal lines.

4) If the host needs to change the operating voltage, a power cycle is required. Power cycle means the power is turned off and supplied again. Power cycle is also needed for accessing SDNAND that are already in Inactive State. To create a power cycle the host shall follow the power down description before power up the SD NAND (i.e. the VCC shall be once lowered to less than 0.5Volt for a minimum period of 1ms)

8. Physical Dimension

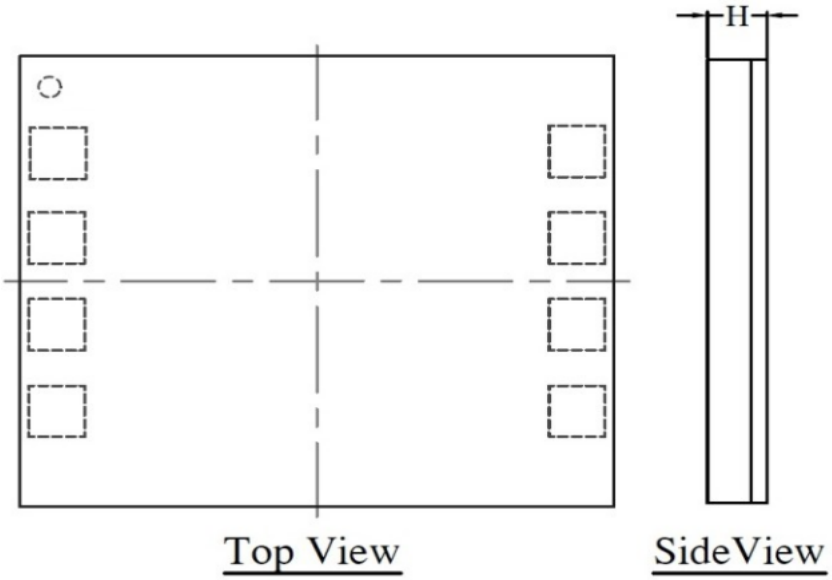


Figure 5:Top View and Side View

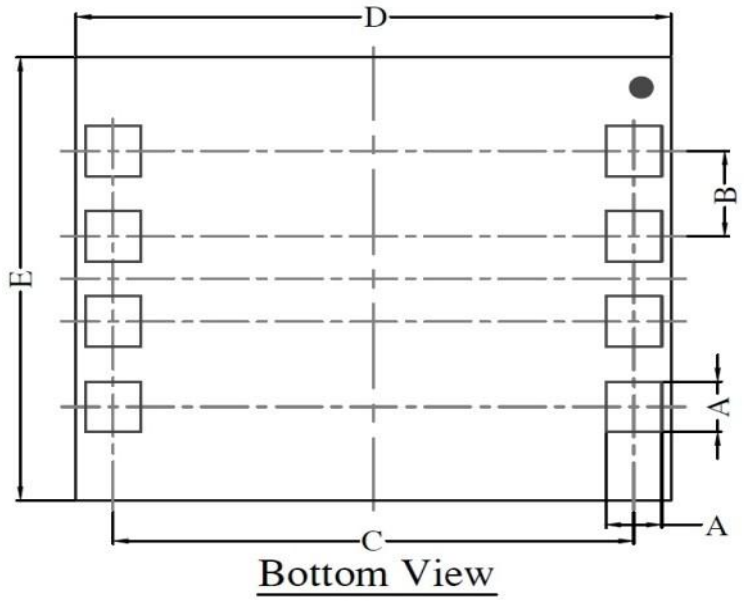


Figure 6: Bottom View

Common Dimensions				
Symbol	Min	Nom	Max	Note
A	0.65	0.75	0.85	
B	1.17	1.27	1.37	
C	6.90	7.00	7.10	
D	7.90	8.00	8.10	
E	6.50	6.60	6.70	
H	0.75	0.85	0.95	

SDNAND Package Dimensions (unit : mm)

Table 6: Zbit SD NAND Package: Dimension

9. Recommended Schematic

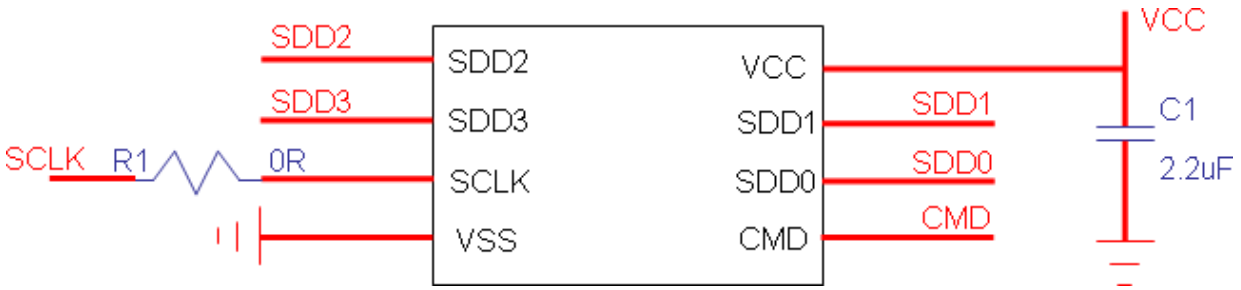
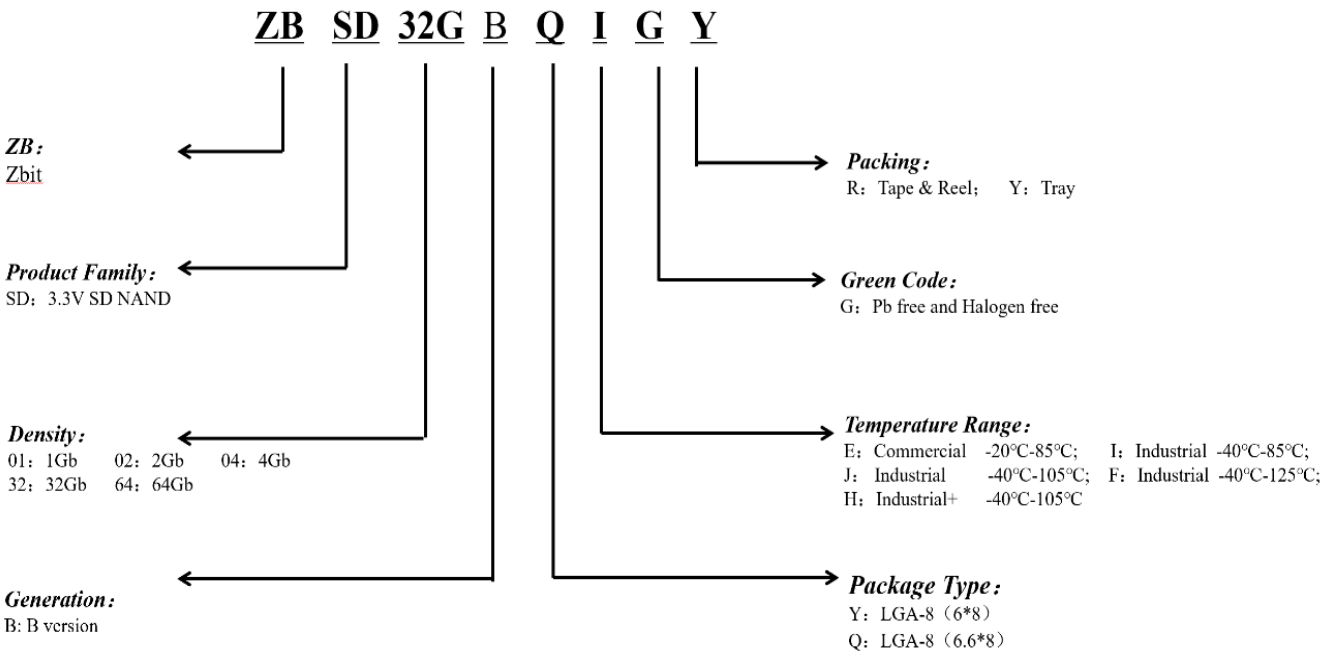


Figure 7: Recommended Schematic

Note:

1) SCLK should be reserved a position for a 0 ohm resistor.
2) Capacitor C1 should be connected with VCC as closely as possible.
3) We recommend that SDD0, SDD1, SDD2, SDD3, SCLK, CMD should be surrounded by GND. If not, please make sure the distance between lines is 2 times wider than the line width.

10. Ordering information



11. Revision History

Version No	Change Description	Date
V1.0	Initial release	2023/5
V1.1	Add Bus Timing info	2024/12
V1.2	Update the product info	2025/05