PE4 series

Enterprise-grade PCIe SSD

Specifications

Capacity
- U.2: 960 GB~7680 GB
- E1.S: 960 GB~7680 GB
- M.2 2280: 960 GB~7680 GB
- M.2 2242: 240 GB~1920 GB
- M.2 2230: 240 GB~960 GB

Components
- Controller: Marvell 88SS1321
- Flash: 1.2GHz 3D TLC
- DRAM: DDR4

Compliance
- PCIe Gen4x4/ Gen4x2/ Gen3x4
- Surprise insertion / surprise removal (SISR) and hot-plug capable (U.2/E1.S support)

Performance (up to)[1]
- Sequential read: 3,500 MB/s
- Sequential write: 3,000 MB/s
- Random 4K read: 400,000 IOPS
- Random 4K write: 50,000 IOPS

Power management
- Auto idle
- PCIe link power management
- Temperature monitoring and throttling

Security
- NVM Format
- Support SED (TCG/AES) (Optional)

Reliability
- Advanced LDPC error correction
- Global static and dynamic wear leveling
- Hardware Power Loss Protection (PLP)
  (For U.2 & E1.S form factor, customized for M.2 2280 and support to 3840GB)
- UBER: <1 sector per 10^{17} bits read
- MTBF: 2.0 million hours

Physical insertion cycles
- Nominal: 2000 (Optional: 5000)

Endurance[2]
- 0.6 DWPD @5 Years
  (Sequential workload: 1.5 DWPD @5 Years)
- TBW:
  - 240GB: 250TB / 480GB: 500TB
  - 960GB: 1000TB / 1920GB: 2000TB
  - 3840GB: 4000TB / 7680GB: 8000TB

Data retention
- JESD218A-compliant

Compatibility
- Windows 11/10/8.1/7
- Windows Server 2016/2012 R2/2012
- CentOS, Fedora, FreeBSD, openSUSE, Red Hat, Ubuntu, VMware ESXi, Citrix, KVM

Mechanical form factor
- U.2: 100.5 mm x 69.85 mm x 7 mm
- M.2 2280: 80 mm x 22 mm x 3.5 mm
- M.2 2242: 42 mm x 22 mm x 3.5 mm
- M.2 2230: 30 mm x 22 mm x 2.15 mm
- E1.S: 111.49 mm x 31.5 mm x 5.9 mm

Power consumption (TYP)
- Max: <12.0 W
- Active: <7.0 W
- Idle: <1.0 W

Environment
- Operating temperature: 0–70 °C
- Storage temperature: -40–85 °C

Shock & vibration
- Operating: 50 G
  (11 ms duration, half sine wave)
- Non-operating: 1500 G
  (0.5 ms duration, half sine wave)
- Vibration: 10 G
  (peak,10–2000 Hz)

Warranty
- 5-year limited warranty[3]

Specification notes:

1. Performance claims
    a. Actual performance may vary based on the hardware, software, and overall system configuration.
    b. Sequential performance is measured with 128 KB transfer size, QD 32 and 4 KB alignment with Iometer.
    c. Random performance is sustained performance measured with 4K/8K transfer size, QD 32 and 4 KB alignment with Iometer.
    d. Performance test platform: CPU: Intel Core i7 4770K; motherboard: ASUS Z87-DELUXE; chipset: Intel Z87 Express; OS: Windows 8.1 Pro x64.
2. Endurance claims
    a. DWPD stands for Drive Writes Per Day. TBW = DWPD * capacity * warranty * 365 / 1000.
    b. Access patterns used for random workload during endurance testing is compliant with the JESD219 standard.
3. Limited warranty details: please refer to limited warranty policy and warranty terms.

Table of Contents

Product datasheet

1. Order information

The following table lists the standard part numbers for Exascend PE4 series SSDs. For customization and design service inquiries, including – but not limited to – custom operating temperature, capacity, over-provisioning, endurance, performance, and power, please contact your Exascend account manager or send us an email at sales@exascend.com.

Table 1: PE4 series SSD product list

PART NUMBER	CAPACITY*	FLASH TYPE	FORM FACTOR
EXPE4R240GB	240GB *	3D TLC	M.2 2230
EXPE4R480GB	480GB *	3D TLC	M.2 2230
EXPE4R960GB	960GB *	3D TLC	M.2 2230
EXPE4Q240GB	240GB *	3D TLC	M.2 2242
EXPE4Q480GB	480GB *	3D TLC	M.2 2242
EXPE4Q960GB	960GB *	3D TLC	M.2 2242
EXPE4Q1920GB	1920GB *	3D TLC	M.2 2242
EXPE4M960GB	960GB *	3D TLC	M.2 2280
EXPE4M1920GB	1920GB *	3D TLC	M.2 2280
EXPE4M3840GB	3840GB *	3D TLC	M.2 2280
EXPE4M7680GB	7680GB *	3D TLC	M.2 2280
EXPE4U960GB	960GB *	3D TLC	U.2
EXPE4U1920GB	1920GB *	3D TLC	U.2
EXPE4U3840GB	3840GB *	3D TLC	U.2
EXPE4U7680GB	7680GB *	3D TLC	U.2
EXPE4U15360GB	15360GB *	3D TLC	U.2
EXPE4E960GB	960GB *	3D TLC	E1.S
EXPE4E1920GB	1920GB *	3D TLC	E1.S
EXPE4E3840GB	3840GB *	3D TLC	E1.S
EXPE4E7680GB	7680GB *	3D TLC	E1.S

2. Part number decoder

1	2	3	4	5	6
EX	PE4	R	240GB	-	**

1. Exascend

2. Product series

(SC1/SC3/PC3/PC4/SE1/SE3/PE3/PE4/SI2/SI3/PI3/PE4/PI4)

3. Form factor

(A=2.5”; B=mSATA; M=M.2 2280; P=M.2 2260; Q=M.2 2242; R=M.2 2230; U=U.2; E=E1.S)

4. Capacity

5. Hyphen

6. Identifier (H= extended temp, WP= with PLP)

3. Product overview

3.1 PE4 series

Exascend provides customizable hardware and firmware design, manufacturing, and service of cutting-edge SSD products and advanced storage systems. Our products are designed specifically for high reliability commercial, enterprise data center, and cloud computing applications. By combining world class design R&D, and superior execution in delivery and support capabilities, Exascend strives to provide customers with the best in class product and service, enabling enhanced boot times, faster application load times, reduced power consumption and extended reliability.

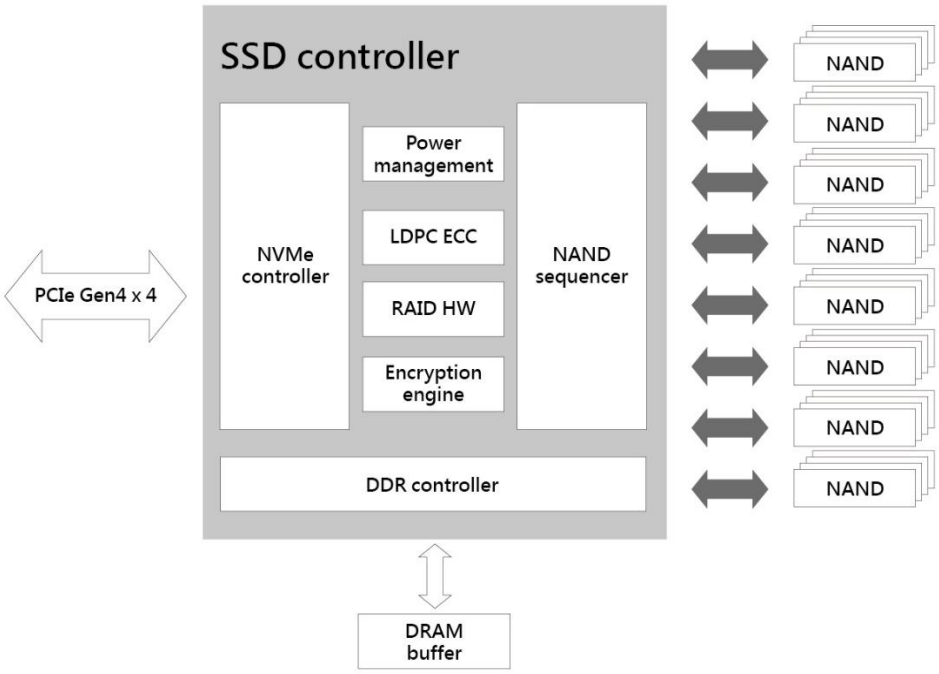
PE4 series product supports U.2, E1.S, and M.2 form factors, integrating high speed PCIe Gen 4 x 4 interface with third generation 3D TLC NAND flash memory technology, delivering capacities up to 8TB.

PE4 series products are offered in two product categories with different over-provisioning.

Key product highlights include:

- High I/O and throughput performance
- Next generation LDPC technology secures NAND endurance
- Advanced Flash management and global wear leveling algorithm extending drive life
- High stability and reliability
- Temperature monitoring and intelligent management

Figure 1: SSD functional logic diagram



3.2 Customization and tuning services

Exascend provides customized hardware and firmware design services, tailoring cutting-edge SSD products for advanced storage systems. Combining world-class R&D and engineering support capabilities, Exascend provides customers with best-in-class products and services, enabling enhanced boot times, faster-loading applications, reduced power consumption, and extended reliability. To learn more about our extended engineering support services, e.g., tailored capacity, over-provisioning, extended operating temperature range, endurance, performance, power, and longevity, please contact your Exascend account manager or send us an email at sales@exascend.com.

4. Detailed specifications

Exascend PE4 series SSD provides you the ultimate performance and ultra-high reliability over traditional hard disk drive by achieving up to 3,500MB/s for sequential read, 3,000MB/s for sequential write, 500,000 IOPS for random read, 55,000 IOPS for steady state random write.

Exascend PE4 series SSD consists solely of semiconductor devices, it does not contain any mechanical part such as platter (disk), motor and suspension as traditional hard disk drive. Thus, it exhibits superior performance, capacity, reliability, ruggedness, low power, and small form factor profiles that qualified to be the best storage solution for enterprise application with extreme workloads and increased MTBF requirements.

Exascend PE4 SSD uses a single-chip Flash controller to manage multiple NAND Flash memory modules. The controller works with a host system to allow data to be written to and read from the Flash memory modules through a PCIe interface.

4.1 Capacity

Table 2: PE4 logical block address configuration

PE4 SERIES	UNFORMATTED CAPACITY (TOTAL USER ADDRESSABLE SECTORS IN LBA MODE)
240 GB	468,862,128
480 GB	937,703,088
960 GB	1,875,385,008
1,920 GB	3,750,748,848
3,840 GB	7,501,476,528
7,680 GB	15,002,931,888

Notes:

- The LBA count shown represents total user-accessible storage capacity and will remain the same throughout the drive's lifetime.
- The total usable capacity of the SSD may be less than the total physical capacity because a small portion of the capacity is used for NAND flash management and maintenance purposes.

4.2 Performance

Table 3: Drive performance – PE4 series

	UNIT	PE4 SERIES							
Capacity	GB	**240GB**	**480GB**	**960GB**	**1920GB**	**3840GB**	**7680GB**	**3840GB**	**7680GB**
Sequential read	MB/s	2,000	3,200	3,200	3,200	2,800	2,200	3,500	3,500
Sequential write	MB/s	450	900	1,800	3,000	2,800	2,200	3,000	3,000
Sustained read (4KB)	IOPS	60K	120K	240K	400K	400K	400K	400K	400K
Sustained write (4KB)	IOPS	15K	15K	30K	50K	50K	50K	50K	50K
DWPD (5 years)	0.6 @ JESD218 1.5 @ Sequential Write								
Form factor		M.2 2230 & 2242		M.2, E1.S & U.2		M.2 2280		E1.S & U.2	

Notes:

- Measured with device connected as secondary drive.
- Actual performance may vary based on the hardware, software, and overall system configuration.
- Sequential performance is measured with 128 KB transfer size, QD 32 and 4 KB alignment with Iometer.
- Random performance is sustained performance measured with 4K/8K transfer size, QD 32 and 4 KB alignment with Iometer.
- Performance test platform: CPU: Intel Core i7 4770K; motherboard: ASUS Z87-DELUXE; chipset: Intel Z87 Express; OS: Windows 8.1 Pro x64.

4.3 Environment specification

Table 4: Environmental specification table

PARAMETER	VALUE
Operating temperature	0–70 °C
Storage temperature	-40–85 °C
Power supply voltage range	U.2 / E1.S: 12.0 V ±10% M.2: 3.3 V ± 5%
Humidity (non-condensing)	5–95% (Operating)
Vibration	10 G (peak, 10–2000 Hz)
Shock (operating)	50 G, (11 ms duration, half sine wave)
Shock (non-operating)	1500 G, (0.5 ms duration, half sine wave)

4.4 Power consumption

Table 5: PE4 series power consumption table

PARAMETER	VALUE	UNIT
Max power (average)	<12.0	W
Active power (average)	<7.0	W
Idle mode power (average)	<1.0	W

4.5 Reliability

Products in the Exascend PE4 series meet or exceed SSD endurance and data retention requirements as specified in the JESD218 standard. Reliability specifications are listed in the following table.

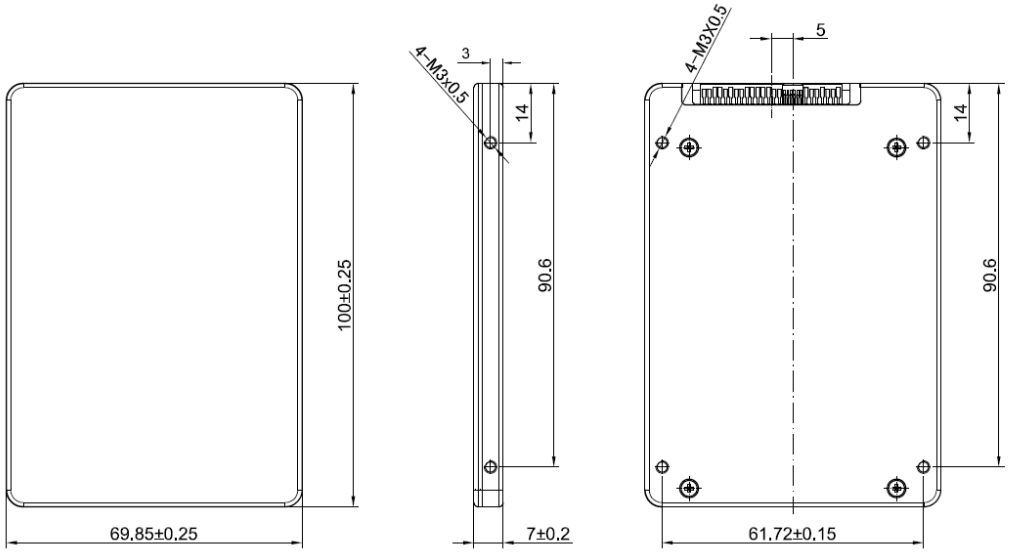
Table 6: Reliability table

PARAMETER	VALUE
Mean Time Between Failures (MTBF) Mean Time Between Failures is a measure of how reliable a hardware product or a component is. The value describes the expected time between two failures.	2,000,000 hours
Uncorrectable Bit Error Rate (UBER) A metric for the rate of occurrence of data errors, equal to the number of data errors per bits read.	<1 sector per 10^{17}
Endurance Rating (TBW) TBW stands for total bytes written whose access pattern is compliant with JESD218 standard.	240GB: 250TB 480GB: 500TB 960GB: 1000TB 1920GB: 2000TB 3840GB: 4000TB 7680GB: 8000TB

5. Physical dimension diagram

5.1 U.2 board

Figure 2: U.2 physical dimension diagram



GENERAL TOLERANCE IS ±0.15mm
DIMENSION UNIT: mm

Table 7: Physical dimensions for U.2

PHYSICAL DIMENSIONS	VALUE	UNIT
Length	100	mm
Width	69.85	mm
Thickness	7	mm

5.2 PCIe M.2 2280

Figure 3: M.2 2280 physical dimension diagram

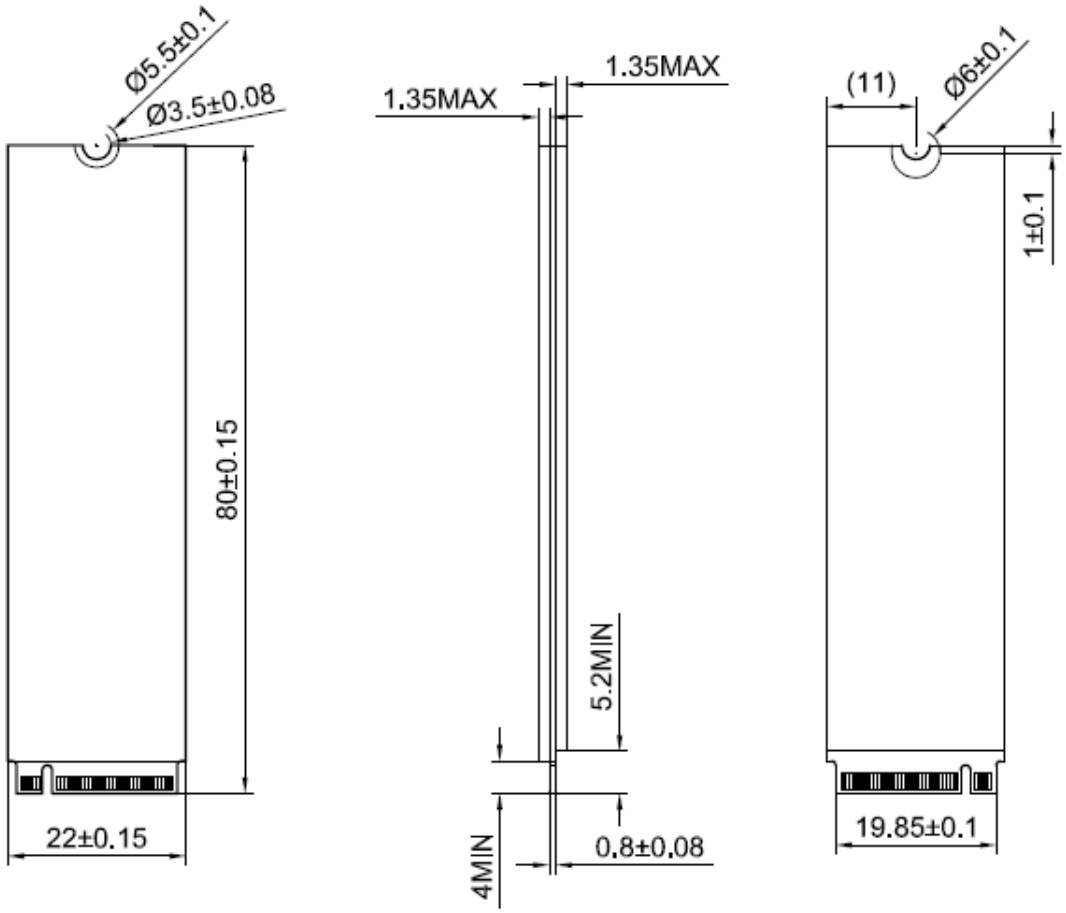


Table 8: Physical dimensions for M.2 2280

PHYSICAL DIMENSIONS	VALUE	UNIT
Length	80	mm
Width	22	mm
Thickness	3.5	mm

5.3 PCIe M.2 2242

Figure 4: M.2 2242 physical dimension diagram

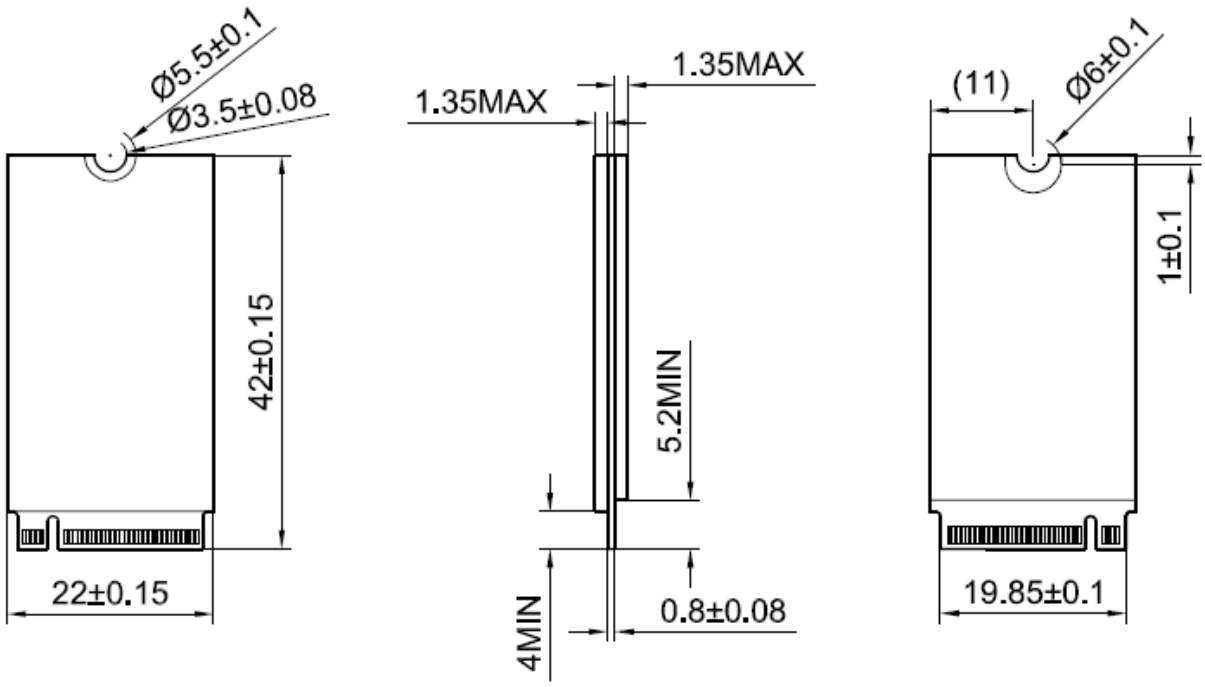


Table 9: Physical dimensions for M.2 2242

PHYSICAL DIMENSIONS	VALUE	UNIT
Length	42	mm
Width	22	mm
Thickness	3.5	mm

5.4 PCIe M.2 2230

Figure 5: M.2 2230 physical dimension diagram

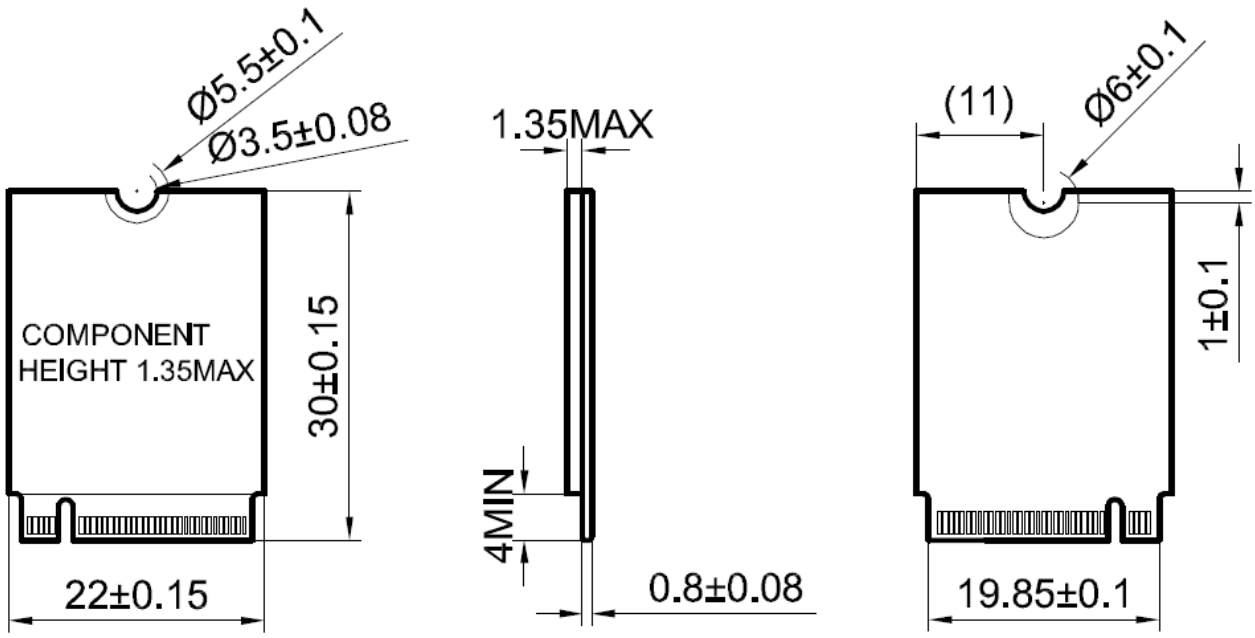


Table 10: Physical dimensions for M.2 2230

PHYSICAL DIMENSIONS	VALUE	UNIT
Length	30	mm
Width	22	mm
Thickness	2.15	mm

5.5 PCIe E1.S without heat sink

Figure 6: E1.S physical dimension diagram

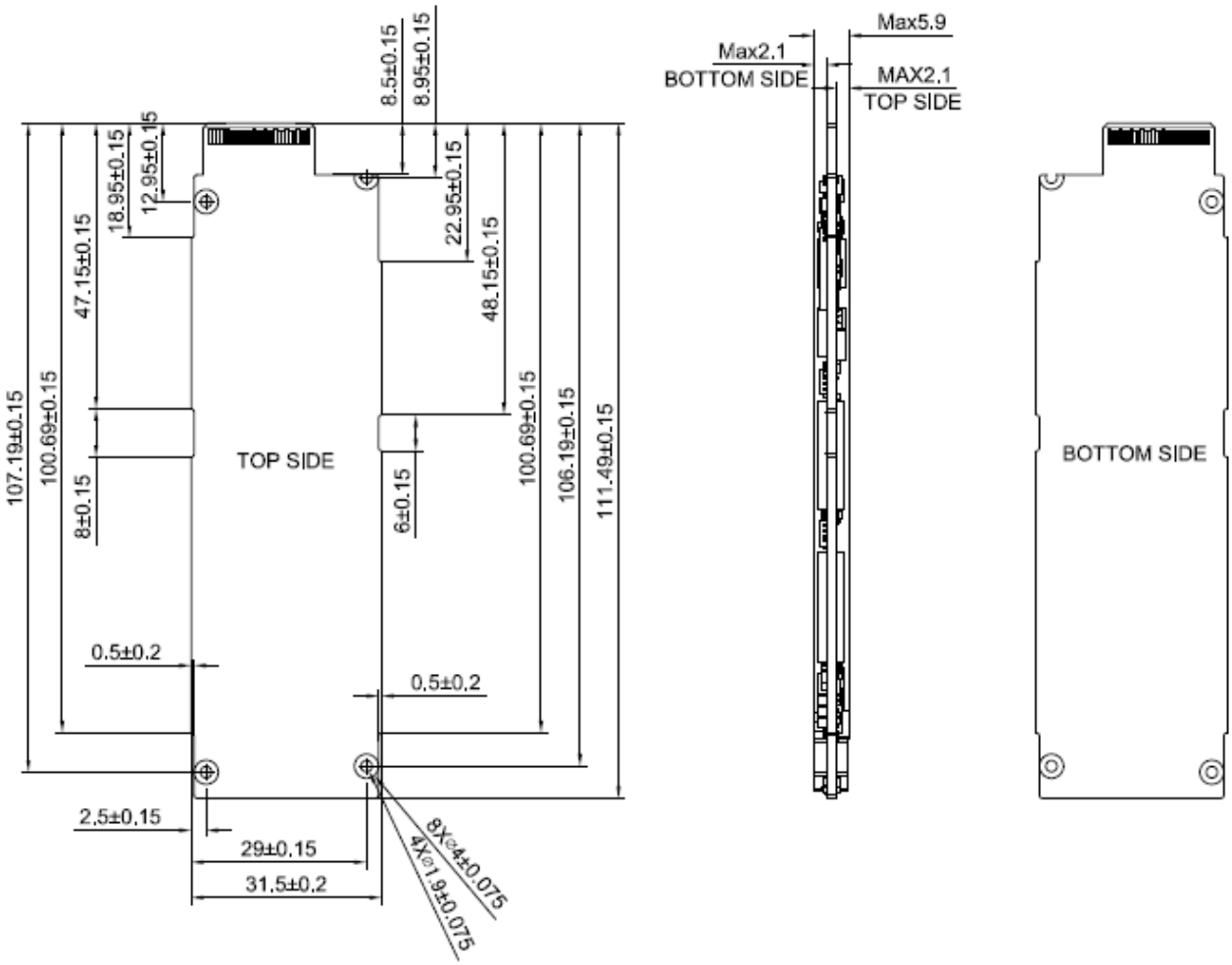


Table 11: Physical dimensions for E1.S

PHYSICAL DIMENSIONS	VALUE	UNIT
Length	111.49	mm
Width	31.5	mm
Thickness	5.9	mm

5.6 PCIe E1.S with heat sink

Figure 7: E1.S physical dimension diagram

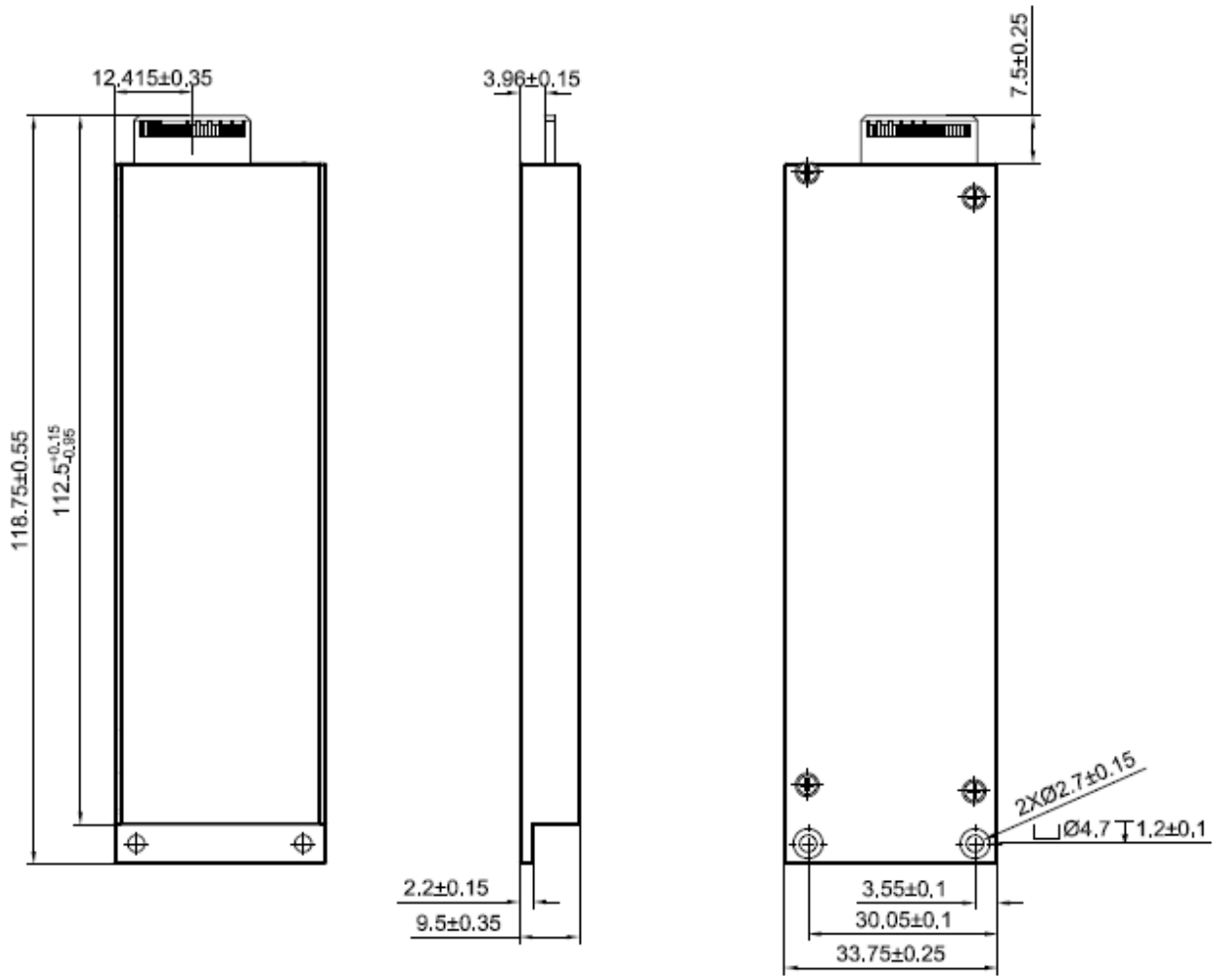


Table 12: Physical dimensions for E1.S

PHYSICAL DIMENSIONS	VALUE	UNIT
Length	118.75	mm
Width	33.75	mm
Thickness	9.5	mm

6. Pin Assignment

6.1 U.2 connector

Table 13: U.2 connector signal name, power pin assignment, and description

PIN NAME	SIGNAL NAME	DESCRIPTION
S1	GND	Ground
S2	Not used	Not used
S3	Not used	Not used
S4	GND	Ground
S5	Not used	Not used
S6	Not used	Not used
S7	GND	Ground
E1	Not used	Not used
E2	Not used	Not used
E3	3.3Vaux	3.3 V Power
E4	Not used	Not used
E5	PERST0#	Fundamental reset port 0
E6	Reserved	Reserved
P1	Not used	Not used (SATA/SAS)
P2	Not used	Not used (SATA/SAS)
P3	CLKREQ	CLKREQ
P4	IfDet_N	Interface detection (drive type)
P5	GND	Ground
P6	GND	Ground
P7	Not used	Not used (SATA/SAS)
P8	Not used	Not used (SATA/SAS)
P9	Not used	Not used (SATA/SAS)
P10	PRSNT_N	Presence detection (also used for drive type)
P11	Activity	Activity signal from the drive
P12	Hot-Plug	Ground
P13	+12V_pre	12V Power
P14	+12V	12 V Power
P15	+12V	12 V Power
E7	REFCLK0+	Reference clock port 0 +
E8	REFCLK0-	Reference clock port 0 -
E9	GND	Ground
E10	PERp0	+ Receive differential pair, channel 0
E11	PERn0	- Receive differential pair, channel 0
E12	GND	Ground
E13	PETn0	- Transmit differential pair, channel 0

E14	PETp0	+ Transmit differential pair, channel 0
E15	GND	Ground
E16	Reserved	Reserved
S8	GND	Ground
S9	Not used	Not used (SATA/SAS)
S10	Not used	Not used (SATA/SAS)
S11	GND	Ground
S12	Not used	Not used (SATA/SAS)
S13	Not used	Not used (SATA/SAS)
S14	GND	Ground
S15	Reserved	Reserved
S16	GND	Ground
S17	PERp1	+ Receive differential pair, channel 1
S18	PERn1	- Receive differential pair, channel 1
S19	GND	Ground
S20	PETn1	- Transmit differential pair, channel 1
S21	PETp1	+ Transmit differential pair, channel 1
S22	GND	Ground
S23	PERp2	+ Receive differential pair, channel 2
S24	PERn2	- Receive differential pair, channel 2
S25	GND	Ground
S26	PETn2	- Transmit differential pair, channel 2
S27	PETp2	+ Transmit differential pair, channel 2
S28	GND	Ground
E17	PERp3	+ Receive differential pair, channel 3
E18	PERn3	- Receive differential pair, channel 3
E19	GND	Ground
E20	PETn3	- Transmit differential pair, channel 3
E21	PETp3	+ Transmit differential pair, channel 3
E22	GND	Ground
E23	SMCLK	SMBus clock
E24	SMDAT	SMBus data
E25	DualPortEn N	Dual port enable

6.2 PCIe M.2 2280/2242/2230 connector

Table 14: M.2 2280/2242/2230 connector signal name, power pin assignment, and description

PIN NAME	SIGNAL NAME	DESCRIPTION
1	GND	Ground
2	3.3V	3.3V Power
3	GND	Ground
4	3.3V	3.3V Power
5	PCIe 3 TXn	PCIe Lane 3 TX-
6	Reserved	Reserved
7	PCIe 3 TXp	PCIe Lane 3 TX+
8	Reserved	Reserved
9	GND	Ground
10	DAS	Device Activity Signal
11	PCIe 3 RXn	PCIe Lane 3 RX-
12	3.3V	3.3V Power
13	PCIe 3 RXp	PCIe Lane 3 RX+
14	3.3V	3.3V Power
15	GND	Ground
16	3.3V	3.3V Power
17	PCIe 2 TXn	PCIe Lane 2 TX-
18	3.3V	3.3V Power
19	PCIe 2 TXp	PCIe Lane 2 TX+
20	NC	No Connection
21	GND	Ground
22	UART RX	Manufacturing Use
23	PCIe 2 RXn	PCIe Lane 2 RX-
24	NC	No Connection
25	PCIe 2 RXp	PCIe Lane 2 RX+
26	Reserved	Reserved
27	GND	Ground
28	Reserved	Reserved
29	PCIe 1 TXn	PCIe Lane 1 TX-
30	Reserved	Reserved
31	PCIe 1 TXp	PCIe Lane 1 TX+
32	UART TX	Manufacturing Use
33	GND	Ground
34	Reserved	Reserved
35	PCIe 1 RXn	PCIe Lane 1 RX-
36	Reserved	Reserved
37	PCIe 1 RXp	PCIe Lane 1 RX+

38	Reserved	Reserved
39	GND	Ground
40	SCL	SMBus_SCL
41	PCIe 0 TXn	PCIe Lane 0 TX-
42	SDA	SMBus_SDA
43	PCIe 0 TXp	PCIe Lane 0 TX+
44	NC	No Connection
45	GND	Ground
46	NC	No Connection
47	PCIe 0 RXn	PCIe Lane 0 RX-
48	NC	No Connection
49	PCIe 0 RXp	PCIe Lane 0 RX+
50	PERST	PCIe Reset
51	GND	Ground
52	CLKREQ	PCIe Clock Request
53	Ref CLKN	PCIe Reference clk-
54	NC	No Connection
55	Ref CLKP	PCIe Reference clk+
56	NC	No Connection
57	GND	Ground
58	NC	No Connection
59	PCIe Module Key	PCIe Module Key
60	PCIe Module Key	PCIe Module Key
61	PCIe Module Key	PCIe Module Key
62	PCIe Module Key	PCIe Module Key
63	PCIe Module Key	PCIe Module Key
64	PCIe Module Key	PCIe Module Key
65	PCIe Module Key	PCIe Module Key
66	PCIe Module Key	PCIe Module Key
67	NC	No Connection
68	NC	No Connection
69	NC	No Connection
70	3.3V	3.3V Power
71	GND	Ground
72	3.3V	3.3V Power
73	GND	Ground
74	3.3V	3.3V Power
75	GND	Ground

6.3 E1.S connector

Table 15: E1.S connector signal name, power pin assignment, and description

PIN NAME	1st mate	SIGNAL NAME
A1	1st mate	GND
A2	1st mate	GND
A3	1st mate	GND
A4	1st mate	GND
A5	1st mate	GND
A6	2nd mate	GND
A7	2nd mate	SMBCLK
A8	2nd mate	SMBDAT
A9	2nd mate	SMBRST#
A10	2nd mate	LED#/ACTIVITY
A11	2nd mate	PERST1#/CLKREQ#
A12	1st mate	PRSNT0#
A13	2nd mate	GND
A14	2nd mate	REFCLKn1
A15	1st mate	REFCLKp1
A16	2nd mate	GND
A17	2nd mate	PERn0
A18	1st mate	PERp0
A19	2nd mate	GND
A20	2nd mate	PERn1
A21	1st mate	PERp1
A22	2nd mate	GND
A23	2nd mate	PERn2
A24	1st mate	PERp2
A25	2nd mate	GND
A26	2nd mate	PERn3
A27	1st mate	PERp3
A28	1st mate	GND
B1	2nd mate	12V
B2	2nd mate	12V
B3	2nd mate	12V
B4	2nd mate	12V
B5	2nd mate	12V
B6	2nd mate	12V
B7	2nd mate	MFG
B8	2nd mate	RFU
B9	2nd mate	DUALPORTEN#

B10	2nd mate	PERST0#
B11	2nd mate	3.3 VAux
B12	2nd mate	PWRDIS
B13	1st mate	GND
B14	2nd mate	REFCLKn0
B15	2nd mate	REFCLKp0
B16	1st mate	GND
B17	2nd mate	PETn0
B18	2nd mate	PETp0
B19	1st mate	GND
B20	2nd mate	PETn1
B21	2nd mate	PETp1
B22	1st mate	GND
B23	2nd mate	PETn2
B24	2nd mate	PETp2
B25	1st mate	GND
B26	2nd mate	PETn3
B27	2nd mate	PETp3
B28	1st mate	GND

7. Compliance

Exascend PE4 series SSD complies with the following specifications:

- FCC
- CE
- RoHS

8. PCI and NVM Express Registers

8.1 PCI Register

8.1.1 PCI Register Summary

Table 16: PCI Register Summary

Start Address	End Address	Name	Type
00h	3Fh	PCI Header	PCI Capability
40h	47h	PCI Power Management Capability	PCI Capability
50h	67h	MSI Capability	PCI Capability
70h	A3h	PCI Express Capability	PCI Capability
B0h	BBh	MSI-X Capability	PCI Capability
100h	12Bh	Advanced Error Reporting Capability	PCI Capability
148h	153h	Device Serial No Capability	PCI Capability
158h	167h	Power Budgeting Capability	PCI Capability
168h	16Fh	Alternative Routing-ID Interpretation Capability	PCI Capability
178h	18Bh	Secondary PCI Express Header	PCI Capability
198h	1A7h	Physical LAYER 16.0 GT/s Extended Capability	PCI Capability
1BCh	1C7h	Margining Extended Capability	PCI Capability
224h	22Bh	Latency Tolerance Reporting (LTR)	PCI Capability
22Ch	23Bh	L1 Substates Capability Register	PCI Capability

8.1.2 PCI Header Register

Table 17: PCI Header Register Summary

Start Address	End Address	Symbol	Description
00h	03h	ID	Identifiers
04h	05h	CMD	Command Register
06h	07h	STS	Device Status
08h	08h	RID	Revision ID
09h	0Bh	CC	Class Codes
0Ch	0Ch	CLS	Cache Line Size
0Dh	0Dh	MLT	Master Latency Timer
0Eh	0Eh	HTYPE	Header Type
0Fh	0Fh	BIST	Built in Self Test
10h	13h	MLBAR (BAR0)	Memory Register Base Address (lower 32-bit)

14h	17h	MUBAR (BAR1)	Memory Register Base Address (upper 32-bit)
18h	1Bh	IDBAR (BAR2)	Index/Data Pair Register Base Address
1Ch	1Fh	BAR3	Reserved
20h	23h	BAR4	Reserved
24h	27h	BAR5	Reserved
28h	2Bh	CCPTR	CardBus CIS Pointer
2Ch	2Fh	SS	Subsystem Identifiers
30h	33h	EROM	Expansion ROM Base Address
34h	34h	CAP	Capabilities Pointer
35h	3Bh	RO	Reserved
3Ch	3Dh	INTR	Interrupt Information
3Eh	3Eh	MGNT	Minimum Grant
3Fh	3Fh	MLAT	Maximum Latency

Table 18: Identifier Register

Bits	Type	Default Value	Description
31:16	RO	1321h	Device ID
0:15	RO	1B4Bh	Vendor ID

Table 19: Command Register

Bits	Type	Default Value	Description
15:11	RO	0h	Reserved
10	RW	0h	Interrupt Disable
9	RO	0h	Fast Back-to-Back Enable (N/A)
8	RW	0h	SERR# Enable (N/A)
7	RO	0h	IDSEL Stepping/Wait Cycle Control (N/A)
6	RW	0h	Parity Error Response Enable
5	RO	0h	VGA Palette Snooping Enable (N/A)
4	RO	0h	Memory Write and Invalidate Enable (N/A)
3	RO	0h	Special Cycle Enable (N/A)
2	RW	0h	Bus Master Enable
1	RW	0h	Memory Space Enable

0	RW	0h	I/O Space Enable

Table 20: Status Register

Bits	Type	Default Value	Description
15	RW	0h	Detected Parity Error
14	RW	0h	Signaled System Error
13	RW	0h	Received Master Abort
12	RW	0h	Received Target Abort
11	RW	0h	Signaled Target Abort (N/A)
10:9	RO	0h	DEVSEL Timing (N/A)
8	RW	0h	Master Data Parity Error Detected
7	RO	0h	Fast Back-to-Back Transaction Capable (N/A)
6	RO	0h	Reserved
5	RO	0h	66MHz Capable (N/A)
4	RO	1h	Capabilities List
3	RO	0h	Interrupt Status
2:1	RO	0h	Reserved
0	RO	0h	Reserved

Table 21: Revision ID Register

Bits	Type	Default Value	Description
7:0	RO	02h	Controller Hardware Revision ID

Table 22: Class Code Register

Bits	Type	Default Value	Description
23:16	RO	01h	Base Class Code
15:8	RO	08h	Sub Class Code
7:0	RO	02h	Programming Interface

Table 23: Cache Line Size Register

Bits	Type	Default Value	Description
7:0	RW	0h	Cache Line Size (N/A)

Table 24: Master Latency Timer Register

Bits	Type	Default Value	Description
7:0	RO	0h	Master Latency Timer (N/A)

Table 25: Header Type Register

Bits	Type	Default Value	Description
7	RO	0h	Multi-Function Device (N/A)
6:0	RO	0h	Reserved

Table 26: Built In Self Test Register

Bits	Type	Default Value	Description
7:0	RO	0h	Built In Self Test (N/A)

Table 27: Memory Register Base Address Lower 32-bits (BAR0) Register

Bits	Type	Default Value	Description
31:14	RW	0h	Base Address
13:4	RO	0h	Reserved
3	RO	0h	Pre-Fetchable
2:1	RO	2h	Address Type (64-bit)
0	RO	0h	Memory Space Indicator (MEMSI)

Table 28: Memory Register Base Address Upper 32-bits (BAR1)

Bits	Type	Default Value	Description
31:0	RO	0h	Base Address

Table 29: Index/Data Pair Register Base Address (BAR2) Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

Table 30: BAR3 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

Table 31: Vendor Specific BAR4 Register

Bits	Type	Default Value	Description

31:0	RO	0h	N/A

Table 32: Vendor Specific BAR5 Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

Table 33: Card bus CIS Pointer Register

Bits	Type	Default Value	Description
31:0	RO	0h	N/A

Table 34: Subsystem Identifier Register

Bits	Type	Default Value	Description
31:16	RO	0100h	Subsystem ID
15:0	RO	1B4Bh	Subsystem Vendor ID

Table 35: Expansion ROM Register

Bits	Type	Default Value	Description
31:17	RW	0h	Expansion ROM Base Address
16:1	RO	0h	Reserved
0	RW	0h	Expansion ROM Enable/Disable

Table 36: Capabilities Pointer Register

Bits	Type	Default Value	Description
7:0	RO	40h	Capability Pointer (Points to PCI Power Management Capability Offset)

Table 37: Interrupt Information Register

Bits	Type	Default Value	Description
15:8	RO	01h	Interrupt Pin
7:0	RW	0h	Interrupt Line

Table 38: Minimum Grant Register

Bits	Type	Default Value	Description
7:0	RO	0h	Minimum Grant

Table 39: Maximum Latency Register

Bits	Type	Default Value	Description
7:0	RO	0h	Maximum Latency

8.1.3 PCI Power Management Register

Table 40: PCI Power Management Capability Register Summary

Start Address	End Address	Symbol	Description
40h	40h	PCIPM_ID	PCI Power Management Capability ID
41h	41h	NEXTCAP	Next Capability Pointer
42h	43h	PCIPM_ID	PC Power Management Capabilities
44h	45h	PCIPM_CS	PCI Power Management Control and Status
46h	46h	PCIPM_CSR_BSE	PMCSR_BSE Bridge Extensions
47h	47h	PCIPM_DATA	Data

Table 41: PCI Power Management Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	50h	Next Capability
7:0	RO	01h	Capability ID

Table 42: PCI Power Management Capability Register

Bits	Type	Default Value	Description
15:11	RO	19h	PME Support (N/A)
10	RO	0h	D2 Support (N/A)
9	RO	0h	D1 Support (N/A)
8:6	RO	0h	AUX Current (N/A)
5	RO	0h	Device Specific Initialization (N/A)
4	RO	0h	Reserved
3	RO	0h	PME Clock (N/A)
2:0	RO	3h	Version (Support for PCI Bus Power Management Interface Spec R1.2)

Table 43: PCI Power Management Control and Status Register

Bits	Type	Default Value	Description

31:24	RO	0h	Data register (N/A)
23	RO	0h	Bus Power/Clock Enable (N/A)
22	RO	0h	B2, B3 support (N/A)
21:16	RO	0h	Reserved
15	RO	0h	PME Status(N/A)
14:13	RO	0h	Data Scale (N/A)
12:9	RO	0h	Data Select (N/A)
8	RW	0h	PME enable (N/A)
7:4	RO	0h	Reserved
3	RO	1h	No Soft Reset
2	RO	0h	Reserved
1:0	RW	0h	Power State

8.1.4 Message Signaled Interrupt Register

Table 44: Message Signaled Interrupt Capability Register Summary

Start Address	End Address	Symbol	Description
50h	51h	MSI_ID	Message Signaled Interrupt Capability ID
52h	53h	MSI_MC	Message Signaled Interrupt Message Control
54h	57h	MSI_MA	Message Signaled Interrupt Message Address
58h	5Bh	MSI_MUA	Message Signaled Interrupt Upper Address
5Ch	5Dh	MSI_MDATA	Message Signaled Interrupt Message Data
60h	63h	MSI_MMASK	Message Signaled Interrupt Mask Bits
64h	67h	MSI_MPEND	Message Signaled Interrupt Pending Bits

Table 45: Message Signaled Interrupt Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	70h	Next Capability
7:0	RO	05h	Capability ID

Table 46: Message Signaled Interrupt Control Register

Bits	Type	Default Value	Description
15:9	RO	0h	Reserved
8	RO	1h	Per Vector Masking Capable
7	RO	1h	64-bit Address Capable
6:4	RW	0h	Multiple Message Enable
3:1	RO	0h	Multiple Message Capable
0	RW	0h	MSI Enable

Table 47: Message Signaled Interrupt Lower Address Register

Bits	Type	Default Value	Description
31:2	RW	0h	Address
1:0	RO	0h	Reserved

Table 48: Message Signaled Interrupt Upper Address Register

Bits	Type	Default Value	Description
31:0	RW	0h	Upper Address

Table 49: Message Signaled Interrupt Message Data Register

Bits	Type	Default Value	Description
31:16	RO	0h	Reserved
0:15	RW	0h	Data

Table 50: Message Signaled Interrupt Mask Bits Register

Bits	Type	Default Value	Description
31:0	RW	0h	Mask Bits

Table 51: Message Signaled Interrupt Pending Bits Register

Bits	Type	Default Value	Description
31:0	RO	0h	Pending Bits

8.1.5 PCI Express Capability Register

Table 52: PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description

70h	71h	PCIE_ID	PCI Express Capability ID
72h	73h	PCIE_CAP	PCI Express Capabilities
74h	77h	PCIE_DCAP	PCI Express Device Capabilities
78h	79h	PCIE_DC	PCI Express Device Control
7Ah	7Bh	PCIE_DS	PCI Express Device Status
7Ch	7Fh	PCIE_LCAP	PCI Express Link Capabilities
80h	81h	PCIE_LC	PCI Express Link Control
82h	83h	PCIE_LS	PCI Express Link Status
94h	97h	PCIE_DCAP2	PCI Express Device Capabilities 2
98h	99h	PCIE_DC2	PCI Express Device Control 2
9Ah	9Bh	PCIE_DS2	PCI Express Device Status 2
9Ch	9Fh	PCIE_LCAP2	PCI Express Link Capabilities 2
A0h	A1h	PCIE_LC2	PCI Express Link Control 2
A2h	A3h	PCIE_LS2	PCI Express Link Status 2

Table 53: PCI Express Capability ID Register

Bits	Type	Default Value	Description
15:8	RO	B0h	Next Pointer (MSI-X Capability)
7:0	RO	10h	Capability ID

Table 54: PCI Express Capabilities Register

Bits	Type	Default Value	Description
15:14	RO	0h	Reserved
13:9	RO	0h	Interrupt Message Number
8	RW	0h	Slot Implementation (N/A)
7:4	RO	0h	Device/Port Type
3:0	RO	2h	Capability Version

Table 55: PCI Express Device Capabilities Register

Bits	Type	Default Value	Description

31:29	RO	0h	Reserved
28	RO	1h	Function Level Reset Capability
27:26	RO	0h	Captured Slot Power Limit Scale
25:18	RO	0h	Captured Slot Power Limit Value
17:16	RO	0h	Reserved
15	RO	1h	Role-based Error Reporting
14:12	RO	0h	Reserved
11:9	RO	7h	Endpoint L1 Acceptable Latency
8:6	RO	7h	Endpoint L0 Acceptable Latency
5	RO	0h	Extended Tag Field Supported
4:3	RO	0h	Phantom Functions Supported
2:0	RO	2h	Max Payload Size Supported (512 payload size)

Table 56: PCI Express Device Control Register

Bits	Type	Default Value	Description
15	RW	0h	Initiate Function Level Reset
14:12	RW	2h	Max Read Request Size
11	RW	0h	Enable No Snoop
10	RW	0h	Aux Power PM Enable (N/A)
9	RW	0h	Phantom Functions Enable (N/A)
8	RW	0h	Extended Tag Enable
7:5	RW	0h	Max Payload Size
4	RW	1h	Enable Relaxed Ordering
3	RW	0h	Unsupported Request Reporting Enable
2	RW	0h	Fatal Error Reporting Enable
1	RW	0h	Non-Fatal Error Reporting Enable
0	RW	0h	Correctable Error Reporting Enable

Table 57: PCI Express Device Status Register

Bits	Type	Default Value	Description
15:6	RO	0h	Reserved

5	RO	0h	Transactions Pending
4	RO	0h	Aux Power Detected
3	RW	0h	Unsupported Request Detected
2	RW	0h	Fatal Error Detected
1	RW	0h	Non-Fatal Error Detected
0	RW	0h	Correctable Error Detected

Table 58: PCI Express Link Capabilities Register

Bits	Type	Default Value	Description
31:24	RW	0h (Port 0)	Port Number
23	RO	0h	Reserved
22	RW	1h	ASPM Optionality Compliance
21	RO	0h	Link Bandwidth Notification Capability (N/A)
20	RO	0h	Data Link Layer Link Active Reporting Capable (N/A)
19	RO	0h	Surprise Down Error Reporting Capable (N/A)
18	RO	1h	Clock Power Management
17:15	RO	6h	L1 Exit Latency
14:12	RO	7h	L0s Exit Latency
11:10	RO	2h	Active State Power Management Support
9:4	RO	4h	Maximum Link Width
3:0	RO	4h	Supported Link Speeds

Table 59: PCI Express Link Control Register

Bits	Type	Default Value	Description
15:14	RO	0h	DRS Signaling Control
13:12	RW	0h	Reserved
11	RW	0h	Link Autonomous Bandwidth Interrupt Enable (N/A)
10	RW	0h	Link Bandwidth Management Interrupt Enable (N/A)
9	RW	0h	Hardware Autonomous Width Disable
8	RW	0h	Enable Clock Power Management
7	RW	0h	Extended Sync

6	RW	0h	Common Clock Configuration
5	RW	0h	Retrain Link
4	RW	0h	Link Disable
3	RW	0h	Read Completion Boundary
2	RO	0h	Reserved
1:0	RW	0h	Active State Power Management Control

Table 60: PCI Express Link Status Register

Bits	Type	Default Value	Description
15	RO	0h	Link Autonomous Bandwidth Status
14	RO	0h	Link Bandwidth Management Status
13	RO	0h	Data Link Layer Link Active
12	RW	1h	Slot Clock Configuration
11	RO	0h	Link Training
10	RO	0h	Reserved
9:4	RO	1h	Negotiated Link Width
3:0	RO	1h	Current Link Speed

Table 61: PCI Express Device Capabilities 2 Register

Bits	Type	Default Value	Description
31	RW	1h	FRS Supported
30:20	RO	0h	Reserved
19:18	RO	0h	OBFF Supported
17:16	RO	0h	Reserved
15:14	RO	0h	LN System CLS (N/A)
13:12	RO	0h	TPH Completer Supported (N/A)
11	RO	1h	Latency Tolerance Reporting Supported
10	RO	0h	No RO-enabled PR-PR Passing (N/A)
9	RO	0h	128-bit CAS Completer Supported (N/A)
8	RO	0h	64-bit Atomic Op Completer Supported (N/A)
7	RO	0h	32-bit Atomic Op Completer Supported (N/A)
6	RO	0h	Atomic Op Routing Supported (N/A)

5	RO	0h	ARI Forwarding Supported (N/A)
4	RO	1h	Completion Timeout Disable Supported
3:0	RO	Fh	Completion Timeout Ranges Supported

Table 62: PCI Express Device Control 2 Register

Bits	Type	Default Value	Description
15:11	RO	0h	Reserved
10	RW	0h	Latency Tolerance Reporting Mechanism Enable
9:6	RO	0h	Reserved
5	RW	0h	ARI Forwarding Enable
4	RW	0h	Completion Timeout Disable
3:0	RW	0h	Completion Timeout Value

Table 63: PCI Express Device Status 2 Register

Bits	Type	Default Value	Description
15:0	RO	0h	Reserved

Table 64: PCI Express Link Capabilities 2 Register

Bits	Type	Default Value	Description
31	RO	1h	DRS Supported
30:25	RO	0h	Reserved
24	RW	1h	Two Retimer Presence Detect Support
23	RW	1h	Retimer Presence Detect Support
22:9	RO	0h	Reserved
8	RO	0h	Cross-Link Supported (N/A)
7:1	RO	Fh	Supported Speeds Vector
0	RO	0h	Reserved

Table 65: PCI Express Link Control 2 Register

Bits	Type	Default Value	Description
15:12	RW	0h	Compliance De-emphasis
11	RW	0	Compliance SOS
10	RW	0	Enter Modified Compliance

9:7	RW	0h	Transmit Margin
6	RW	0	Selectable De-Emphasis (N/A)
5	RW	0	Hardware Autonomous Speed Disable
4	RW	0	Enter Compliance
3:0	RW	4h	Target Link Speed 1h: 2.5 GT/s (Gen 1) 2h: 5.0 GT/s (Gen 2) 3h: 8 GT/s (Gen 3) 4h: 16 GT/s(Gen 4)

Table 66: PCI Express Link Status 2 Register

Bits	Type	Default Value	Description
15:6	RO	0	Reserved
5	RW	0	Link Equalization Request
4	RO	0	Equalization Phase 3 Successful
3	RO	0	Equalization Phase 2 Successful
2	RO	0	Equalization Phase 1 Successful
1	RO	0	Equalization Complete
0	RO	1	Current De-Emphasis

8.1.6 MSI-X Register

Table 67: MSI-X Capability Register Summary

Start Address	End Address	Symbol	Description
B0h	B1h	MSIX_ID	MSI-X Capability ID
B2h	B3h	MSIX_CAP	MSI-X Message Control
B4h	B7h	MSIX_TBL	MSI-X Table Offset and Table BIR
B8h	BBh	MSIX_PBA	MSI-X PBA Offset and PBA BIR

Table 68: MSI-X Identifier Register

Bits	Type	Default Value	Description

15:8	RO	00h	Next Capability
7:0	RO	11h	Capability ID

Table 69: MSI-X Control Register

Bits	Type	Default Value	Description
15	RW	0	MSI-X Enable
14	RW	0	Function Mask
13:11	RO	0h	Reserved
10:0	RO	42h	Table Size

Table 70: MSI-X Table Offset Register

Bits	Type	Default Value	Description
31:3	RO	400h	Table Offset
2:0	RO	0	Table BIR

Table 71: MSI-X Pending Bit Array Offset Register

Bits	Type	Default Value	Description
31:3	RO	600h	Pending Bit Array Offset
2:0	RO	0	Pending Bit Array BIR

8.1.7 Advanced Error Reporting Register

Table 72: Advanced Error Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
100h	103h	AER_ID	AER Capability ID
104h	107h	AER_UCES	AER Uncorrectable Error Status
108h	10Bh	AER_UCEM	AER Uncorrectable Error Mask
10Ch	10Fh	AER_UCESEV	AER Uncorrectable Error Severity
110h	113h	AER_CES	AER Correctable Error Status
114h	117h	AER_CEM	AER Correctable Error Mask
118h	11Bh	AER_CC	AER Advanced Error Capabilities and Control
11Ch	12Bh	AER_HL	AER Header Log

Table 73: AER Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	148h	Next Pointer (Points to Secondary PCI Express Extended Capability Header Offset)
19:16	RO	2h	Capability Version
15:0	RO	1h	Capability ID

Table 74: AER Uncorrectable Error Status Register

Bits	Type	Default Value	Description
31:23	RO	0h	Reserved
22	RW	0h	Uncorrectable Internal Error Status (N/A)
21	RO	0h	Reserved
20	RW	0h	Unsupported Request Error Status
19	RW	0h	ECRC Error Status
18	RW	0h	Malformed TLP Status
17	RW	0h	Receiver Overflow Status
16	RW	0h	Unexpected Completion Status
15	RW	0h	Completer Abort Status
14	RW	0h	Completion Timeout Status
13	RW	0h	Flow Control Protocol Error Status
12	RW	0h	Poisoned TLP Status
11:6	RO	0h	Reserved
5	RW	0h	Surprise Down Error Status (N/A)
4	RW	0h	Data Link Protocol Error Status
3:0	RO	0h	Reserved

Table 75: AER Uncorrectable Error Mask Register

Bits	Type	Default Value	Description
31:25	RO	0h	Reserved
24	RW	0h	Atomic Op Egress Blocked Mask (N/A)
23	RW	0h	MC Blocked TLP Mask (N/A)

22	RW	1h	Uncorrectable Internal Error Mask
21	RW	0h	ACS Violation Mask (N/A)
20	RW	0h	Unsupported Request Error Mask
19	RW	0h	ECRC Error Mask
18	RW	0h	Malformed TLP Mask
17	RW	0h	Receiver Overflow Mask
16	RW	0h	Unexpected Completion Mask
15	RW	0h	Completer Abort Mask
14	RW	0h	Completion Timeout Mask
13	RW	0h	Flow Control Protocol Error Mask
12	RW	0h	Poisoned TLP Mask
11:6	RO	0h	Reserved
5	RW	0h	Surprise Down Error Mask (N/A)
4	RW	0h	Data Link Protocol Error Mask
3:0	RO	0h	Reserved

Table 76: AER Uncorrectable Error Severity Register

Bits	Type	Default Value	Description
31:25	RO	0h	Reserved
24	RW	0h	Atomic Op Egress Blocked Severity (N/A)
23	RO	0h	Reserved
22	RW	1h	Uncorrectable Internal Error Severity (N/A)
21	RO	0h	Reserved
20	RW	0h	Unsupported Request Error Severity
19	RW	0h	ECRC Error Severity
18	RW	1h	Malformed TLP Severity
17	RW	1h	Receiver Overflow Severity
16	RW	0h	Unexpected Completion Severity
15	RW	0h	Completer Abort Severity
14	RW	0h	Completion Timeout Severity
13	RW	1h	Flow Control Protocol Error Severity

12	RW	0h	Poisoned TLP Severity
11:6	RO	0h	Reserved
5	RW	1h	Surprise Down Error Severity (N/A)
4	RW	1h	Data Link Protocol Error Severity
3:0	RO	0h	Reserved

Table 77: AER Correctable Error Status Register

Bits	Type	Default Value	Description
31:16	RO	0h	Reserved
15	RW	0h	Header Log Overflow Status
14	RW	0h	Corrected Internal Error Status
13	RW	0h	Advisory Non-Fatal Error Status
12	RW	0h	Replay Timer Timeout Status
11:9	RO	0h	Reserved
8	RW	0h	Replay Number Rollover Status
7	RW	0h	Bad DLLP Status
6	RW	0h	Bad TLP Status
5:1	RO	0h	Reserved
0	RW	0h	Received Error Status

Table 78: AER Correctable Error Mask Register

Bits	Type	Default Value	Description
31:16	RO	0h	Reserved
15	RW	1h	Header Log Overflow Status
14	RW	1h	Corrected Internal Error Mask
13	RW	1h	Advisory Non-Fatal Error Mask
12	RW	0h	Replay Timer Timeout Mask
11:9	RO	0h	Reserved
8	RW	0h	Replay Number Rollover Mask
7	RW	0h	Bad DLLP Mask
6	RW	0h	Bad TLP Mask
5:1	RO	0h	Reserved

0	RW	0h	Received Error Mask

Table 79: AER Capabilities and Control Register

Bits	Type	Default Value	Description
31:11	RO	0h	Reserved
10	RW	0h	Multiple Header Recording Enable
9	RO	0h	Multiple Header Recording Capable
8	RW	0h	ECRC Check Enable
7	RO	1h	ECRC Check Capable
6	RW	0h	ECRC Generation Enable
5	RO	1h	ECRC Generation Capable
4:0	RO	0h	First Error Pointer

Table 80: AER Header Log Register

Bits	Type	Default Value	Description
127:120	RO	0h	Header Byte 0
119:112	RO	0h	Header Byte 1
111:104	RO	0h	Header Byte 2
103:96	RO	0h	Header Byte 3
95:88	RO	0h	Header Byte 4
87:80	RO	0h	Header Byte 5
79:72	RO	0h	Header Byte 6
71:64	RO	0h	Header Byte 7
63:56	RO	0h	Header Byte 8
55:48	RO	0h	Header Byte 9
47:40	RO	0h	Header Byte 10
39:32	RO	0h	Header Byte 11
31:24	RO	0h	Header Byte 12
23:16	RO	0h	Header Byte 13
15:8	RO	0h	Header Byte 14
7:0	RO	0h	Header Byte 15

8.1.8 Device Serial Number Capability Register

Table 81: Device Serial Number Capability Summary

Start Address	End Address	Symbol	Description
148h	14Bh	DSN_ID	Device Serial Number Capability ID
14Ch	14Fh	DSN_LR	Serial Number Register (Lower DW)
150h	153h	DSN_UR	Serial Number Register (Upper DW)

Table 82: Device Serial Number Capability Register Header

Bits	Type	Default Value	Description
31:20	RO	158h	Next Capability Offset
19:16	RO	1h	Capability Version
15:0	RO	3h	PCI Express Extended Capability ID

Table 83: Serial Number Register Header (Lower DW)

Bits	Type	Default Value	Description
31:0	RO	0h	Serial Number register (Lower DW)

Table 84: Serial Number Register Header (Upper DW)

Bits	Type	Default Value	Description
31:0	RO	0h	Serial Number register (Upper DW)

8.1.9 Power Budgeting Extended Capability Register

Table 85: Power Budgeting Extended Capability Register Summary

Start Address	End Address	Symbol	Description
158h	15Bh	PB_ID	Power Budgeting Extended Capability ID
15Ch	15Fh	PB_SR	Data Select Register
160h	163h	PB_DR	Data Register
164h	167h	PB_BCR	Power Budget Capability Register

Table 86: Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	168h	Next Capability Offset
19:16	RO	1h	Capability Version

15:0	RO	4h	PCI Express Extended Capability ID

Table 87: Data Select Register

Bits	Type	Default Value	Description
31:8	RO	0h	Reserved
7:0	RW	0h	Data Select

Table 88: Data Register

Bits	Type	Default Value	Description
31:21	RO	0h	Reserved
20:18	RO	0h	Power Rail
17:15	RO	0h	Type
14:13	RO	0h	PM State
12:10	RO	0h	PM Sub State
9:8	RO	0h	Data Scale
7:0	RO	0h	Base Power

Table 89: Power Budget Capability Register

Bits	Type	Default Value	Description
31:1	RO	0h	Reserved
0	RW	1h	System Allocated

8.1.10 Alternative Routing-ID Interpretation Capability Register

Table 90: Alternative Routing-ID Interpretation Capability Register Summary

Start Address	End Address	Symbol	Description
168h	16Bh	ART_ID	Alternative Routing-ID Interpretation Capability ID
16Ch	16Dh	ARI_CA	Alternative Routing-ID Interpretation Capability
16Eh	15Fh	ARI_CL	Alternative Routing-ID Interpretation Control

Table 91: Power Budgeting Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	178h	Next Capability Offset
19:16	RO	1h	Capability Version

15:0	RO	Eh	Alternative Routing-ID Interpretation Capability ID

Table 92: Capability Register

Bits	Type	Default Value	Description
15:8	RO	0h	Next Function Number
1	RO	0h	ACS Function Groups Capability
0	RO	0h	MFVC Function Groups Capability

Table 93: Controller Register

Bits	Type	Default Value	Description
15:7	RO	0h	Reserved
6:4	RW	0h	Function Group
3:2	RW	0h	Reserved
1	RW	0h	ACS Function Groups Enable
0	RW	0h	MFVC Function Groups Enable

8.1.11 Secondary PCI Express Register

Table 94: Secondary PCI Express Capability Register Summary

Start Address	End Address	Symbol	Description
178h	17Bh	SPE_ID	Secondary PCI Express Capability
17Ch	17Fh	PCIE_LC3	PCI Express Link Control 3
180h	183h	PCIE_LE	PCI Express Lane Error Status
184h	185h	PCIE_L0EC	PCI Express Lane 0 Equalization Control
186h	187h	PCIE_L1EC	PCI Express Lane 1 Equalization Control
188h	189h	PCIE_L2EC	PCI Express Lane 2 Equalization Control
18Ah	18Bh	PCIE_L3EC	PCI Express Lane 3 Equalization Control

Table 95: Secondary PCI Express Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	198h	Next Pointer
19:16	RO	1h	Capability Version
15:0	RO	19h	Capability ID (Secondary PCI Express Extended capability)

Table 96: PCI Express Link Control 3 Register

Bits	Type	Default Value	Description
31:2	RO	0h	Reserved
1	RO	0h	Link Equalization Request Interrupt Enable
0	RO	0h	Perform Equalization

Table 97: PCI Express Lane Error Status Register

Bits	Type	Default Value	Description
31:4	RO	0h	Reserved
3:0	RW	0h	Lane Error Status Bits

Table 98: PCI Express Lane 0 Equalization Register

Bits	Type	Default Value	Description
15	RO	0h	Reserved
14:12	RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RO	0h	Reserved
6:4	RO	0h	Downstream Port 8.0T/s Receiver Preset Hint
3:0	RO	0h	Downstream Port 8.0T/s Transmitter Preset

Table 99: PCI Express Lane 1 Equalization Register

Bits	Type	Default Value	Description
15	RO	0h	Reserved
14:12	RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RO	0h	Reserved
6:4	RO	0h	Downstream Port 8.0T/s Receiver Preset Hint (N/A)
3:0	RO	0h	Downstream Port 8.0T/s Transmitter Preset (N/A)

Table 100: PCI Express Lane 2 Equalization Register

Bits	Type	Default Value	Description
15	RO	0h	Reserved
14:12	RO	7h	Upstream Port 8.0T/s Receiver Preset Hint

11:8	RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RO	0h	Reserved
6:4	RO	0h	Downstream Port 8.0T/s Receiver Preset Hint
3:0	RO	0h	Downstream Port 8.0T/s Transmitter Preset

Table 101: PCI Express Lane 3 Equalization Register

Bits	Type	Default Value	Description
15	RO	0h	Reserved
14:12	RO	7h	Upstream Port 8.0T/s Receiver Preset Hint
11:8	RO	Fh	Upstream Port 8.0T/s Transmitter Preset
7	RO	0h	Reserved
6:4	RO	0h	Downstream Port 8.0T/s Receiver Preset Hint
3:0	RO	0h	Downstream Port 8.0T/s Transmitter Preset

8.1.12 Physical LAYER 16.0 GT/s Extended Capability Register

Table 102 Physical LAYER 16.0 GT/s Extended Capability Register Summary

Start Address	End Address	Symbol	Description
198h	19Bh	PL_16GTS_ID	Physical LAYER 16.0 GT/s Extended Capability Header
19Ch	19Fh	PL_16GTS_CA	16.0 GT/s Capability Register
1A0h	1A3h	PL_16GTS_CL	16.0 GT/s Control Register
1A4h	1A7h	PL_16GTS_SA	16.0 GT/s status Register

Table 103 Physical LAYER 16.0 GT/s Extended Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	1BCh	Next Pointer
19:16	RO	1h	Capability Version
15:0	RO	26h	Capability ID (Physical LAYER 16.0 GT/s Extended capability)

Table 104: 16.0 GT/s Capability Register

Bits	Type	Default Value	Description
31:0	RO	0h	Reserved

Table 105: 16.0 GT/s Controller Register

Bits	Type	Default Value	Description
31:0	RO	0h	Reserved

Table 106: 16.0 GT/s Status Register

Bits	Type	Default Value	Description
31:5	RO	0h	Reserved
4	RW	0h	Link Equalization Request 16.0 GT/S
3	RO	0h	Equalization 16.0 GT/S Phase 3 Successful
2	RO	0h	Equalization 16.0 GT/S Phase 2 Successful
1	RO	0h	Equalization 16.0 GT/S Phase 1 Successful
0	RO	0h	Equalization 16.0 GT/S Complete

8.1.13 Margining Extended Capability Register

Table 107: Margining Extended Capability Register Summary

Start Address	End Address	Symbol	Description
1BCh	1BFh	MARG_ID	Margining Extended Capability Header
1C0h	1C1h	MARG_L0_SA	Margining Port Capability
1C2h	1C3h	MARG_L0_CL	Margining Port Status
1C4h	1C5h	MARG_L1_SA	Margining Lane Control
1C6h	1C7h	MARG_L1_CL	Margining Lane Status

Table 108: Margining Extended Capability ID Register

Bits	Type	Default Value	Description
31:20	RO	224h	Next Pointer
19:16	RO	1h	Capability Version
15:0	RO	27h	Capability ID (Margining Extended capability)

Table 109: Margining Port Capability Register

Bits	Type	Default Value	Description
15:1	RO	0h	Reserved
0	RW	0h	Margining User Driver Software

Table 110: Margining Port Status Register

Bits	Type	Default Value	Description
15:2	RO	0h	Reserved
1	RO	0h	Margining Software Ready
0	RO	0h	Margining Ready

Table 111: Margining Lane Control Register

Bits	Type	Default Value	Description
15:8	RW	0h	Margin Payload
7	RW	0h	Reserved
6	RW	0h	Usage Model
5:3	RW	0h	Margin Type
2:0	RW	0h	Receiver Number

Table 112: Margining Lane Status Register

Bits	Type	Default Value	Description
15:8	RO	0h	Margin Payload Status
7	RO	0h	Reserved Status
6	RO	0h	Usage Model Status
5:3	RO	0h	Margin Type Status
2:0	RO	0h	Receiver Number Status

8.1.14 Latency Tolerance Reporting Capability Register

Table 113: Latency Tolerance Reporting Capability Register Summary

Start Address	End Address	Symbol	Description
224h	227h	LTR_ID	Latency Tolerance Reporting (LTR) Capability ID
228h	229h	LTR_SLR	LTR Max Snoop Latency Register
22Ah	22Bh	LTR_NSLR	LTR Max No-Snoop Latency Register

Table 114: LTR Extended Capability Header

Bits	Type	Default Value	Description
31:20	RO	22Ch	Next Capability Offset
19:16	RO	1h	Capability Version

15:0	RO	18h	PCI Express Extended Capability ID

Table 115: LTR Max Snoop latency Register

Bits	Type	Default Value	Description
15:13	RO	0h	Reserved
12:10	RW	0h	Max Snoop latency Scale
9:0	RW	0h	Max Snoop latency Value

Table 116: LTR Max No Snoop latency Register

Bits	Type	Default Value	Description
15:13	RO	0h	Reserved
12:10	RW	0h	Max No Snoop Latency Scale
9:0	RW	0h	Max No Snoop Latency Value

8.1.15 L1 Substates Capability Register

Table 117: L1 Substates Capability Register Summary

Start Address	End Address	Symbol	Description
22Ch	22Fh	L1S_CID	L1 Substate Capability ID
230h	233h	L1S_CR	L1 Substate Capability Register
234h	237h	L1S_C1R	L1 Substate Control 1 Register
238h	23Bh	L1S_C2R	L1 Substate Control 2 Register

Table 118: L1 Substates Extended Capability Header

Bits	Type	Default Value	Description
31:20	RW	0h	Next Capability Offset
19:16	RW	1h	Capability Version
15:0	RW	1Eh	PCI Express Extended Capability ID

Table 119: L1 Substates Capability Register

Bits	Type	Default Value	Description
31:24	RO	0h	Reserved
23:19	RW	5h	Port Power on value
18	RO	0h	Reserved

17:16	RO	0h	Port T_Power on scale
15:8	RO	Ah	Port Common mode restore time
7:5	RO	0h	Reserved
4	RO	1h	L1 PM Substates Supported
3	RO	1h	ASPM PM L1.1 Supported
2	RO	1h	ASPM PM L1.2 Supported
1	RO	1h	PCI PM L1.1 Supported
0	RO	1h	PCI PM L1.2 Supported

Table 120: L1 Substates Control1 Register

Bits	Type	Default Value	Description
31:29	RW	0h	LTR L1.2 Threshold Scale
28:26	RO	0h	Reserved
25:16	RW	0h	LTR L1.2 Threshold value
15:8	RO	0h	Common mode restore time(N/A)
7:4	RO	0h	Reserved
3	RW	0h	ASPM PM L1.1 Supported
2	RW	0h	ASPM PM L1.2 Supported
1	RW	0h	PCI PM L1.1 Supported
0	RW	0h	PCI PM L1.2 Supported

Table 121: L1 Substates Control2 Register

Bits	Type	Default Value	Description
31:8	RO	0h	Reserved
7:3	RW	5h	T_POWER_ON Value
2	RO	0h	Reserved
1:0	RW	0h	T_POWER_ON Scale

8.2 NVM Express Register

8.2.1 Register Summary

Table 122: Register Summary

Start Address	End Address	Name	Type
00h	07h	CAP	Controller Capabilities
08h	0Bh	VS	Version
0Ch	0Fh	INTMS	Interrupt Mask Set
10h	13h	INTMC	Interrupt Mask Clear
14h	17h	CC	Controller Configuration
18h	1Bh	Reserved	Reserved
1Ch	1Fh	CSTS	Controller Status
20h	23h	NSSR	NVM Subsystem Reset (Optional)
24h	27h	AQA	Admin Queue Attributes
28h	2Fh	ASQ	Admin Submission Queue Base Address
30h	37h	ACQ	Admin Completion Queue Base Address
38h	5Bh	Optional	Optional
5Ch	DFFh	Reserved	Reserved
E00h	E1Bh	Optional	Optional
E1Ch	FFFh	Reserved	Command Set Specific
1000h	1003h	SQ0TDBL	Submission Queue 0 Tail Doorbell (Admin)
1000h + (1 * (4 << CAP.DSTRD))	1003h + (1 * (4 << CAP.DSTRD))	CQ0HDBL	Completion Queue 0 Head Doorbell (Admin)
...			
1000h+ (2y * (4 << CAP.DSTRD))	1003h + (2y * (4 << CAP.DSTRD))	SQyTDVL	Submission Queue y Tail Doorbell
1000h + ((2y + 1) * (4 << CAP.DSTRD))	1003h + ((2y + 1) * (4 << CAP.DSTRD))	CQYHDBL	Completion Queue y Head Doorbell

8.2.2 Controller Register

Table 123: Controller Capabilities

Bits	Type	Name	Default Value	Description
63:56	RO	-	0h	Reserved
55:52	RO	MPSMAX	3h	Memory Page Size Maximum (Maximum is 4KB)

51:48	RO	MPSMIN	0h	Memory Page Size Minimum (Minimum is 4KB)
47:45	RO	-	0h	Reserved
44:37	RO	CSS	1h	Command Sets Supported 1h: NVM command set
36	RO	NSSRS	0h	NVM Subsystem Reset Supported
35:32	RO	DSTRD	0h	Doorbell Stride 0: Stride of 4 bytes
31:24	RO	TO	FFh	Timeout
23:19	RO	-	0h	Reserved
18:17	RO	AMS	1h	Arbitration Mechanism Supported (Weighted Round Robin with Urgent supported)
16	RO	CQR	1h	Contiguous Queues Required
15:00	RO	MQES	1FFh	Maximum Queue Entries Supported

Table 124: Version

Bits	Type	Name	Default Value	Description
31:16	RO	MJR	1h	Major Version Number
15:0	RO	MNR	400h	Minor Version Number

Table 125: Interrupt Mask Set

Bits	Type	Name	Default Value	Description
31:0	RW1S	IVMS	0h	Interrupt Vector Mask Set

Table 126: Interrupt Mask Clear

Bits	Type	Name	Default Value	Description
31:00	RW	IVMC	0h	Interrupt Vector Mask Clear

Table 127: Controller Configuration

Bits	Type	Name	Default Value	Description
31:24	RO	-	0h	Reserved
23:20	RW	IOCQES	0h	I/O Completion Queue Entry Size (Configured as a power of 2) (Should be set to 4 for a 16-byte entry size)

19:16	RW	IOSQES	0h	I/O Submission Queue Entry Size (Configured as a power of 2) (Should be set to 6 for a 64-byte entry size)
15:14	RW	SHN	0h	Shutdown Notification 0h: No notification 1h: Normal shutdown notification 2h: Abrupt shutdown notification 3h: Reserved CSTS.SHST indicates shutdown status.
13:11	RW	AMS	0h	Arbitration Mechanism Selected 0h: Round Robin No other values supported.
10:7	RW	MPS	0h	Memory Page Size MPS is 2^(12+MPS) Shall be within CAP.MPSMAX and CAP.MPSMIN ranges.
6:4	RW	CSS	0h	Command Set Selected 0h: NVM Command Set No other values supported
3:1	RO	-	0h	Reserved
0	RW	EN	0h	Enable When set to 1, controller shall process commands. When cleared to 0, controller shall not process commands. This field is subject to CSTS.RDY and CAP.TO restrictions.

Table 128: Controller Status

Bits	Type	Name	Default Value	Description
31:6	RO	-	0h	Reserved
5	RW	PP	0h	Processing Paused
4	RW	NSSRO	0h	NVM Subsystem Reset Occurred
3:2	RO	SHST	0h	Shutdown Status 0h: Normal operation, no shutdown requested. 1h: Shutdown processing occurring. 2h: Shutdown processing complete. 3h: Reserved
1	RO	CFS	0h	Controller Fatal Status

0	RO	RDY	0h	1h: Controller ready to process commands. 0h: Controller shall not process commands.

Table 129: Admin Queue Attributes

Bits	Type	Name	Default Value	Description
31:28	RO	-	0h	Reserved
27:16	RW	ACQS	0h	Admin Completion Queue Size Max: 4096 (Value of 4095h - 0's-based value)
15:12	RO	-	0h	Reserved
11:0	RW	ASQS	0h	Admin Submission Queue Size Max: 4096 (Value of 4095h - 0's-based value)

Table 130: Admin Submission Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ASQB	0h	Admin Submission Queue Base Address
11:0	RO	-	0h	Reserved

Table 131: Admin Completion Queue Base Address

Bits	Type	Name	Default Value	Description
63:12	RW	ACQB	0h	Admin Completion Queue Base Address
11:0	RO	-	0h	Reserved

Table 132: Submission Queue Tail y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO	-	0h	Reserved
15:0	RW	SQT	0h	Submission Queue Tail

Table 133: Completion Queue Head y Doorbell

Bits	Type	Name	Default Value	Description
31:16	RO	-	0h	Reserved
15:0	RW	CQH	0h	Completion Queue Head

9. Supported NVMe commands

Exascend PE4 series SSDs support the NVMe commands that are shown in the following table. For details about the NVMe commands, please refer to the NVMe 1.4 command set specifications.

9.1 Admin Commands

Table 134: Admin Commands

Admin Commands	Opcode (Hex)	S/O
Delete I/O Submission Queue	00h	S
Create I/O Submission Queue	01h	S
Get Log Page	02h	S
Delete I/O Completion Queue	04h	S
Create I/O Completion Queue	05h	S
Identify	06h	S
Abort	08h	S
Set feature	09h	S
Get feature	0Ah	S
Asynchronous event request	0Ch	S
Namespace Management	0Dh	O
Firmware commit	10h	S
Firmware image download	11h	S
Device Self-test	14h	O
Namespace Management	15h	O
Format NVM	80h	S
Security Send	81h	O
Security Receive	82h	O
Sanitize	84h	O

Note: S-support O-optional

9.1.1 Identify Command

Table 135: Identify Controller Data Structure

Bytes	O/M	Default Value	Description
1:0	M	1B4Bh	PCI Vendor ID
3:2	M	1B4Bh	PCI Subsystem Vendor ID

23:4	M	##############	Serial Number (ASCII), #: Variables
63:24	M	##############	Model Number (ASCII)
71:64	M	########	Firmware Revision, #: Variables
72	M	0h	Recommended Arbitration Burst
75:73	M	70B3D5h	IEEE OUI
76	O	0h	Multi-Interface Capabilities and Namespace Sharing Capability Bit 2: 1h - Controller is associated with an SR-IOV Virtual Function 0h - Controller is associated with a PCI Function Bit 1: 1h - Device has Two or More Controller 0h - Device has One Controller Bit 0: 1h - Device has Two or More physical PCI Express ports 0h - Device has One PCI Express port
77	M	6h	Maximum Data Transfer Size 6h: 256KB
79:78	M	1321h	Controller ID (CNTLID)
83:80	M	10400h	Controller Version
87:84	M	0h	RTD3 Resume Latency
91:88	M	0h	RTD3 Entry Latency
95:92	M	0h	OAES
99:96	M	0h	CTRATT
101:100	O	0h	RRLS
110:102	-	0h	Reserved
111	M	1h	Controller Type (CNTRLTYPE)
127:112	O	0h	FRU Globally Unique Identifier (FGUID)
129:128	O	0h	CRDT1
131:130	O	0h	CRDT2
133:132	O	0h	CRDT3
239:134	-	0h	Reserved
255:240	M	-	NVMe Management Interface Specification for Definition

257:256	M	56h	Optional Admin Command Support Bits 15:10 – Reserved Bit 9 if set to '1', then the controller supports the Get LBA Status capability (refer to section 8.22). If cleared to '0', then the controller does not support the Get LBA Status capability. Bit 8 if set to '1', then the controller supports the Doorbell Buffer Config command. If cleared to '0', then the controller does not support the Doorbell Buffer Config command. Bit 7 if set to '1', then the controller supports the Virtualization Management command. If cleared to '0', then the controller does not support the Virtualization Management command. Bit 6 if set to '1', then the controller supports the NVMe-MI Send and NVMe-MI Receive commands. If cleared to '0', then the controller does not support the NVMe-MI Send and NVMe-MI Receive commands. Bit 5 if set to '1' then the controller supports Directives. If cleared to '0' then the controller does not support Directives. A controller that supports Directives shall support the Directive Send and Directive Receive commands. Bit 4 if set to '1' then the controller supports the Device Self-test command. If cleared to '0' then the controller does not support the Device Self-test command. Bit 3: 1h - Namespace Management and Namespace Attachment Commands Supported Bit 2: 1h – Firmware Activate/Download Supported Bit 1: 1h Format NVM Supported Bit 0: 0 Security Send and Security Receive Not Supported
258	M	3h	Abort Command Limit (Maximum number of concurrently outstanding Abort commands) (0's-based value)
259	M	3h	Asynchronous Event Request Limit (Maximum number of concurrently outstanding Asynchronous Event Request commands) (0's-based value)
260	M	2h	Firmware Updates Bits7:5– Reserved Bits4 – 1h Controller supports firmware activation without a reset.0h Controller requires a reset for firmware to be activated. Bits3:1– Number of firmware slots Bit 0 – 1h Slot 1 is read only

261	M	2h	Log Page Attributes Bits 7:1 – Reserved Bit 0: 0h SMART data is global for all namespaces
262	M	3Fh	Error Log Page Entries (Number of Error Information log entries stored by controller) (0's-based value)
263	M	5h	Number of Power States Support (0's-based value)
264	M	1h	Admin Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates Admin Vendor Specific Commands use the format defined. in Admin and NVM Vendor Specific Commands (Optional) table of NVM Express spec.
265	O	1h	Autonomous Power State Transition Attributes (APSTA)
267:266	M	166h	Warning Composite Temperature Threshold
269:268	M	170h	Critical Composite Temperature Threshold
271:270	O	0h	Maximum Time for Firmware Activation
275:272	O	0h	Host Memory Buffer Preferred Size
279:276	O	0h	Host Memory Buffer Minimum Size
295:280	O	1BF244B0h * 512 (240GB) 37E436B0h * 512 (480GB) 6FC81AB0h * 512 (960GB) DF8FE2B0h * 512 (1920GB) 1BF1F72B0h * 512 (3840GB) 37E3E92B0h *512 (7680GB)	Total NVM Capacity
311:296	O	0h	Unallocated NVM Capacity
315:312	O	0h	Replay Protected Memory Block Support (N/A)
317:316	O	0h	Extended Device Self-test Time (EDSTT)
318	O	0h	Device Self-test Options (DSTO)
319	M	1h	Firmware Update Granularity (FWUG)
321:320	M	0h	Keep Alive Support (KAS)
323:322	O	0h	Host Controlled Thermal Management Attributes (HCTMA)

325:324	O	0h	Minimum Thermal Management Temperature (MNTMT)
327:326	O	0h	Maximum Thermal Management Temperature (MXTMT)
331:328	O	40000002h	Sanitize Capabilities (SANICAP)
335:332	O	0h	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS)
337:336	O	0h	Host Memory Maximum Descriptors Entries (HMMAXD)
339:338	O	0h	NVM Set Identifier Maximum (NSETIDMAX)
341:340	O	0h	Endurance Group Identifier Maximum (ENDGIDMAX)
342	O	0h	ANA Transition Time (ANATT)
343	O	0h	Asymmetric Namespace Access Capabilities (ANACAP)
347:344	O	0h	ANA Group Identifier Maximum (ANAGRPMAX)
351:348	O	0h	Number of ANA Group Identifiers (NANAGRPID)
355:352	O	0h	Persistent Event Log Size (PELS)
511:356	-	0h	Reserved
512	M	66h	Submission Queue Entry Size Bits 7:4 – 6h Max SQES (64 bytes) Bits 3:0 – 6h Required SQES (64 bytes)
513	M	44h	Completion Queue Entry Size Bits 7:4 – 4h Max SQES (16 bytes) Bits 3:0 – 4h Required SQES (16 bytes)
515:514	-	0h	Reserved
519:516	M	1h	Number of Namespaces
521:520	M	1Fh	Optional NVM Command Support Bits 15:6 – Reserved Bit 5 – 1h Reservations Supported, 0h Not support Reservations. Bit 4 – 1h Save field in Set Feature & Select field in Get Feature Supported 0h Not support Save field in Set Feature & Select field in Get Feature Bit 3 – 1h Write Zeros Supported 0h Not support Write Zeros Bit 2 – 1h Dataset Management Supported 0h Not support Dataset Management Bit 1 – 1h Write Uncorrectable Supported

			0h Not support Write Uncorrectable Bit 0 – 1h Compare Supported 0h Not support Compare
523:522	M	0h	Fused Operation Support Bits 15:1 – Reserved Bit 0 – 0h Compare/Write Fused Operation Not Supported
524	M	0h	Format NVM Attributes Bits 7:3 – Reserved Bit 2 – 1h Cryptographic Erase Bit 1 – 1h Secure Erase Per Namespace Bit 0 – 0h Format Per Namespace
525	M	0h	Volatile Write Cache 0h – No VWC present
527:526	M	FFh	Atomic Write Unit Normal
529:528	M	7h	Atomic Write Unit Power Fail (0's-based value)
530	M	1h	NVM Vendor Specific Command Configuration Bits 7:1 – reserved Bit 0 – Indicates NVM Vendor Specific Commands use the format defined in NVM Express specification
531	M	0h	Namespace Write Protection Capabilities (NWPC)
533:532	O	0h	ACWU
535:534	-	0h	Reserved
539:536	O	0h	SGL Support (SGLS) - No SGL support
543:540	O	0h	Maximum Number of Allowed Namespaces (MNAN)
767:544	-	0h	Reserved
1023:768	M	'nqn.2020-03.com.exascend:nvme:nvm-subsystem-sn-##########'	NVM Subsystem NVMe Qualified Name (######: Serial Number (ASCII)) This field specifies the NVM Subsystem NVMe Qualified Name as a UTF-8 null-terminated string
1791:1024	-	0h	Reserved
2047:1792	-	0h	Reserved (Refer to the NVMe over Fabrics specification)
Power State Descriptors			

2079:2048	M	Refer to 'Power State 0 Descriptor Data Structure'	Power State 0 Descriptor
2111:2080	O	Refer to 'Power State 1 Descriptor Data Structure'	Power State 1 Descriptor
2143:2112	O	Refer to 'Power State 2 Descriptor Data Structure'	Power State 2 Descriptor
2175:2144	O	Refer to 'Power State 3 Descriptor Data Structure'	Power State 3 Descriptor
2207:2176	O	Refer to 'Power State 4 Descriptor Data Structure'	Power State 4 Descriptor
2239:2208	O	Refer to 'Power State 5 Descriptor Data Structure'	Power State 5 Descriptor
…	-	0h	N/A
3071:3040	O	0h	Power State 31 Descriptor (N/A)
Vendor Specific			
4095:3072	-	-	Exascend Reserved

Table 136: Identify Power State 0 Descriptor Data Structure

Bits	Power State 0	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale (APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload (APW)
175:160	0h	Active Power (ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale (IPS)
149:144	0h	Reserved
143:128	0h	Idle Power (IDLP)
127:125	0h	Reserved
124:120	0h	Relative Write Latency
119:117	0h	Reserved
116:112	0h	Relative Write Throughput
111:109	0h	Reserved

108:104	0h	Relative Read Latency
103:101	0h	Reserved
100:96	0h	Relative Read Throughput
95:64	0h	Exit Latency
63:32	0h	Entry Latency
31:26	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Reserved
15:00	320h	Maximum Power

Table 137: Identify Power State 1 Descriptor Data Structure

Bits	Power State 1	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale (APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload (APW)
175:160	0h	Active Power (ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale (IPS)
149:144	0h	Reserved
143:128	0h	Idle Power (IDLP)
127:125	0h	Reserved
124:120	1h	Relative Write Latency
119:117	0h	Reserved
116:112	1h	Relative Write Throughput
111:109	0h	Reserved
108:104	1h	Relative Read Latency
103:101	0h	Reserved
100:96	1h	Relative Read Throughput
95:64	0h	Exit Latency

63:32	0h	Entry Latency
31:26	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Reserved
15:00	190h	Maximum Power

Table 138: Identify Power State 2 Descriptor Data Structure

Bits	Power State 2	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale (APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload (APW)
175:160	0h	Active Power (ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale (IPS)
149:144	0h	Reserved
143:128	0h	Idle Power (IDLP)
127:125	0h	Reserved
124:120	2h	Relative Write Latency
119:117	0h	Reserved
116:112	2h	Relative Write Throughput
111:109	0h	Reserved
108:104	2h	Relative Read Latency
103:101	0h	Reserved
100:96	2h	Relative Read Throughput
95:64	0h	Exit Latency
63:32	0h	Entry Latency
31:26	0h	Reserved
25	0h	Non-Operational State

24	0h	Max Power Scale
23:16	0h	Reserved
15:00	C8h	Maximum Power

Table 139: Identify Power State 3 Descriptor Data Structure

Bits	Power State 3	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale (APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload (APW)
175:160	0h	Active Power (ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale (IPS)
149:144	0h	Reserved
143:128	0h	Idle Power (IDLP)
127:125	0h	Reserved
124:120	3h	Relative Write Latency
119:117	0h	Reserved
116:112	3h	Relative Write Throughput
111:109	0h	Reserved
108:104	3h	Relative Read Latency
103:101	0h	Reserved
100:96	3h	Relative Read Throughput
95:64	0h	Exit Latency
63:32	0h	Entry Latency
31:26	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Reserved
15:00	64h	Maximum Power

Table 140: Identify Power State 4 Descriptor Data Structure

Bits	Power State 4	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale (APS)
181:179	0h	Reserved
178:176	0h	Active Power Workload (APW)
175:160	0h	Active Power (ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale (IPS)
149:144	0h	Reserved
143:128	0h	Idle Power (IDLP)
127:125	0h	Reserved
124:120	4h	Relative Write Latency
119:117	0h	Reserved
116:112	4h	Relative Write Throughput
111:109	0h	Reserved
108:104	4h	Relative Read Latency
103:101	0h	Reserved
100:96	4h	Relative Read Throughput
95:64	7530h	Exit Latency
63:32	7530h	Entry Latency
31:26	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Reserved
15:00	2BCh	Maximum Power

Table 141: Identify Power State 5 Descriptor Data Structure

Bits	Power State 5	Description
255:184	0h	Reserved
183:182	0h	Active Power Scale (APS)

181:179	0h	Reserved
178:176	0h	Active Power Workload (APW)
175:160	0h	Active Power (ACTP)
159:152	0h	Reserved
151:150	0h	Idle Power Scale (IPS)
149:144	0h	Reserved
143:128	0h	Idle Power (IDLP)
127:125	0h	Reserved
124:120	5h	Relative Write Latency
119:117	0h	Reserved
116:112	5h	Relative Write Throughput
111:109	0h	Reserved
108:104	5h	Relative Read Latency
103:101	0h	Reserved
100:96	5h	Relative Read Throughput
95:64	C350h	Exit Latency
63:32	C350h	Entry Latency
31:26	0h	Reserved
25	0h	Non-Operational State
24	0h	Max Power Scale
23:16	0h	Reserved
15:00	64h	Maximum Power

Table 142: Identify Namespace Data Structure

Bytes	O/M	Default Value		Description
7:0	M	240GB	1BF244B0h (512B)	Namespace Size
		480GB	37E436B0h (512B)	
		960GB	6FC81AB0h (512B)	
		1920GB	DF8FE2B0h (512B)	
		3840GB	1BF1F72B0h (512B)	
		7680GB	37E3E92B0h (512B)	

15:8	M	240GB 480GB 960GB 1920GB 3840GB 7680GB	1BF244B0h (512B) 37E436B0h (512B) 6FC81AB0h (512B) DF8FE2B0h (512B) 1BF1F72B0h (512B) 37E3E92B0h (512B)	Namespace Capacity
23:16	M	0h		Namespace Utilization
24	M	0h		Namespace Features
25	M	0h		Number of LBA Formats
26	M	0h		Formatted LBA Size Bits 7:5 – Reserved Bit 4: Metadata interleaved or separate (based on LBA format) Bit 3:0 – Indicates LBA format.
27	M	0h		Metadata Capabilities Bits 7:2 – Reserved Bit 1 – Supports Metadata as separate buffer. Bit 0 – Supports Metadata as extended LBA.
28	M	0h		End-to-end Data Protection Capabilities Bits 7:5 – Reserved Bit 4 – Supports protection information as last 8 bytes of Metadata. Bit 3 – Supports protection information as first 8 bytes of metadata. Bit 2 – Supports Type 3 protection information. Bit 1 – Supports Type 2 protection information. Bit 0 – Supports Type 1 protection information.
29	M	0h		End-to-End Data Protection Type Settings Bits 7:4 – Reserved Bit 3 – 1: Protection information transferred as first 8 bytes of metadata Bit 3 – 0: Protection information transferred as last 8 bytes of metadata. Bit 2:0 – 000b: Protection information disabled Bit 2:0 – 1h: Protection type 1 enabled Bit 2:0 – 2h: Protection type 2 enabled. Bit 2:0 – 3h: Protection type 3 enabled
30	O	0h		Namespace Multi-path I/O and Namespace sharing Capabilities (NMIC) Bits 7:1 - Reserved Bit 0 - 1: Accessible by two or more controllers

			Bit 0 - 0: Private namespace
31	O	0h	Reservation Capabilities (RESCAP) Bits 7 - Reserved Bits 6 - 1: Namespace supports the Exclusive Access (All Registrants reservation type) Bit 5 - 1: Namespace supports the Write Exclusive (All Registrants reservation type) Bit 4 - 1: Namespace supports the Exclusive Access (Registrants only reservation type) Bit 3 - 1: Namespace supports the Write Exclusive (Registrants only reservation type) Bit 2 - 1: Namespace supports the Exclusive Access Reservation type Bit 1 - 1: Namespace supports the Write Exclusive Reservation type Bit 0 - 1: Namespace supports the Persist Through Power Loss capability
32	O	0h	Format Progress Indicator (FPI)
33	-	0h	Reserved
35:34	O	0h	Namespace Atomic Write Unit Normal(N/A)
37:36	O	0h	Namespace Atomic Write Unit Power Fail(N/A)
39:38	O	0h	Namespace Atomic Compare & Write Unit(N/A)
41:40	O	0h	Namespace Atomic Boundary Size Normal(N/A)
43:42	O	0h	Namespace Atomic Boundary Offset(N/A)
45:44	O	0h	Namespace Atomic Boundary Size Power Fail(N/A)
47:46	-	0h	Reserved
63:48	O	1BF244B0h * 512 (240GB) 37E436B0h * 512 (480GB) 6FC81AB0h * 512 (960GB) DF8FE2B0h * 512 (1920GB) 1BF1F72B0h * 512 (3840GB) 37E3E92B0h * 512 (7680GB)	NVM Capacity (NVMCAP)
103:64	-	0h	Reserved
119:104	O	##########################h	Namespace Globally Unique Identifier (NGUID) #: Variables *NGUID specifies data in a big-endian format.
127:120	O	##########################h	IEEE Extended Unique Identifier (EUI64) #: Variables *EUI64 specifies data in a big-endian format.

131:128	M	refer to 'LBA Format 0 Data Structure'	LBA Format 0 Support
135:132	O	0h	LBA Format 1 Support (N/A)
139:136	O	0h	LBA Format 2 Support (N/A)
143:140	O	0h	LBA Format 3 Support (N/A)
147:144	O	0h	LBA Format 4 Support (N/A)
…			
191:188	O	0h	LBA Format 15 Support (N/A)
383:192	-	0h	Reserved
Vendor Specific			
4095:384	-	-	Exascend Reserved

Table 143: LBA Format 0 Data Structure

Bits	Name	Default Value	Description
31:26		0h	Reserved
25:24	RP	0h	Relative Performance
23:16	LBADS	9h	LBA Data Size
15:00	MS	0h	Metadata Size

9.2 NVM Commands

Table 144: NVM Commands

NVM Commands	Opcode (Hex)	S/O
Flush	00h	S
Write	01h	S
Read	02h	S
Write Uncorrectable	04h	S
Compare	05h	S
Write Zeroes	08h	S
Dataset Management	09h	S

Note: S-support O-optional

9.3 Log Pages

Table 145: Log Pages

Log Page Name	Log Identifier (Hex)	S/O
Error Information	01h	S
SMART / Health Information	02h	S
Firmware Slot Information	03h	S
Commands Supported and Effects	05h	S
Device Self-test	06h	O
Sanitize Status	81h	O

Note: S-support O-optional

9.4 NVMe Features

Table 146: NVMe Features

Feature Name	Feature Identifier (Hex)	S/O
Arbitration	01h	S
Power Management	02h	S
Temperature Threshold	04h	S
Number of Queues	07h	S
Interrupt Coalescing	08h	S
Interrupt Vector Configuration	09h	S
Asynchronous Event Configuration	0Bh	S
Autonomous Power State Transition	0Ch	S
Sanitize Config	17h	0

Note: S-support O-optional

10. S.M.A.R.T. support

10.1 Overview of S.M.A.R.T. support

Data storage drives capture a variety of information during operation that may be used to analyze drive "health." Drive manufacturers have adopted S.M.A.R.T. (Self-Monitoring, Analysis, and Reporting Technology) to help warn system software, a system administrator, or a user of impending drive failure, when time still remains to take preventive action. The S.M.A.R.T. standard defines the protocols for reporting errors and for invoking self-tests to collect and analyze data on demand. The specification is flexible and provides for individual manufacturers to define their own unique vendor-specific information. This section describes the baseline S.M.A.R.T. commands and attributes supported by products in the Exascend PE4 series. Further, it is recommended to consult the list of public S.M.A.R.T. attributes.

10.2 S.M.A.R.T. health information

Table 147: S.M.A.R.T. health information

BYTE	DESCRIPTION
00	**Critical warning:** This field indicates critical warnings for the state of the controller. Each bit corresponds to a critical warning type; multiple bits may be set. If a bit is cleared to '0', then that critical warning does not apply. Critical warnings may result in an asynchronous event notification to the host. Bits in this field represent the current associated state and are not persistent.
2:1	**Composite temperature:** Contains a value corresponding to a temperature in degrees Kelvin that represents the current composite temperature of the controller and namespace(s) associated with that controller. The manner this value is computed is implementation-specific and may not represent the actual temperature of any physical point in the NVM subsystem. The value of this field may be used to trigger an asynchronous event. Warning and critical overheating composite temperature threshold values are reported by the WCTEMP and CCTEMP fields in the Identify Controller data structure.
3	**Available spare:** Contains a normalized percentage (0 to 100%) of the remaining spare capacity available.
4	**Available spare threshold:** When the *available spare* falls below the threshold indicated in this field, an asynchronous event completion may occur. The value is indicated as a normalized percentage (0 to 100%).
5	**Percentage used:** Contains a vendor-specific estimate of the percentage of NVM subsystem life used based on the actual usage and the manufacturer's prediction of NVM life. A value of 100 indicates that the estimated endurance of the NVM in the NVM subsystem has been consumed but may not indicate an NVM subsystem failure. The value allowed to exceed 100. Percentages greater than 254 shall be represented as 255. This value shall be updated once per power-on hour (when the controller is not in a sleep state).
47:32	**Sectors read:** Contains the number of 512-byte user data units read from the controller; This value is reported in thousands (i.e., a value of 1 corresponds to 1000 units of 512 bytes read) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data read to 512-byte units.
63:48	**Sectors written:** Contains the number of 512-byte user data units written to the controller. This value is reported in thousands (i.e., a value of 1 corresponds to 1000 units of 512 bytes written) and is rounded up. When the LBA size is a value other than 512 bytes, the controller shall convert the amount of data written to 512-byte units. For the NVM* command set, logical blocks written as part of write operations shall be included in this value.
79:64	**Host read commands:** Indicates the number of read commands completed by the controller. For the NVM command set, this is the number of *compare* and *read* commands
95:80	**Host write commands:** Indicates the number of write commands completed by the controller. For the NVM command set, this is the number of *write* commands.
111:96	**Controller busy time:** Contains the amount of time the controller is busy with I/O commands. The controller is busy when there is a command outstanding to an I/O queue (specifically, a command was issued via an I/O submission queue tail doorbell write and the corresponding completion queue entry has not been posted yet to the associated I/O completion queue). This value is reported in minutes.

127:112	**Power cycles:** Contains the number of power cycles.
143:128	**Power-on hours:** Indicates the number of actively power-on hours. This does not include time the controller was powered and in a lower state condition.
159:144	**Number of unsafe shutdowns:** Indicates the number of unsafe shutdowns. This count is incremented when a shutdown notification (CC.SHN) is not received prior to loss of power
175:160	**Number of media errors:** Indicates the number of occurrences where the controller detected an unrecovered data integrity error. Errors such as uncorrectable ECC, CRC checksum failure, or LBA tag mismatch are included in this field.
195:192	**Warning composite temperature time:** Indicates the amount of time in minutes that the controller is operational and the Composite Temperature is greater than or equal to the Warning Composite Temperature Threshold (WCTEMP) field and less than the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure. If the value of the WCTEMP or CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
199:196	**Critical composite temperature time:** Contains the amount of time in minutes that the controller is operational, and the Composite Temperature is greater the Critical Composite Temperature Threshold (CCTEMP) field in the Identify Controller data structure. If the value of the CCTEMP field is 0h, then this field is always cleared to 0h regardless of the Composite Temperature value.
201:200	**Temperature sensor 1:** Contains the current temperature reported by temperature sensor 1 in degrees Kelvin.

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- the period ending when the device's Lifespan indicator has reached 0% or below.

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Revision history

Table 148: PE4 datasheet revision history

REVISION	DESCRIPTION	DATE
001	First released	November, 2021
002	Add M.2 2242	March, 2022
003	Add SMbus Signal	March, 2022
004	Add SED (TCG/AES)	May, 2022
005	Add 4TB & 8TB for M.2 2280	June, 2022
006	Update performance	August, 2022
007	Add sustained read/write (4KB) IOPS	November, 2022
008	Modify format	February, 2023
009	Modify E1.S physical dimension diagram	March, 2023
010	Add M.2 2230/2242 240GB/480GB/1920GB	April, 2023
011	Add physical insertion cycles	April, 2023
012	Modify format	May, 2023
013	Add M.2 2242 240G/480G	Jul, 2023
014	Add PCI and NVM Express Registers/Supported NVMe commands	August, 2023
015	Modify Sustained Read/Write IOPS Modify M.2 2230 Dimension Modify Pin Assignment	September, 2023