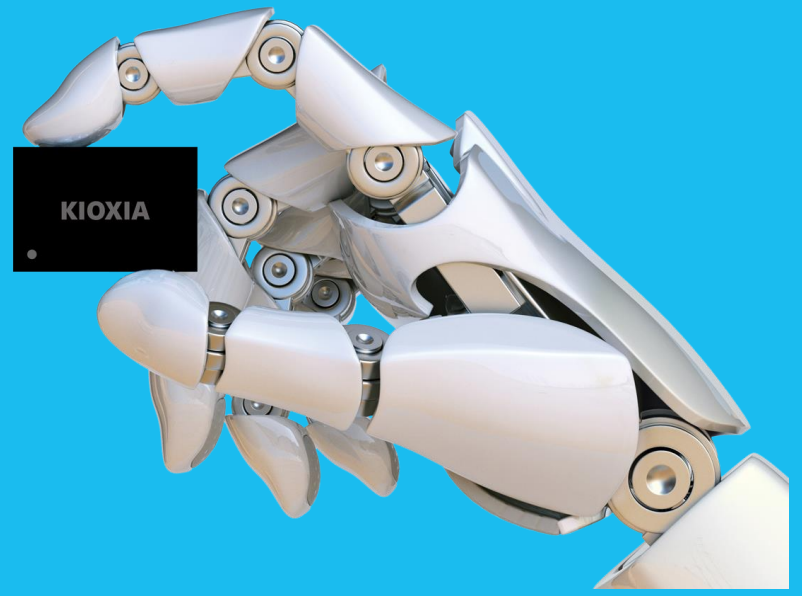
SLC NAND Flash Memory Products Roadmap

Memory Application Engineering Dept.2
Memory Division
January, 2021

KIOXIA

Overview



Demand for SLC NAND Flash Memory

Market Trend	Embedded Systems are becoming 'SMARTER'!
System Requirement	Large Density Memory Device is needed
Memory Requirement	**Compared to NOR Flash memory, lower bit cost and larger density SLC NAND Flash Memory demand is increasing!**

- Smart TV, Smart Watch, Smart Device, Smart Home, Smart Meter
- Many new innovative IOT devices
- Faster communication protocols (4G LTE, 5G, WiFi, GPON,etc.)
- Richer user interface and intelligent application software

- Larger firmware size
- Larger application software
- Larger size of user data and system log data

KIOXIA SLC NAND Flash Memory Product Family

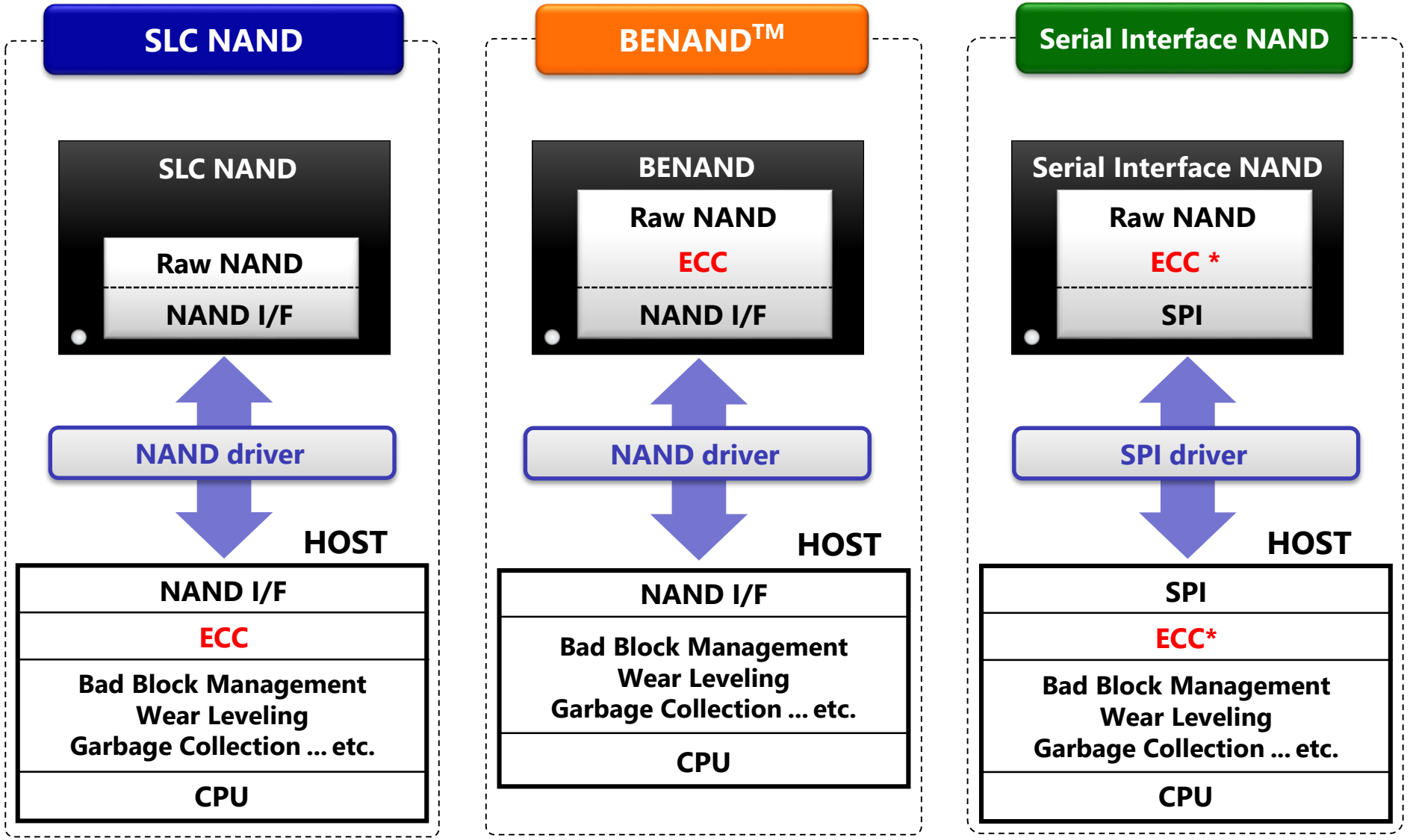
Parallel interface

Parallel interface

Serial interface

- BENAND™: Built-in ECC NAND
- All other company names, product names, and service names mentioned herein may be trademarks of their respective companies.

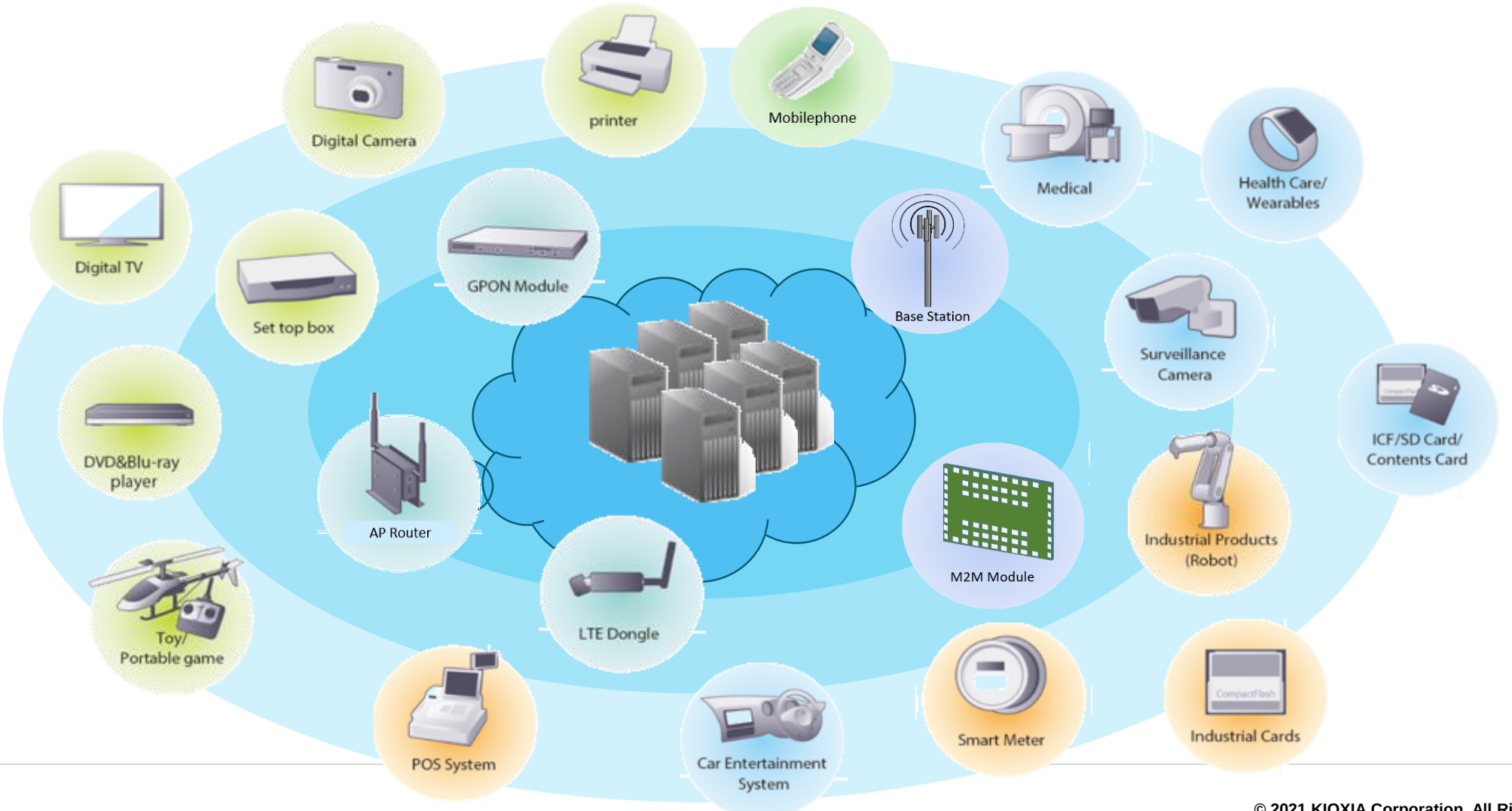
SLC NAND Flash Memory Product Concept



* The ECC logic in Serial Interface NAND can be enabled and disabled by the customers.

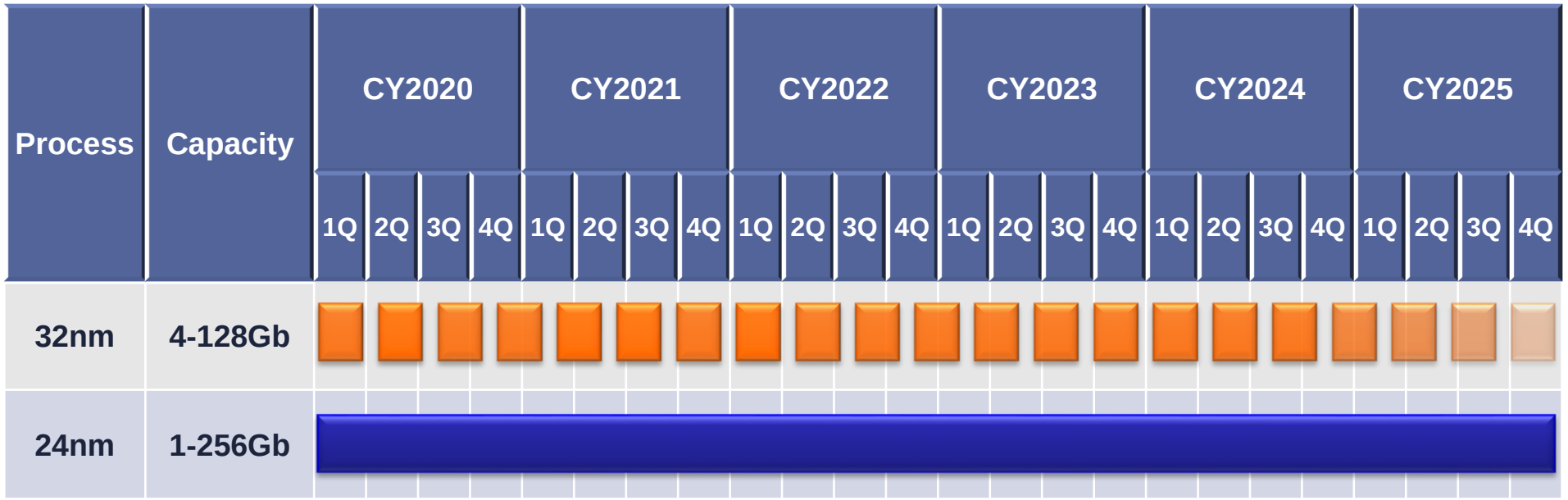
Target Application

KIOXIA NAND targets wide range of embedded applications.
These applications are examples of target for SLC NAND product family.



SLC NAND Technology Roadmap

KIOXIA will provide long-term support for SLC products and would like to grow our business with customers



Notice:
- This roadmap is subject to change without notice.
- Broken lines in 32nm process depend on business conditions.
- 24nm SLC NAND includes BENAND and Serial Interface NAND.

Process 32nm 24nm

SLC NAND Flash Memory Product Lineup

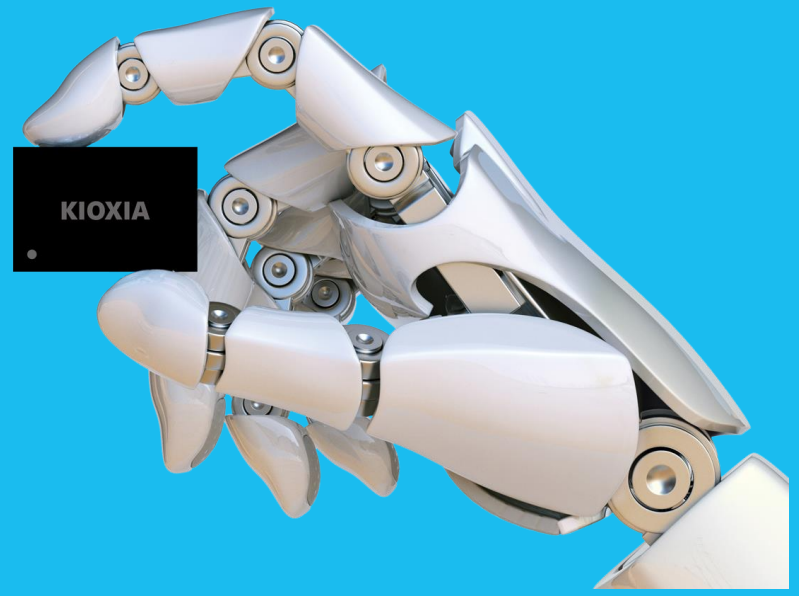
24nm SLC NAND Product Lineup

Density	SLC NAND	BENAND™	Serial Interface NAND
256Gb	32Gb × 8 *		
128Gb	32Gb × 4		
64Gb	32Gb × 2		
32Gb	32Gb		
16Gb	4Gb × 4		
8Gb	4Gb × 2	4Gb × 2	4Gb x 2
4Gb	4Gb / 2Gb × 2	4Gb / 2Gb × 2	4Gb
2Gb	2Gb	2Gb	2Gb
1Gb	1Gb	1Gb	1Gb

* 256Gbit SLC NAND product is only available on Toggle I/F.

- ✓ Offers wide lineup of density and package type
- ✓ Adopted in a wide range of applications from consumer use to industrial use because of its high Read / Write speed and high reliability
- ✓ BENAND™ with built-in ECC in SLC NAND and Serial Interface NAND with interface of Serial Peripheral Interface are available

SLC NAND Flash Memory
(Raw SLC NAND)



SLC NAND

To meet needs of diverse customers' application, our SLC NAND flash memory products offer wide line-up of density and package type.

SLC NAND is adopted in a wide range of applications from consumer use to industrial use because of its high Read and Write speed and high reliability.

➢ Features of SLC NAND

✓ 24nm SLC NAND process technology

✓ Available diverse package lineup for customer's needs
48TSOP (12 x 20 mm) / 63BGA (9 x 11 mm) / 67BGA (6.5 x 8 mm)

✓ Offers wide lineup of density
1Gbit, 2Gbit, 4Gbit, 8Gbit and 16Gbit are available in a lineup

* Please contact the KIOXIA sales representative for information about 32Gb die products.

SLC NAND Roadmap (1Gbit - 4Gbit)

Density	Page/ Block Size	Process	CY2020				CY2021				CY2022				CY2023				CY2024				CY2025			
			1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
1Gbit	2KB/ 128KB	24nm	1Gb x 1Chip																							
2Gbit		24nm	2Gb x 1Chip																							
4Gbit		24nm	2Gb x 2Chips (1CE)																							
	4KB/ 256KB	32nm																								
		24nm	4Gb x 1Chip																							

Notice:
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- Broken lines in 32nm process depend on business conditions.

Process: 32nm | 24nm

SLC NAND Roadmap (8Gbit - 32Gbit)

Density	Page/ Block Size	Process	CY2020				CY2021				CY2022				CY2023				CY2024				CY2025			
			1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
8Gbit	4KB/ 256KB	32nm																								
		24nm	4Gb x 2Chips (1CE)																							
16Gbit		32nm																								
		24nm	4Gb x 4Chips (2CE)																							
32Gbit		32nm																								

Notice:
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- Broken lines in 32nm process depend on business conditions.

Process 32nm 24nm

SLC NAND Roadmap (32Gb die products: 32Gbit - 256Gbit)

Density	Page/ Block Size	Process	CY2020				CY2021				CY2022				CY2023				CY2024				CY2025			
			1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
32Gbit	8KB/ 1MB	24nm	32Gb x 1chip																							
64Gbit		24nm	32Gb x 2chips																							
128Gbit		24nm	32Gb x 4chips																							
256Gbit		24nm	32Gb x 8chips																							

Notice:
- This roadmap is subject to change without notice.
- 24nm 32Gbit die base products are Vcc=3.3V only.
- Requires ECC 24bits/1KB correction and data randomization for 24nm 32Gbit die based products.

Process **24nm**

Interface Lineup

Density	Interface	
	Legacy	Toggle 2.0
32Gbit	✓	-
64Gbit	✓	✓
128Gbit	✓	✓
256Gbit	-	✓

1Gbit / 2Gbit SLC NAND Specification

SLC NAND Die Density		1Gbit		2Gbit	
NAND Design Rule		24nm		24nm	
ECC Requirement		8bit/512Byte		8bit/512Byte	
Architecture	Power Supply	3.3V	1.8V	3.3V	1.8V
	Page Size [Bytes]	2048+128		2048+128	
	Pages Per Block	64		64	
	Block Size [Bytes]	128K+8K		128K+8K	
	Valid Blocks	1004 - 1024		2008 - 2048	
	Plane	1		2	
Operation	Cache Operation	Support		Support	
	Multi Page/Block Operation	Not Support		Support	
Performance	tWC & tRC (Max. Data Rate)	25ns		25ns	
	tPROG (typ.)	300µs		300µs	
	tR (max)	25µs		25µs	
	tBERASE (typ.)	2.5ms	3.5ms	2.5ms	3.5ms
Package (Temp.)	TSOP48 (0 to 70°C / -40 to 85°C)	✓	-	✓	-
	FBGA63 (-40 to 85°C)	✓	✓	✓	✓
	FBGA67 (-40 to 85°C)	✓	✓	✓	✓

4Gbit / 8Gbit SLC NAND Specification

SLC NAND Die Density		4Gbit				8Gbit	
NAND Design Rule		32nm		24nm		32nm	
ECC Requirement		4bit/512Byte		8bit/512Byte		4bit/512Byte	
Architecture	Power Supply	3.3V	1.8V	3.3V	1.8V	3.3V	1.8V
	Page Size [Bytes]	4096+224		4096+256		4096+232	
	Pages Per Block	64		64		64	
	Block Size [Bytes]	256K+14K		256K+16K		256K+14.5K	
	Valid Blocks	2008 - 2048		2008 - 2048		4016 - 4096	
	Plane	2		2		2	
Operation	Cache Operation	Support		Support		Support	
	Multi Page/Block Operation	Support		Support		Support	
Performance	tWC & tRC (Max. Data Rate)	25ns		25ns		25ns	
	tPROG (typ.)	300µs		300µs		300µs	
	tR (max)	30µs		25µs		30µs	
	tBERASE (typ.)	3ms		2.5ms	3.5ms	3ms	
Package (Temp.)	TSOP48 (0 to 70°C / -40 to 85°C)	✓	-	✓	-	✓	-
	FBGA63 (-40 to 85°C)	✓	✓	✓	✓	✓	✓
	FBGA67 (-40 to 85°C)	-	-	✓	✓	-	-

32Gbit die SLC NAND Specification

SLC NAND Die Density		32Gbit	
NAND Design Rule		24nm	
Interface		Legacy	Toggle 2.0
ECC Requirement		24bit/1KByte	24bit/1KByte
Architecture	Power Supply	3.3V	3.3V *
	Page Size [Bytes]	8K+1K	8K+1K
	Pages Per Block	128	128
	Block Size [Bytes]	1M+128K	1M+128K
	Valid Blocks	4036 - 4156	4036 - 4156
	Plane	2	2
Operation	Cache Operation	Support	Support
	Multi Page/Block Operation	Support	Support
Performance	tWC & tRC (Max. Data Rate)	20ns	400MT/s
	tPROG (typ.)	400µs	400µs
	tR (typ./ max)	35µs/45µs	35µs/45µs
	tBERASE (typ.)	4.5ms	4.5ms
Package (Temp.)		TSOP48 (0 to 70°C / -40 to 85°C)	BGA132 (0 to 70°C / -40 to 85°C)

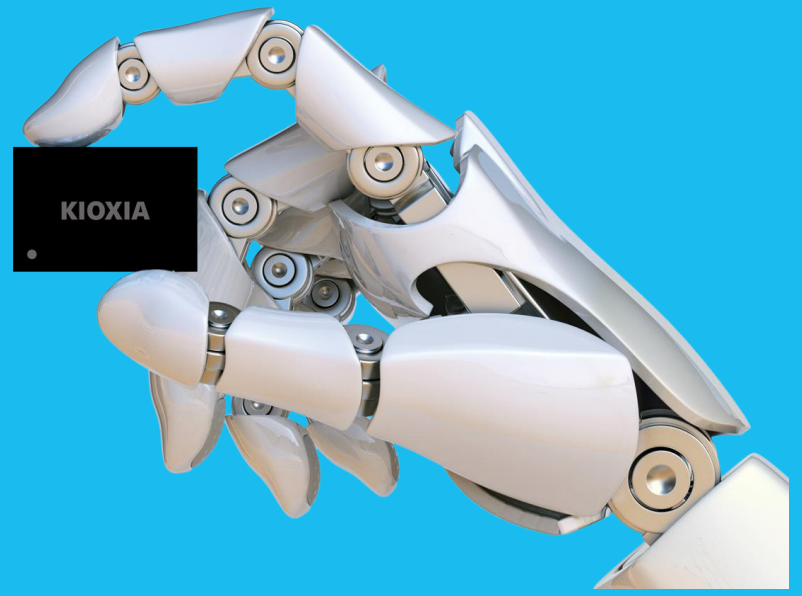
✓ Required data randomization for 24nm 32Gbit die based products.

* VccQ and Vcc may be distinct and unique voltages on Toggle I/F product.
The device shall support one of the following VccQ/Vcc combinations,

Vcc = 3.3V, VccQ = 3.3V
Vcc = 3.3V, VccQ = 1.8V

3.3V VccQ is not supported for the case where transfer rate is greater than 100MHz.

BENAND™
(Built-in ECC NAND)



BENAND™

BENAND (Built-in ECC NAND) is a SLC NAND memory device which has an Internal Hardware ECC Engine.

Using BENAND it is possible for customers to use 24nm SLC NAND flash memory technology even when their platform cannot support higher bit ECC.

- Features of BENAND

  - ✓ Embedded ECC engine
    Provides information of ECC correction, ECC on Host controller is not required

  - ✓ 24nm SLC NAND process technology

  - ✓ Offers wide line-up of density
    1Gbit, 2Gbit, 4Gbit, and 8Gbit are available in a lineup

  - ✓ Compatibility of SLC NAND
    Interface, basic functions and command sequence follows SLC NAND

BENAND Roadmap

Density	Page/ Block Size	Process	CY2020				CY2021				CY2022				CY2023				CY2024				CY2025			
			1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
1Gbit	2KB/ 128KB	24nm	1Gb x 1Chip																							
2Gbit		24nm	2Gb x 1Chip																							
4Gbit		24nm	2Gb x 2Chips (1$\overline{CE}$)																							
	4KB/ 256KB	24nm	4Gb x 1Chip																							
8Gbit		24nm	4Gb x 2Chips (1$\overline{CE}$)																							

Notice:
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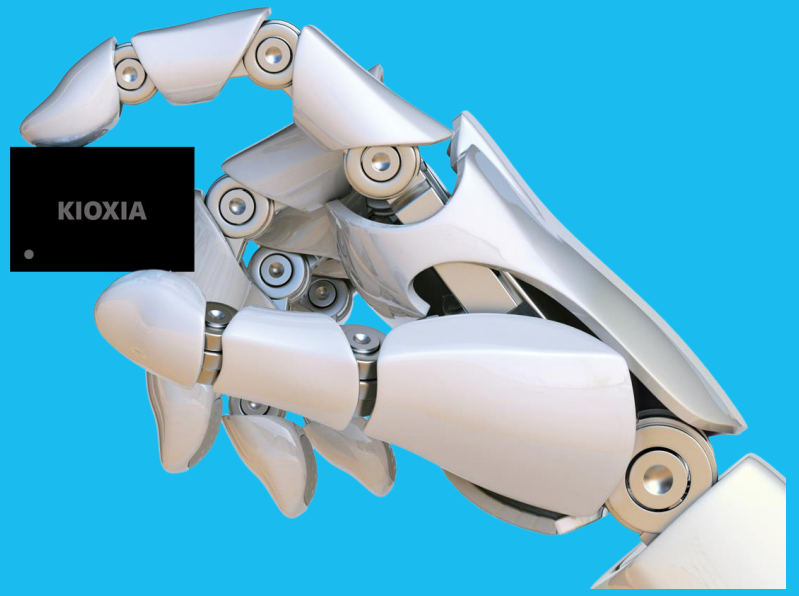
Process 24nm

1/2/4Gbit BENAND Specification

BENAND Die Density		1Gbit		2Gbit		4Gbit	
NAND Design Rule		24nm		24nm		24nm	
ECC Requirement		Not Required		Not Required		Not Required	
Architecture	Power Supply	3.3V	1.8V	3.3V	1.8V	3.3V	1.8V
	Page Size [Bytes]	2048+64		2048+64		4096+128	
	Pages Per Block	64		64		64	
	Block Size [Bytes]	128K+4K		128K+4K		256K+8K	
	Valid Blocks	1004 - 1024		2008 - 2048		2008 - 2048	
	Plane	1		2		2	
Operation	Cache Operation	Not Support		Not Support		Not Support	
	Multi Page/Block Operation	Not Support		Support		Support	
Performance	tWC & tRC (Max Data Rate)	25ns		25ns		25ns	
	tPROG (typ.)	330µs		330µs		340µs	
	tR (typ./max)	40µs / 120µs		40µs / 120µs		55µs / 220µs	
	tBERASE (typ.)	2.5ms	3.5ms	2.5ms	3.5ms	2.5ms	3.5ms
Package (Temp.)	TSOP48 (0 to 70°C / -40 to 85°C)	✓	-	✓	-	✓	-
	FBGA63 (-40 to 85°C)	✓	✓	✓	✓	✓	✓
	FBGA67 (-40 to 85°C)	✓	✓	✓	✓	✓	✓

✓ tR and tPROG of AC timing parameters for BENAND includes the internal ECC operation time.
✓ For more information, please refer to datasheet of respective product.

Serial Interface NAND



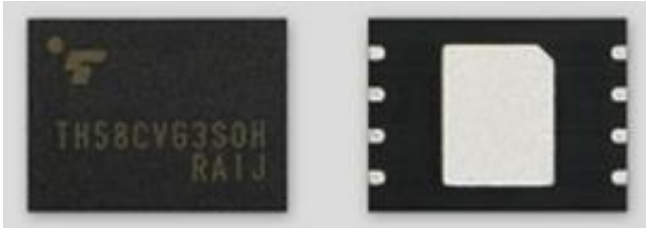
Serial Interface NAND

Serial Interface NAND is a SLC NAND memory device with Serial Peripheral Interface (SPI).
SPI is one of the most common interfaces in SoC today and is offered in small package size.

* The ECC function in Serial Interface NAND can be enabled and disabled by the customers.

➢ Features of Serial Interface NAND

- ✓ Host can control the device by a low pin count
  Supports Mode 0 and Mode 3 of Serial Peripheral Interface (SPI)
- ✓ Embedded ECC engine
  Provides information of ECC correction, ECC on Host controller is not required
- ✓ 24nm SLC NAND process technology
- ✓ Offers wide line-up of density
  1Gbit, 2Gbit, 4Gbit and 8Gb are available in a lineup
- ✓ Available in small package
  6 x 8mm WSON8



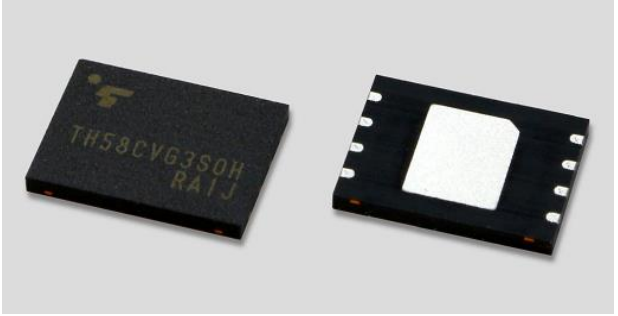
WSON Package

2nd Generation Serial NAND Overview

Uplifting the application with KIOXIA's Serial NAND

■ Lineup

NAND Generation	: 24nm
Density	: 1 / 2 / 4 / 8Gb
Package	: WSON8
Vcc	: 3.3V / 1.8V
Operation Temp.	: -40 to 85 deg.



■ Feature

Max. CLK Frequency	: 133MHz
Interface	: SPI (x1, x2, x4) Mode 0, Mode 3
ECC *	: 8bit ECC for each 528Byte is implemented.

* The ECC function in Serial Interface NAND can be enabled and disabled by the customers.

Serial Interface NAND Roadmap

Density	Page/ Block Size	Process	CY2020				CY2021				CY2022				CY2023				CY2024				CY2025			
			1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q	1Q	2Q	3Q	4Q
1Gbit	2KB/ 128KB	24nm																								
2Gbit		24nm																								
4Gbit	4KB/ 256KB	24nm																								
8Gbit	4KB/ 256KB	24nm	4Gb x 2Chips																							

Notice:
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1st generation

2nd generation

Serial Interface NAND Specification (2nd Generation)

Density			1Gbit		2Gbit		4Gbit		8Gbit	
NAND Design Rule			24nm		24nm		24nm		24nm	
I/F Specification			SPI (x1, x2, x4) Mode 0, Mode 3							
ECC Requirement			8bit ECC for each 528Byte is implemented.							
Architecture	Power Supply		3.3V	1.8V	3.3V	1.8V	3.3V	1.8V	3.3V	1.8V
	Page Size [Bytes]	Internal ECC On	2048+64		2048+64		4096+128		4096+128	
		Internal ECC Off	2048+128		2048+128		4096+256		4096+256	
	Pages Per Block		64		64		64		64	
	Block Size [Bytes]	Internal ECC On	128K+4K		128K+4K		256K+8K		256K+8K	
		Internal ECC Off	128K+8K		128K+8K		256K+16K		256K+16K	
	Valid Blocks		1004 - 1024		2008 - 2048		2008 - 2048		4016 - 4096	
Performance	Data Transfer Rate (max)		133MHz		133MHz		133MHz		133MHz	
	tPROG (typ.)		360µs		360µs		450µs		450µs	
	tR (typ.)		70µs		70µs		115µs		115µs	
	tBERASE (typ.)		2.0ms	2.7ms	2.0ms	2.7ms	2.0ms	2.7ms	2.0ms	2.7ms
Special Function			Block Protection(OTP), ECC Bit Flip Count Report							
Package & Temperature			WSON8 -40 to 85°C							

Notice:
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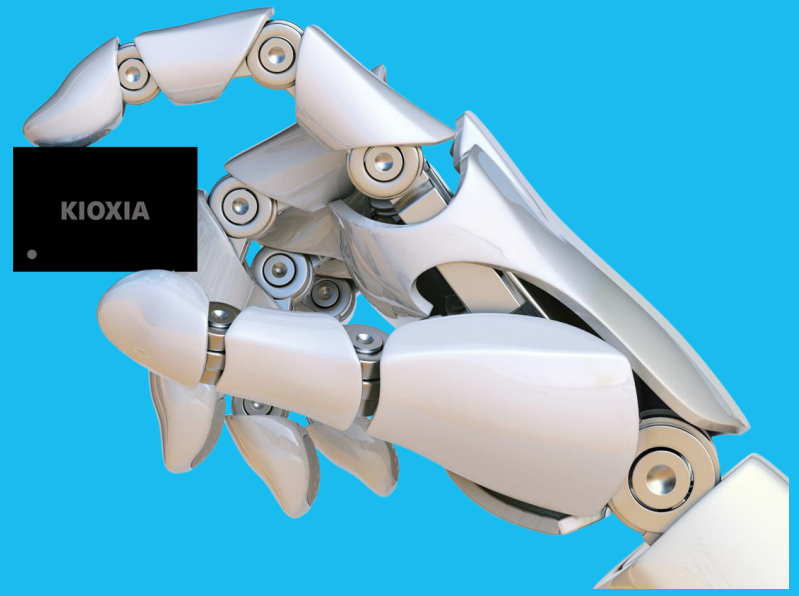
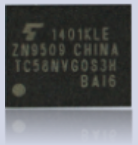
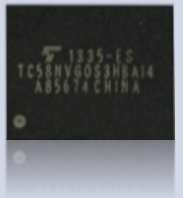
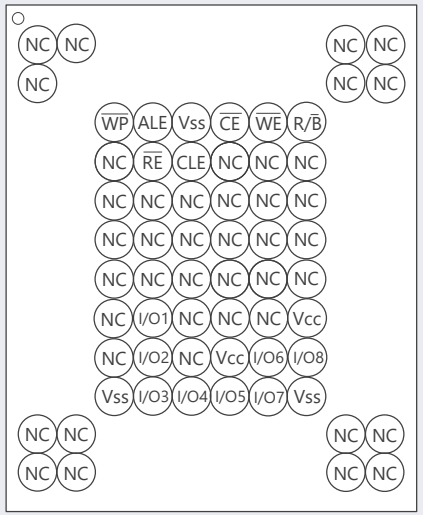
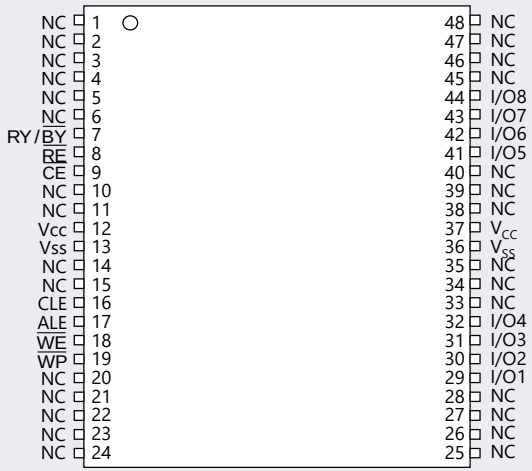
Package Information



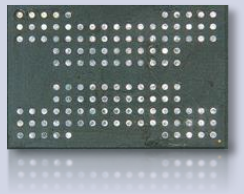
24nm SLC NAND/ BENAND Package

Type	FBGA67		FBGA63		TSOP48	
Size	6.5 x 8mm		9 x 11mm		12 x 20mm	
Vcc	3.3V&1.8V		3.3V&1.8V		3.3V	
Temp.	-40 to 85°C		-40 to 85°C		0 to 70°C / -40 to 85°C	
Pin/Ball	67Balls		63Balls		48Pins	
Pitch	0.8mm		0.8mm		0.5mm	
Pin Assignment (Top View)						

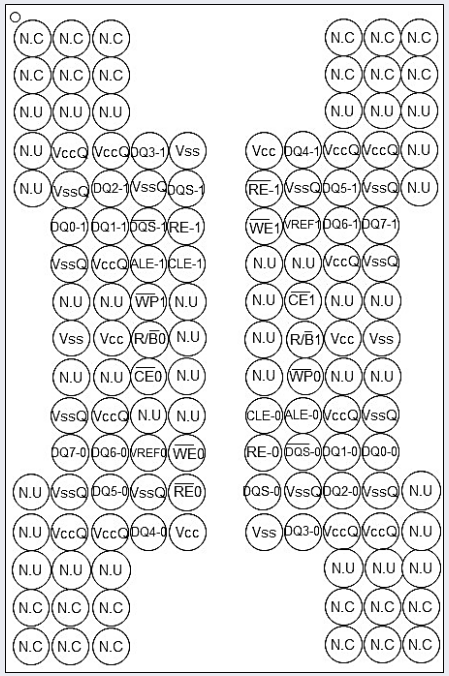
Lineup	SLC NAND	BENAND	SLC NAND	BENAND	SLC NAND	BENAND
1Gbit	✓	✓	✓	✓	✓	✓
2Gbit	✓	✓	✓	✓	✓	✓
4Gbit	✓	✓	✓	✓	✓	✓
8Gbit	✓	✓	✓	✓	✓	✓
16Gbit	-	-	-	-	✓	-
32Gbit	-	-	-	-	✓ (Legacy I/F)	-
64Gbit	-	-	-	-	✓ (Legacy I/F)	-
128Gbit	-	-	-	-	✓ (Legacy I/F)	-

24nm 32Gb die SLC NAND Package (Toggle I/F)

Type	BGA132
Size	12 x 18mm
Vcc	3.3V *
Temp.	0 to 70°C / -40 to 85°C
Ball	132Balls
Pitch	1.0mm



Pin Assignment (Top View)



Lineup	SLC NAND
64Gbit	✓ (Toggle I/F)
128Gbit	✓ (Toggle I/F)
256Gbit	✓ (Toggle I/F)

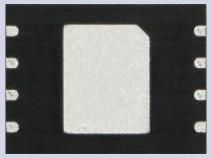
* VccQ and Vcc may be distinct and unique voltages on Toggle I/F product.
The device shall support one of the following VccQ/Vcc combinations,

Vcc = 3.3V, VccQ = 3.3V
Vcc = 3.3V, VccQ = 1.8V

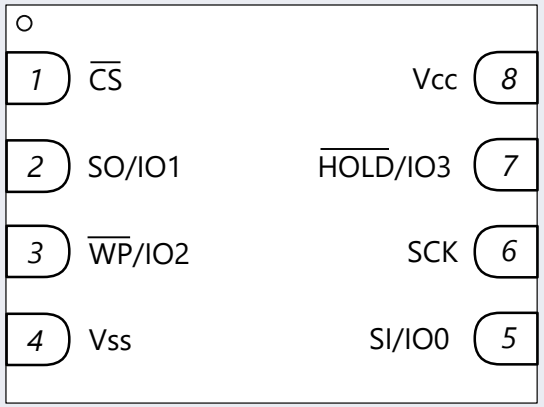
3.3V VccQ is not supported for the case where transfer rate is greater than 100MHz.

24nm Serial Interface NAND Package (2nd Generation)

Type	WSON8
Size	6 x 8mm
Vcc	3.3V&1.8V
Temp.	-40 to 85°C
Pin	8Pins
Pitch	1.27mm



Pin Assignment (Top View)



Lineup	Serial Interface NAND
1Gbit	✓
2Gbit	✓
4Gbit	✓
8Gbit	✓

Our Mission

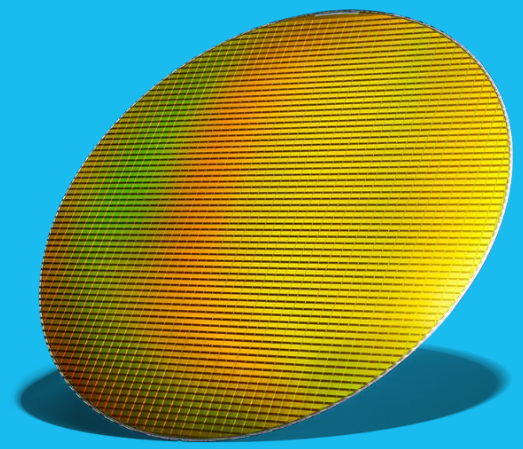
Uplifting the world with “memory”

By evolving “memory,” we create uplifting experiences and change the world.

The name KIOXIA is a combination of the Japanese word *kioku* meaning “memory” and the Greek word *axia* meaning “value” – which forms the foundation of the company’s vision.

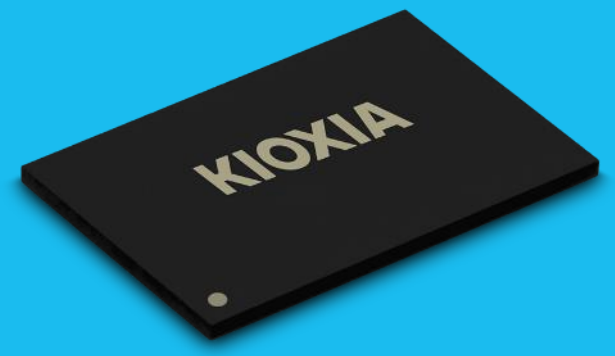
Unleashing the potential of “memory” to create new value.

Application Guide & Comments



KIOXIA

Reliability Guidance



Reliability Guidance

Overview

This reliability guidance is intended to provide some guidance related to using NAND Flash memory. For detailed reliability data on each SLC NAND Flash memory product, please refer to the reliability note of the respective product.

Each NAND Flash memory cell has a floating gate which is isolated by the insulator, i.e. silicon dioxide. In the Write(Program) operation, the electrons are injected into the floating gate and the cell data is changed to '0'(zero). On the other hand, the electrons are ejected from the floating gate by the Erase operation and all of the cell data in this block is changed to '1'(one).

NAND Flash memory cells are gradually worn out and their reliability level is degraded by repeating the Write and Erase operations of '0' data in each block because electrons move in and out of the floating gate at each '0' data Write and Erase operation. The reliability of NAND Flash memory cells during the actual usage on system level depends on the usage and environmental conditions. KIOXIA adopts the checker pattern data, 0x55 & 0xAA for alternative Write/Erase cycles, for the reliability test.

Generally, a block should be marked as bad when a program status failure or erase status failure is detected. Although random bit errors may occur during use, it does not necessarily mean that a block is bad.

NAND Flash memory management, including, but not limited to, Bad Block Management, ECC treatment and Wear Leveling, should be recognized and incorporated into system design. ECC treatment for read data is mandatory against random bit errors, and the host should monitor ECC status to take appropriate measures such as rewrite (Data Refresh) in consideration of Wear Leveling before an uncorrectable ECC error occurs. If such ECC treatment is not implemented, read failure due to random bit errors may occur even before program or erase status failure.

To realize a robust system design, it is generally necessary to prevent the concentration of Write/Erase cycles at specific blocks by adopting Wear Leveling, which manages to distribute Write/Erase cycles evenly among NAND Flash memory. It is also necessary to avoid dummy '0' data writes, e.g. '0' data padding, which accelerate block endurance degradation.

For details, please refer to the following pages which explain ideas to realize a robust system design based on NAND Flash memory reliability.

Reliability Parameter

Write/Erase Endurance

The cumulative bad block count will increase along with the number of Write/Erase cycles.
Since NAND Flash memory has a limitation regarding Write/Erase Endurance, Write or Erase failure may occur in a cell, page, or block.
These failures are detected by doing a status read after either an Auto Page Program or Auto Block Erase operation.
To prevent a failure caused by the excessive number of Write/Erase cycles on a specific block, implementation of Wear Leveling by the host side is necessary to average the number of Write/Erase cycles to each block.

Data Retention

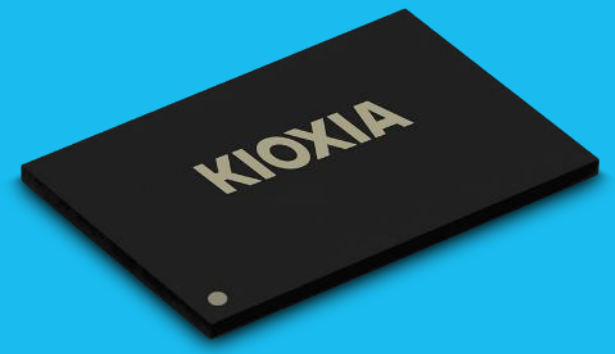
The data in NAND Flash memory may change after a certain amount of storage time. This is due to charge loss or charge gain.
After block erasure and reprogramming, the block may become usable again.
Data Retention time is generally influenced by the number of Write/Erase cycles and temperature.
To prevent read failure due to Data Retention, ECC treatment for read data is mandatory against random bit errors, and the host should monitor ECC status to take appropriate measures before an uncorrectable error occurs.

Read Disturb

A Read operation may disturb the data in NAND Flash memory. The data may change due to charge gain.
Usually, bit errors occur on other pages in the block, not the page being read. After a large number of read cycles (between block erases), a tiny charge may build up and can cause a cell to be soft programmed to another state.
After block erasure and reprogramming, the block may become usable again.
Read Disturb capability is generally influenced by the number of Write/Erase cycles.
A large number of read cycles (between block erases) requires careful attention.
To prevent read failure due to Read Disturb, ECC treatment for read data is mandatory against random bit errors, and the host should monitor ECC status to take appropriate measures before an uncorrectable error occurs.

*For the detailed reliability data for each SLC NAND product, please refer to reliability note of respective product.

SLC NAND Flash memory Management



NAND Flash memory Management 1

NAND Flash memory realizes Gigabit class memory via advanced processing technology. When using the device, please understand that the reliability characteristics and NAND Flash memory management, including, but not limited to, Bad Block Management, ECC treatment and Wear Leveling, should be recognized and incorporated into the system design.

Bad Block Management

There are two types of Bad Block.

(a) Initial Bad Block

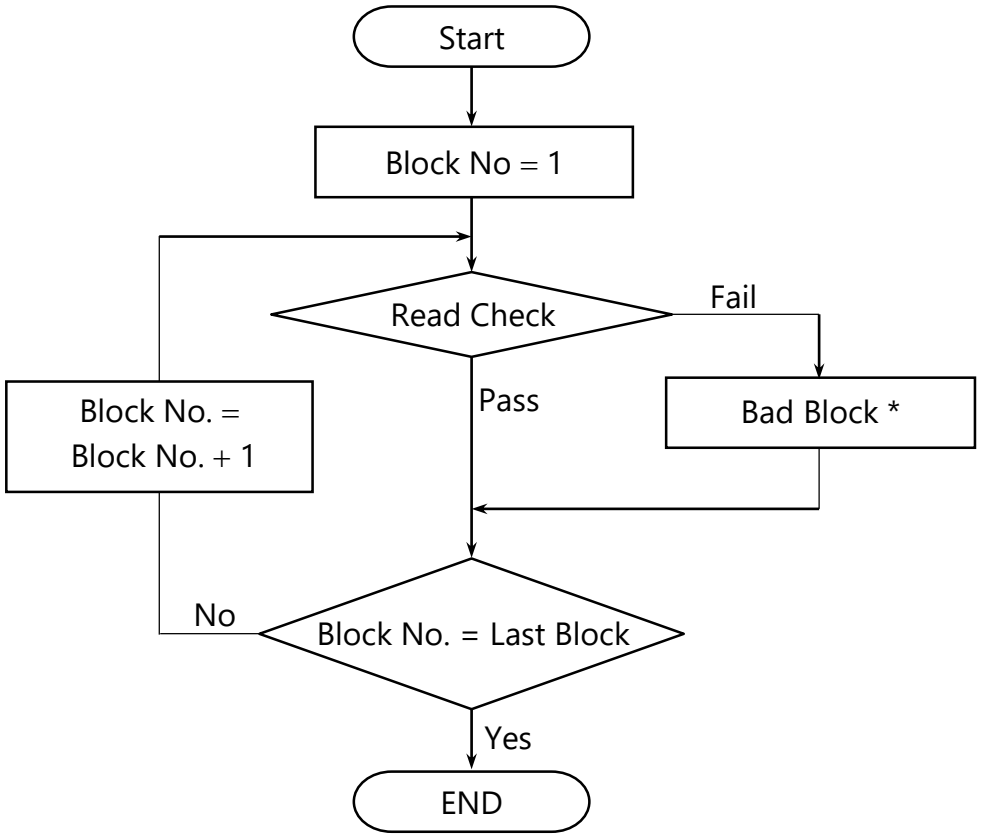
NAND Flash memory may contain unusable blocks at the time of brand-new state. These blocks are called Initial Bad Blocks.
It is necessary to confirm if the product contains initial bad blocks at the point of first use, and DO NOT use those bad block.

< Example Test Flow for 24nm SLC NAND products >

Data in all pages are marked as '0' for the initial bad block. The user is able to detect the initial bad block with the Read Check operation to any column in a page for each block. If the data is 00h, this block should be marked as the bad block.

* DO NOT execute the Erase operation to the detected bad blocks.

* For Bad Block Test Flow of BENAND and Serial NAND devices during Read Check, regardless of the result of Status Read (ECC Pass or Fail), use the read data value to judge if it is a Bad Block.



Test Flow for Initial Bad Block Detection

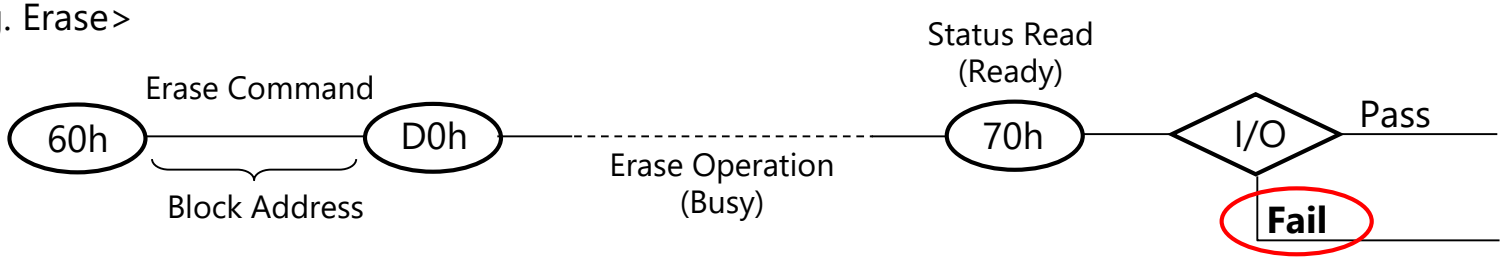
NAND Flash memory Management 2

(b) Acquired Bad Block

NAND Flash memory cells are gradually degraded by repeating the Write and Erase operations, and acquired bad blocks may occur during the Program or Erase operations. Acquired bad blocks are detected by doing a status read after either the Auto Page Program or Auto Block Erase operation. DO NOT use detected acquired bad blocks.

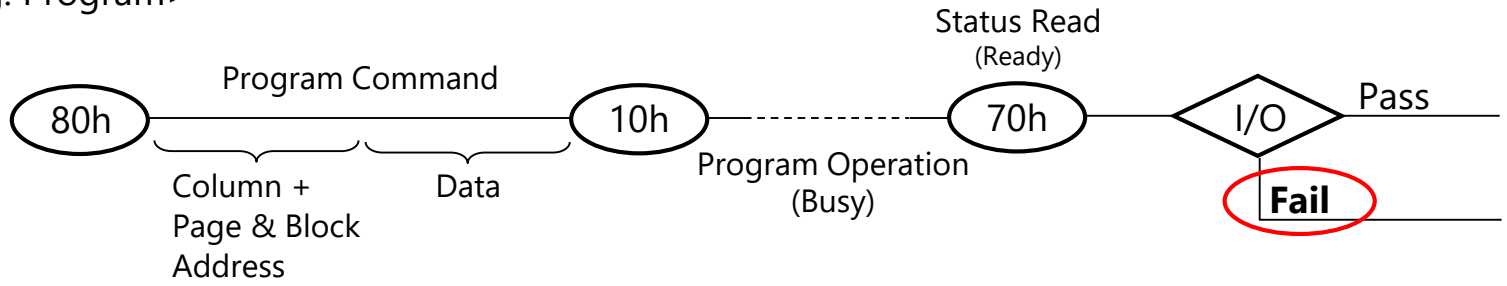
Operation	Failure Mode		How to detect and handle
Erase	Block	Erase Fail	Detect "Fail" at Status Read after Erase Operation → Replace to another Block
Program	Page	Program Fail	Detect "Fail" at Status Read after Program Operation → Replace to another Block

<e.g. Erase>



When "Fail" is detected at Status Read, mark block as a bad block.

<e.g. Program>



When "Fail" is detected at Status Read, mark block as a bad block.

*Please check datasheets for details such as Block replacement.

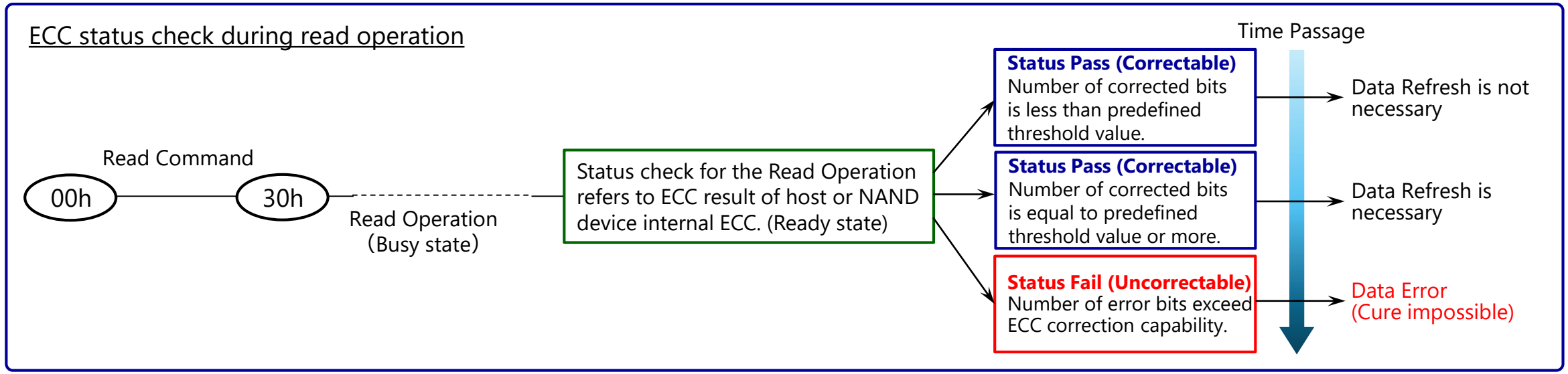
NAND Flash memory Management 3

ECC (Error Correction Code)

ECC treatment for read data is mandatory against random bit errors, and the host should monitor ECC status to take appropriate measures such as rewrite in consideration of Wear Leveling before an uncorrectable error occurs.
24nm 1Gbit/2Gbit/4Gbit/8Gb/16Gb SLC NAND requires 8bit/512Byte ECC to be managed by the host controller.
BENAND and Serial Interface NAND have an embedded hardware ECC engine. Using BENAND or Serial Interface NAND, it is possible for customers to use the latest 24nm SLC NAND flash memory technology even when their platform cannot support higher bit ECC.

Read status check during read operation

In addition to after the Program and Erase operations, it is necessary to perform a status check during the Read operation.
The status check for the Read operation is important to detect random bit errors due to data retention, read disturb, etc. and judge if the Data Refresh (Rewrite) operation is necessary.

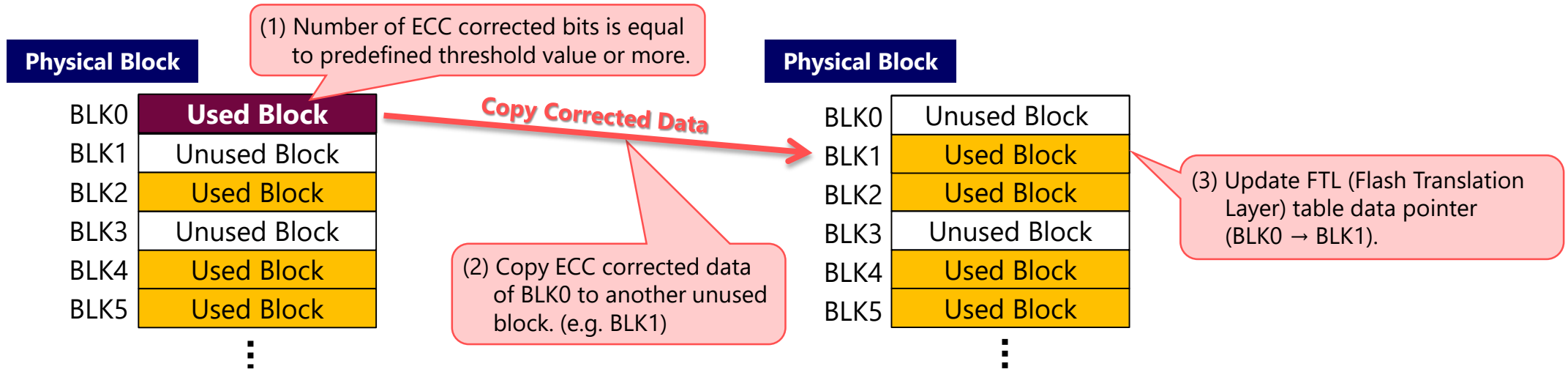


NAND Flash memory Management 4

Data Refresh (Rewrite) Operation

Data in NAND Flash memory may be changed due to Data Retention, Read Disturb, etc. Host should monitor ECC status to take appropriate measures such as Data Refresh by copying the corrected data to another unused block. The Data Refresh operation results in a higher reliability system against data error. Since Data Refresh conducts a Write/Erase operation, it is necessary to consider Wear Leveling.

Example of Data Refresh Operation



Note : BENAND & Serial Interface NAND products have built in ECC functions and have command support for checking the internal ECC status.

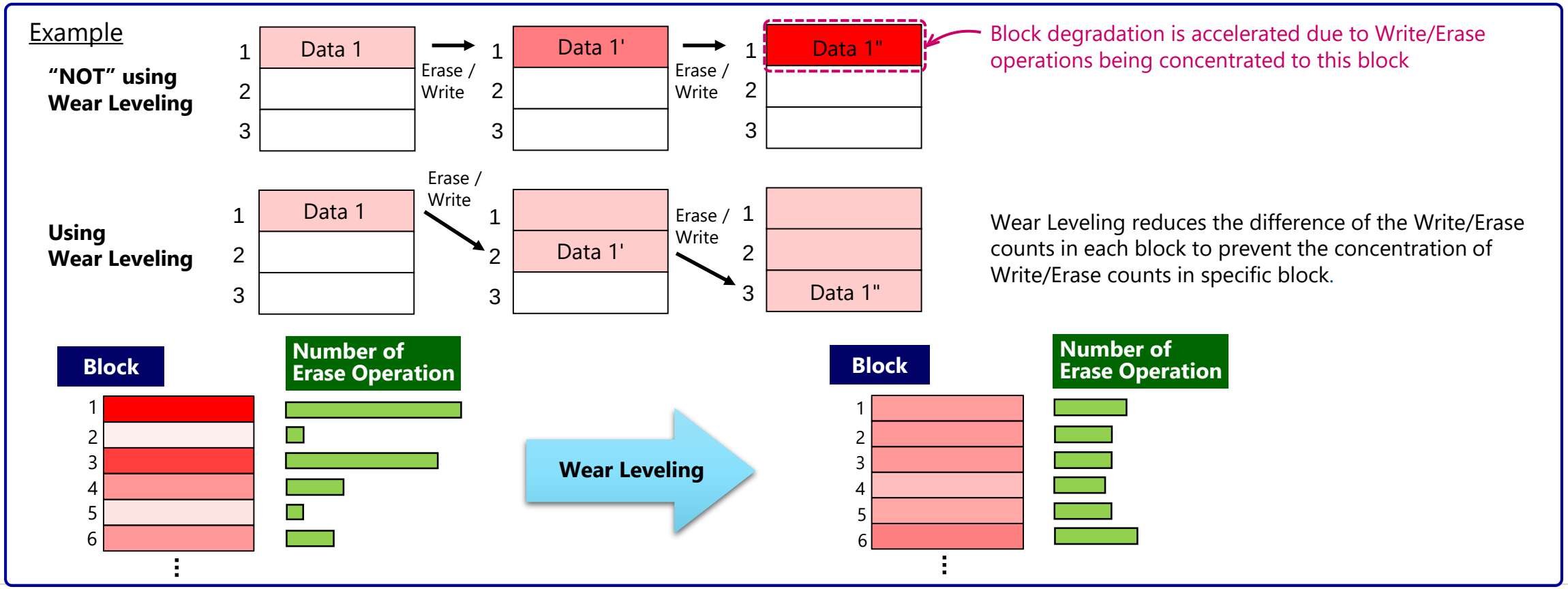
- ✓ BENAND supports the Status Read (70h) and ECC Status Read (7Ah) commands.
- ✓ Serial NAND supports ECC Bit Flip Count Detection, ECC Bit Flip Count Report and ECC Maximum Bit Flip Count Report.

For detail information, please refer to the respective product's datasheet.

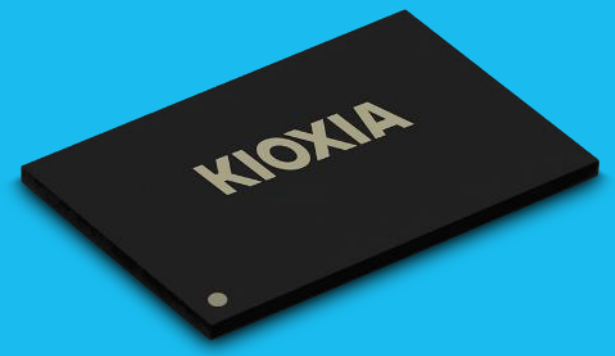
NAND Flash memory Management 5

Averaging of Write/Erase Cycles Across Blocks (Wear Leveling)

The number of Write/Erase operations in NAND Flash memory is limited. If Write/Erase operations are concentrated to specific blocks, it will accelerate the cell degradation at these blocks. Therefore, in usages with cycles of high amounts of Write/Erase operations, the measures should be implemented to ensure that Write/Erase operations are delivered evenly to each block among NAND Flash memory.
In general, manage Write/Erase counts and then apply an averaging procedure such as Wear Leveling to prevent the concentration of Write/Erase operations to specific blocks. Wear Leveling should be managed at host side.



Technical Considerations for SLC NAND Flash Memory Usage



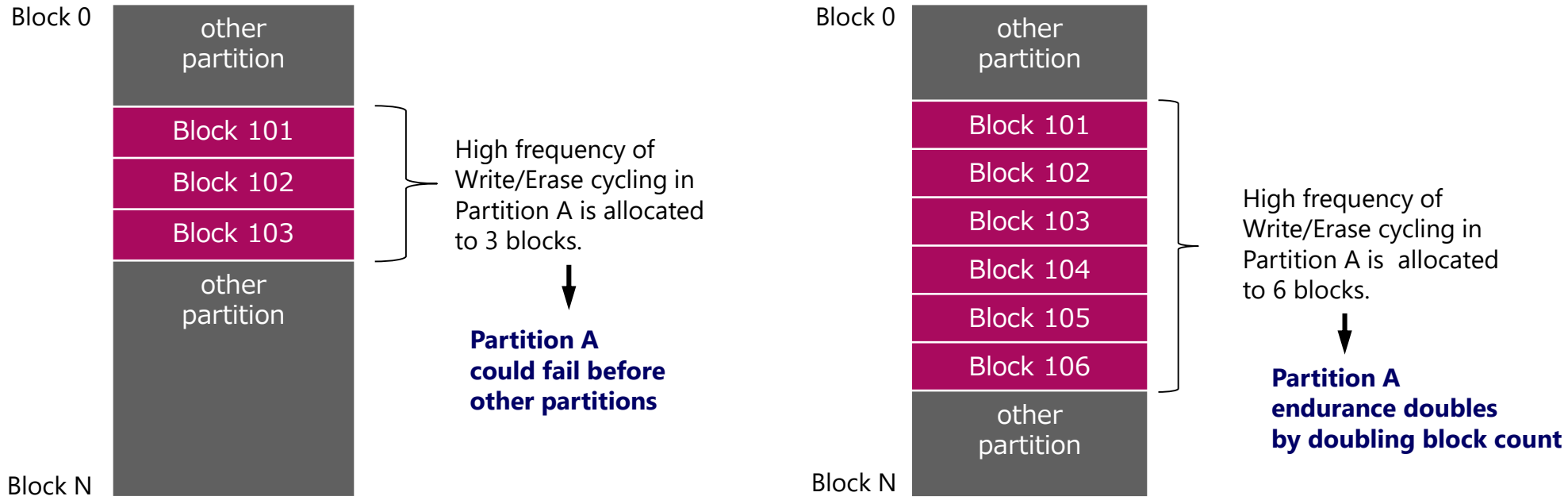
NAND Flash memory usage consideration 1

Partition size considerations for high Write/Erase cycling partitions

An appropriate Wear Leveling algorithm should be used to avoid concentrated access to specific blocks. For partitions with high frequency Write/Erase cycling, it is necessary to allocate an adequate partition size with a sufficient number of blocks for Wear Leveling.

Insufficient partition size settings for high Write/Erase cycling partition can accelerate NAND cell degradation and cause such a partition to fail earlier than the other partitions.

Example of partition size consideration



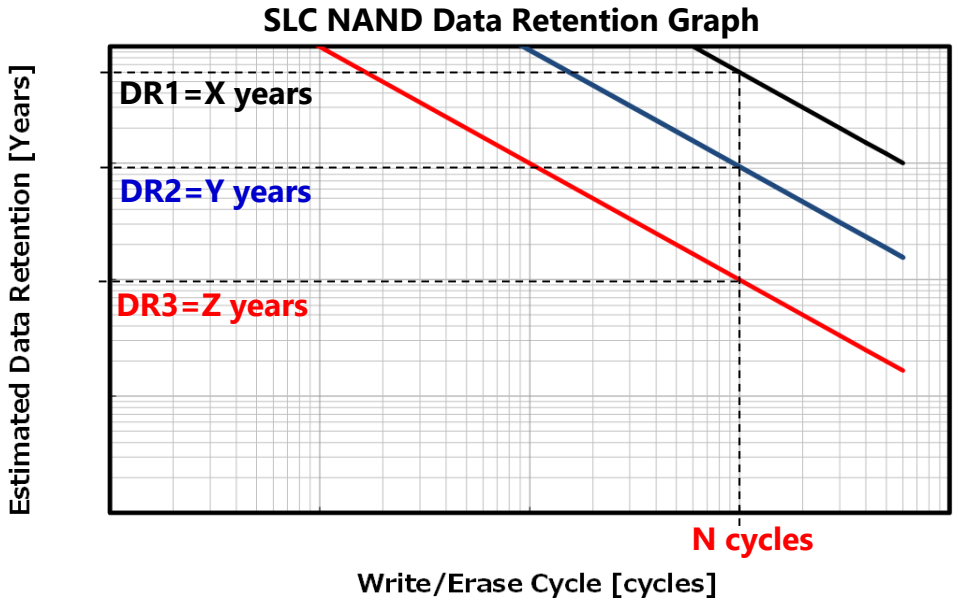
With the same Wear Leveling, doubling the block count of a partition can double the Write/Erase endurance of the partition.

NAND Flash memory usage consideration 2

Temperature dependence of Data Retention

The data in NAND Flash memory may change after a certain amount of storage time. The Data Retention time is influenced by Write/Erase cycles and temperature. At higher temperatures, the Data Retention capability of NAND Flash memory degrades.

Example of Data Retention temperature dependency



- Data Retention@ Room Temp.
- Data Retention@ High Temp1.
- Data Retention@ High Temp2.
  (High Temp2 > High Temp1)

For specific Write/Erase cycles = N cycles and different temperatures, Data Retention time varies as X > Y > Z years.

* If the operating environment includes higher temperatures, the effect of higher temperatures on data retention of NAND Flash memory should be recognized and appropriate design measures, such as data refresh, should be implemented to meet the target system reliability and improve overall reliability.
* If necessary, please request the Data Retention graph for higher temperatures to KIOXIA.

NAND Flash memory usage consideration 3

NAND Flash memory cell data consideration for NAND cell reliability

A NAND Flash memory cell has a value of '1' when erased and a value of '0' when programmed.
In general, programming a '0' bit to a NAND cell causes greater stress to the NAND cell than programming a '1' bit.
When programming a '0' bit, the electrons are injected into the floating gate and the cell data is changed to '0'(zero).
On the other hand, if in an Erase operation the electrons are ejected from the floating gate, then all of the cell data in this block will be '1'(one).
Therefore it is necessary to avoid dummy '0' data write, e.g. '0' data padding.
If there is a high percentage of fixed '0' bits in the data pattern along with continuous Write and Erase cycling, it can lead to faster block endurance degradation.

Example: NAND cell array with '0' data padding

1 : "1" data cell 0 : "0" data cell

0	1	0	0	1	0	0	0	0	0	0	0
0	1	0	1	1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0	0	0	0
1	1	0	0	1	0	0	0	0	0	0	0
0	0	1	1	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0
0	1	0	1	0	0	0	0	0	0	0	0
1	0	1	0	1	0	0	0	0	0	0	0

User data area Remaining area

(a) Accelerate block endurance degradation by fixed dummy "0" data write

0	1	0	0	1	1	1	1	1	1	1	1
0	1	0	1	1	1	1	1	1	1	1	1
1	0	1	0	0	1	1	1	1	1	1	1
1	1	0	0	1	1	1	1	1	1	1	1
0	0	1	1	0	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1
0	1	0	1	0	1	1	1	1	1	1	1
1	0	1	0	1	1	1	1	1	1	1	1

User data area Remaining area

(b) "1" data for Remaining area (Recommended)

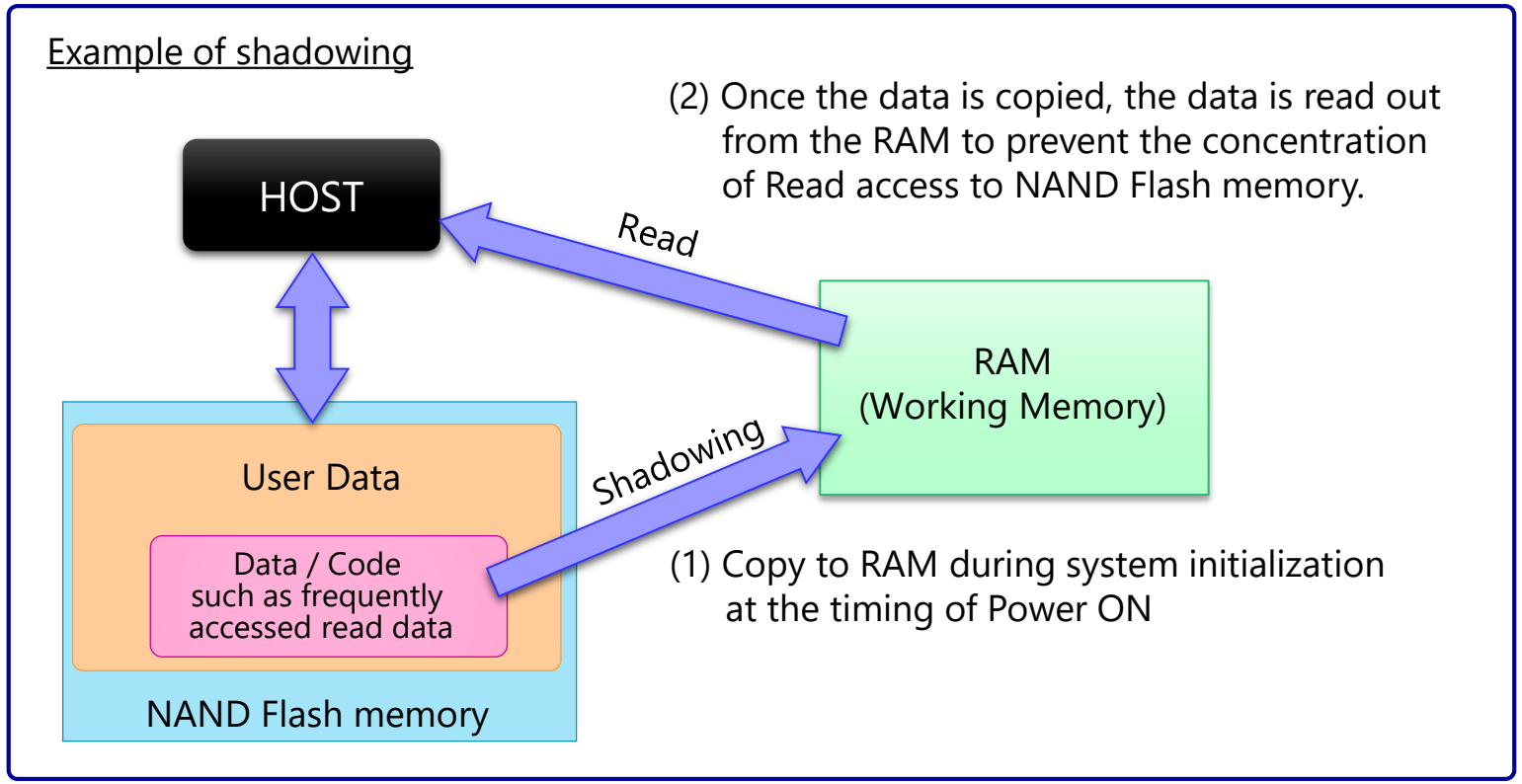
NAND Flash memory usage consideration 4

Shadowing technique to improve performance and reduce Read Disturb stress

When the frequency of read cycles (between block erases) is estimated to be high, apply procedures such as block erasure and reprogramming (refer to Data Refresh (Rewrite) Operation) or data copy into RAM (e.g. DRAM, SRAM) to prevent the concentration of Read access to NAND Flash memory.
Shadowing is the process in which data stored in NAND Flash memory (e.g. program / image code such as frequently accessed read data) is copied to RAM during system initialization. Once the data is copied, the data is read out from the RAM to prevent the concentration of Read access to NAND Flash memory.

Expected Benefits of Shadowing

- ✓ Since Read access speed from RAM is generally faster than that of NAND Flash memory, it can be expected to improve system performance.
- ✓ By copying the data to RAM during system initialization and reading the data from RAM during system operation, it is possible to reduce the Read access to NAND Flash memory. As a result, improvement of reliability against data errors such as Read Disturb can be expected.



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KIOXIA

UFS & e-MMC Roadmap

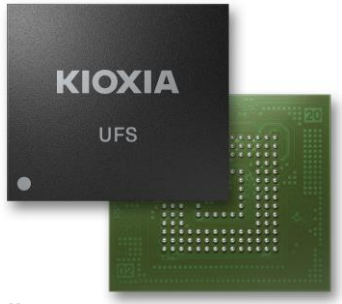
Aug. 2021

Memory Application Engineering Dept. 1
Memory Division
KIOXIA Corporation

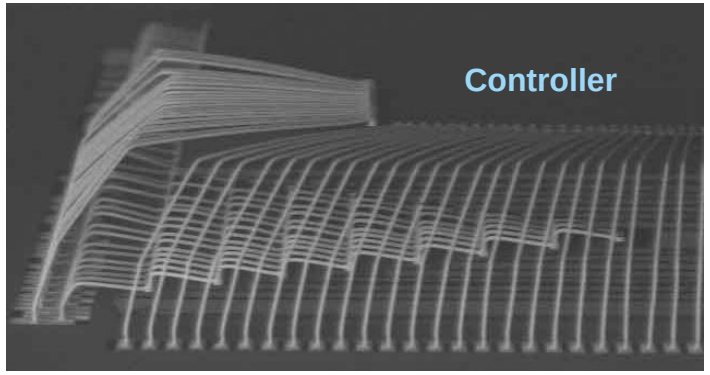
KIOXIA

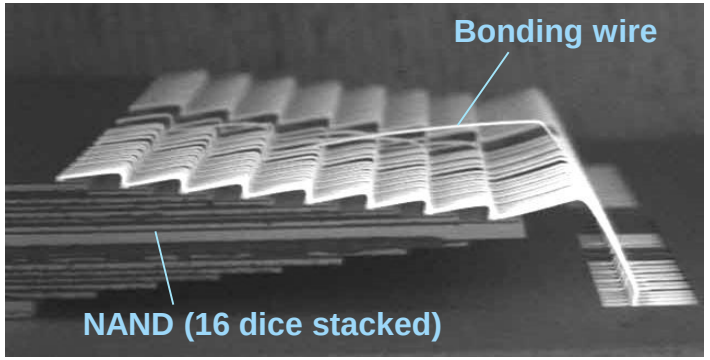
UFS & e-MMC Overview

UFS & e-MMC Introduction



e.g. 153ball BGA, 11.5x13mm, 0.5mm ball pitch



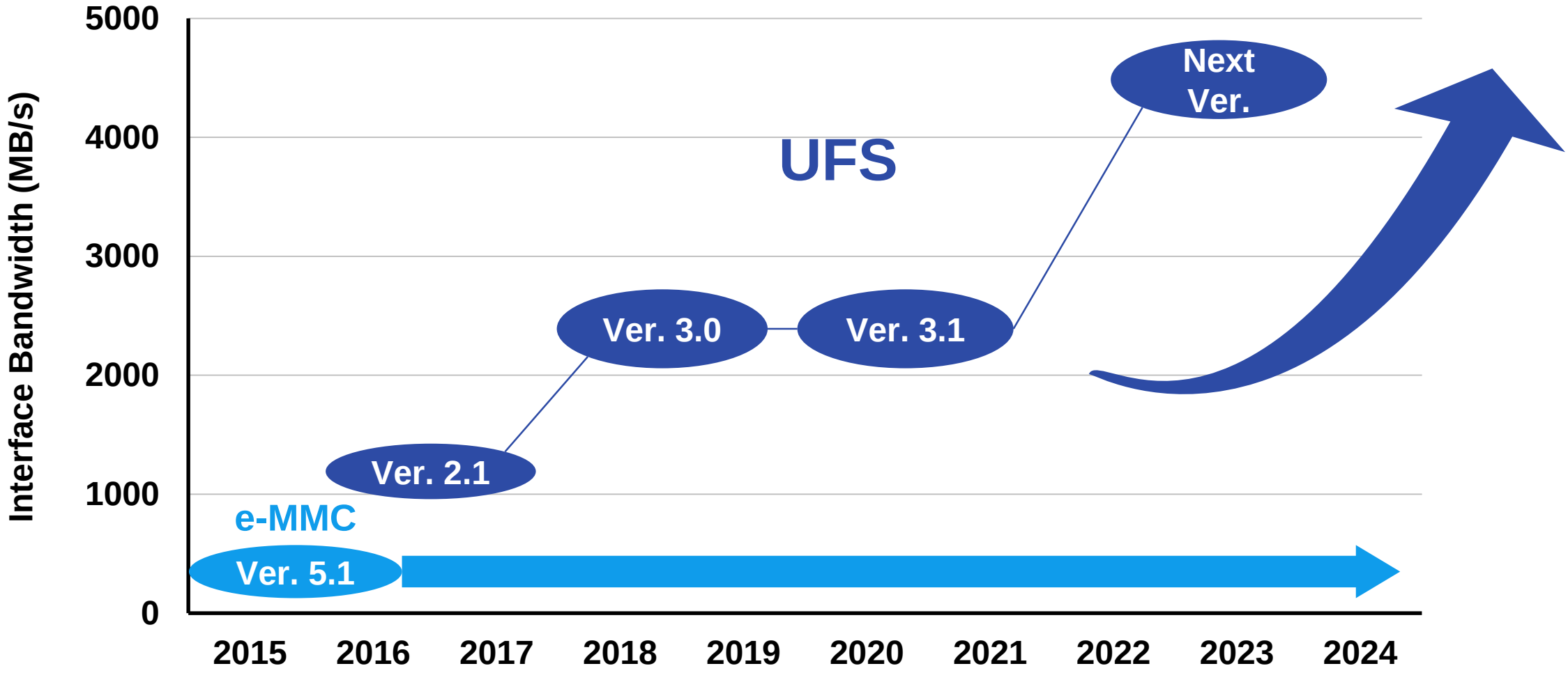


- Single-package with combined controller and flash memory dice
- Both UFS and e-MMC are standardized on JEDEC

		UFS	e-MMC
Year		2014 -	2007 -
I/F	Bus	Serial Interface Send Host → UFS Receive Full Duplex	Parallel (x8) Interface Host — e-MMC Send OR Receive Half Duplex
	Speed	Max. 1160MB/s (HS-G3(5.8Gbps) x 2lanes with v2.0/2.1) Max. 2320MB/s (HS-G4(11.6Gbps) x 2lanes with v3.0/3.1)	Max. 400MB/s (HS400 with Ver.5.0/5.1)
	Pin Count	1 lane : 6 (4 I/O and 2 control) 2 lane : 10 (8 I/O and 2 control)	11 (8 I/O and 3 control)
	Signal Amp.	200mVp-p	1.8V or 1.2V
Command Set		SCSI	MMC

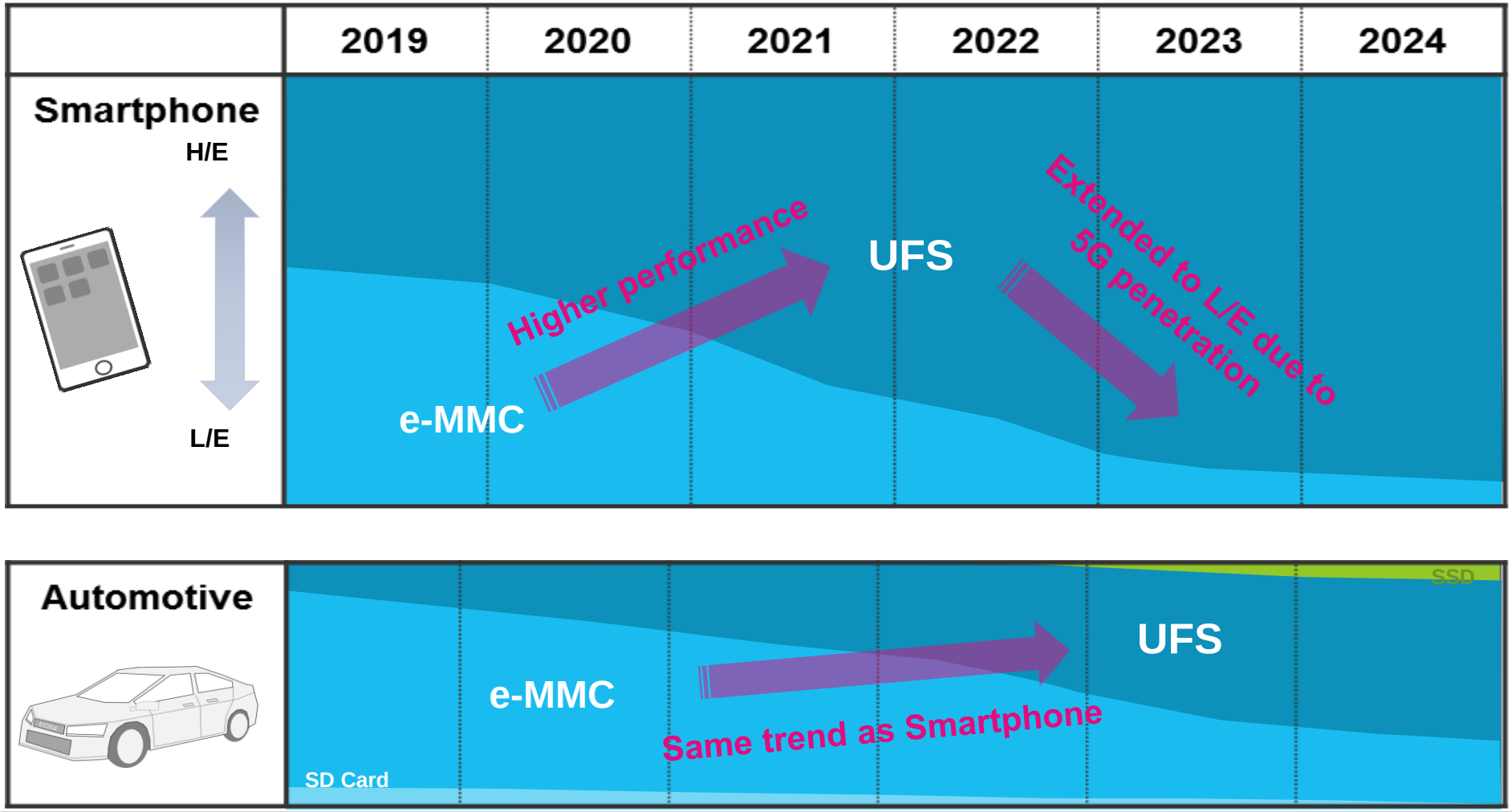
UFS & e-MMC Interface Bandwidth

UFS has a great scalability



Flash Storage Interface Trend

UFS interface is widely spreading over smartphone and automotive applications



UFS & e-MMC Technology Roadmap

UFS : Evolve larger density and higher performance
e-MMC : continuing ver5.1 support

		2019	2020	2021	2022	2023	2024
JEDEC Standard	UFS	2.1 3.0	3.1		Next	Note: The release schedule of next version has not been fixed yet.	
	e-MMC	5.1					
KIOXIA Roadmap	UFS	Ver. 2.1 32GB~256GB	Ver. 3.0 128GB~512GB	Ver. 3.1 128GB~1TB	Next Version	Consumer Grade : Tc = -25 to +85 °C	
	e-MMC	Ver. 5.1 4GB~128GB : Consumer Grade : Tc = -25 to +85 °C 8GB~256GB : Industrial Grade : Ta = -40 to +105 °C(Tc = +115 °C Max)					

Note: 4GB e-MMC is compliant with JEDEC Ver.5.0.
This roadmap does not specify EOL of each generation. EOL should be discussed and decided in good faith between the customer and KIOXIA

Managed FLASH evolution

UFS Lineup * Please contact your local sales to make sure of the availability of UFS2.1/3.0 products

Grade	UFS Ver.	Generation	Density	Part Number	qTotalRawDevice Capacity	Boot LU (Max.)	RPMB LU	PKG (mm)
Consumer (Tc = -25 to +85 °C)	2.1*	Gen6	32GB	THGAF8G8T23BAIL	32,015,122,432 Byte	64MB	16MB*2	11.5x13x0.8
			64GB	THGAF8G9T43BAIR	64,005,079,040 Byte	128MB		11.5x13x1.0
			128GB	THGAF8T0T43BAIR	127,984,992,256 Byte			
			256GB	THGAF8T1T83BAIR	255,944,818,688 Byte			
	3.0*	Gen8	128GB	THGJFCT0T44BAIL	127,984,992,256 Byte	- *1		11.5x13x0.8
			256GB	THGJFCT1T84BAIC	255,944,818,688 Byte			11.5x13x0.95
			512GB	THGJFCT2T84BAIC	511,864,471,552 Byte			
	3.1	Gen9/*Gen9.5*	128GB	THGJFAT0T44BAIL ***THGJFHT0T44BAIL***	127,984,992,256 Byte			11.5x13x0.8
			256GB	THGJFAT1T84BAIR	255,944,818,688 Byte			11.5x13x1.0
			512GB	THGJFAT2T84BAIR	511,864,471,552 Byte			11.5x13x1.0
			1TB	*THGJFHT3TB4BAIF*	1023,703,777,280 Byte			11.5x13x1.1
		Gen10	256GB	THGJFGT1E45BAIL	TBD			11.5x13x0.8
				THGJFGT1E45BAIP				11x13x0.8
			512GB	THGJFGT2T85BAIR	TBD			11.5x13x1.0
				THGJFGT2T85BAIU				11x13x1.0

*1 Size of Boot LU can be configured during system configuration by setting dNumAllocUnits, and its max. value is defined by dEnhanced1MaxNAllocU.
*2 User can partition by four region

e-MMC Lineup

Grade	Density	Operating Temperature	Part Number	Package (mm)
Consumer 15nm	4GB	-25 to +85 °C	THGBMNG5D1LBAIT	10x11x0.8
			THGBMNG5D1LBAIL	11.5x13x0.8
	8GB		THGBMJG6C1LBAIL	
	16GB		THGBMJG7C1LBAIL	
	32GB		THGBMJG8C2LBAIL	
Consumer BiCS3	16GB		THGAMRG7T13BAIL	11.5x13x0.8
	32GB		THGAMRG8T13BAIL	
	64GB		THGAMRG9T23BAIL	
	128GB		THGAMRT0T43BAIR	11.5x13x1.0
Industrial 15nm	8GB	-40 to +105 °C	THGBMJG6C1LBAU7	11.5x13x1.0
	16GB		THGBMJG7C2LBAU8	11.5x13x1.2
	32GB		THGBMJG8C4LBAU8	
	64GB		THGBMJG9C8LBAU8	

UFS & e-MMC Lineup

M1PCZ00-283
June., 2021

	Product	UFS			e-MMC		e-MMC (Industrial)
	Operating Temp.	-25C to 85C			-25C to 85C		-40C to 105C
	Vcc / Vccq	Vcc 3.3V / Vccq2 1.8V	Vcc 3.3 or 2.5V / Vccq 1.2V		Vcc 3.3V / Vccq 3.3or1.8V	Vcc 3.3V / Vccq 1.8V	Vcc 3.3V / Vccq 3.3 or 1.8V
	Status	MP	MP	CS	MP	MP	MP
Density	4GB				e-MMC 5.0 10x11/ 11.5x13x0.8		
	8GB				e-MMC 5.1 11.5x13x0.8		e-MMC 5.1 11.5x13x1.0
	16GB				e-MMC 5.1 11.5x13x0.8	e-MMC 5.1 11.5x13x0.8	e-MMC 5.1 11.5x13x1.2
	32GB	UFS 2.1 11.5x13x0.8			e-MMC 5.1 11.5x13x0.8	e-MMC 5.1 11.5x13x0.8	e-MMC 5.1 11.5x13x1.2
	64GB	UFS 2.1 11.5x13x1.0				e-MMC 5.1 11.5x13x0.8	e-MMC 5.1 11.5x13x1.2
	128GB	UFS 2.1 11.5x13x1.0	UFS 3.0 11.5x13x0.8	UFS 3.1 11.5x13x0.8		e-MMC 5.1 11.5x13x1.0	
	256GB	UFS 2.1 11.5x13x1.0	UFS 3.0 11.5x13x0.95	UFS 3.1 11.5x13x1.0		*BiCS FLASH*™	
	512GB		UFS 3.0 11.5x13x0.95	UFS 3.1 11.5x13x1.0			
	1TB			UFS 3.1 11.5x13x1.1			

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