AXP323 PMIC For Multi-Core High-Performance System

1 Features

- 3 DCDCs

  DCDC1: 0.5~1.2V, 10mV/step,
  1.22~1.54V, 20mV/step,
  1.6~3.4V, 0. 1V/step,
  IMAX=3A@VIN=5V

  DCDC2: 0.5~1.2V, 10mV/step,
  1.22~1.54V, 20mV/step,
  IMAX=3A@VIN=5V

  DCDC3: 0.5~1.2V, 10mV/step,
  1.22~1.84V, 20mV/step,
  IMAX=3A@VIN=5V

  Efficiency: 82%@5V-0.9V-1A

  DCDC1/2/3: COT Buck Converter

  DCDC1/2 support dual phase, IMAX=5A

- 3 LDOs

  RTCLDO:1.8/2.5/2.8/3.3V,IMAX=30mA

  ALDO1: 0.5~3.5V, 0.1V/step, IMAX=300mA, Ipeak>600mA

  DLDO1: 0.5~3.5V, 0.1V/step, IMAX=500mA, Ipeak>900mA

- Support TWSI(Two Wire Serial Interface), slave address is 0x36 or 0x37(7 bits) by customization
- Internal temperature sensor and over temperature protection
- DCDC over/under voltage protection
- Customization for DCDC/LDO start up sequence and default voltage

2 Applications

- OTT box
- IPC

3 Description

AXP323 is a highly integrated power management IC targeting at applications that require multi-channel power conversion outputs. AXP323 can be used with other BMU together to provides battery management solutions for various portable devices. It can also be used in low-power battery-free solutions such as IPC and smart speakers, fully meeting the requirements of application processor systems for relatively complex and precise power control.

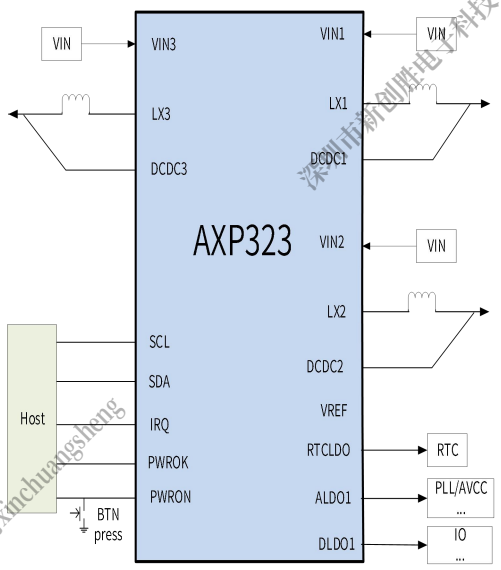
AXP323 supports 6 channel power outputs (including 3 channel DCDCs and 3 channel LDOs). DCDC1 and DCDC2 support dual phase for heavy current application. To ensure the security and stability of the power system, AXP323 integrates protection circuits such as over-voltage protection (OVP), under-voltage protection (UVP), over-current protection (OCP) and over temperature protection (OTP). Moreover, AXP323 features power management functions such as power on/off, sleep and wakeup, which reflects the management value of chip integration.

AXP323 supports TWSI for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

Device Information

Part Number	Package	Body Size
AXP323	QFN-20	3mm * 3mm

Simplified Application Diagram



Revision History

Revision	Date	Author	Description
1.0	Nov. 04, 2022	AWA 1017	Initial version
1.1	May 04, 2023	AWA 1017	1. Update Chapter 8.

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4 Pin Configuration and Functions

Figure 4-1 Pin Map

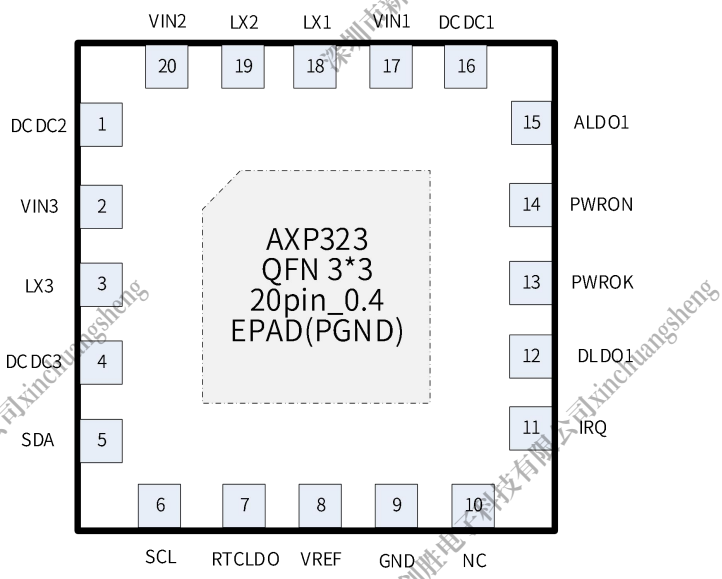


Table 4-1 Pin Description

Pin		I/O(1)	Description
No	Name		
1	DCDC2	I	DCDC2 feedback pin
2	VIN3	PI	DCDC3 input source
3	LX3	PO	Inductor pin for DCDC3
4	DCDC3	I	DCDC3 feedback pin
5	SDA	IO	Data pin for serial interface
6	SCL	IO	Clock pin for serial interface
7	RTCLDO	PO	Can be customized as a always on LDO for powering the RTC module
8	VREF	AIO	Internal reference voltage, external 1uF capacitor
9	GND	GND	GND for internal analog circuit
10	NC	/	Keep floating
11	IRQ	IO	Interrupt Indication / Power On / Wake Up
12	DLDO1	PO	Output pin of DLDO1
13	PWROK	IO	Power good indication output
14	PWRON	I	Power On-Off key input Can be customized as EN pin
15	ALDO1	PO	Output pin of ALDO1
16	DCDC1	I	DCDC1 feedback pin
17	VIN1	PI	DCDC1 input source
18	LX1	PO	Inductor pin for DCDC1
19	LX2	PO	Inductor pin for DCDC2
20	VIN2	PI	DCDC2 input source

(1)**O** for output, **I** for input, **IO** for input/output, **D** for digital, **A** for analog, **P** for power, and **G** for ground.

5 Specifications

5.1 Absolute Maximum Ratings (1)

Table 5-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN1/VIN2/VIN3	Input Voltage	-0.3	7	V
Ta	Operating Temperature Range	-40	85	℃
TJ	Junction Temperature Range	-40	125	℃
Ts	Storage Temperature Range	-40	150	℃
TLEAD	Maximum Soldering Temperature (at leads, 10sec)		300	℃

(1)Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

Table 5-2 ESD Ratings

		VALUE	UNIT
VESD	Human body model(HBM)(1)	±2000	V
	Charged device model(CDM)(2)	±750	V

(1) Reference: ESDA/JEDEC JS-001-2017.
(2) Reference: JEDEC EIA/JESD22-C101F.

5.3 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN	Input voltage	3.0	5.5	V

5.4 Thermal Information

Table 5-4 Thermal Information

Thermal Metric(1)		VALUE	UNIT
θJA	Junction-to-ambient thermal resistance	32.6	℃/W
θJB	Junction-to-board thermal resistance	6.82	
θJC	Junction-to-case(top) thermal resistance	12.32	

(1)Thermal metrics are calculated refer to JEDEC document JESD51. The values are based on simulation.

5.5 Electrical Characteristics

V_{IN} =5V, T_A=25°C

Table 5-5 Electrical Characteristics

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
PMIC Under Voltage						

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OFF}	PMIC Under Voltage Power off			2.6		V
Off Mode Current						
I_{OFF}	OFF Mode Current	V_{IN} =5V		10		μA
TWSI						
VCC	Input Supply Voltage		1.8	3.3		V
ADDRESS	TWSI Slave Address (7 bits)			0x36/ 0x37		
f_{SCK}	Clock Operating Frequency			0.4		MHz
V_{IL}	SCK/SDA Logic Low Voltage				0.3VCC	V
V_{IH}	SCK/SDA Logic Low Voltage		0.7VCC			MHz
DCDC						
f_{OSC}	Oscillator Frequency			1.5		MHz
Efficiency		5V-0.9V-1A		82%		
DCDC1						
V_{IN1}	VIN1 Input Voltage		V_{OFF}		5.5	V
I_{DC1OUT}	Available Output Current	V_{IN1} =5V		3000		mA
V_{DC1OUT}	Output Voltage Range		0.5		3.4	V
V_{DC1_STEP}	Output Voltage Step	V_{DC1OUT}=0.5~1.2V		10		mV/ step
		V_{DC1OUT}=1.22~1.54V		20		
		V_{DC1OUT}=1.6~3.4V		100		
V_{DC1_ACC}	Output Voltage Accuracy	V_{DC1OUT}<=1V, CCM mode		±30		mV
		V_{DC1OUT}>1V, CCM mode		±3%		
V_{DC1_OVP}	Over Voltage Protection			120%* V_{DC1OUT}		V
V_{DC1_UVP}	Under Voltage Protection			85%* V_{DC1OUT}		V
DCDC2						
V_{IN2}	VIN2 Input Voltage		V_{OFF}		5.5	V
I_{DC2OUT}	Available Output Current	V_{IN2} =5V		3000		mA
V_{DC2OUT}	Output Voltage Range		0.5		1.54	V
V_{DC2_STEP}	Output Voltage Step	V_{DC2OUT}=0.5~1.2V		10		mV/ step
		V_{DC2OUT}=1.22~1.54V		20		
V_{DC2_ACC}	Output Voltage Accuracy CCM mode	V_{DC2OUT}<=1V, CCM mode		±30		mV
		V_{DC2OUT}>1V, CCM mode		±3%		
V_{DC2_OVP}	Over Voltage Protection			120%* V_{DC2OUT}		V
V_{DC2_UVP}	Under Voltage Protection			85%* V_{DC2OUT}		V
DCDC3						

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN3}	VIN3 Input Voltage		V_{OFF}		5.5	V
I_{DC3OUT}	Available Output Current	V_{IN3}=5V		3000		mA
V_{DC3OUT}	Output Voltage Range		0.5		1.84	V
V_{DC3_STEP}	Output Voltage Step	V_{DC3OUT}=0.5~1.2V		10		mV/ step
		V_{DC3OUT}=1.22~1.84V		20		mV/ step
V_{DC3_ACC}	Output Voltage Accuracy CCM mode	V_{DC3OUT}<=1V, CCM mode		±30		mV
		V_{DC3OUT}>1V, CCM mode		±3%		
V_{DC3_OVP}	Over Voltage Protection			120%* V_{DC3OUT}		V
V_{DC3_UVP}	Under Voltage Protection			85%* V_{DC3OUT}		V
RTCLDO						
V_{RTCLDO}	Output Voltage	I_{RTC_VCC}=1mA		1.8/ 2.5/ 2.8/ 3.3		V
I_{RTCLDO}	Output Current			30		mA
ALDO1						
V_{ALDO1}	Output Voltage Range	I_{ALDO1}=1mA	0.5		3.5	V
V_{ALDO1_STEP}	Output Voltage Step			100		mV/ step
V_{ALDO1_ACC}	Output Voltage Accuracy	V_{ALDO1}<=1V		±40		mV
		V_{ALDO1}>1V		±3%		
I_{ALDO1}	Output Current			300		mA
DLDO1						
V_{DLDO1}	Output Voltage Range	I_{DLDO1}=1mA	0.5		3.5	V
V_{DLDO1_STEP}	Output Voltage Step			100		mV/ step
V_{DLDO1_ACC}	Output Voltage Accuracy	V_{DLDO1}<=1V		±50		mV
		V_{DLDO1}>1V		±3%		
I_{DLDO1}	Output Current			500		mA

6 Detail Description

6.1 Overview

AXP323 is a highly integrated power management IC targeting at applications that require multi-channel power conversion outputs. AXP323 can be used with other BMU together to provides battery management solutions for various portable devices. It can also be used in low-power battery-free solutions such as IPC and smart speakers, fully meeting the requirements of application processor systems for relatively complex and precise power control.

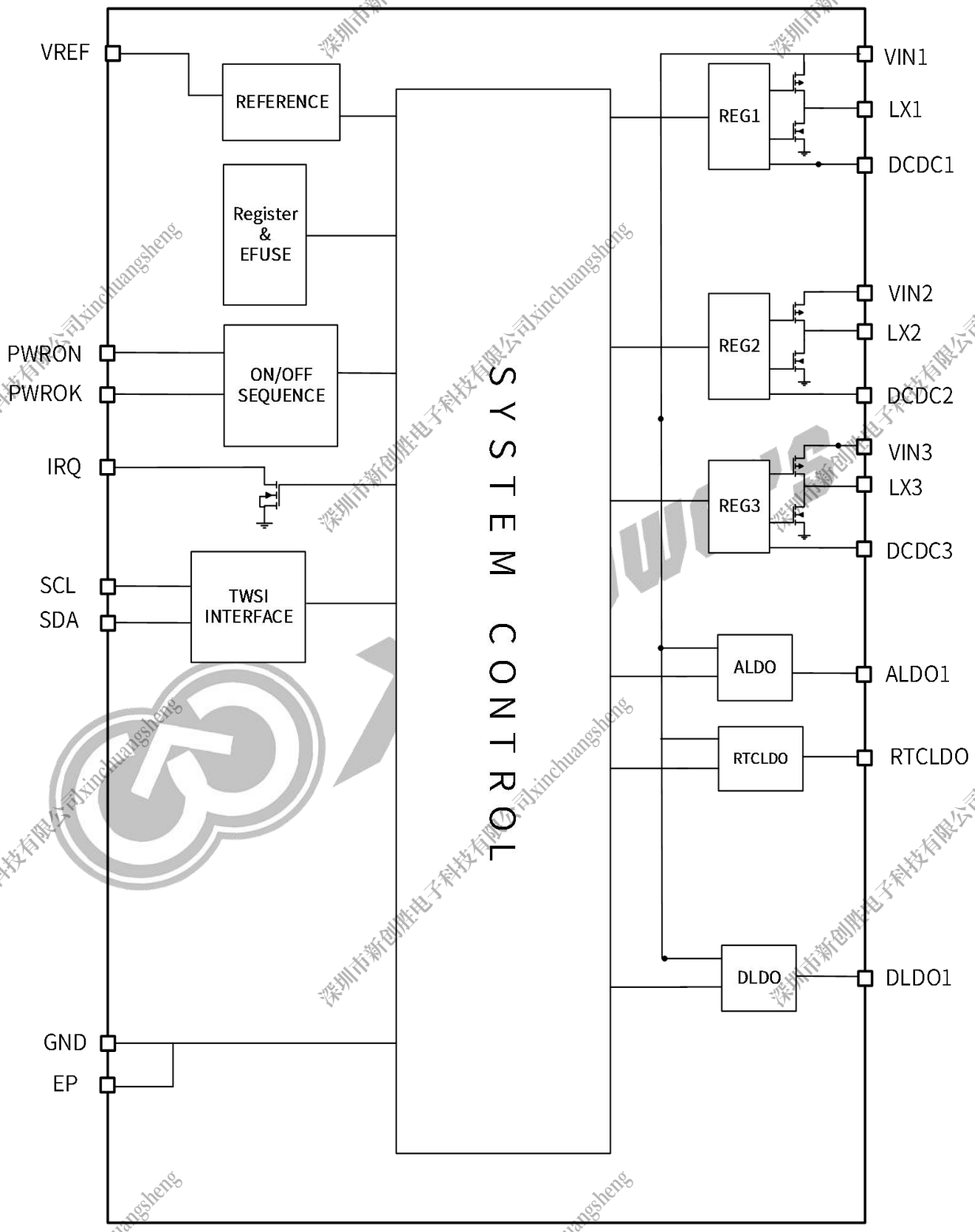
AXP323 supports 6 channel power outputs (including 3 channel DCDCs and 3 channel LDOs). DCDC1 and DCDC2 support dual phase for heavy current application. To ensure the security and stability of the power system, AXP323 integrates protection circuits such as over-voltage protection (OVP), under-voltage protection (UVP) and over temperature protection (OTP). Moreover, AXP323 features power management functions such as power on/off, sleep and wakeup, which reflects the management value of chip integration .

AXP323 provides a fast interface (Two Wire Serial Interface, TWSI) for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

AXP323 is available in 3mm x 3mm 20-pin QFN package.

6.2 Function Block Diagram

Figure 6-1 Function Block Diagram



6.3 TWSI Communication

When AXP323 powers on, SCK/SDA pin of TWSI will be pulled up to IO Power and then Host can adjust and monitor AXP323 with rich feedback information. The default slave address is 0x6C/0x6D.

Note: "Host" here refers to system processor.

Figure 6-2 Waveform of TWSI

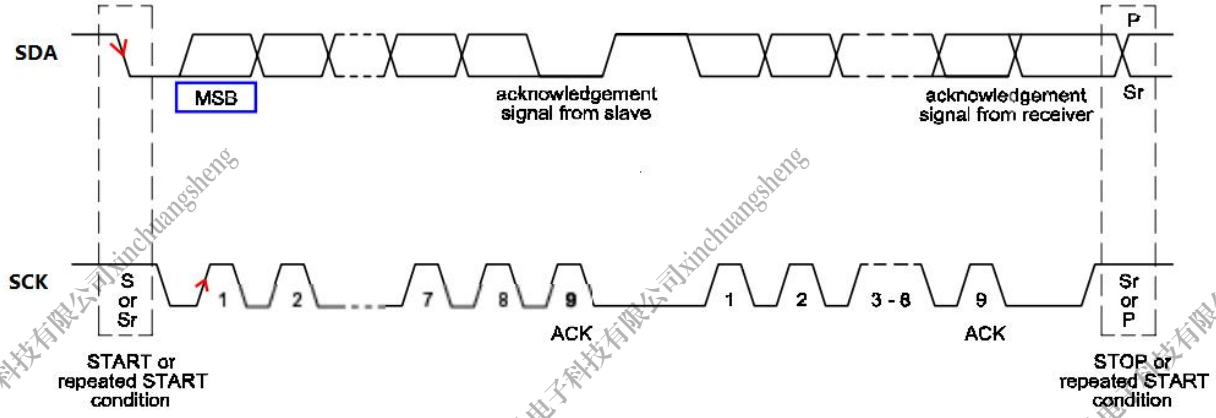


Table 6-1 Read and write address of TWSI

BYTE	BIT							
	MSB	6	5	4	3	2	1	0
WRITE	0	1	1	0	1	1	0	0
READ	0	1	1	0	1	1	0	1

Figure 6-3 Timing of TWSI

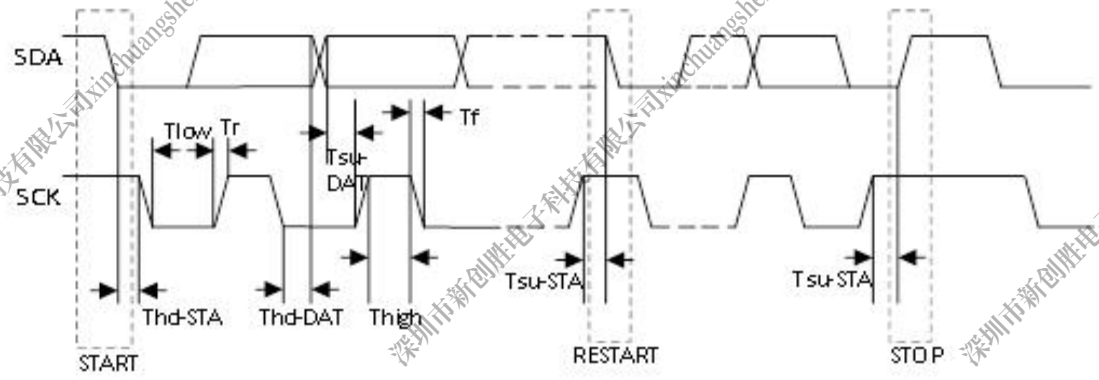


Table 6-2 Timing constants

Parameter	Symbol	Stander mode			Fast mode			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SCK clock frequency	Fsck	0	-	100	0	-	400	kHz
Setup time in START	Tsu-STA	4.7	-	-	0.6	-	-	us
Hold time in START	Thd-STA	4.0	-	-	0.6	-	-	us
Setup time in Data	Tsu-DAT	250	-	-	100	-	-	ns
Hold time in Data	Thd-DAT	0	-	-	0	-	0.9	us
Setup time in STOP	Tsu-STO	4.0	-	-	0.6	-	-	us
SCK low level time	Tlow	4.7	-	-	1.3	-	-	us
SCK high level time	Thigh	4.0	-	-	0.6	-	-	us

Parameter	Symbol	Stander mode			Fast mode			Unit
		MIN	TYP	MAX	MIN	TYP	MAX	
SDA/SCK falling time	Tf	-	-	300	20	-	300	ns
SDA/SCK rising time	Tr	-	-	1000	20	-	300	ns

6.4 Power On/Off & Reset

AXP323 has power off and power on status. When at off state, all voltage outputs are turned off except RTCLDO (If customized as always on). The total power consumption is typically 6uA(if RTCLDO is always on, consumption is about 10uA).

6.4.1 Power on-off Key (POK)

EN/PWRON pin can be configured as PWRON pin or EN pin by customization. The default is PWRON pin. The Power on-off Key (POK) can be connected between PWRON pin and GND of AXP323. AXP323 can automatically identify the four status(Long-press, Short-press, Negative edge, Positive edge) and then correspond respectively.

6.4.2 Power on

1.When EN/PWRON pin is customized as PWRON pin, power on sources include:

(1).POK. AXP323 can be powered on by pressing and holding POK for a period of time that longer than "ONLEVEL".

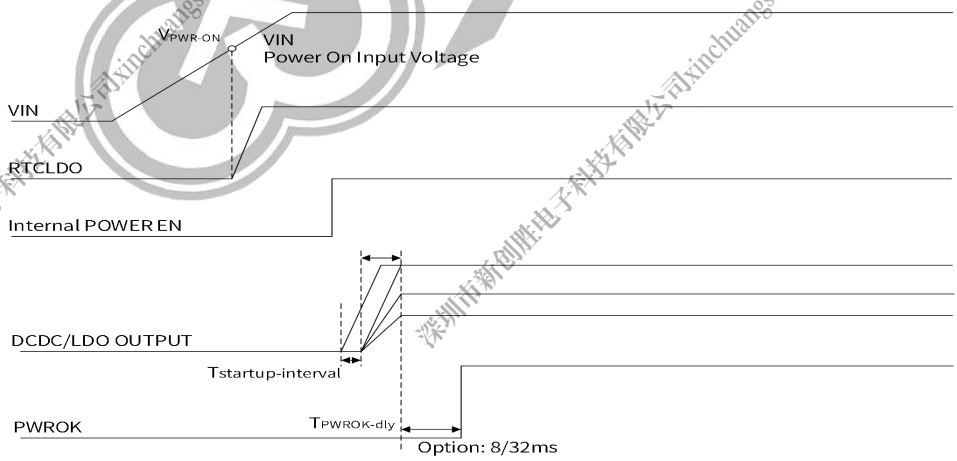
(2).VIN low to high. The function can be configured by customization.

(3).IRQ Low level. IRQ pin is low level for more than 16ms. The power-on function can be customized.

2.When EN/PWRON pin is customized as EN pin , AXP323 can be powered on by EN pin from low to high(>1.2V).

After power on, DCDC and LDO will be soft booted in preset timing sequence.

Figure 6-4 Power On Sequence



6.4.3 Power Off

1.When EN/PWRON pin is customized as PWRON pin, power off sources include:

(1).POK. AXP323 can be powered off by pressing and holding POK for a period of time that longer than "OFFLEVEL". The function can be configured by REG1BH[1] and REG1BH[0] decides whether the PMIC auto turns on or not when it shuts down after OFFLEVEL POK.

(2).Write "1" to REG1AH[7].

(3).VIN high to low. When VIN<VOFF, AXP323 will be powered off. The default of V_{OFF} is 2.6V.

(4).VIN>5.8V.

(5).The output voltage of DCDC is 15% lower than the setting value. The function can be configured by REG1DH[3:1].

(6).The output voltage of DCDC is 20% larger than the setting value. The function can be configured by REG1DH[0].

(7).DLDO1 over-current(>1A). The function can be configured by REG1DH[4].

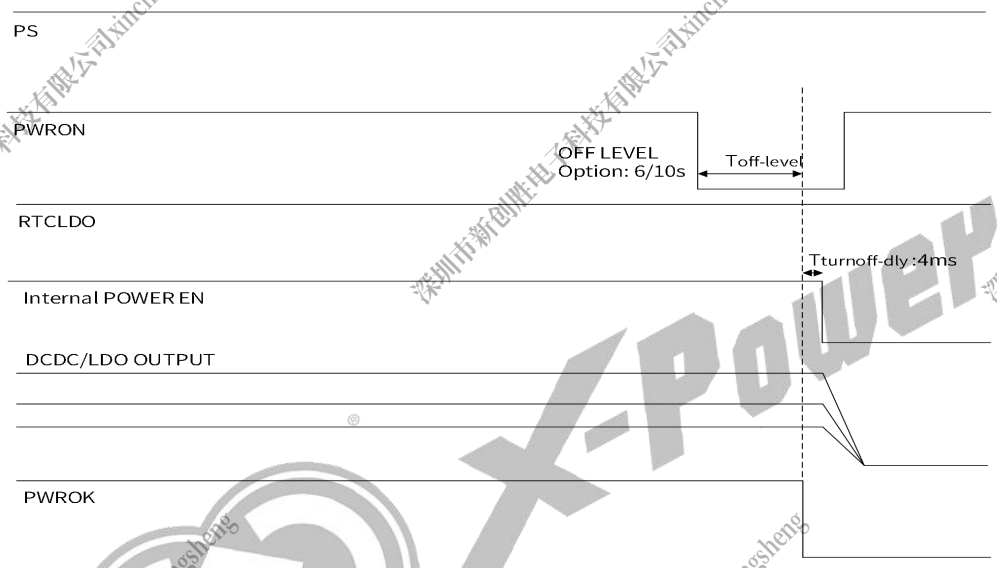
(8).Die temperature is over the warning level2(125°C). The function can be configured by REG1AH[1].

2.When EN/PWRON pin is customized as EN pin ,

(1).AXP323 can be powered off by EN pin from high to low.(<1.0V)

(2).The same as the power off source (3)~(8) used as PWRON pin.

Figure 6-5 Power Off Sequence



6.4.4 Sleep and wakeup

When the running system needs to enter Sleep mode, Maybe one or several power outputs should be disabled or changed to other voltage. The function can be configured by REG1CH[0]. Wakeup can be initiated by the following sources:

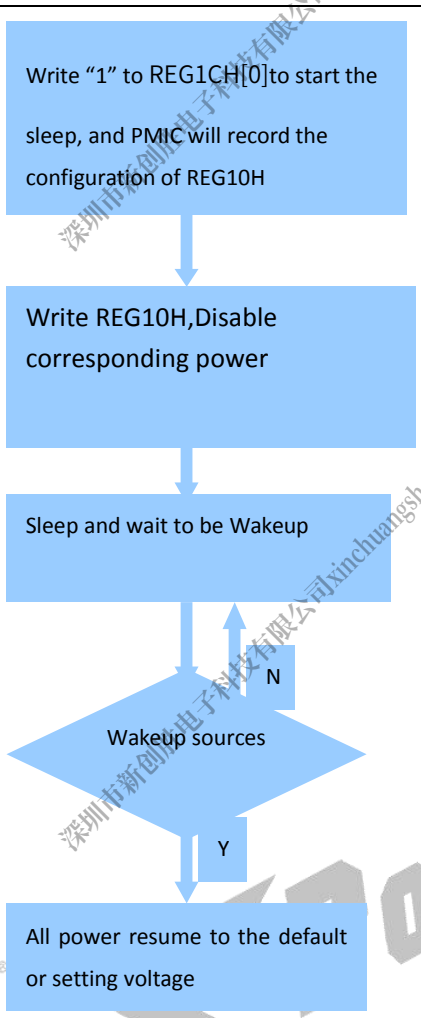
1.Software wakeup (REG1CH[1] is set to 1).

2.IRQ pin wakeup (REG1CH[4]=1 and IRQ pin is low level for more than 16ms by triggering an IRQ interrupt (POKPIRQ (REG20H[7]=1) or POKPNRQ (REG20H[6]=1) or POKSIRQ (REG20H[5]=1) or POKLIRQ (REG20H[4]=1) or DCDC3 UVP interrupt (REG20H[3]=1) or DCDC2 UVP interrupt (REG20H[2]=1) or OVP interrupt(REG 20H[0]=1)); or externally pull the IRQ pin low for more than 16ms.

These sources will make the all PMIC power outputs resume to the default voltage or the setting voltage, which is configured by REG1CH[2], and all shutdown powers will resume by the startup sequence.

See the control process under sleep and wakeup modes as below.

Figure 6-6 Sleep and wakeup



6.4.5 Reset

The PMIC has system reset and power on reset(POR).

- System reset

System reset means the PMIC is power off first and then power on. The power off and power on sequence of each output is the same with the normal power on sequence, and the corresponding registers are reset. During system reset, RTCLDO is always on (if RTCLDO is customized to be always on). There are two ways of system reset.

(1).PWROK drive low.

The PWROK pin can be used as the reset signal of application system. During AXP323 startup, PWROK outputs low level, which will be pulled up to startup the system after output voltage reaches the regulated value.

When application system works normally, If the PWROK pin is driven low by external key or other reasons, the AXP323 will be restarted. The function can be configured by REG1AH[4].

(2).Write “1” to REG1AH[6] to restart the PMIC.

- Power on reset(POR)

Power on reset means all the internal logic will be reset. When at power on reset state, all voltage outputs DCDC/LDO including RTCLDO are turned off and then turned on.

6.5 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP323.

Table 6-3 Power output information

Output Path	Type	Default Voltage	Startup Sequence	Application Suggestion	Load Capacity(Max)
DCDC1	BUCK	Customization	Customization	GPU	3000mA
DCDC2	BUCK			CPU	3000mA
DCDC3	BUCK			DRAM	3000mA
ALDO1	LDO			PLL/AVCC……	300mA
DLDO1	LDO			IO	500mA
RTCLDO	LDO			RTC	30mA

AXP323 includes three synchronous step-down DCDCs and three LDOs. The work frequency of DCDC is 1.5MHz by default. External small inductors and capacitors can be connected.

All DCDC/LDOs support the discharge function. It means that when the output is turned off, the charge on the external capacitor can be quickly released through the internal discharge path.

DCDC2 has DVM enable option configured by REG14H[7]. In DVM mode, when there is a change in the output voltage, DCDC2 will change to the new targeted value step by step. It supports two kinds of DVM slope: 1 step/20us and 1step/40us. The slope can be chosen by REG12H[4].

AXP323 can configure the default voltage, the startup sequence and other control of all power output.

Startup sequence:The startup sequence has four levels from 0 to 3. When the sequence is 0, it means the output is booted at the first step. When the sequence code is 1, it means the output is booted at the second step. When the sequence code is 2, it means the output is booted at the third step. When the sequence is 3, it means the output is not booted by default. The startup interval can be customized as 2/4/16/32ms.

6.6 Interrupt

PMIC interrupt controller monitors the trigger events such as under voltage, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enable bits are set to 1 (Refer to registers REG20H), corresponding IRQ status will be set to 1 (Refer to registers REG21H), and IRQ pin (open drain) will be pulled down. When host detects triggered IRQ signal, host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing “1” to the status bit.

Table 6-4 Interrupt information

Bit	IRQ	DESCRIPTION
REG20H[7]	IRQ1	PWRON positive edge
REG20H[6]	IRQ2	PWRON negative edge
REG20H[5]	IRQ3	PWRON short press
REG20H[4]	IRQ4	PWRON long press
REG20H[3]	IRQ5	DCDC3 under voltage
REG20H[2]	IRQ6	DCDC2 under voltage
REG20H[0]	IRQ7	IC over temperature

6.7 Register

6.7.1 Register List

Address	Description	R/W	Default
00	Power ON Source indication	R	
10	on-off control	R/W	XXH
12	DCDC mode control1	R/W	00H
13	DCDC1 Voltage control	R/W	XXH

Address	Description	R/W	Default
14	DCDC2 Voltage control	R/W	XXH
15	DCDC3 Voltage control	R/W	XXH
16	ALDO1 Voltage control	R/W	XXH
17	DLDO1 Voltage control	R/W	XXH
1A	Power off, Restart Control	R/W	20H
1B	Power off sequence,POK control	R/W	06H
1C	Power wakeup control	R/W	00H
1D	Output monitor control	R/W	1FH
1E	POK settings	R/W	80H
20	IRQ Enable	R/W	31H
21	IRQ Status	R/W	00H
22	DCDC mode control2	R/W	00H

6.7.2 Register Description

6.7.2.1 REG 00H: Power ON source indication

Reset: system reset

Bit	Description	R/W
7-5	Reserved	R
4	Startup by EN from L go H when VIN is High,or VIN from L go high when EN is High	R
3	Startup by IRQ pin	R
2	Startup by PWRON Press	R
1	Reserved	R
0	Startup by VIN from L go H	R

6.7.2.2 REG 10H: on-off control

Default: XXH

Reset: system reset

Bit	Description		R/W	Default
7-5	Reserved		RW	0
4	DLDO1 on-off control	0: off; 1: on	RW	Customization
3	ALDO1 on-off control		RW	
2	DCDC3 on-off control		RW	
1	DCDC2 on-off control		RW	
0	DCDC1 on-off control		RW	

6.7.2.3 REG 12H: DCDC mode control1

Default: 00H

Reset: system reset

Bit	Description	R/W	Default
7	DCDC2 FCCM mode: 0: NOT FCCM	RW	0

	1: FCCM		
6	DCDC3 FCCM mode: 0: NOT FCCM 1: FCCM	RW	0
5	DCDC1 FCCM mode: 0: NOT FCCM 1: FCCM	RW	0
4	DCDC2 DVM voltage ramp control 0: 1step/20us 1: 1step/40u	RW	0
3-0	Reserved	RW	0

6.7.2.4 REG 13H: DCDC1 voltage control

Default: XXH

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC1 voltage setting bit4-0: 0.5~1.2V, 10mV/step, 71steps 1.22~1.54V, 20mV/step, 17steps 1.6~3.4V, 100mV/step, 19 step	RW	Customization

6.7.2.5 REG 14H: DCDC2 voltage control

Default: XXH

Reset: system reset

Bit	Description	R/W	Default
7	DCDC2 DVM on-off control 0: disable 1: enable	RW	0
6-0	DCDC2 voltage setting bit6-0: 0.5~1.2V, 10mV/step, 71steps 1.22~1.54V, 20mV/step, 17steps	RW	Customization

6.7.2.6 REG 15H: DCDC3 voltage control

Default: XXH

Reset: system reset

Bit	Description	R/W	Default
7	Reserved	RW	0
6-0	DCDC3 voltage setting bit6-0: 0.5~1.2V, 10mV/step, 71steps 1.22~1.84V, 20mV/step, 32steps	RW	Customization

6.7.2.7 REG 16H: ALDO1 voltage control

Default: XXH

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	ALDO1 voltage setting bit4-0: 0.5~3.5V, 100mV/step, 31steps	RW	Customization

6.7.2.8 REG 17H: DLDO1 voltage control

Default: XXH

Reset: system reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4-0	DLDO1 voltage setting bit4-0: 0.5~3.5V, 100mV/step, 31steps	RW	Customization

6.7.2.9 REG 1AH: Power off sequence,POK control

Default: 20H

Reset: bit [7:6] is System reset,other bits is power on reset

Bit	Description	R/W	Default
7	Soft power off control. Write 1 to this bit will power off the PMIC, and this bit will clear itself	RW	0
6	Soft restart control. Write 1 to this bit will restart the PMIC, and this bit will clear itself	RW	0
5	Enable for PMIC to monitor the status of PWROK pin to judge whether PMIC starts up normally 0: disable 1: enable	RW	1
4	Enable to restart the PMIC by PWROK drive low 0: disable 1: enable	RW	0
3-2	Reserved	RW	0
1	The PMIC shut down or not when die temperature is over the warning level 2 0: not shutdown 1: shutdown	RW	0
0	Over temperature protection threshold configuration 0: 125°C 1: 145°C	RW	0

6.7.2.10 REG 1BH: Power off sequence、pwron key off control

Default: 06H

Reset: Power on reset

Bit	Description	R/W	Default
7-4	Reserved	RW	0000
3	Output power down sequence control 0: at the same time 1: the reverse of the startup	RW	0
2	Enable for 4ms delay when PMIC power off normally	RW	1

	0: disable 1: enable		
1	Enable bit for the function which will shut down the PMIC when POK is larger than OFFLEVEL 0: disable 1: enable	RW	1
0	The PMIC auto turn on or not when it shut down after OFFLEVEL POK 0: disable 1: enable	RW	0

6.7.2.11 REG 1CH: Power wake up Control

Default: 00H

Reset: bit[3]&[1:0] is System reset,other bits are Power on reset

Bit	Description	R/W	Default
7-5	Reserved	RW	0
4	IRQ Pin low to wakeup 0 : disable 1 : enable	RW	0
3	PWROK drive low or not when Power wake up 0: not drive low 1: drive low in wake up period	RW	0
2	Voltage recovery control when the PMIC wakeup 0: recovery to the default 1: Do nothing to the voltage(depend on the voltage before wakeup)	RW	0
1	Software wakeup write 1 to this bit, the output power will be waked up, and this bit will clear itself	RW	0
0	Sleep function enable	RW	0

6.7.2.12 REG 1DH: Output monitor control

Default: 1FH

Reset: Power on reset

Bit	Description	R/W	Default
7-5	Reserved	RW	000
4	DLDO1 over current turn off PMIC function 0: disable 1: enable	RW	1
3	DCDC3 under voltage turn off PMIC function 0: disable 1: enable	RW	1
2	DCDC2 under voltage turn off PMIC function 0: disable 1: enable	RW	1
1	DCDC1 under voltage turn off PMIC function 0: disable 1: enable	RW	1
0	If voltage of DCDC is over 20%(30%) of the setting value, the PMIC shutdown or not.（OVP） 0: not shutdown 1: shutdown	RW	1

6.7.2.13 REG 1EH: POK setting

Default: 80H

Reset: Power on reset

Bit	Description	R/W	Default
7	Reserved	RW	1
6-2	Reserved	RW	0
1	OFFLEVEL setting 0: 6s 1: 10s	RW	0
0	IRQLEVEL setting 0: 1.5s 1: 2.5s	RW	0

6.7.2.14 REG 20H: IRQ Enable

Default: 31H

Reset: System reset

Bit	Description	R/W	Default
7	PWRON positive edge IRQ enable	RW	0
6	PWRON negative edge IRQ enable	RW	0
5	PWRON short press IRQ enable	RW	1
4	PWRON long press IRQ enable	RW	1
3	DCDC3 under voltage IRQ enable	RW	0
2	DCDC2 under voltage IRQ enable	RW	0
1	Reserved	RW	0
0	Die over temperature protection IRQ enable	RW	1

6.7.2.15 REG 21H: IRQ Status

Default: 00H

Reset: System reset

Bit	Description	R/W	Default
7	PWRON positive edge IRQ,write 1 to clear it	RW	0
6	PWRON negative edge IRQ,write 1 to clear it	RW	0
5	PWRON short press IRQ,write 1 to clear it	RW	0
4	PWRON long press IRQ,write 1 to clear it	RW	0
3	DCDC3 under voltage IRQ,write 1 to clear it	RW	0
2	DCDC2 under voltage IRQ,write 1 to clear it	RW	0
1	Reserved	RW	0
0	Die over temperature protection IRQ,write 1 to clear it	RW	0

6.7.2.16 REG 22H: DCDC mode control2

Default: 00H

Reset: Power on reset

Bit	Description	R/W	Default
7-3	Reserved	RW	0
2	DCDC frequency 0: 1.5MHz 1: 2MHz	RW	0
1	DCDC1/2 dual phase enable 0: disable 1: enable	RW	0
0	Reserved	RW	0

7 Application Information

7.1 DCDC/LDO Design

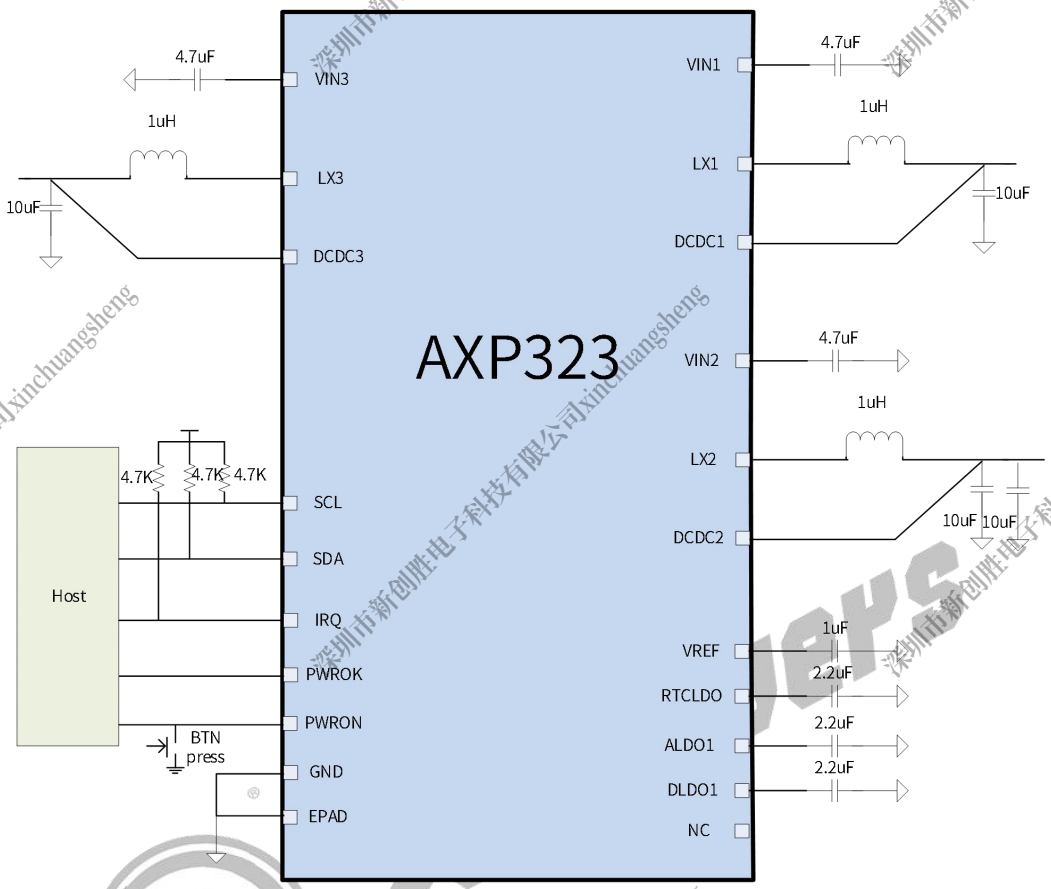
1. Output capacitance of LDO is not smaller than 1uF.
2. For unused LDO, the output pin just stays floating and dose not need an external capacitor.
3. Each DCDC uses a 1uH inductor. Its saturation current of inductor should be 30% higher than the load current, and the internal resistance is less than 30mohm.
4. Output capacitance of each DCDC is not smaller than 10uF.

7.2 IO Design

1. TWSI: Pull up SDA and SCK to a source, such as RTCLDO.
2. Pull up IRQ with a 4.7kΩ resistor to a source, such as RTCLDO.
3. If the system needs a reset key, just connect a key between PWROK pin and GND.
4. Use RC(510Ω+100nF) to connect the PWRON key between PWRON pin and GND

7.3 Typical Application

Figure 7-1 Typical Application

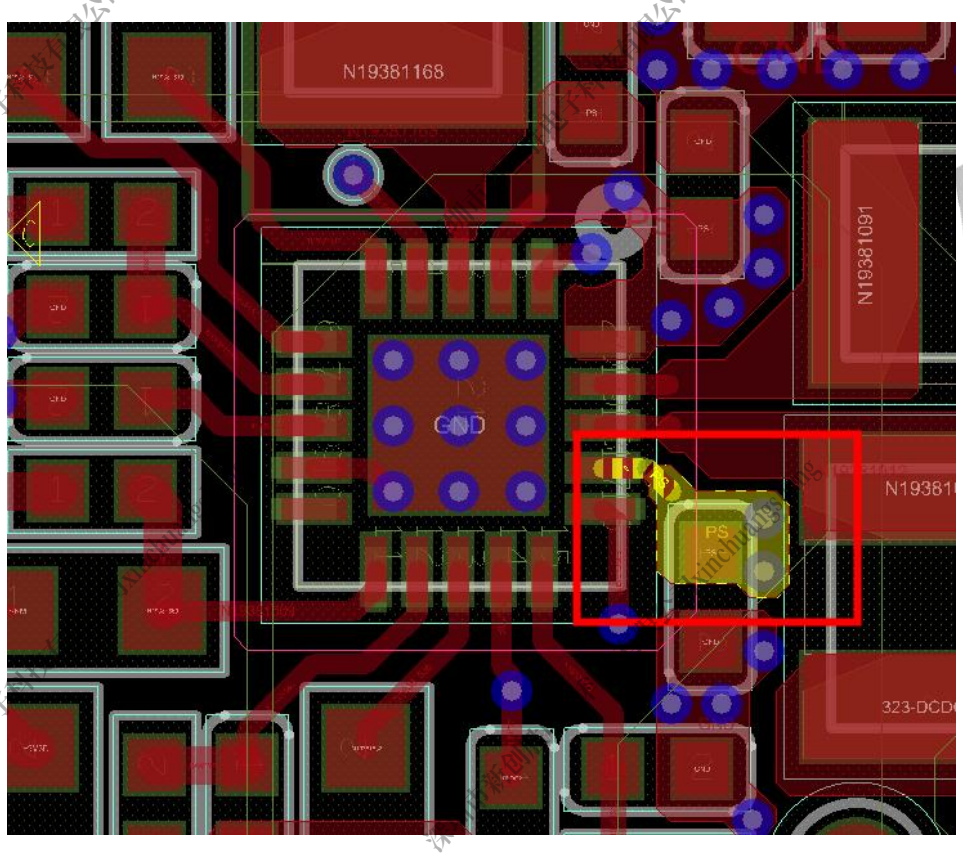


8 PCB Layout Guideline

Line width of high current path such as power input and output need to be widened to reduce line impedance, voltage drop and loss.

- Line width of DCDC input and output: >=150mil
- Line width of output depends on load current.
- The DCDC feedback lines need to be well shielded to avoid parallel layout with high-frequency signals on the same layer such as LX.
- Inductors of DCDCs are close to PMIC and output capacitors are close to inductors.
- Input capacitors of DCDCs are close to input pins(VIN1/VIN2/VIN3) and the input power enters the input pins after passing through the input capacitors. Refer to the following figure(input power -> via -> capacitor -> input pin).

Figure 8-1 PCB reference

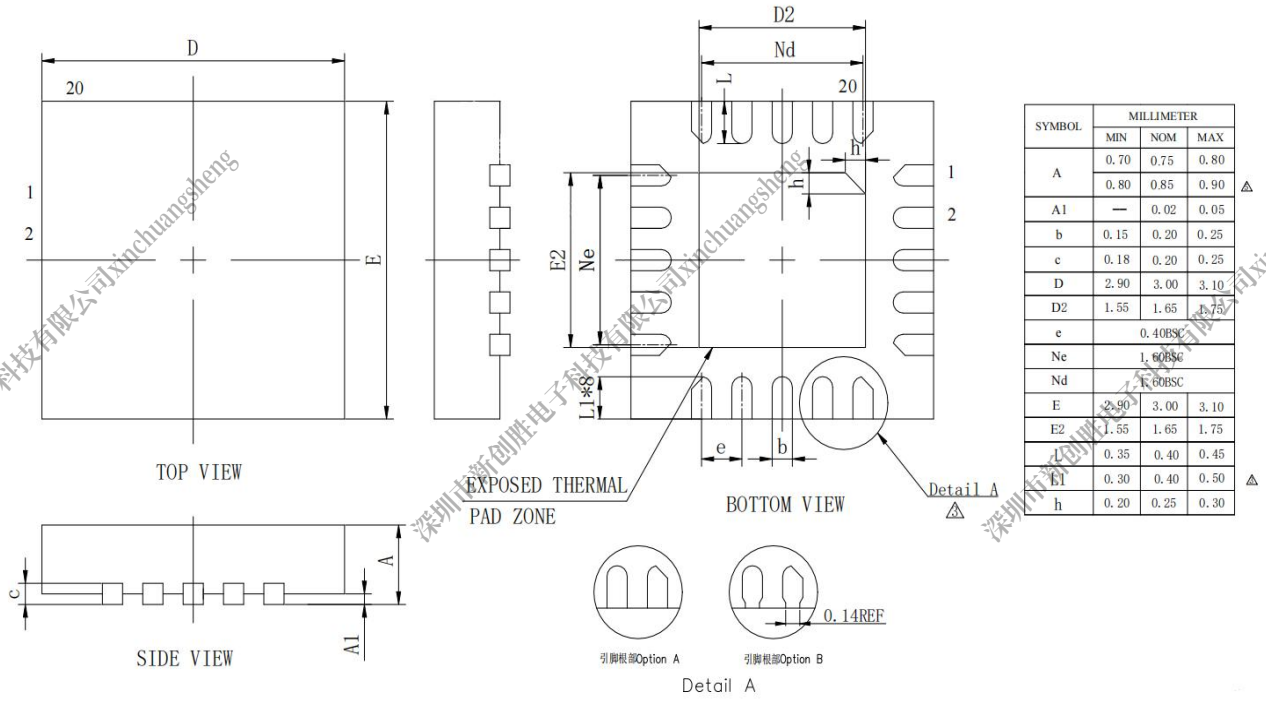


9 Package,Carrier,Storage and Baking Information

9.1 Package Information

AXP323 package is QFN3mm*3mm, 20-pin. Figure 9-1 shows AXP323 package.

Figure 9-1 Package information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
	0.80	0.85	0.90 ⚠
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
e	0.40BSC		
Ne	1.60BSC		
Nd	1.60BSC		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
L	0.35	0.40	0.45
L1	0.30	0.40	0.50 ⚠
h	0.20	0.25	0.30

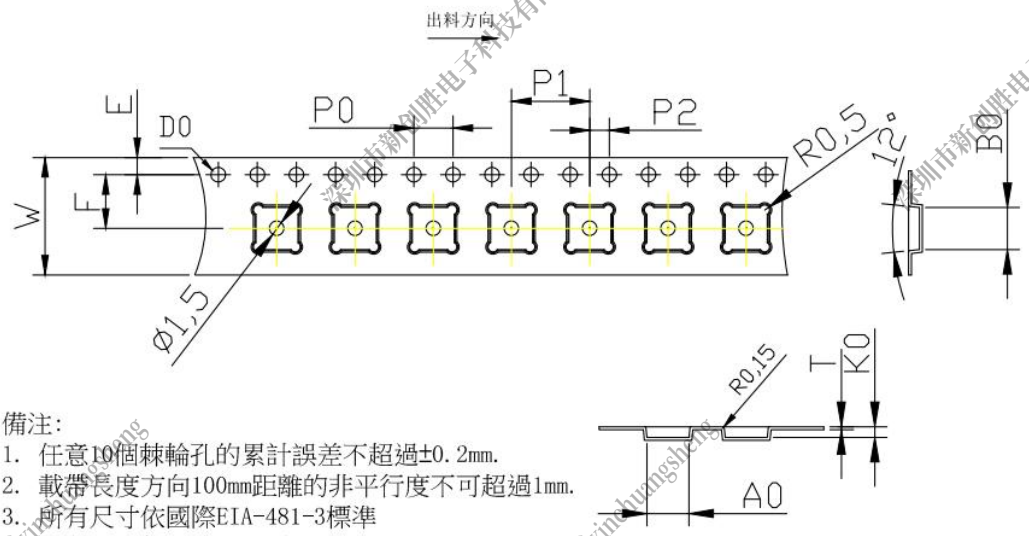
Figure 9-2 AXP323 marking

Table 9-1 AXP323 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP323	Product name	Fixed
2	LLLLLBA	Lot number	Dynamic
3	XXX1	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

9.2 Carrier

Figure 9-3 AXP323 Tape Dimension Drawing



備注:
1. 任意10個棘輪孔的累計誤差不超過±0.2mm.
2. 載帶長度方向100mm距離的非平行度不可超過1mm.
3. 所有尺寸依國際EIA-481-3標準
4. 材質: 黑色 PS料, 厚度 0.3 ±0.05mm.
5. 表面电阻率10^{5}~$10^{10}\Omega$。
6. 产品符合ROHS标准。

ITEM	W	A0	B0	K0	P0	P1	P2	F	S	E	D0	T
DIM	12±0.30	3.30±0.1	3.30±0.1	1.10±0.1	4.0±0.1	8.00±0.1	2.0±0.1	5.5±0.1	0.0±0.1	1.75±0.1	1.5$^{+0.10}_{0.00}$	0.3±0.05

Table 9-2 AXP323 Packing Quantity Information

Type	Quantity	Part Number
Tape	3000pcs/Tape	AXP323

9.3 Storage

9.3.1 Moisture Sensitivity Level(MSL)

A package’s MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in Table 9-3.

Table 9-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C/85%RH
2	1 year	≤30°C/60%RH
2a	4 weeks	≤30°C/60%RH
3	168 hours	≤30°C/60%RH
4	72 hours	≤30°C/60%RH
5	48 hours	≤30°C/60%RH
5a	24 hours	≤30°C/60%RH
6	Time on Label(TOL)	≤30°C/60%RH

AXP323 device samples are classified as MSL3.

9.3.2 Bagged Storage Conditions

The shelf life of AXP323 are defined in Table 9-4.

Table 9-4 AXP323 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

9.3.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP323 is as follows.

Table 9-5 Out-of-bag Duration

Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest *IPC/JEDEC J-STD-020C*.

9.4 Baking

It is not necessary to bake AXP323 if the conditions specified in Section 9.3.2 and Section 9.3.3 have not been exceeded. It is necessary to bake AXP323 if any condition specified in Section 9.3.2 and Section 9.3.3 have been exceeded.

Table 9-6 AXP323 Baking Conditions

Surrounding	Condition	Note
Nitrogen	Tray: 125°C/8 hours Tape: 60°C/72 hours	Recommended condition. It is recommended to bake once, no more than three times.

10 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. Figure 10-1 shows the typical reflow profile of AXP323 device sample.

Figure 10-1 AXP323 typical reflow profile

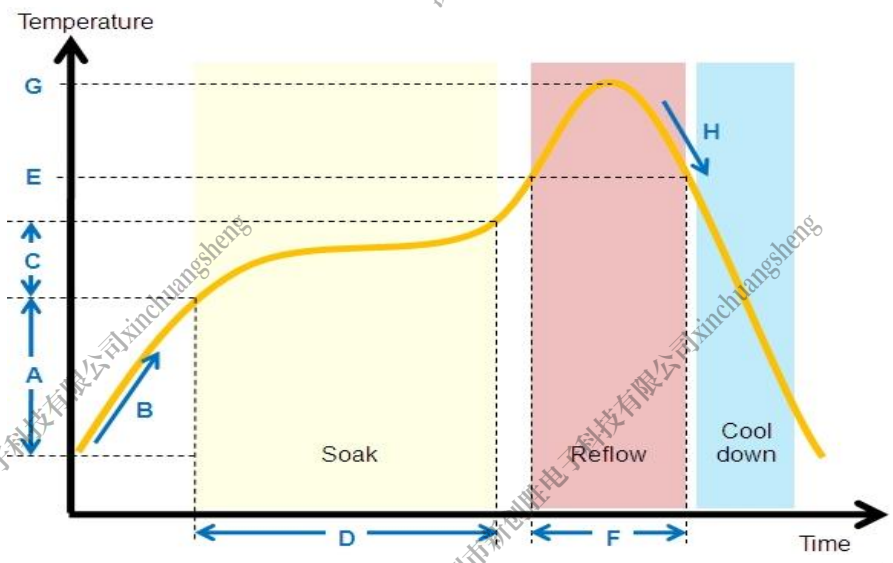


Table 10-1 AXP323 Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C/sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	⩽4°C/sec

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