NSD8306

Multi-channel Half Bridge Driver

Datasheet (EN) 1.0

Product Overview

The NSD8306 is a multi-channel half-bridge driver for automotive applications including HVAC flap DC motors, side mirror adjustment / fold motors, general relays, or other LEDs.

With the different connection configuration of half-bridge power stage outputs, the device can driver DC motors in simultaneous, sequential, or parallel mode. The outputs also support DC motor in forward, reverse, slow decay, and fast decay operation.

The device includes 6x internal configurable PWM generators, which allow for flexible control for LED dimming or motor current limitation during start up or stall condition.

The integrated serial peripheral interface (SPI) controls all outputs and provides diagnostic information including normal operation, POR, VM undervoltage/overvoltage, overcurrent, over temperature protection and open load status.

The device features sleep mode with low quiescent current when EN input is low or VDD falls below POR threshold.

Applications

- HVAC DC motors
- Side mirror adjustment and mirror fold
- Relays
- LEDs

Device Information

Part Number	*Package*	*Body Size*
NSD8306-Q1HTSXR	HTSSOP24	7.80mm × 4.40mm

Key Features

- 6x half bridge driver
  - HS/LS Rdson: 0.75ohm typ at 25°C
  - Device 1A per HB channel, 3A max for all channel all on
  - Half bridge output can be in parallel
- Wide 4.5V to 36V (configurable) operating Voltage
- Very low quiescent sleep mode
- PWM mode with internal PWM generation on each channel
  - 4 PWM frequency options: 80Hz/100Hz/200Hz/2000 Hz
  - 8-bit duty resolution (1/255, ~0.4 % duty)
  - Slew rate control for supporting 200, 2000Hz
- Integrated diagnosis and fault protection features
  - VM undervoltage & overvoltage protection (UV&OV)
  - Overcurrent / short circuit Protection (OCP/SCP)
  - Over temperature warning & shutdown
  - Open load diagnosis
  - Dedicated nFault indicator pin
- HTSSOP24, 7.8mm X 4.4mm with exposed PAD

Functional Block Diagrams

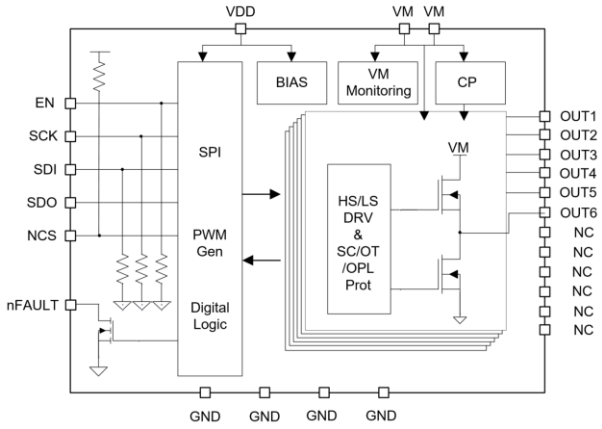


Figure 1. NSD8306 Block Diagram

1. Pin Configuration and Functions

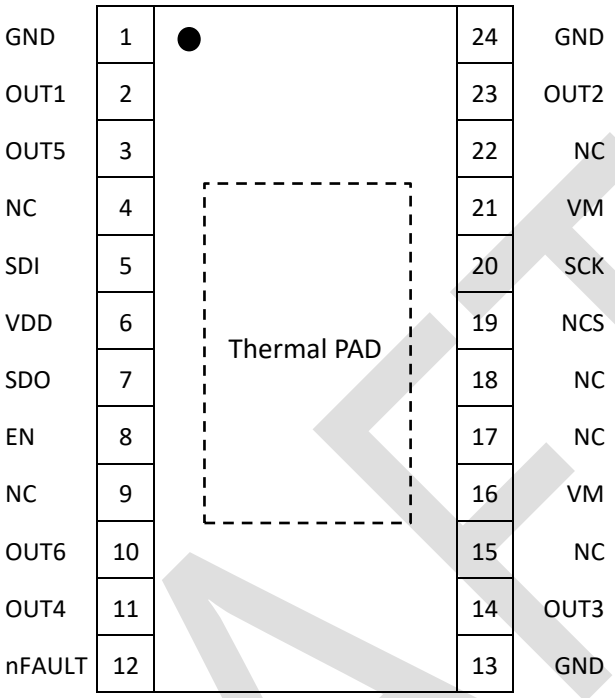


Figure 2. NSD8306 Pinout

Table 1. NSD8306 Pin Description

SYMBOL	NO.	TYPE	DESCRIPTION
GND	1,13, 24	PWR	Pins for ground connection, all ground pins should be externally connected together.
OUT1	2	O	Half-bridge output1 pin.
OUT5	3	O	Half-bridge output5 pin.
SDI	5	I	SPI data input pin
VDD	6	PWR	Logic supply input pin,
SDO	7	O	SPI data output pin
EN	8	I	Driver enable input pin with internal pull down (active HIGH). If EN input pin is pulled low, all OUTx go to tri-state and device move to low-power sleep state.
NC	4,9,15, 17,18,22	-	Not connected
OUT6	10	O	Half-bridge output6 pin.

OUT4	11	O	Half-bridge output4 pin.
nFAULT	12	O	Fault alert indicator output (active LOW). Open drain structure requires external pull up resistor, typical 4.7Kohm can be used.
OUT3	14	O	Half-bridge output3 pin.
VM	16,21	PWR	5V to 36V power supply. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitor (>10uF) needs to guarantee VM pin voltage in maximum range. Put the 0.1uF and bulk capacitor (>10uF) close to the VM pin. Two VM pins should be externally connected together.
NCS	19	I	SPI chip select input pin.
SCK	20	I	SPI clock input pin.
OUT2	23	O	Half-bridge output2 pin.
Thermal PAD	—		Thermal pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

2. Absolute Maximum Ratings

SYMBOL	PARAMETER	MIN	MAX	UNIT
VM	Power supply voltage	–0.3	40	V
VDD	Logic supply voltage	–0.3	6	V
V_{SDI}, V_{SDO}, V_{NCS}, V_{SCK}, V_{EN}, V_{nFAULT}	Logic input/ouput voltage (EN, SDI, SDO, NCS, SCK, nFAULT)	–0.3	VDD+0.3	V
V_{OUTX}	Output voltage (OUTx) DC condition	–0.3	40	V
	Output voltage (OUTx) AC condition, Iout=1A for t<500ms	-1	40	V

3. ESD Ratings

SYMBOL	PARAMETER	VALUE	UNIT
VESD_HBM	Human Body Model (HBM), VMx & VOUTx pins per ANSI/ESDA/JEDEC JS-001	±4000	V
	Human Body Model (HBM), other pins per ANSI/ESDA/JEDEC JS-001	±2000	V
VESD_CDM	Charged device model (CDM), Corner pins, per JEDEC specification JS-002	±750	V
	Charged device model (CDM), other pins, per JEDEC specification JS-002	±500	V

4. Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNIT
VM	VM supply, normal voltage range	4.5		18	V
	VM supply, extended voltage range (1)	18		Vov	V
	VM supply, over voltage range (2)	Vov		40	V
VDD	VDD supply voltage	3		5.5	V
EN, NCS, SCK, SDO, SDI, nFAULT	Logic input / output voltage	0		5.5	V

(1) Device is capable of full functional operation; however, parameter characteristic is not guarantee, deviation is possible.

(2) No damage to device, and power stage will be disabled during overvoltage range. Full functional operation will resume when battery voltage returns to normal voltage range.

5. Thermal Information

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	Thermal resistance, junction to case		2.7		°C/W
Rthja	Thermal resistance, junction to ambient, on 2-layer PCB		62		°C/W
	Thermal resistance, junction to ambient, on 4-layer PCB based on JEDEC standard		30		°C/W

6. Electrical characteristics

T_j = -40°C to 150°C, VM=4.5V to 18V, VDD=3.0 to 5V, unless otherwise specified.

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VM)						
I_{VM}	VM operating supply current	VM = 13.5V, EN=HIGH, all output off		0.5	1	mA
		VM = 13.5V, EN=HIGH, all high side on			5	mA
I_{VM_SLEEP}	VM sleep current	VM = 13.5V, -40≤Tj≤85°C, EN=LOW, total current of all VM pin			3	μA
V_{UV}	VM undervoltage threshold	VM falls until UVLO triggers	3.6		4.1	V
		VM rises until operation recovers	3.9		4.4	V
V_{UV_HYS}	VM undervoltage hysteresis			400		mV
t_{UV}	VM undervoltage deglitch time	Guaranteed by digital scan		10		us
V_{OV}	VM overvoltage	VM increasing, switch off, OVP_H = 0	21		25	V
		VM decreasing, switch on, OVP_H = 0	19		23	V
		VM increasing, switch off, OVP_H = 1	32		36	V
		VM decreasing, switch on, OVP_H = 1	30		34	V
V_{OV_HYS}	VM overvoltage hysteresis			2		V
t_{OV}	VM overvoltage deglitch time	Guaranteed by digital scan		10		us

VDD SUPPLY INPUT (VDD)						
I_{VDD}	Input current of VDD	EN=High, all outputs off, SPI not active			3	mA
		EN=High, SPI active 5MHz, all high side on			5	mA
I_{VDD_SLEEP}	Input current of VDD in sleep mode	EN=LOW, SPI inactive -40≤Tj≤85°C		1	2.5	uA
$V_{VDD\_POR\_H}$	POR high threshold	VDD increasing	2.5		3	V
$V_{VDD\_POR\_L}$	POR low threshold	VDD decreasing	2.3		2.8	V
LOGIC CONTROL INPUT (EN, NCS, SDI, SCK)						
V_{IL}	Input logic low voltage				0.3*VDD	V
V_{IH}	Input logic high voltage		0.7*VDD			V
V_{HYS}	Input logic hysteresis			0.5		V
R_{PD}	Pulldown resistance	EN, SDI, SCK	50	100	150	kΩ
R_{PU}	Pullup resistance	NCS	50	100	150	kΩ
C_{IN}	Input capacitance	NCS, SDI, SCK pin, Specified by design			15	pF
$T_{Deglitch}$	Deglitch filter on EN falling and rising			10	20	us
T_{WAKE}	Wake-up time	After EN low to high			150	us
NFAULT OUTPUT (OPEN DRAIN)						
V_{OL_nFault}	Output low voltage	I_{OD} = 5mA			0.5	V
I_{LEAK_nFault}	Output high leakage current	V_{OD} = 5V	-1		1	uA
SDO OUTPUT (PUSH PULL)						
V_{OL_SDO}	SDO Output low voltage	Io = 2mA			0.5	V
V_{OH_SDO}	SDO Output high voltage	Io = 2mA	VDD-0.5			V
I_{LEAK_SDO}	SDO tristate leakage	NCS high, 0<V_{SDO}<VDD	-1		1	uA
C_{OUT}	Output capacitance	Specified by design			30	pF
HALF BRIDGE OUTPUS (OUT1, OUT2, OUT3, OUT4, OUT5, OUT6)						
$R_{DS(ON)}$	High-side or Low-side FET on resistance	I = 0.5 A, Tj = 25°C		0.75	1.1	Ω
		I = 0.5 A, Tj = 150°C			1.5	Ω

I_{LEAK_HS}	HS OFF-state leakage	VOUTx = 0V, EN = 1	-2	-1	-	uA
		VOUTx = 0V, EN = 0	-2	-1	-	uA
I_{LEAK_LS}	LS OFF-state leakage	VOUTx = 13.5V, EN = 1	-	1	2	uA
		VOUTx = 13.5V, EN = 0	-	1	2	uA
t_{RISE} t_{FALL}	Output rise time Output fall time High side or low side	VM = 13.5 V, resistive load 100 ohm, HBx_SR = 0		0.6		V/µs
		VM = 13.5 V, resistive load 100 ohm, HBx_SR = 1		2.5		V/µs
t_{PD}	Propagation delay (high side / low side ON/OFF)	HBx_SR = 0	5	12	25	µs
		HBx_SR = 1	3	5	10	µs
t_{DEAD}	Cross protection time, high to low / low to high	HBx_SR = 0	8	20	32	µs
		HBx_SR = 1	2	5	15	µs
OVERCURRENT PROTECTION						
I_{OC}	Over current threshold	Half bridge low side	1		1.6	A
		Half bridge high side	-1.6		-1	A
t_{OC}	OC deglitch filter time	OC_Filter bit = 000		10		µs
		OC_Filter bit = 001		5		
		OC_Filter bit = 010		2.5		
		OC_Filter bit = 011		1		
		OC_Filter bit = 100		60		
		OC_Filter bit = 101		40		
		OC_Filter bit = 110		30		
		OC_Filter bit = 111		20		
ON STATE OPEN LOAD DIAGNOSIS						
I_{OL}	Open load threshold	Half bridge low side, HBx_OPL_TH = 0	3	10	20	mA
		Half bridge high side, HBx_OPL_TH = 0	-20	-10	-3	mA
t_{OL}	Open load filter time	HBx_OPL_TH = 0, guarantee by digital scan	2	3	4	ms
I_{OL_LOW}	Low open load threshold	Half bridge low side, HBx_OPL_TH = 1	0.3	1	2	mA
		Half bridge high side, HBx_OPL_TH = 1	-2	-1	-0.3	mA

t_{OL_LOW}	Low open load filter time	HBx_OPL_TH = 1, guarantee by digital scan	0.2	0.3	0.4	ms
ON STATE OPEN LOAD DIAGNOSIS						
I_{PU}	Diag pull up current	HBx_IPUPD_MODE = 0	133	200	266	uA
	Diag pull up current	HBx_IPUPD_MODE = 1	666	1	1.5	mA
I_{PD}	Diag pull down current	HBx_IPUPD_MODE = 0	400	600	800	uA
	Diag pull down current	HBx_IPUPD_MODE = 1	2	3	4.5	mA
V_{STA_HB}	Off state status threshold	OUTx pin	0.54 *VDD	0.6*VDD	0.66*VDD	V
THERMAL PROTECTION						
OT_{WARN}	Thermal warning temperature		120	140	160	°C
T_{HYS_OTW}	Thermal warning hysteresis			20		°C
OT_{SD}	Thermal shutdown temperature		150	170	190	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis			20		°C
SPI AC TIMINGS						
T_{cll}	Minimum time CLK = LOW (5)	Application info	85			ns
T_{clh}	Minimum time CLK = HIGH (4)	Application info	85			ns
T_{pcld}	Propagation delay (SCLK to data at SDO active) (B)	Cload=30pF			30	ns
T_{lead}	CLK change L/H after NCS = LOW (2)	Application info	100			ns
T_{scld}	SDI input setup time (CLK change H/L after SDI data valid) (F)	Application info	30			ns
T_{hcld}	SDI input hold time (SDI data hold after CLK change H/L) (C)	Application info	30			ns
T_{sclch}	CLK low before NCS low (1)	Application info	125			ns

T_{lag}	CLK low before NCS high (6)	Application info	100			ns
T_{hclch}	CLK high after NCS high	Application info	100			ns
T_{onncs}	NCS min high time (9)	Application info	1			us
T_{pchdz}	NCS L/H to SDO @ high impedance (E)	Cload=30pF			75	ns
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info			5	MHz

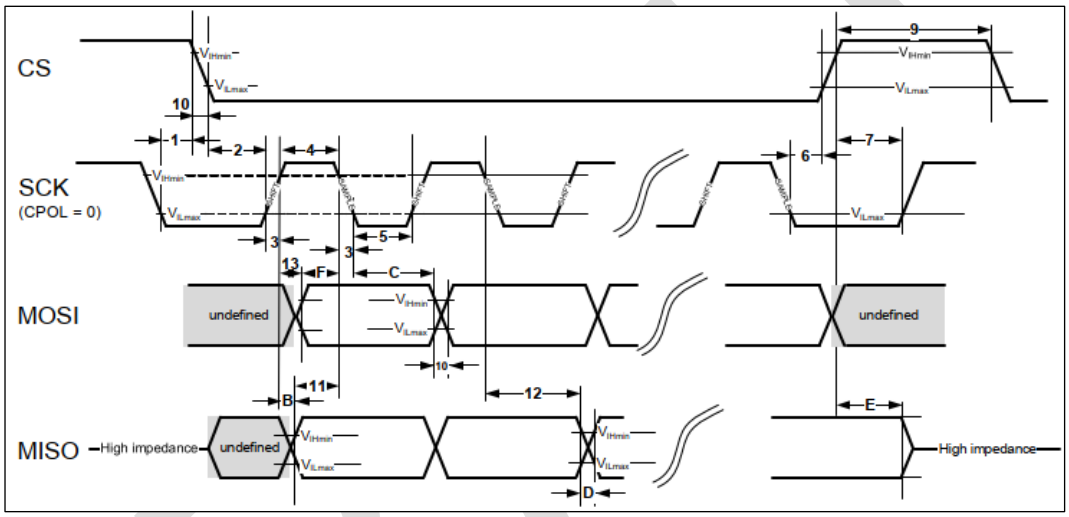


Figure 3. SPI timing diagram

7. Functional description

7.1. VM & VM UV / OV protection

VM is the supply voltage, range from 4.5v to 36v with typical case 13.5v power supply. It is recommended to put at both 100nF ceramic and >10uF bulk electrolytic capacitor closed to each VM pin.

When VM power supply pin voltage falls below the undervoltage threshold (V_{UV}) over 10us typ. undervoltage deglitch time, half bridge outputs OUTx becomes OFF. When VM rise above the $V_{UV,}$ the device automatically resumes operation.

When VM power supply pin voltage rises above the overvoltage threshold (V_{OV}) over 10us typ. overvoltage deglitch time, half bridge outputs OUTx becomes OFF. When VM decrease under the $V_{OV,}$ the device automatically resumes operation. OVP_H register bit set the two different VM input overvoltage threshold.

7.2. VDD

VDD pin accepts wide supply range from 3v to max 5.5v which intends for the compatibility with both 3.3v and 5v system supply. 100nF X7R ceramic capacitor is suggested to put closed to VDD pin.

Internal block, SPI interface, digital block will be inactive when VDD drops below $V_{VDD\_POR\_L}$, so including charge pump and all half bridge drivers are switched off. Once VDD > $V_{VDD\_POR\_H}$, internal digital is reset, and status register NPOR bit is set to 0 and can be cleared to 1 by SPI readout (if RD_CLR_EN=1) or CLR_FLT = 1 command.

7.3. EN input

The EN pin signal is common for all output channels. When it is driven low, internal logic / register is reset, charge pump / all outputs are disabled, and device enter sleep mode.

After EN transition from low to high at VDD > $V_{VDD\_POR\_H}$, device come out sleep mode at finishing internal POR and NPOR=0.

A T_{WAKE} time shall be wait for charge pump reach regulated voltage once device move from sleep to normal operation.

7.4. Half bridge output stage, OUT1 ~ OUT6

The half bridge drivers are designed to drive DC motor or general used inductive/resistive load like LED.

The power stage outputs (out1~out6) can be in parallel to support higher load current.

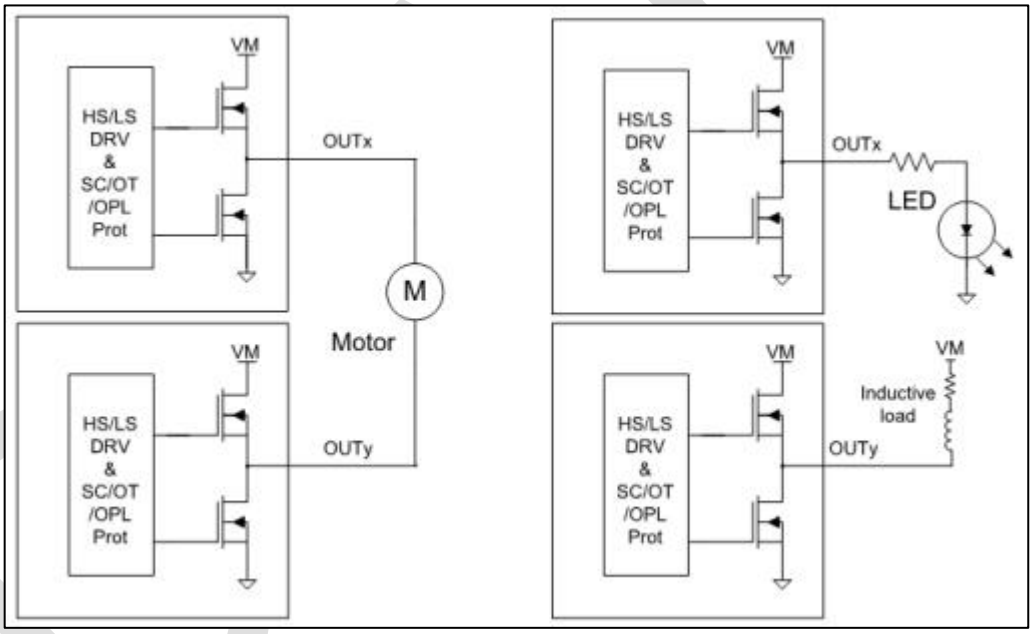


Figure 4. Power stage output block diagram

7.4.1. SPI Control ON/OFF operation

To directly operate half bridge output by only SPI ON/OFF control, the two group register as below shall be controlled in following steps.

1. HBx_PWM_EN bit configuration in register HB_PWM_CTRL1 and FW_PWM_CTRL_2
2. HBx_HS_EN or HBx_LS_EN bit configuration in register HB_CTRL1 / HB_CTRL2 / CTRL3

Note:

- HBx_PWM_EN bit shall be configured or keep default value '0' for SPI control ON/OFF operation

- One specific half bridge, HBx_HS_EN and HBx_LS_EN shall not be '1' at the same time, otherwise, the specific half bridge will be HIZ until this same bridge HS and LS control bit both high condition is removed

Example of activation of HB1_HS / HB1_LS and HB2_HS / HB2_LS to drive motor by SPI control as table 2 shown

Table 2. Half bridge SPI control register setting example

EN	HB1 register setting	HB2 register setting	OUT1	OUT2
LOW	x	x	HIZ	HIZ
High	HB1_PWM_EN=0 HB1_HS_EN=0 HB1_LS_EN=0	HB2_PWM_EN=0 HB2_HS_EN=0 HB2_LS_EN=0	HIZ	HIZ
High	HB1_PWM_EN=0 HB1_HS_EN=1 HB1_LS_EN=0	HB2_PWM_EN=0 HB2_HS_EN=0 HB2_LS_EN=1	High	Low
High	HB1_PWM_EN=0 HB1_HS_EN=0 HB1_LS_EN=1	HB2_PWM_EN=0 HB2_HS_EN=0 HB2_LS_EN=1	Low	Low
High	HB1_PWM_EN=0 HB1_HS_EN=0 HB1_LS_EN=1	HB2_PWM_EN=0 HB2_HS_EN=1 HB2_LS_EN=0	Low	High
High	HB1_PWM_EN=0 HB1_HS_EN=1 HB1_LS_EN=0	HB2_PWM_EN=0 HB2_HS_EN=1 HB2_LS_EN=0	High	High

7.4.2. PWM control operation

PWM control is based on internal digital PWM generator and map control block. It is suggested to set following registers

- PWM frequency / duty cycle / map control

  (1) PWMx_FREQ bit in PWM_FREQ_CTRL1 / PWM_FREQ_CTRL2 registers
  Total 8 PWM generator, 2bit configuration for each PWM freq as (80Hz / 100Hz / 200Hz / 2000Hz) in +/-30% variation for full operating and temperature range.

  (2) PWMx_DUTY_CYCLE bit in PWM_DC_CTRL1~PWM_DC_CTRL8 registers
  8bit configuration of PWMx_DUTY_CYCLE define the duty cycle of generated PWMx as 100%*BIT value /255

  (3) HBx_PWM_MAP bit in PWM_MAP_CTRL1~PWM_MAP_CTRL6 registers
  3bit for each Half bridge, which allows independent and flexible selection from PWM1~PWM8

- Half bridge driver setting for PWM

  (1) HBx_PWM_EN bit in HB_PWM_CTRL1, FW_PWM_CTRL2

  HBx_PWM_EN bit changed to '1' will enable the selected half bridge operation control by mapped PWM

  (2) HBx_HS_EN / HBx_LS_EN in HB_CTRL1~HB_CTRL3

  Set HBx_HS_EN or HBx_LS_EN bit at '1' to enable the PWM activated Power FET stage.

- Active / passive freewheeling setting in PWM

  (1) HBx_FW bit in FW_CTRL_1, FW_PWM_CTRL_2 registers

  When the particular half bridge channel is chosen to use PWM, it is also possible to select the active or passive freewheeling option for the half bridge channel, by HBx_FW control bit.

  Example of active HB1 SPI ON and HB2 LS in PWM mode / HB2 HS in passive or active freewheeling to drive motor / inductive load

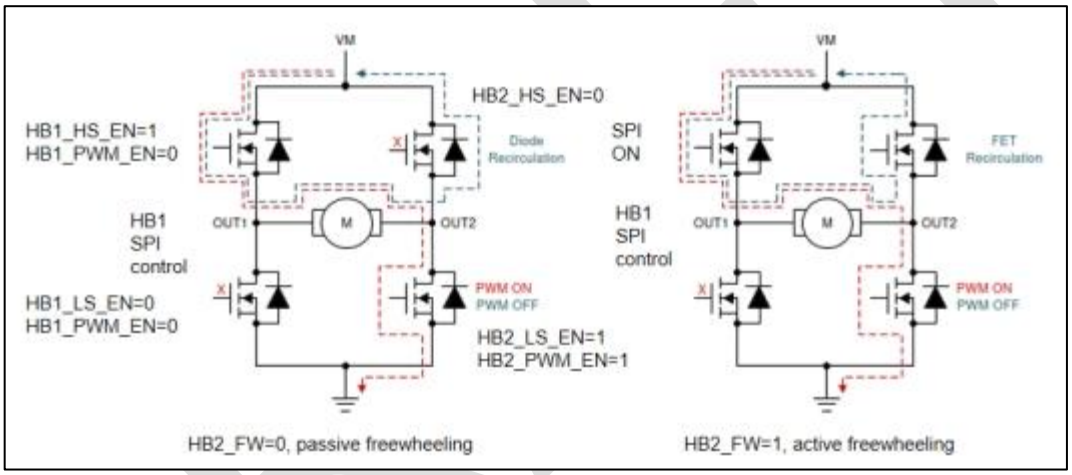


Figure 5. Passive freewheeling vs. active freewheeling

Note:

- Active freewheeling function automatically turns on the freewheeling FET, after the driving FET turns off at PWM ON->OFF and cross protection time t_{DEAD} elapsed

- HBx_FW bit value is not effective when HBx_PWM_EN bit is configured as SPI control ON/OFF

- PWM enable / disable

  (1) PWMx_DIS bit in HB_PWM_CTRL2

  PWM channel independent enable / disable bit

Example of PWM mode control register setting and steps

1. Configure PWMx_DIS bit into '1' (PWM stopped and off) for selected PWM channel
2. Configure active or passive free-wheeling in FW_CTRL register
3. Assign the PWM channel for selected half-bridge output in PWM_MAP_CTRL register
4. Configure the PWM frequency in PWM_FREQ_CTRL register
5. Configure the PWM duty cycle in PWM_DC_CTRL register
6. Assign the channel driven mode SPI on/off or PWM operation by HBx_PWM_EN in HB_PWM_CTRL register

7. Select the channel HS or LS to be driven by HBx_HS_EN or HBx_LS_EN in HB_CTRL register
8. Active and begin the PWM by PWMx_DIS bit to '0

7.4.3. Output in parallel

For SPI ON/OFF control in parallel, it is recommended to select half bridge channel in same register, ie HB1, HB2, HB3, HB4 HS / LS control bit are all in HB_CTRL_1 register, while HB5, HB6 are in HB_CTRL_2.

For PWM control in parallel, to ensure the HS or LS activated simultaneously, it is mandatory to put the PWM activation in the last step for PWM mode control register setting.

7.5. Half bridge protection and diagnosis

7.5.1. Overcurrent protection

The integrated overcurrent protection function provides the half bridge high side against short to ground or half bridge low side against short to battery.

When the current pass the half bridge high side (VM->highside->OUTx) or flow into the half bridge low side (OUTx->low side->GND), once I_{OC} overcurrent threshold is exceeded, an overcurrent deglitch filter t_{OC} starts and internal circuit limits current at I_{LIM}.

Upon the overcurrent condition last until t_{OC} expiration, the particular half bridge (including high side and low side) are disabled. The OC status bit shall report the corresponding HS or LS which trigger OC. nFAULT pin also asserts low if OC_MASK_FLT is set '0'.

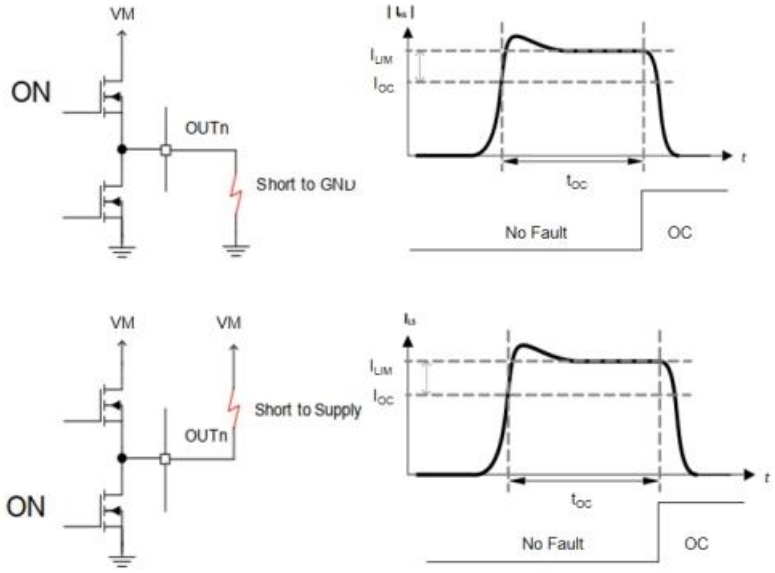
Note:

1. Even the half bridge output is disabled due to overcurrent protection mechanism, the HBx_HS_EN or HBx_LS_EN bit remains previous state, unless user change the value through SPI.
2. When device operate in high voltage up to 36v, short t_{OC} (OC_Filter bit in OPL_OC_CTRL3 register) is suggested.

For example, if only HB1 LS is short to battery and detected, OC_STA_1 register HB1_LS_OC bit is asserted while HB1_HS_OC bit not affected, for output stage, both HB1 HS and LS are disabled.

To resume normal driving, besides the overcurrent condition disappear, it is also required to clear the OC status bit by SPI reading (RD_CLR_EN=1) or writing CLR_FLT bit '1' to trigger clear fault command.

Anyhow if overcurrent condition short than t_{OC} deglitch filter, the OC event is not confirmed and HB driver keeps normal status.



The device also provides two slew rate options in case half bridge output stage turn off caused by OC protection. High slew rate turns off (typ 2.5v/us) used in default for OC as OC_OFF_SR bit in OPL_OC_CTRL_3 is set to '0', while slow slew rate turns off in OC condition (OC_OFF_SR=1) shall be carefully evaluated for device operating ambient condition and power dissipation.

7.5.2. Open load in ON state

The load current is monitored in each activated output stage for open load detection in ON state.

If the load current is below open load detection threshold I_{OL} for at least typ.2ms (t_{OL}), the corresponding open load bit is set in status register.

The device also provide HBx_OPL_TH selection bit for lower open load threshold I_{OL_LOW} and the corresponding filter time t_{OL_LOW}, which targets for low current loads ie. LED.

Furthermore, two bits, OPL_HB_ACT bit and OPL_mask_FLT bit in OPL_OC_CTRL_2 register, can be configured for open load fault reaction.

OPL_HB_ACT bit determines whether half bridge output status is impacted by ON state open load fault. Default value '0' will disable faulty half bridge HS and LS, while setting the bit value to '1' can choose open load only as information flag and half bridge control / operation not impacted.

OPL_mask_FLT bit determines whether nFault output pin status is impacted by ON state open load fault. Default value '0' unmasks and generates nFault low at open load detected, while changing to '1' will mask open load fault and doesn't report on nFault output.

User can clear the OL status bit by SPI reading (RD_CLR_EN=1) or writing CLR_FLT bit '1' to trigger clear fault command to determine whether open load is still present or disappeared.

Note:

1. For DC motor application, it is recommended to use SPI ON/OFF short activation of outputs (e.g. 3ms) to test DC motor open load status without changing the mechanical state of motor.

2. For LED load application, PWM control might be used, the lower open load threshold and shorter filter shall be chosen. During PWM OFF/freewheeling state, open load detection is blanked.

Each half bridge ON state open load detection can be disabled by HBx_OPL_DIS bit in OPL_CTRL_1/2 register, in case ON state open load not required.

7.5.3. OFF-state diagnosis

Each half bridge OUTx integrates internal pull up current / pull down current and comparator for off-state diagnosis.

Pull up current or pull down current are individually controlled as enable / disable by register OPL_CTRL_5 and OPL_CTRL_6 bit setting values.

The OUTx pin voltage is compared with VSTA_HB to determine its off-state logic status (HIGH or LOW) in real time and reported in HB_STA1 register.

Note:

Half bridge/H-bridge application connection is different with HS or LS usage. It is suggested to follow the following off-state diagnosis step including the pull up / down current enable/disable and OUTx status judgement through microcontroller.

7.5.4. Overtemperature

To protect power stage from overheat, dedicated thermal sensor is placed close to each half bridge power stage, if the temperature increases above the OTwarn, a temperature warning flag is set in SPI STA_0 register, half bridge output operation is not impacted. Once the sensed temperature over the second OT_{SD} threshold, the corresponding OTSD flag is set and power MOSFET channel is automatically disabled.

nFAULT pin can be configured for OTwarn event report upon OTW_MASK_FLT bit setting. Anyhow OTSD will always asserted nFAULT to low.

OTwarn and OTSD flag bit are latched. In order to reactive the output stage after OTSD and release nFAULT pin, the temperature drops below T_{SD}-$T_{HYS,}$ and the thermal shutdown OTSD bit shall be clear by SPI command.

7.5.5. Fault Protection Summary

EVENT	VM			VDD	EN	Thermal		Load current		
	OV1 t>tov	OV2 t>tov	UV	UV	H->L	OVER TEMPERATURE Warning	OVER TEMPERATURE shutdon	OC	OL in ON	
	SPI CTRL_0 register OVP_H bit					OTW_MASK_FLT		OC_MASK_FLT	OPL_HB_ACT OPL_mask_FLT	
FLAG READ BY SPI	VM_OV	VM_OV	VM_UV	NPOR		OTWARN	OTSD	HBx_HS_OC HBx_LS_OC	HBx_HS_OPL HBx_LS_OPL	
Internal supply	○	○	○	▲	▲	○	○	○	○	
Internal OSC	○	○	○	▲	▲	○	○	○	○	
Charge pump	○	○	▲	▲	▲	○	○	○	○	
OUT1~OUT12	▲	▲	▲	▲	▲	○	▲	▲*1	▲*2 *1	
nFault	△	△	△	-	-	△*3	△	△*4	△*5	
SPI communication	○	○	○	▲	▲	○	○	○	○	
SPI REGISTERS	○	○	○	▲	▲	○	○	○	○	

x	detection	*1	The fault output off state, caused by OC or OL in ON, is latched until the corresponding retart condition is met.
○	normal operation	*2	On state open load switch off the corresponding HB channel both HS and LS output, if OPL_HB_ACT bit =0.
-	not active	*3	OTW_MASK_FLT =1 means that overtemperature warning triggers nFAULT low
●	partial functionality	*4	OC_MASK_FLT =0 unmasks and report on nFAULT if OC happens
▲	stop/reset	*5	OPL_mask_FLT=0 unmasks and report on nFAULT if Open load on state detected
△	active LOW		

7.6. SPI interface

The following table summarizes the SPI interface designed.

Table 55 – SPI Interface quick look

Parameter	Description
Protocol	in frame
Single Frame Length	16 bit, MSB first
Frame protection	frame length check
Max. Frequency	5 MHz
CPOL	0
CPHA	1
Master/Slave onfiguration	Slave

The falling edge of NCS defines the start of the SPI frames. It samples the SDI line at the falling edge of SCK, while the output data is shifted out on SDO line at the rising edge of SCK (CPOL='0' CPHA = '1'). The end of SPI frame is defined by a rising edge of NCS.

7.6.1. Frame Length Check

For each command received, the SPI peripheral checks the number of clock edges at SCK pin. If the total number of edges is not a multiple of 16, the frame content is discarded and an SPI_ERR bit will be returned upon next iteration.

7.6.2. Error Frame

In case one of the following error occurs, the SPI_ERR diagnosis bit will be returned upon next communication iteration:

- Frame Length error
- Invalid address

7.6.3. SPI Frame structure

Each SDI input frame has 16 bits with the following structure:

- 2 operation command bit C1 / C0 '00' for write operation, '01' for read operation
- 6 ADDRESS bits
- 8 DATA bits

	MSB								LSB
BIT	15	14	13	12	11	10	9	8	[7:0]
SDI	C1	C0	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	DATA

Register frame SDO responses the selected address and register content bit values. It has with the following structure:

- 2bit '1' , reserved
- 6bits, UV event / OV event , Overtemperature, NPOR and power stage status OC, OL
- 8 DATA bits

	MSB								LSB
BIT	15	14	13	12	11	10	9	8	[7:0]
SDO	1	1	OT	OL	OC	UV	OV	NPOR	DATA

Note:

For SPI write operation, the SDO response data is the value which is currently written to.

For SPI read operation, the SDO response data is the value which register address has been read.

7.6.4. Parallel and daisy chain capability

SPI communication between microcontroller (SPI master) and multiple these devices (slave) can be operated in parallel or in daisy chain.

Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and

SCK, but every slave connects dedicated own NCS.

Daisy chain operation: multi devices are connected with shared one NCS and SCK, while each device SDI and SDO are daisy-chain connected.

7.6.5. Registers map

SECT	REG_NAME	REG_ ADDR	bits							
			D7	D6	D5	D4	D3	D2	D1	D0
Status registers	STA_0	0x00	Reserved	OTSD	OTWARN	OPL	OC	VM_UV	VM_OV	NPOR
	OC_STA_1	0x01	HB4_HS_OC	HB4_LS_OC	HB3_HS_OC	HB3_LS_OC	HB2_HS_OC	HB2_LS_OC	HB1_HS_OC	HB1_LS_OC
	OC_STA_2	0x02	Reversed				HB6_HS_OC	HB6_LS_OC	HB5_HS_OC	HB5_LS_OC
	OPL_STA_1	0x04	HB4_HS_OPL	HB4_LS_OPL	HB3_HS_OPL	HB3_LS_OPL	HB2_HS_OPL	HB2_LS_OPL	HB1_HS_OPL	HB1_LS_OPL
	OPL_STA_2	0x05	Reversed				HB6_HS_OPL	HB6_LS_OPL	HB5_HS_OPL	HB5_LS_OPL
	HB_STA_1	0x2B	Reversed		HB6_STA	HB5_STA	HB4_STA	HB3_STA	HB2_STA	HB1_STA
Control registers	GEN_CTRL_0	0x07	OFF_DIAG_COMP_EN	DEVICE_ID			OC_MASK_FLT	OTW_NMASK_FLT	OVP_H	DIAG_CLR
	HB_CTRL_1	0x08	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
	HB_CTRL_2	0x09	Reversed				HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
	HB_PWM_CTRL1	0x0B	Reversed		HB6_PWM_EN	HB5_PWM_EN	HB4_PWM_EN	HB3_PWM_EN	HB2_PWM_EN	HB1_PWM_EN
	HB_PWM_CTRL2	0x0C	PWM8_DIS	PWM7_DIS	PWM6_DIS	PWM5_DIS	PWM4_DIS	PWM3_DIS	PWM2_DIS	PWM1_DIS
	FW_CTRL_1	0x0D	Reversed		HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW
	PWM_MAP_CTRL_1	0x0F	Reserved	Reserved	HB2_PWM_MAP			HB1_PWM_MAP		
	PWM_MAP_CTRL_2	0x10	Reserved	Reserved	HB4_PWM_MAP			HB3_PWM_MAP		
	PWM_MAP_CTRL_3	0x11	Reserved	Reserved	HB6_PWM_MAP			HB5_PWM_MAP		
	PWM_FREQ_CTRL1	0x13	PWM4_FREQ		PWM3_FREQ		PWM2_FREQ		PWM1_FREQ	
	PWM_FREQ_CTRL2	0x14	PWM8_FREQ		PWM7_FREQ		PWM6_FREQ		PWM5_FREQ	
	PWM_DC_CTRL1	0x15	PWM1_DUTY_CYCLE							
	PWM_DC_CTRL2	0x16	PWM2_DUTY_CYCLE							
	PWM_DC_CTRL3	0x17	PWM3_DUTY_CYCLE							
	PWM_DC_CTRL4	0x18	PWM4_DUTY_CYCLE							
	PWM_DC_CTRL5	0x19	PWM5_DUTY_CYCLE							
	PWM_DC_CTRL6	0x1A	PWM6_DUTY_CYCLE							

	PWM_DC_CTRL7	0x1B	PWM7_DUTY_CYCLE						
	PWM_DC_CTRL8	0x1C	PWM8_DUTY_CYCLE						
	HB_SR_CTRL_1	0x1D	Reversed		HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
	HB_SR_CTRL_2	0x1E	Reversed							
	OPL_CTRL_1	0x1F	Reversed		HB6_OPL_DIS	HB5_OPL_DIS	HB4_OPL_DIS	HB3_OPL_DIS	HB2_OPL_DIS	HB1_OPL_DIS
	OPL_OC_CTRL_2	0x20	OPL_mask_FLT	OPL_HB_ACT	Reserved	OC_OFF_SR	reversed			
	OPL_OC_CTRL_3	0x21	OC_FILTER			Reserved	reversed			
	OPL_CTRL_4	0x22	Reversed		HB6_OPL_TH	HB5_OPL_TH	HB4_OPL_TH	HB3_OPL_TH	HB2_OPL_TH	HB1_OPL_TH
	OPL_CTRL_5	0x23	Reversed							
	OPL_CTRL_6	0x24	Reversed							
	GEN_CTRL_1	0x25	SS_MOD		SS_DEV	RD_CLR_EN	unlock	SPI_ERR	Device_VER	
	OPL_CTRL_5	0x28	HB4_OFF_PU_EN	HB4_OFF_PD_EN	HB3_OFF_PU_EN	HB3_OFF_PD_EN	HB2_OFF_PU_EN	HB2_OFF_PD_EN	HB1_OFF_PU_EN	HB1_OFF_PD_EN
	OPL_CTRL_6	0x29	Reversed				HB6_OFF_PU_EN	HB6_OFF_PD_EN	HB5_OFF_PU_EN	HB5_OFF_PD_EN
	OPL_CTRL_8	0x2D	Reversed		HB6_IPUPD_MODE	HB5_IPUPD_MODE	HB4_IPUPD_MODE	HB3_IPUPD_MODE	HB2_IPUPD_MODE	HB1_IPUPD_MODE
	OPL_CTRL_9	0x2E	OCPH_CONF	VM_OVPH_CONF	IDCH_CONF	TDEAD_MON_EN	Reversed			

Register Name	Address	Field Name	Type	Bit Offset	Bit Width	Reset Value	Description
STA_0	0x0						
		Reserved	RO	7	1	0x0	0: reversed (default value).
		OTSD	RLR	6	1	0x0	0: No over temperature shutdown happen (default value) 1: over temperature shutdown detected. Error latched and all outputs disabled.
		OTWARN	RLR	5	1	0x0	0: No over temperature warning happen (default value) 1: over temperature warning detected.
		OPL	RO	4	1	0x0	0: No open load detected (default value) 1: open load detected in at least one of power stages.
		OC	RO	3	1	0x0	0: No overcurrent detected (default value) 1: overcurrent detected in at least one of power stages. Error latched and corresponding outputs disabled.
		VM_UV	RLR	2	1	0x0	0: No VM undervoltage detected (default value) 1: VM undervoltage detected. Error latched and all outputs disabled.
		VM_OV	RLR	1	1	0x0	0: No VM overvoltage detected (default value) 1: VM overvoltage detected. Error latched and all outputs disabled.
		NPOR	RLR	0	1	0x0	0: POR due to VDD supply or EN (default value) 1: No POR
OC_STA_1	0x1						
		HB4_HS_OC	RLR	7	1	0x0	0: No overcurrent in HB4 high side detected (default value) 1: overcurrent detected in HB4 high side. Error latched, HB4 HS is disabled.
		HB4_LS_OC	RLR	6	1	0x0	0: No overcurrent in HB4 low side detected (default value) 1: overcurrent detected in HB4 low side. Error latched, HB4 LS is disabled.
		HB3_HS_OC	RLR	5	1	0x0	0: No overcurrent in HB3 high side detected (default value) 1: overcurrent detected in HB3 high side. Error latched, HB3 HS is disabled.
		HB3_LS_OC	RLR	4	1	0x0	0: No overcurrent in HB3 low side detected (default value) 1: overcurrent detected in HB3 low side. Error latched, HB3 LS is disabled.
		HB2_HS_OC	RLR	3	1	0x0	0: No overcurrent in HB2 high side detected (default value) 1: overcurrent detected in HB2 high side. Error latched, HB2 HS is disabled.
		HB2_LS_OC	RLR	2	1	0x0	0: No overcurrent in HB2 low side detected (default value) 1: overcurrent detected in HB2 low side. Error latched, HB2 LS is disabled.
		HB1_HS_OC	RLR	1	1	0x0	0: No overcurrent in HB1 high side detected (default value) 1: overcurrent detected in HB1 high side. Error latched, HB1 HS is disabled.

		HB1_LS_OC	RLR	0	1	0x0	0: No overcurrent in HB1 low side detected (default value) 1: overcurrent detected in HB1 low side . Error latched, HB1 LS is disabled.
OC_STA_2	0x2						
		Reserved	RO	7	1	0x0	0: reversed (default value).
		Reserved	RO	6	1	0x0	0: reversed (default value).
		Reserved	RO	5	1	0x0	0: reversed (default value).
		Reserved	RO	4	1	0x0	0: reversed (default value).
		HB6_HS_OC	RLR	3	1	0x0	0: No overcurrent in HB6 high side detected (default value) 1: overcurrent detected in HB6 high side . Error latched, HB6 HS is disabled.
		HB6_LS_OC	RLR	2	1	0x0	0: No overcurrent in HB6 low side detected (default value) 1: overcurrent detected in HB6 low side . Error latched, HB6 LS is disabled.
		HB5_HS_OC	RLR	1	1	0x0	0: No overcurrent in HB5 high side detected (default value) 1: overcurrent detected in HB5 high side . Error latched, HB5 HS is disabled.
		HB5_LS_OC	RLR	0	1	0x0	0: No overcurrent in HB5 low side detected (default value) 1: overcurrent detected in HB5 low side . Error latched, HB5 LS is disabled.
OPL_STA_1	0x4						
		HB4_HS_OPL	RLR	7	1	0x0	0: No open load in HB4 high side detected (default value) 1: open load detected in HB4 high side . Error latched
		HB4_LS_OPL	RLR	6	1	0x0	0: No open load in HB4 low side detected (default value) 1: open load detected in HB4 low side . Error latched
		HB3_HS_OPL	RLR	5	1	0x0	0: No open load in HB3 high side detected (default value) 1: open load detected in HB3 high side . Error latched
		HB3_LS_OPL	RLR	4	1	0x0	0: No open load in HB3 low side detected (default value) 1: open load detected in HB3 low side . Error latched
		HB2_HS_OPL	RLR	3	1	0x0	0: No open load in HB2 high side detected (default value) 1: open load detected in HB2 high side . Error latched
		HB2_LS_OPL	RLR	2	1	0x0	0: No open load in HB2 low side detected (default value) 1: open load detected in HB2 low side . Error latched
		HB1_HS_OPL	RLR	1	1	0x0	0: No open load in HB1 high side detected (default value) 1: open load detected in HB1 high side . Error latched
		HB1_LS_OPL	RLR	0	1	0x0	0: No open load in HB1 low side detected (default value) 1: open load detected in HB1 low side . Error latched

OPL_STA_2	0x5						
		Reserved	RO	7	1	0x0	0: reversed (default value).
		Reserved	RO	6	1	0x0	0: reversed (default value).
		Reserved	RO	5	1	0x0	0: reversed (default value).
		Reserved	RO	4	1	0x0	0: reversed (default value).
		HB6_HS_OPL	RLR	3	1	0x0	0: No open load in HB6 high side detected (default value) 1: open load detected in HB6 high side . Error latched
		HB6_LS_OPL	RLR	2	1	0x0	0: No open load in HB6 low side detected (default value) 1: open load detected in HB6 low side . Error latched
		HB5_HS_OPL	RLR	1	1	0x0	0: No open load in HB5 high side detected (default value) 1: open load detected in HB5 high side . Error latched
		HB5_LS_OPL	RLR	0	1	0x0	0: No open load in HB5 low side detected (default value) 1: open load detected in HB5 low side . Error latched
HB_STA_1	0x2B						
		Reserved	RO	7	1	0x0	0: reversed (default value).
		Reserved	RO	6	1	0x0	0: reversed (default value).
		HB6_STA	RO	5	1	0x0	0: HB6 output voltage status low (<Vth) 1: HB6 output voltage status high(>Vth)
		HB5_STA	RO	4	1	0x0	0: HB5 output voltage status low (<Vth) 1: HB5 output voltage status high(>Vth)
		HB4_STA	RO	3	1	0x0	0: HB4 output voltage status low (<Vth) 1: HB4 output voltage status high(>Vth)
		HB3_STA	RO	2	1	0x0	0: HB3 output voltage status low (<Vth) 1: HB3 output voltage status high(>Vth)
		HB2_STA	RO	1	1	0x0	0: HB2 output voltage status low (<Vth) 1: HB2 output voltage status high(>Vth)
		HB1_STA	RO	0	1	0x0	0: HB1 output voltage status low (<Vth) 1: HB1 output voltage status high(>Vth)
GEN_CTRL_0	0x7						
		OFF_DIAG_COMP_EN	RW	7	1	0x0	0: all half bridge OFF state diagnosis comparators are disabled, comparator output keeps default value 0 1: all half bridge OFF state diagnosis comparators are enabled
		DEVICE_ID	RO	4	3	by products	100 = NSD8306 101 = NSD8306 110 = NSD8310 111 = NSD8312 others reversed

		OC_MASK_FLT	RW	3	1	0x0	0: overcurrent unmasked, reported on nfault, (default value) 1: overcurrent event is masked, not reported on nfault
		OTW_NMASK_FLT	RW	2	1	0x0	0: overtemperature warning masked, not reported on nfault (default value) 1: overtemperature warning unmasked, reported on nfault
		OVP_H	RW	1	1	0x0	0: VM overvoltage voltage threshold at 21v (default value) 1: Higher overvoltage protection threshold, VM up to 36v
		DIAG_CLR	WO	0	1	0x0	0: no action - clear all fault (default value) 1: Trigger action - clear all fault
HB_CTRL_1	0x8						
		HB4_HS_EN	RW	7	1	0x0	0: HB4 high side disabled (default value) 1: HB4 high side enabled
		HB4_LS_EN	RW	6	1	0x0	0: HB4 low side disabled (default value) 1: HB4 low side enabled
		HB3_HS_EN	RW	5	1	0x0	0: HB3 high side disabled (default value) 1: HB3 high side enabled
		HB3_LS_EN	RW	4	1	0x0	0: HB3 low side disabled (default value) 1: HB3 low side enabled
		HB2_HS_EN	RW	3	1	0x0	0: HB2 high side disabled (default value) 1: HB2 high side enabled
		HB2_LS_EN	RW	2	1	0x0	0: HB2 low side disabled (default value) 1: HB2 low side enabled
		HB1_HS_EN	RW	1	1	0x0	0: HB1 high side disabled (default value) 1: HB1 high side enabled
		HB1_LS_EN	RW	0	1	0x0	0: HB1 low side disabled (default value) 1: HB1 low side enabled
HB_CTRL_2	0x9						
		Reserved	RW	7	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	6	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	5	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	4	1	0x0	0: reversed (default value). 1: not allowed
		HB6_HS_EN	RW	3	1	0x0	0: HB6 high side disabled (default value) 1: HB6 high side enabled
		HB6_LS_EN	RW	2	1	0x0	0: HB6 low side disabled (default value) 1: HB6 low side enabled
		HB5_HS_EN	RW	1	1	0x0	0: HB5 high side disabled (default value) 1: HB5 high side enabled

		HB5_LS_EN	RW	0	1	0x0	0: HB5 low side disabled (default value) 1: HB5 low side enabled
HB_PWM_CTRL1	0xB						
		Reserved	RW	7	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	6	1	0x0	0: reversed (default value). 1: not allowed
		HB6_PWM_EN	RW	5	1	0x0	0: HB6 operate in SPI ON/OFF mode (default value) 1: HB6 operate in PWM mode
		HB5_PWM_EN	RW	4	1	0x0	0: HB5 operate in SPI ON/OFF mode (default value) 1: HB5 operate in PWM mode
		HB4_PWM_EN	RW	3	1	0x0	0: HB4 operate in SPI ON/OFF mode (default value) 1: HB4 operate in PWM mode
		HB3_PWM_EN	RW	2	1	0x0	0: HB3 operate in SPI ON/OFF mode (default value) 1: HB3 operate in PWM mode
		HB2_PWM_EN	RW	1	1	0x0	0: HB2 operate in SPI ON/OFF mode (default value) 1: HB2 operate in PWM mode
		HB1_PWM_EN	RW	0	1	0x0	0: HB1 operate in SPI ON/OFF mode (default value) 1: HB1 operate in PWM mode
HB_PWM_CTRL2	0xC						
		PWM8_DIS	RW	7	1	0x0	0: PWM8 enable (default value) 1: PWM8 disable
		PWM7_DIS	RW	6	1	0x0	0: PWM7 enable (default value) 1: PWM7 disable
		PWM6_DIS	RW	5	1	0x0	0: PWM6 enable (default value) 1: PWM6 disable
		PWM5_DIS	RW	4	1	0x0	0: PWM5 enable (default value) 1: PWM5 disable
		PWM4_DIS	RW	3	1	0x0	0: PWM4 enable (default value) 1: PWM4 disable
		PWM3_DIS	RW	2	1	0x0	0: PWM3 enable (default value) 1: PWM3 disable
		PWM2_DIS	RW	1	1	0x0	0: PWM2 enable (default value) 1: PWM2 disable
		PWM1_DIS	RW	0	1	0x0	0: PWM1 enable (default value) 1: PWM1 disable
FW_CTRL_1	0xD						
		Reserved	RW	7	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	6	1	0x0	0: reversed (default value). 1: not allowed

		HB6_FW	RW	5	1	0x0	0: HB6 operate in passive free-wheeling (default value) 1: HB6 operate in active free-wheeling
		HB5_FW	RW	4	1	0x0	0: HB5 operate in passive free-wheeling (default value) 1: HB5 operate in active free-wheeling
		HB4_FW	RW	3	1	0x0	0: HB4 operate in passive free-wheeling (default value) 1: HB4 operate in active free-wheeling
		HB3_FW	RW	2	1	0x0	0: HB3 operate in passive free-wheeling (default value) 1: HB3 operate in active free-wheeling
		HB2_FW	RW	1	1	0x0	0: HB2 operate in passive free-wheeling (default value) 1: HB2 operate in active free-wheeling
		HB1_FW	RW	0	1	0x0	0: HB1 operate in passive free-wheeling (default value) 1: HB1 operate in active free-wheeling
PWM_MAP_CTRL_1	0xF						
		Reserved	RW	7	1	0x0	Reserved
		Reserved	RW	6	1	0x0	Reserved
		HB2_PWM_MAP	RW	3	3	0x0	HB2 PWM MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
		HB1_PWM_MAP	RW	0	3	0x0	HB1 PWM MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
PWM_MAP_CTRL_2	0x10						
		Reserved	RW	6	2	0x00	00: reserved
		HB4_PWM_MAP	RW	3	3	0x0	HB4 PWM MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8

		HB3_PWM_MAP	RW	0	3	0x0	HB3 PWM MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
PWM_MAP_CTRL_3	0x11						
		Reserved	RW	7	1	0x0	Reserved
		Reserved	RW	6	1	0x0	Reserved
		HB6_PWM_MAP	RW	3	3	0x0	HB6 PWM MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
		HB5_PWM_MAP	RW	0	3	0x0	HB5 PWM MAP configuration 000: PWM1 (default value) 001: PWM2 010: PWM3 011: PWM4 100: PWM5 101: PWM6 110: PWM7 111: PWM8
PWM_FREQ_CTRL1	0x13						
		PWM4_FREQ	RW	6	2	0x0	PWM4 frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
		PWM3_FREQ	RW	4	2	0x0	PWM3 frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
		PWM2_FREQ	RW	2	2	0x0	PWM2 frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz

		PWM1_FREQ	RW	0	2	0x0	PWM1 frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
PWM_FREQ_CTRL2	0x14						
		Reserved	RW	7-6	2	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	5-4	2	0x0	0: reversed (default value). 1: not allowed
		PWM6_FREQ	RW	3-2	2	0x0	PWM6 frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
		PWM5_FREQ	RW	1-0	2	0x0	PWM5 frequency configuration 00: 80Hz (default value) 01: 100Hz 10: 200Hz 11: 2kHz
PWM_DC_CTRL1	0x15						
		PWM1_DUTY_CYCLE	RW	0	8	0x0	PWM1 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL2	0x16						
		PWM2_DUTY_CYCLE	RW	0	8	0x0	PWM2 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL3	0x17						
		PWM3_DUTY_CYCLE	RW	0	8	0x0	PWM3 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL4	0x18						
		PWM4_DUTY_CYCLE	RW	0	8	0x0	PWM4 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL5	0x19						
		PWM5_DUTY_CYCLE	RW	0	8	0x0	PWM5 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL6	0x1A						
		PWM6_DUTY_CYCLE	RW	0	8	0x0	PWM6 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL7	0x1B						

		PWM7_DUTY_CYCLE	RW	0	8	0x0	PWM7 duty cycle calculation = 100% * BIT value /255
PWM_DC_CTRL8	0x1C						
		PWM8_DUTY_CYCLE	RW	0	8	0x0	PWM8 duty cycle calculation = 100% * BIT value /255
HB_SR_CTRL_1	0x1D						
		Reserved	RW	7	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	6	1	0x0	0: reversed (default value). 1: not allowed
		HB6_SR	RW	5	1	0x0	0: HB6 power stage output rise / fall slew rate 0.6 V/us 1: HB6 power stage output rise / fall slew rate 2.5 V/us
		HB5_SR	RW	4	1	0x0	0: HB5 power stage output rise / fall slew rate 0.6 V/us 1: HB5 power stage output rise / fall slew rate 2.5 V/us
		HB4_SR	RW	3	1	0x0	0: HB4 power stage output rise / fall slew rate 0.6 V/us 1: HB4 power stage output rise / fall slew rate 2.5 V/us
		HB3_SR	RW	2	1	0x0	0: HB3 power stage output rise / fall slew rate 0.6 V/us 1: HB3 power stage output rise / fall slew rate 2.5 V/us
		HB2_SR	RW	1	1	0x0	0: HB2 power stage output rise / fall slew rate 0.6 V/us 1: HB2 power stage output rise / fall slew rate 2.5 V/us
		HB1_SR	RW	0	1	0x0	0: HB1 power stage output rise / fall slew rate 0.6 V/us 1: HB1 power stage output rise / fall slew rate 2.5 V/us
OPL_CTRL_1	0x1F						
		Reserved	RW	7	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	6	1	0x0	0: reversed (default value). 1: not allowed
		HB6_OPL_DIS	RW	5	1	0x0	0: HB6 active open load enable 1: HB6 active open load disable
		HB5_OPL_DIS	RW	4	1	0x0	0: HB5 active open load enable 1: HB5 active open load disable
		HB4_OPL_DIS	RW	3	1	0x0	0: HB4 active open load enable 1: HB4 active open load disable
		HB3_OPL_DIS	RW	2	1	0x0	0: HB3 active open load enable 1: HB3 active open load disable
		HB2_OPL_DIS	RW	1	1	0x0	0: HB2 active open load enable 1: HB2 active open load disable

		HB1_OPL_DIS	RW	0	1	0x0	0: HB1 active open load enable 1: HB1 active open load disable
OPL_OC_CTRL_2	0x20						
		OPL_mask_FLT	RW	7	1	0x0	0: open load unmasked, reported on nfault, (default value) 1: open load event is masked, not reported on nfault
		OPL_HB_ACT	RW	6	1	0x0	11
		Reserved	RW	5	1	0x0	0: reversed
		OC_OFF_SR	RW	4	1	0x0	0: OCP event fast turn off slew rate (default value) 1: OCP event slow turn off slew rate
		Reserved	RW	3	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	2	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	1	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RW	0	1	0x0	0: reversed (default value). 1: not allowed
OPL_OC_CTRL_3	0x21						
		OC_FILTER	RW	5	3	0x0	OCP deglitch filter timing 000: 10us 001: 5us 010: 2.5us 011: 1us 100: 60us 101: 40us 110: 30us 111: 20us
		Reserved	RW	4	1	0x0	Reserved, '0' shall be used
		Reserved	RO	3	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RO	2	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RO	1	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RO	0	1	0x0	0: reversed (default value). 1: not allowed
OPL_CTRL_4	0x22						
		Reserved	RO	7	1	0x0	0: reversed (default value). 1: not allowed
		Reserved	RO	6	1	0x0	0: reversed (default value). 1: not allowed
		HB6_OPL_TH	RW	5	1	0x0	0: HB6 active open load normal threshold and long open load filter used

							1: HB6 active open load low threshold and short open load filter used
		HB5_OPL_TH	RW	4	1	0x0	0: HB5 active open load normal threshold and long open load filter used 1: HB5 active open load low threshold and short open load filter used
		HB4_OPL_TH	RW	3	1	0x0	0: HB4 active open load normal threshold and long open load filter used 1: HB4 active open load low threshold and short open load filter used
		HB3_OPL_TH	RW	2	1	0x0	0: HB3 active open load normal threshold and long open load filter used 1: HB3 active open load low threshold and short open load filter used
		HB2_OPL_TH	RW	1	1	0x0	0: HB2 active open load normal threshold and long open load filter used 1: HB2 active open load low threshold and short open load filter used
		HB1_OPL_TH	RW	0	1	0x0	0: HB1 active open load normal threshold and long open load filter used 1: HB1 active open load low threshold and short open load filter used
Reversed	0x23						
		Reserved	RW	7	1	0x0	0: reversed
		0	RW	6	1	0x0	0: reversed
		0	RW	5	1	0x0	0: reversed
		0	RW	4	1	0x0	0: reversed
		0	RW	3	1	0x0	0: reversed
		0	RW	2	1	0x0	0: reversed
		0	RW	1	1	0x0	0: reversed
		0	RW	0	1	0x0	0: reversed
Reversed	0x24						
		Reserved	RW	7	1	0x0	0: reversed
		0	RW	6	1	0x0	0: reversed
		0	RW	5	1	0x0	0: reversed
		0	RW	4	1	0x0	0: reversed
		0	RW	3	1	0x0	0: reversed
		0	RW	2	1	0x0	0: reversed
		0	RW	1	1	0x0	0: reversed
		0	RW	0	1	0x0	0: reversed
GEN_CTRL_1	0x25						
		SS_MOD	RW	6	2	0x00	spread spectrum configuration 00: disable spread spectrum 01: modulation freq 15.625 kHz 10: modulation freq 31.25 kHz 11: modulation freq 62.5 kHz
		SS_DEV	RW	5	1	0x0	0: modulation deviation 5% (typ) 1: modulation deviation 10% (typ)

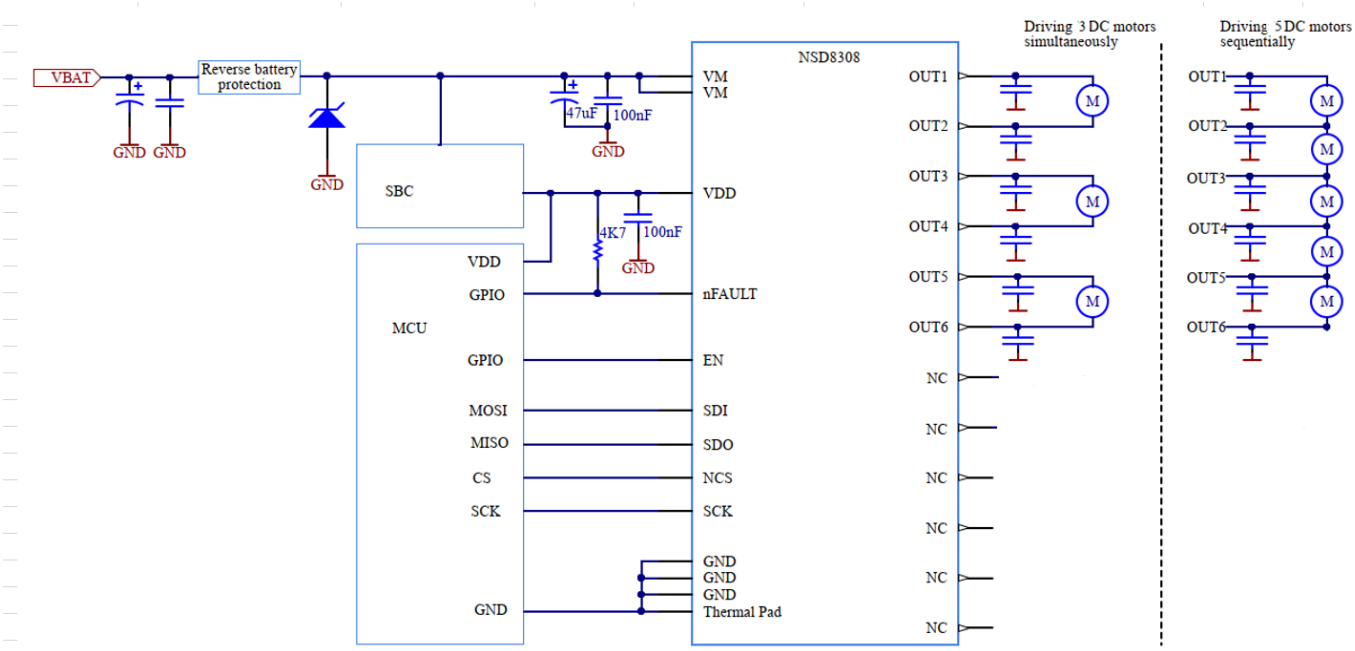
		RD_CLR_EN	RW	4	1	0x0	0: SPI read clear diagnosis flag disable 1: SPI read clear diagnosis flag enable
		unlock	RW	3	1	0x0	0: OPL_CTRL_9 address 0x2E register bit 7~bit4 (OCPH_CONF, VM_OVPH_CONF, IDCH_CONF, TDEAD_MON_EN） 4 bits are in lock， write operation is ignored 1. OPL_CTRL_9 address 0x2E register bit 7~bit4 (OCPH_CONF, VM_OVPH_CONF, IDCH_CONF, TDEAD_MON_EN） 4 bits are unlock， write operation is available.
		SPI_ERR	RLR	2	1	0x0	0: No SPI protocol error is detected (default value). 1: An SPI protocol error is detected.
		Device_VER	RO	0	2	0x01	00: reserved 01: version AA 10: reserved 11: reserved
OPL_CTRL_5	0x28						
		HB4_OFF_PU_EN	RW	7	1	0x0	0: HB4 off state open load pull up current disabled 1: HB4 off state open load pull up current enabled
		HB4_OFF_PD_EN	RW	6	1	0x0	0: HB4 off state open load pull down current disabled 1: HB4 off state open load pull down current enabled
		HB3_OFF_PU_EN	RW	5	1	0x0	0: HB3 off state open load pull up current disabled 1: HB3 off state open load pull up current enabled
		HB3_OFF_PD_EN	RW	4	1	0x0	0: HB3 off state open load pull down current disabled 1: HB3 off state open load pull down current enabled
		HB2_OFF_PU_EN	RW	3	1	0x0	0: HB2 off state open load pull up current disabled 1: HB2 off state open load pull up current enabled
		HB2_OFF_PD_EN	RW	2	1	0x0	0: HB2 off state open load pull down current disabled 1: HB2 off state open load pull down current enabled
		HB1_OFF_PU_EN	RW	1	1	0x0	0: HB1 off state open load pull up current disabled 1: HB1 off state open load pull up current enabled
		HB1_OFF_PD_EN	RW	0	1	0x0	0: HB1 off state open load pull down current disabled 1: HB1 off state open load pull down current enabled
OPL_CTRL_6	0x29						
		Reserved	RO	7	1	0x0	0: reversed (default value).
		Reserved	RO	6	1	0x0	0: reversed (default value).
		Reserved	RO	5	1	0x0	0: reversed (default value).
		Reserved	RO	4	1	0x0	0: reversed (default value).
		HB6_OFF_PU_EN	RW	3	1	0x0	0: HB6 off state open load pull up current disabled 1: HB6 off state open load pull up current enabled

		HB6_OFF_PD_EN	RW	2	1	0x0	0: HB6 off state open load pull down current disabled 1: HB6 off state open load pull down current enabled
		HB5_OFF_PU_EN	RW	1	1	0x0	0: HB5 off state open load pull up current disabled 1: HB5 off state open load pull up current enabled
		HB5_OFF_PD_EN	RW	0	1	0x0	0: HB5 off state open load pull down current disabled 1: HB5 off state open load pull down current enabled
OPL_CTRL_8	0x2D						
		Reserved	RO	7	1	0x0	0: reversed (default value).
		Reserved	RO	6	1	0x0	0: reversed (default value).
		HB6_IPUPD_MODE	RW	5	1	0x0	0: HB6 off diag fast charge current disable (low pull up / pull down current) 1: HB6 off diag fast charge current enable
		HB5_IPUPD_MODE	RW	4	1	0x0	0: HB5 off diag fast charge current disable (low pull up / pull down current) 1: HB5 off diag fast charge current enable
		HB4_IPUPD_MODE	RW	3	1	0x0	0: HB4 off diag fast charge current disable (low pull up / pull down current) 1: HB4 off diag fast charge current enable
		HB3_IPUPD_MODE	RW	2	1	0x0	0: HB3 off diag fast charge current disable (low pull up / pull down current) 1: HB3 off diag fast charge current enable
		HB2_IPUPD_MODE	RW	1	1	0x0	0: HB2 off diag fast charge current disable (low pull up / pull down current) 1: HB2 off diag fast charge current enable
		HB1_IPUPD_MODE	RW	0	1	0x0	0: HB1 off diag fast charge current disable (low pull up / pull down current) 1: HB1 off diag fast charge current enable
OPL_CTRL_9	0x2E						
		OCPH_CONF	RW	7	1	0x0	0: OCP threshold typ 1.3A 1: OCP threshold typ 1.7A
		VM_OVPH_CONF	RW	6	1	0x0	0: OVPH threshold typ 31v 1: OVPH threshold typ 37V
		IDCH_CONF	RW	5	1	0x0	configure HS and LS discharge pull down current level 0: pull down current level normal 1: pull down current level high
		TDEAD_MON_EN	RW	4	1	0x1	0: Tdead is determined by internal fixed timing 1: Tdead is determined by internal feedback signal
		Reserved	RO	3	1	0x0	0: reversed (default value).
		Reserved	RO	2	1	0x0	0: reversed (default value).
		Reserved	RO	1	1	0x0	0: reversed (default value).
		Reserved	RO	0	1	0x0	0: reversed (default value).

8. Application information

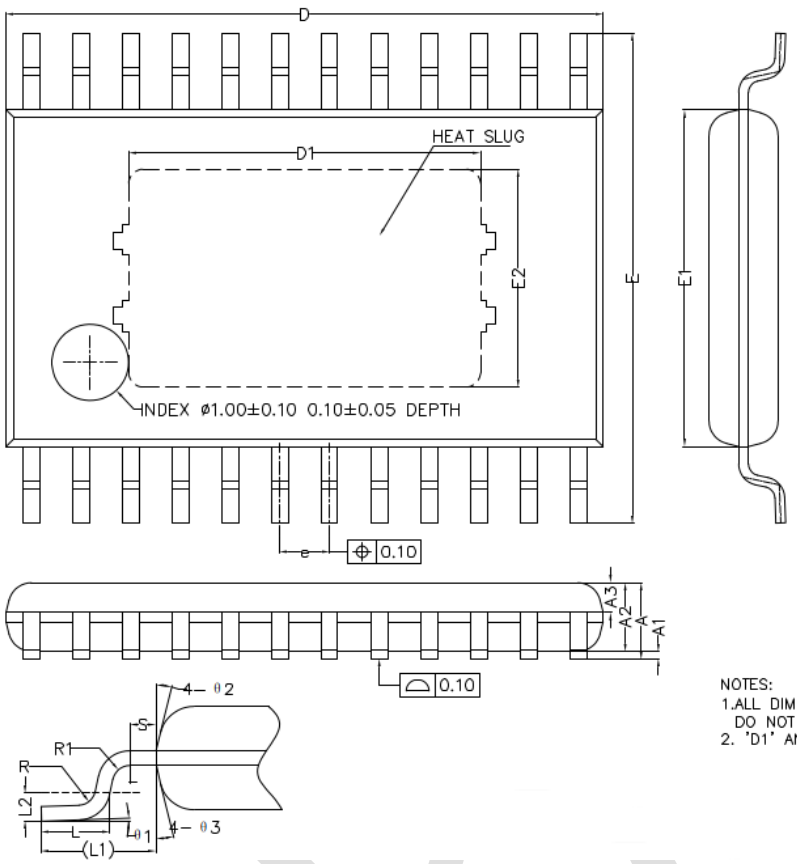
8.1. Application diagram

Figure 4. Typical application connection



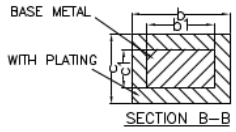
9. Package information

9.1. HTSSOP24 package information



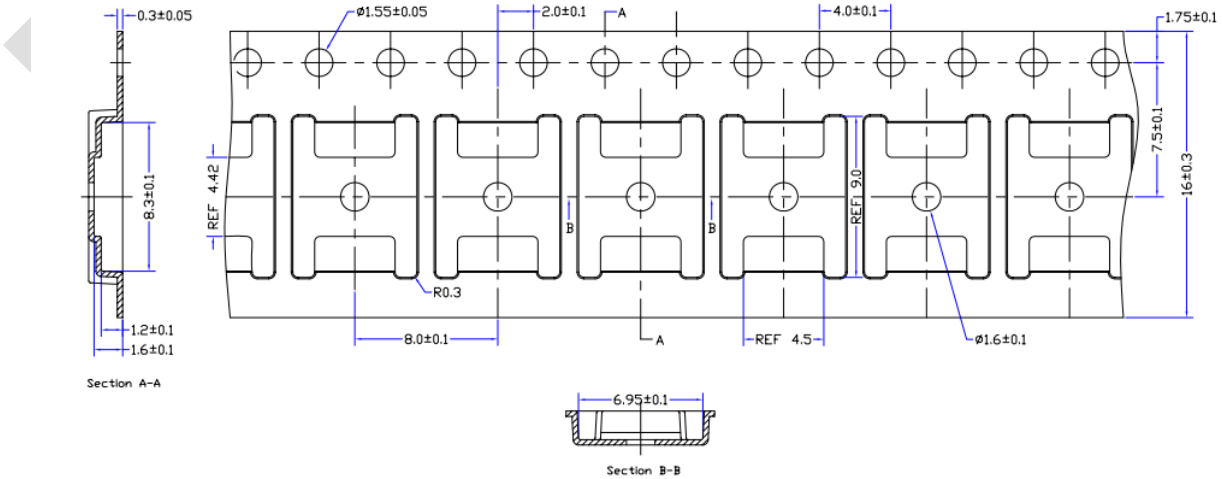
COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	–	–	1.20
A1	0.05	–	0.15
A2	0.80	0.90	1.00
A3	0.34	0.39	0.44
b	0.20	–	0.29
b1	0.19	0.22	0.25
c	0.10	–	0.19
c1	0.10	0.13	0.15
D	7.70	7.80	7.90
D1		4.60REF	
E	6.20	6.40	6.60
E1	4.30	4.40	4.50
E2		2.85REF	
e	0.55	0.65	0.75
L	0.45	0.60	0.75
L1		1.00REF	
L2		0.25BSC	
R	0.09	–	–
R1	0.09	–	–
S	0.20	–	–
θ1	0°	–	8°
θ2	12°	14°	16°
θ3	12°	14°	16°



NOTES:
1.ALL DIMENSIONS REFER TO JEDEC STANDARD MO-153 ADT
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
2. 'D1' AND 'E2' ARE VARIABLES DEPENDING ON DIE PAD SIZES.

9.2. HTSSOP24 packaging information



NOTES:
1.MATERIAL:Black conductive polystyrene
2.ALL DIMS IN MM

10. Revision History

Revision	Description	Date
1.0	Initial version	2021/11/5