



V881 Family

The 4K30 High-Definition AI Vision Processor Datasheet

Key Features

Processor

- Dual-core RISC-V C907, up to 1.4 GHz
 - 16 KB I-cache and 16 KB D-cache per core
 - Supports 128 KB L2 cache
- Single-core RISC-V E907 MCU, up to 800 MHz
- NPU, Supporting 1 TOPS @ INT8, compatible with common CNN operators

Memory & Storage

- Supports SD 3.0 and eMMC 5.1
- 1 x octal DTR mode SPI Flash interface
- 1 x quad SQPI PSRAM interface

Video Engine

- Video decoding
 - JPEG baseline, up to 1920x1080@60fps
- Video encoding
 - H.265 MP@L5.0, up to 3840x2160@35fps
 - H.264 BP/MP/HP@L5.1, up to 3840x2160@30fps
 - JPEG baseline, up to 3840x2160@30fps

Video Input

- 1 x 8/10/12/16-bit Parallel CSI
- 1*4-lane/2*2-lane/3*1-lane MIPI CSI
 - Up to 1.5 Gbit/s per lane
 - Compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.1

Video Output

- One panel interface
 - Parallel RGB interface, up to 1280x800@60fps
 - Serial RGB interface, up to 800 x 480@60fps
 - i8080 interface, up to 800x480@60fps

Audio

- Supports 2 ADCs and 1 DAC

- 2 single-ended audio inputs: MICIN1P, MICIN2P
- 1 single-ended audio output: LINEOUTP
- 1 I2S/PCM interface:
 - Supports up to 16 channels
 - Sampling rate: 8 kHz – 384 kHz
 - Bit width: 8–32 bits

Peripherals Interfaces

- 1 x USB2.0 DRD
- 3 x SPI (supports SPI DSI), 4 x TWI, 4 x UART
- 1 x 10/100 Mbit/s Ethernet port with RMII interface
- 16-ch PWM, 4-ch GPADC (GPADC pad can be used by GPIO)
- SDIO3.0

Security Subsystem

- AES, DES, 3DES, and SM4 encryption and decryption algorithms
- MD5, SHA, and SM3 hash algorithms
- RSA, ECC, SM2 signature and verification algorithms
- 160-bit hardware pseudo random number generator (PRNG) with 175-bit seed
- 256-bit hardware true random number generator (TRNG)
- Integrated 2048-bit eFuse for chip ID and security application

Device Summary

Orderable Device(s)	Package
V881MX-XXX	TFBGA 317 balls 12 mm x 12 mm
V881M3-XXX	QFN 128 pins 12.3 mm x 12.3 mm
V881M2-WB2 V881M3-WB2	TFBGA 194 balls 11.9 mm x 6.9 mm

See Table 2-1 for details.

Revision History

Revision	Date	Author	Description
1.01	August 24, 2026	AWA1896	- Added a new device: V881M2-WB2. - Updated pin names of No.93 and No.5 for QFN 128 pin package.
1.00	May 20, 2026	AWA1896	Table 2-1 Differentiated Features: Updated NPU performance for V881M3-WB2. Section 3.3.1 Image Signal Processor (ISP): Added lens distortion correction and fisheye distortion correction function. Chapter 4 Pin Description: Changed the signal name from “RMII-EPHY-25/50M” to “RMII-EPHY-25M”. Figure 7-2 TFBGA 11.9 mm x 6.9 mm Pin Map: Updated ball names of K11, L2, L10, L11, and M5.
0.90	February 11, 2026	AWA1896	Initial Release Version

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About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the V881 family. For details about register descriptions of each module, see the *V881_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting <https://open.allwinnertech.com/>.

Revision Number Definition

Revision 1.00-1.0x

This document is released based on the verifications in small volume production. The information in this document may be modified, calibrated and supplemented hereafter.

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If you have any questions about the document, please contact us to confirm and obtain the latest version.

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

Test Item	Description
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

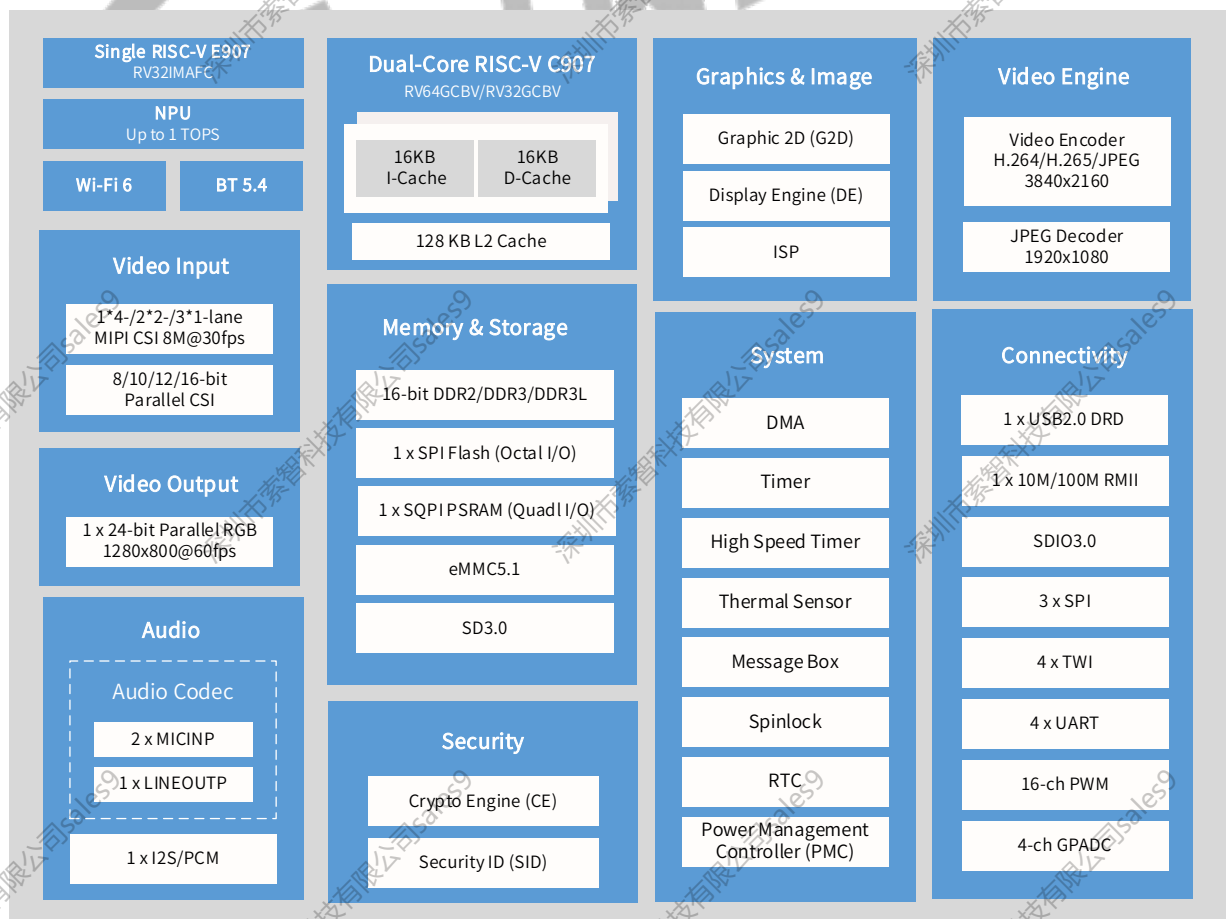
The V881 is a high-performance encoding processor featuring an upgraded AI-ISP imaging unit and an H.264/H.265 encoder capable of processing 8MP high-definition video, with support for real-time input from three cameras.

With enhanced general-purpose and specialized computing power, along with EIS (Electronic Image Stabilization) and focus acceleration, the V881 is ideal for AI live-streaming cameras, handheld devices, drone FPV systems, and a wide range of industrial vision applications.

The V861 has the following highlights:

- Performance Upgrade: Dual-core CPU support, 4K@35fps encoding, and 1 TOPS NPU computing power.
- Picture Quality Upgrade: Next-generation ISP algorithm enhancements with AI-ISP 2.0 enabling around-the-clock AI imaging.
- Interface Upgrade: Supports 3x1-lane/2x2-lane/ 1x4-lane MIPI-CSI video input and RGB888 video output.
- Low-Power Solution: Features low-power sleep/wake-up, Always-On-Video (AOV) support, millisecond-level cold-start sensor imaging, and cold-start display solutions.

Figure 1-1 System Block Diagram



2 Differentiated Features

The following table provides the differences of orderable device(s) covered by this document.

Table 2-1 Differentiated Features

Features	V881MX-XXX	V881M3-XXX	V881M2-WB2	V881M3-WB2
C907	2 x C907, up to 1.4 GHz			
E907	1 x E907, up to 800 MHz			
NPU	Up to 1 TOPS			
H.265 Encoding	Up to 3840x2160@35fps		Up to 3840x2160@30fps	
H.264 Encoding	Up to 3840x2160@30fps		Up to 3840x2160@25fps	
JPEG Encoding	Up to 3840x2160@30fps		Up to 1920x1080@60fps	
Wi-Fi	Supports external Wi-Fi		SIP Wi-Fi	
DDR	External DDR2/DDR3/DDR3L	SIP 128 MB DDR3/DDR3L	SIP 64 MB DDR2	SIP 128 MB DDR3/DDR3L
eMMC	Up to eMMC5.1	Up to eMMC4.41	Up to eMMC5.1	Up to eMMC5.1
SDC	2 x quad-I/O SDC (SDC0/1) 1 x octal-I/O SDC (SDC2)	3 x quad-I/O SDC (SDC0/1/2)	1 x quad-I/O SDC (SDC0) 1 x octal-I/O SDC (SDC2)	1 x quad-I/O SDC (SDC0) 1 x octal-I/O SDC (SDC2)
PWM	16 channels	16 channels	14 channels	14 channels
UART	4 (UART0/1/2/3)	4 (UART0/1/2/3)	2 (UART0/2)	2 (UART0/2)
SPI	3 (SPI0/1/2)	3 (SPI0/1/2)	2 (SPI0/1)	2 (SPI0/1)
SPI Flash	Octal I/O	Quad I/O	Octal I/O	Octal I/O
LCD	1 x 24-bit parallel RGB	1 x 24-bit parallel RGB	1 x 8-bit serial RGB	1 x 8-bit serial RGB
Parallel CSI	1 x 16-bit parallel CSI	1 x 16-bit parallel CSI	Not support	Not support
GPIO	8 groups (PA, PC, PD, PE, PF, PG, PH, PL) Total 113 I/Os	8 groups (PA, PC, PD, PE, PF, PG, PH, PL) Total 94 I/Os	6 groups (PA, PC, PD, PF, PH, PL) Total 61 I/Os	6 groups (PA, PC, PD, PF, PH, PL) Total 61 I/Os

Features	V881MX-XXX	V881M3-XXX	V881M2-WB2	V881M3-WB2
Package	TFBGA 317 balls, 12 mm x 12 mm	QFN 128 pins, 12.3mm x 12.3mm	TFBGA 194 balls, 11.9 mm x 6.9 mm	TFBGA 194 balls, 11.9 mm x 6.9 mm

3 Features

3.1 Processors

- Dual-core RISC-V C907
 - 16 KB I-Cache + 16 KB D- Cache per core
 - Shared 128 KB L2 Cache
 - RV32 and RV64 architectures
 - RV64GCBV + RV32GCBV instruction sets
 - Compatible with RVA22
 - All cores support FPU and DP64 VPU
 - Integrated with 128-bit vector unit and supports RVV1.0
- Single-core RISC-V E907
 - 16 KB I-Cache + 8 KB D- Cache
 - RV32IMAFC instruction set
- NPU: supports 1 TOPS @ INT8, compatible with common CNN operators

3.2 Memory

3.2.1 Internal Memory

- 132KB SRAM C for system boot

3.2.2 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
 - SD Card
 - eMMC
 - SPI NOR Flash (Quad Mode and Single Mode)
 - SPI NAND Flash
- Supports mandatory upgrade process through USB
- Supports BOOT-SEL and eFuse module to select the boot media type
- Supports normal boot and secure boot

3.2.3 SDRAM

- 16-bit DDR2/DDR3/DDR3L interface
- Up to 2 ranks
- Memory capacity up to 2G Bytes

- 16 address lines and three bank address lines per channel
- Clock frequency up to 1056 MHz for DDR3 and DDR3L
- Clock frequency up to 660 MHz for DDR2

3.2.4 SD/MMC Host Controller (SMHC)



NOTE

It is advised that users select different interfaces according to the recommended scenarios; otherwise, performance loss or protocol integrity compromise may occur.

- Three SD/MMC Host Controller (SMHC) interfaces
 - SMHC0 (SDC0) supports up to SD3.0 (recommended) or SDIO3.0
 - SMHC1 (SDC1) supports up to SD3.0 or SDIO3.0(recommended).
 - SMHC2 (SDC2) supports up to SD3.0, SDIO3.0, eMMC5.1(recommended), or MMC4.41
- The SMHC0 and SMHC1 support the following:
 - 1-bit or 4-bit data width
 - Maximum performance:
 - SDR mode 150 MHz@1.8 V IO pad
 - DDR mode 50 MHz@1.8 V IO pad
 - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 supports the following:
 - 1-bit, 4-bit, or 8-bit data width
 - Maximum performance:
 - SDR mode 150 MHz@1.8V IO pad
 - DDR mode 150 MHz@1.8V IO pad
 - SDR mode 50 MHz@3.3V IO pad
 - DDR mode 50 MHz@3.3V IO pad
- For SD/SDIO:
 - SDR104/DDR50 modes for SD3.0/SDIO3.0 require 1.8V IO power supply
 - SD3.0 requires independent power supply and voltage switching between 1.8V and 3.3V in the design solution
 - Supports SDIO interrupts in 1-bit and 4-bit modes
- For eMMC:
 - Supports eMMC boot operation and alternative boot operation
 - Supports eMMC Command Queue
 - Supports HS400 mode and HS200 mode
 - HS200/HS400 mode require 1.8V IO power supply
 - HS400 mode requires a DS signal

3.2.5 SPI Flash Controller (SPIF)

- One SPIF controller
- Supports multiple SPI mode
 - Standard SPI
 - Dual-Output/Dual-Input SPI and Dual I/O SPI
 - Quad-Output/Quad-Input SPI, Quad I/O, and QPI
 - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
 - Programmable serial data frame length: 1 bit to 32 bits
- Supports XIP mode of operation for executing code from FLASH memory
- Supports Single Transfer Rate (STR) mode and Dual Transfer Rate (DTR) mode, and DTR mode supports DQS signal
- High Speed Clock Frequency
 - 150MHz for STR Mode
 - 100MHz for DTR Mode
- Software Write Protection
 - Write protection for all/portion of memory via software
 - Top/Bottom Block protection
- Programmable delay between transactions
- Supports Mode0, Mode1, Mode2 and Mode3
- Supports control signal configuration
 - One chip select to support multiple peripherals
 - Polarity and phase of the Chip Select (SPIF_CS) and SPI Clock (SPIF_CLK) are configurable
- Supports private DMA
 - Supports chain transmission
 - Supports descriptor in 8-word length

3.2.6 SQPI PSRAM Controller

- Supports a maximum frequency of 120MHz
- Supports any frequency ratio between AHB and SPI clocks
- Supports 6 configurable offset address segments
- Supports SPI 1/2/4-wire mode for transmission/reception, and SPI Mode 0/1/2/3
- Supports out-of-order read/write and XIP (eXecute In Place) code execution via CBUS
- Compatible with SQPI PSRAM
- Supports fault protection and interrupt mechanisms
- Enables seamless software switching between SBUS/CBUS access modes

3.3 Image Processing

3.3.1 Image Signal Processor (ISP)

- Supports multiple sensors (up to 4) input
- Supports raw8/10/12
- Maximum resolution:
 - online: 3264x4224
 - offline: 5592x4224
- Performance of one sensor:
 - online: 6M@30fps (linear), 6M@30fps (2f-wdr)
 - offline: 8M@30fps (linear), 8M@30fps (2f-wdr)
- Supports multiple data streams (up to 16) output
 - YUV422/YUV420/RGB888/RGB565 output
 - Graphic mirror and flip
 - 1/64~1x scale down
- Supports ISP tuning tool for the PC (online/offline/remote debugging)
- Supports Algorithm Features:
 - Crop
 - 2F-WDR
 - Dynamic Range Compression (DRC)
 - Local Tone Mapping
 - Local Dynamic Contrast Improvement
 - Black Level Correction
 - Digital Gain
 - White Balance
 - Len Shading Correction (LSC)
 - Lens Distortion Correction
 - Fisheye Distortion Correction
 - Gamma Correction
 - Fix Pattern Noise (FPN)
 - Defect Pixel Correction (DPC)
 - Cross Talk Correction (CTC)
 - Chromatic Aberration Correction (CAC)
 - Noise Reduction (2D/3D)
 - Bayer Interpolation
 - Sharpness
 - Color Enhancement (3D-LUT)
 - Adjustable 3A functions: Automatic White Balance (AWB), Automatic Exposure (AE), and Automatic Focus (AF)

- Anti-flick Detection Statistics
- Histogram Statistics

3.4 Graphics Processing

3.4.1 Display Engine (DE)

- One display output, size up to 1280 x 800@60fps
- Two alpha blending channels
- One overlay layer in video channel, and has an independent scaler.
- Four overlay layers in UI channel and no scaler support
- Supports potter-duff compatible blending operation
- Input format
 - Semi-planar of YUV422/YUV420/YUV411
 - Planar of YUV422/YUV420/ YUV411
 - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Supports Frame Packing/Top-and-Bottom/Side-by-Side Full format data.
- SmartColor2.0 for excellent display experience
 - Hue gain, saturation gain, and value gain controller
 - Fully programmable color matrix
 - Dynamic gamma
- Supports write back for verification

3.4.2 Graphic 2D (G2D)

- Supports mixer layer size up to 2048x2048 pixels, rotate size up to 4096x4096 pixels
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function above
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter, 32-phase 4-tap vertical anti-alias filter.
- Supports window clip
- Supports FillRectangle, BitBlt, StretchBlt and MaskBlt
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate
- Supports 4 Thread RCQ function for mixer and rotate
- Supports dither

3.5 Video Engine

3.5.1 Video Encoding

- H.265 MP@L5.0, up to 3840x2160@35fps
- H.264 BP/MP/HP@L5.1, up to 3840x2160@30fps
- JPEG Baseline Encoding, up to 3840x2160@30fps

3.5.2 JPEG Baseline Decoding

- Supports YUV400/YUV420/YUV411/YUV422/YUV444
- Maximum supported picture size is 8192 x 8192
- Minimum supported picture size is 1x1
- Supports up to 1920x1080@60fps, and 180 million pixels per second.

3.6 Video Input Interfaces

3.6.1 MIPI CSI

- Supports 4-lane, 2+2-lane, or 1+1+1-lane MIPI Interface
 - MIPI CSI2 V1.1
 - MIPI DPHY V1.1
 - Up to 1.5 Gbit/s per lane
- Three MIPI PHYs
 - MIPI PHY A: 2 data lanes (lane 0/1) + 1 clock lane
 - MIPI PHY B: 2 data lanes (lane 0/1) + 1 clock lane
 - MIPI PHY C:
 - Data lane: shared with PHY A's data lane 1
 - Clock lane shared with PHY B's data lane 1
- Pixel formats
 - RAW 8/10/12/14/16 bit
 - YUV422/YUV420 8 bit
 - RGB888 and RGB565

3.6.2 Parallel CSI

- Supports 8/10/12/16-bit width
- Supports BT.656, BT.601, BT.1120, and Digital Camera (DC) protocol
- Supports ITU-R BT.656 up to 4*720P@30fps
- Supports ITU-R BT.1120 up to 4*1080P@30fps
- Supports BT.656 2/4-channel time-multiplexed format
- Dual Data Rate (DDR) sample mode with maximum pixel clock of 148.5MHz

3.7 Video Output Interfaces

3.7.1 LCD

- One panel interface
 - Parallel RGB interface with DE/SYNC RGB mode, up to 1280x800@60fps
 - Serial RGB interface, up to 800 x 480@60fps
 - i8080 interface, up to 800x480@60fps
 - Supports BT.656 interface NTSC and PAL
 - Implements RGB888-equivalent output from lower-bit outputs (RGB565/RGB666) via temporal-spatial dithering algorithm
- Supports outputting pulses to achieve synchronization between sensor and TCON_LCD.

3.8 System Peripherals

3.8.1 Clock Controller Unit (CCU)

- Supports clock configuration and clock generation for most corresponding system modules
- Supports software-controlled clock gating and software-controlled reset for most corresponding modules and buses
- PLL configuration, total 7 PLLs:
 - PLL_CPU
 - PLL_DDR
 - PLL_PERI
 - PLL_VIDEO
 - PLL_CSI
 - PLL_AUDIO
 - PLL_NPU

3.8.2 Power Reset Clock Management (PRCM)

- APBS/AHBS Clock Configuration
- PPU/RTC Clock Configuration
- PPU/RTC Gating and Reset
- PLL LDO Enable
- RAM configuration control
- System NMI interrupt configuration

3.8.3 RTC

- One on-chip 16MHz RC oscillator

- Embedded with a 16-bit day counter, a 5-bit hour counter, a 6-bit minute counter, and a 6-bit second counter
- Uses a 32.867 kHz low-frequency oscillator as the count clock
- 1 kHz counting frequency
- Supports millisecond (ms) counter in RTC
- Configurable initial value by software anytime
- Supports generating interrupt and waking up the external devices with the timing alarms function
- 8 general purpose registers for storing the power-off information in RTC domain
- Supports PMC (Power Management Controller) functionality and external PMU (Power Management Unit) connectivity
 - PWRON key functions: Power-on/wakeup/interrupt
 - VBUS insertion functions: Power-on/wakeup/interrupt
 - Configurable IRQ interrupt pin for power-on/wakeup/interrupt after initial power on
 - Configurable alarm-based power-on/wakeup after initial power on
 - Abnormal power loss detection (VDD-SYS, VCC-IO)
 - Configurable power sequencing with independent MASK control for standby mode power rails
 - PWRON key long-press functions: Force power off/restart/interrupt-only mode
 - Power event record: Tracks power-on/power-off sources
 - Watchdog reset options: restart/global reset only/PAD signal output through RESET pin

3.8.4 Message Box (MSGBOX)

- 2 message boxes for communication between C907 and E907 through one-way channels
- Each MSGBOX has 2 users
 - User is the receiver or transmitter of a message box
 - Each MSGBOX has one receiver (user0) and one transmitter (user1)
 - For E907_MSGBOX, user 0 is E907 and user 1 is C907
 - For C907_MSGBOX, user 0 is C907 and user1 is E907.
- Configurable number of channels and maximum 4 channels
- The FIFO depth of a channel is 8
- The FIFO width of a channel is 32 bits
- Supports interrupts

3.8.5 Spinlock

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable

3.8.6 Thermal Sensor Controller (THS)

- Three thermal sensors
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Supports $\pm 5^{\circ}\text{C}$ error limit from -40°C to 60°C , and $\pm 3^{\circ}\text{C}$ from 60°C to 125°C

3.8.7 Timer

- Two timers
 - Alternative count clock: SYS 32k or HOSC. The SYS 32k can be either the internal or external low-frequency clock, and the external one has more accuracy.
 - Supports 8 prescale factors
 - Programmable 32-bit down timer
 - Supports two timing modes: periodic mode and single counting mode
 - Generates an interrupt when the count is decreased to 0
- Supports AVS
 - Single clock source: HOSC
 - Programmable 33-bit up timer
 - Supports updating the initial value anytime
 - 12-bit frequency divider factor
 - Supports Pause/Start function

3.8.8 High Speed Timer (HSTimer)

- Single clock source: AHB with normal working frequency of 192 MHz and could provide clocks with higher accuracy
- Supports 7 prescale factors
- Configurable 56-bit down timer
- Supports 2 timing modes: periodic mode and one-shot mode
- Supports the test mode
- Generates an interrupt when the count is decreased to 0

3.8.9 Watchdog Timer (WDT)

- Two watchdogs: C907_WDT and E907_WDT
- Clock sources: CLK32K_HOSC and CLK32K
- Two modes available
 - Generates interrupt only
 - Reset system
- 15 configurable initial count value
- Generates timeout interrupts

- Generates reset signals
- Supports restarting the timing

3.9 Audio

3.9.1 Audio codec

- One audio digital-to-analog (DAC) channel
 - SNR 95dB $\pm$ 3dB, THD+N -85 $\pm$ 3dB
 - Output amplitude $\geq$ 0.54Vrms, Crosstalk $\leq$ -75 $\pm$ 3dB
 - Supports 16-bit and 20-bit sample resolution
 - Supports DAC sample rates from 8kHz to 192kHz
- Two audio analog-to-digital (ADC) channels
 - SNR 95dB $\pm$ 3dB, THD+N -80 $\pm$ 3dB
 - Input amplitude $\geq$ 880mFS@3.2Vpp input
 - Supports 16-bit and 20-bit sample resolution
 - Supports ADC sample rates from 8kHz to 48kHz
- Two audio inputs:
 - Two single-ended microphone inputs (MICIN1P/MICIN2P)
- One analog audio output:
 - One single-ended line-out output (LINEOUTP)
- Supports Dynamic Range Controller for adjusting DAC playback and ADC capture
- One 128x20-bit transmit FIFO for DAC and one 128x20-bit receive FIFO for ADC
- Programmable FIFO thresholds
- Supports DMA and interrupts

3.9.2 I2S/PCM

- 1x I2S/PCM (I2S0)
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
 - Left-justified, Right-justified, PCM mode, and TDM format
 - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and receive data FIFOs
 - Programmable FIFO thresholds
 - 128 x 32-bit TXFIFO, 64 x 32-bit RXFIFO
- Supports multiple function clocks
 - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and peripheral I2S/PCM satisfy timing parameters)
 - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode (Only if the IO PAD and peripheral I2S/PCM satisfy timing parameters)

- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
 - Up to 16 channels ($f_s = 48 \text{ kHz}$) which has adjustable width from 8 bits to 32 bits
 - Sample rate from 8 kHz to 384 kHz ($\text{sample rate} * \text{channel} * \text{slot width} \leq 24.576 \text{ MHz}$)
 - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

3.10 Peripheral Interfaces

3.10.1 GPIO

- 8 groups of ports (PA, PC, PD, PE, PF, PG, PH, PL)
- Software control for each signal pin
- Each GPIO peripheral can produce an interrupt
- Pull-up/Pull-down/no-Pull register control
- Control the direction of every signal
- 4 drive strengths in each operating mode
- Up to 113 interrupts
- Configurable interrupt mode: positive edge/ negative edge/ high level /low level/ double edge(positive/negative)
- Interrupt sampling clock:
 - Supports 32kHz and 24MHz
 - Configurable divider ratios: 1/2/4/8/16/32/64/128

3.10.2 USB2.0 DRD

- Compatible with USB2.0 Specification
- Supports USB Host Function
 - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
 - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
 - Supports High-Speed (HS, 480 Mbit/s)
 - Supports Full-Speed (FS, 12 Mbit/s)
 - Supports Low-Speed (LS, 1.5 Mbit/s)
 - Supports only 1 USB Root Port shared between EHCI and OHCI
- Supports USB Device Function
 - Supports High-Speed (HS, 480 Mbit/s)
 - Supports Full-Speed (FS, 12 Mbit/s)
 - Supports bi-directional Endpoint0 for Control transfer
 - Supports 6 Endpoints IN (including control endpoint 0), 6 Endpoints OUT (including control endpoint 0)
 - Supports up to (8KB+64Bytes) FIFO for EPs (Including EP0)

- Supports interface to an external Normal DMA controller for every EPs (Endpoint1, Endpoint2, Endpoint3, Endpoint4, Endpoint5)
- Supports an internal DMA Controller for data transfer with memory
- Supports High-bandwidth Isochronous & Interrupt transfers
- Supports Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Supports Automatic ping capabilities
- Supports Soft connect/disconnect function
- Supports all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Device and Host controller share an 8K SRAM and a physical PHY

3.10.3 GMAC



NOTE

The gigabit speeds of the GMAC are not supported on this chip.

- One 10/100 Mbit/s Ethernet port, connecting to external RMII PHY
- Compatible with the IEEE 802.3-2002 standard
- Supports both full-duplex and half-duplex operation
- Programmable frame length to support Standard or Jumbo Ethernet frames
- Separate 32-bit status returned for transmission and reception packets
- Optimization for packet-oriented DMA transfers with frame delimiters
- Supports linked-list descriptor list structure
- Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention: each descriptor can transfer up to 2KB of data
- Comprehensive status reporting for normal operation and transfers with errors
- Supports 1KB TXFIFO for transmission packets and 2KB RXFIFO for reception packets
- Programmable interrupt options for different operational conditions
- Supports MDIO Interface (Clause22) Interface for PHY device configuration and management

3.10.4 UART

- Up to 4 UART controllers: UART0, UART1, UART2, UART3
- Compatible with industry-standard 16450/16550 UARTs
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
 - Each of them is 64 bytes for UART0
 - Each of them is 128 bytes for UART1-3
- Supports baud rate generator from APB bus clock
 - Speed up to 6.25 Mbit/s with 100 MHz APB clock

- Speed up to 1.5 Mbit/s with 24 MHz APB clock
- Supports 5-8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports TX/RX DMA Slave interface
- Supports Software/ Hardware Flow Control
- Supports RS-485/9-bit mode
- Supports Auto-Flow by using CTS & RTS (excluding UART0)

3.10.5 PWM

- Maximum 16 independent PWM channels
 - Supports PWM output in cycle mode
 - Supports PWM output in pulse mode, and the pulse number is configurable, ranging from 0 to $(2^{16}-1)$
 - Output frequency range:
 - 0 to 24 MHz if the clock source is HOSC
 - 0 to 100 MHz if the clock source is APB0 clock
 - Various duty-cycle: 0% to 100%
 - Minimum resolution: 1/65536
- Maximum 8 complementary pairs output
 - Supports dead-zone generator, and the dead-time is configurable. Configurable dead-time range: 0 to (2^8-1)
- Maximum 4 groups of PWM channel output for controlling stepper motors
 - Supports PWM0-15 any plural channels to form a group, and output the same duty-cycle pulse
 - In the group mode, the relative phase of the output waveform for each channel is configurable, with a range of 0 to $(2^{16}-1)$
- Maximum 16 channels of input capture
 - Supports detection at the rising and falling edges
 - Supports pulse-width measurement, with a range of 0 to $(2^{16}-1)$
- Maximum 16 channels of input waveform counting, with a range of 0 to $(2^{32}-1)$

3.10.6 SPI and SPI_DBI

- Up to 3 SPI controllers
 - SPI0 and SPI2, supporting SPI mode
 - SPI1, supporting SPI mode and display bus interface (DBI) mode

SPI mode

- Supports multiple SPI modes
 - Master mode and slave mode for standard SPI
 - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI

- Master mode for Quad-Output/Quad-Input SPI
- Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
- Supports the maximum clock frequency: 100 MHz
- Supports TX/RX DMA Slave interface
- Supports Data Sample Mode for master mode and both two slave modes
 - Mode0, Mode1, Mode2 and Mode3
- Supports control signal configuration for master mode and both two slave modes
 - Two chip selects to support multiple peripherals
 - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

DBI mode

- DBI Type C 3 Line/4 Line Interface Mode
- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane
- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

3.10.7 Two Wire Interface (TWI)

- Up to 4 TWI controllers
- Compliant with I2C bus standard
- Supports master mode or slave mode
- Supports 7-bit standard address and 10-bit extended address.
- Supports standard mode (100 kbit/s) and high-speed mode (400 kbit/s).
- Supports general call and start byte.
- Master mode features:
 - Supports the bus arbitration in the case of multiple master devices.
 - Supports clock synchronization and bit and byte waiting.
 - Supports packet transmission and DMA
- Slave mode features:
 - Interrupt on address detection

3.10.8 General Purpose ADC (GPADC)

- Successive-Approximation Register ADC (SAR ADC) with 4 pads (padin0, padin1, padin2, padin3)
 - padin0 is connected to GPADC0 pin
 - padin1 is connected to GPADC1 pin
 - padin2 is connected to PD21/GPADC2 pin, and can be used by GPIO or GPADC2
 - padin3 is connected to PD22/GPADC3 pin, and can be used by GPIO or GPADC3

- One internal IBIAS_RESCAL channel supports resistance calibration
- 64 FIFO depth of data register
- 12-bit sampling resolution
- Up to 1 MHz sampling frequency
- Input voltage: 0 V to 1.8 V.
- 3.3 V voltage tolerance
- Supports data comparison and interrupts
- Two operation modes
 - Single conversion mode
 - Continuous conversion mode

3.11 Wi-Fi

- Wi-Fi Standards: 802.11a/b/g/n/ac/ax
- Frequency Bands:
 - 2.4 GHz: 20/40 MHz
 - 5 GHz: 20/40/80 MHz (1T1R)
- Bluetooth Support: BLE/BT 5.4

3.12 Security

3.12.1 Crypto Engine (CE)

- Symmetrical algorithm:
 - AES symmetrical algorithm
 - Key size: 128/192/256 bits
 - CFB mode includes: CFB1, CFB8, CFB64, and CFB128
 - CTR mode includes: CTR16, CTR32, CTR64, and CTR128
 - Supports ECB, CBC, CTS, OFB, CBC-MAC, GCM, and XTS modes
 - Supports XTS-AES symmetrical algorithm: key size: 256/512 bits
 - DES symmetrical algorithm
 - CTR mode, includes: CTR16, CTR32, and CTR64
 - Supports ECB, CBC, and CBC-MAC mode
 - Supports 3DES, SM4 symmetrical algorithm
- Hash algorithms
 - Supports MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
 - Supports HMAC-SHA1, HMAC-SHA256
 - Supports multi-packagemode for these ones
 - Supports hardware padding

- Random bit generator algorithms
 - Supports PRNG, 175 bits seed width, and output with multiple of 5 words
 - Supports TRNG, post-process by hardware with SHA256, output with multiple of 8 words
 - Supports TRNG single/double entropy source mode
 - Supports TRNG healthy test
 - Supports Instantiate/Reseed/Generate/Uninstantiate 4 process
 - Supports prediction resistance requests
 - Supports 8 separate suits of Internal State
 - Maxim 2^{32} BYTE length of Entropy input, Nonce, Personalization, Additional input. And length is multiple of word
- Public key algorithms
 - Supports RSA public key algorithms: 512/1024/2048/3072/4096-bit width
 - Supports ECC public key algorithms: 160/224/256/384/521-bit width
 - Supports SM2 algorithms

3.12.2 Security ID (SID)

- 2048-bit eFuse
- One-time programming
- Supports error bit position correction and ECC checksum
- Read/write protection
- SSK backup and read/write protection backup

3.13 Package

- TFBGA 317 balls, 12 mm x 12 mm body size, 1.19 mm height (maximum), 0.5 mm ball pitch, 0.3 mm ball size.
- QFN 128 pins, 12.3 mm x 12.3 mm body size, 1.90 mm height (maximum),
- TFBGA 194 balls, 11.9 mm x 6.9 mm body size, 1.248 mm height (maximum), 0.5 mm ball pitch, 0.3 mm ball size.

4 Pin Description



NOTE

The V881 is configured with different sets of pin characteristic and GPIO multiplexing. The following takes V881MX-XXX as an example. For the pin description of other devices, see [V881M2&M3-WB2_PINOUT.xlsx](#) and [V881M3-XXX_PINOUT.xlsx](#).

4.1 Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Ball#**: Package ball numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] Default Buffer Strength: Defines the default drive strength of the associated output buffer. There are total four levels for buffer strength: 2 mA for level0; 3 mA for level1; 4 mA for level2; 6 mA for level3.

N/A means Not Applicable.

[7] I/O Power Supply: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

4.1.1 SDRAM

Table 4-1 SDRAM Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
AA11	SDQ0	I/O	N/A	N/A	N/A	VCC-DRAM
W11	SDQ1	I/O	N/A	N/A	N/A	VCC-DRAM
AB11	SDQ2	I/O	N/A	N/A	N/A	VCC-DRAM
V11	SDQ3	I/O	N/A	N/A	N/A	VCC-DRAM
AA9	SDQ4	I/O	N/A	N/A	N/A	VCC-DRAM
AC11	SDQ5	I/O	N/A	N/A	N/A	VCC-DRAM
V9	SDQ6	I/O	N/A	N/A	N/A	VCC-DRAM
AB10	SDQ7	I/O	N/A	N/A	N/A	VCC-DRAM
W7	SDQ8	I/O	N/A	N/A	N/A	VCC-DRAM
AC4	SDQ9	I/O	N/A	N/A	N/A	VCC-DRAM
AC7	SDQ10	I/O	N/A	N/A	N/A	VCC-DRAM
AA5	SDQ11	I/O	N/A	N/A	N/A	VCC-DRAM
AB4	SDQ12	I/O	N/A	N/A	N/A	VCC-DRAM
AC8	SDQ13	I/O	N/A	N/A	N/A	VCC-DRAM
Y5	SDQ14	I/O	N/A	N/A	N/A	VCC-DRAM
AA7	SDQ15	I/O	N/A	N/A	N/A	VCC-DRAM
AB8	SDQS0P	I/O	N/A	N/A	N/A	VCC-DRAM
AB9	SDQS0N	I/O	N/A	N/A	N/A	VCC-DRAM
AB5	SDQS1P	I/O	N/A	N/A	N/A	VCC-DRAM
AB6	SDQS1N	I/O	N/A	N/A	N/A	VCC-DRAM

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
Y9	SDQM0	I/O	N/A	N/A	N/A	VCC-DRAM
V7	SDQM1	I/O	N/A	N/A	N/A	VCC-DRAM
AC14	SCKP	O	N/A	N/A	N/A	VCC-DRAM
AC13	SCKN	O	N/A	N/A	N/A	VCC-DRAM
AB12	SCKE0	O	N/A	N/A	N/A	VCC-DRAM
V17	SCKE1	O	N/A	N/A	N/A	VCC-DRAM
AC22	SA0	O	N/A	N/A	N/A	VCC-DRAM
AB22	SA1	O	N/A	N/A	N/A	VCC-DRAM
AB19	SA2	O	N/A	N/A	N/A	VCC-DRAM
W23	SA3	O	N/A	N/A	N/A	VCC-DRAM
AB20	SA4	O	N/A	N/A	N/A	VCC-DRAM
Y23	SA5	O	N/A	N/A	N/A	VCC-DRAM
AB21	SA6	O	N/A	N/A	N/A	VCC-DRAM
U15	SA7	O	N/A	N/A	N/A	VCC-DRAM
AA19	SA8	O	N/A	N/A	N/A	VCC-DRAM
AB23	SA9	O	N/A	N/A	N/A	VCC-DRAM
AA15	SA10	O	N/A	N/A	N/A	VCC-DRAM
AA17	SA11	O	N/A	N/A	N/A	VCC-DRAM
AB16	SA12	O	N/A	N/A	N/A	VCC-DRAM
Y22	SA13	O	N/A	N/A	N/A	VCC-DRAM
W17	SA14	O	N/A	N/A	N/A	VCC-DRAM
W19	SA15	O	N/A	N/A	N/A	VCC-DRAM
AC16	SBA0	O	N/A	N/A	N/A	VCC-DRAM
W15	SBA1	O	N/A	N/A	N/A	VCC-DRAM
AC20	SBA2	O	N/A	N/A	N/A	VCC-DRAM
AC17	SRAS	O	N/A	N/A	N/A	VCC-DRAM
AB15	SCAS	O	N/A	N/A	N/A	VCC-DRAM
AA13	SWE	O	N/A	N/A	N/A	VCC-DRAM
AB14	SCS0	O	N/A	N/A	N/A	VCC-DRAM
Y19	SCS1	O	N/A	N/A	N/A	VCC-DRAM

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
AB18	SODT0	O	N/A	N/A	N/A	VCC-DRAM
W20	SODT1	O	N/A	N/A	N/A	VCC-DRAM
AA22	SRST	O	N/A	N/A	N/A	VCC-DRAM
W13	SZQ	AI	N/A	N/A	N/A	VCC-DRAM
U13	SVREF	P	N/A	N/A	N/A	VCC-DRAM
R10, R11, R12, R13, R14	VCC-DRAM	P	N/A	N/A	N/A	N/A
T16	VDD18- DRAM	P	N/A	N/A	N/A	N/A
V13	DDR3- SZQ1	AO	N/A	N/A	N/A	VCC-DRAM

4.1.2 GPIO Groups

4.1.2.1 Port A

Table 4-2 Port A Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
A17	PA0	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
B17	PA1	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
B22	PA2	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
A22	PA3	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
B20	PA4	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
B21	PA5	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
A19	PA6	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
A20	PA7	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
B18	PA8	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
B19	PA9	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
C22	PA10	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
B23	PA11	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
E15	PA12	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
C15	PA13	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
D15	PA14	I/O	Z	PU/PD	4 mA	VCC-PA/VCC18-MCSI
C17	PA15	I/O	Z	PU/PD	4 mA	VCC-PA
D17	PA16	I/O	Z	PU/PD	4 mA	VCC-PA
D23	PA17	I/O	Z	PU/PD	4 mA	VCC-PA
D22	PA18	I/O	Z	PU/PD	4 mA	VCC-PA
C19	PA19	I/O	Z	PU/PD	4 mA	VCC-PA
E21	PA20	I/O	Z	PU/PD	4 mA	VCC-PA
E20	PA21	I/O	Z	PU/PD	4 mA	VCC-PA
F17	VCC18-MCSI	P	N/A	N/A	N/A	N/A
E19	VCC-PA	P	N/A	N/A	N/A	N/A

4.1.2.2 Port C

Table 4-3 Port C Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
K22	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
G21	PC1	I/O	PU	PU/PD	4 mA	VCC-PC
E22	PC2	I/O	PU	PU/PD	4 mA	VCC-PC
G22	PC3	I/O	PU	PU/PD	4 mA	VCC-PC
H23	PC4	I/O	Z	PU/PD	4 mA	VCC-PC
J22	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
H22	PC6	I/O	Z	PU/PD	4 mA	VCC-PC
G23	PC7	I/O	Z	PU/PD	4 mA	VCC-PC
F22	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
E23	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
G20	PC10	I/O	Z	PU/PD	4 mA	VCC-PC

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
G19	PC11	I/O	Z	PU/PD	4 mA	VCC-PC
J20	VCC-PC	P	N/A	N/A	N/A	N/A

4.1.2.3 Port D

Table 4-4 Port D Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
A14	PD0	I/O	Z	PU/PD	4 mA	VCC-PD
E13	PD1	I/O	Z	PU/PD	4 mA	VCC-PD
D13	PD2	I/O	Z	PU/PD	4 mA	VCC-PD
C13	PD3	I/O	Z	PU/PD	4 mA	VCC-PD
B13	PD4	I/O	Z	PU/PD	4 mA	VCC-PD
E11	PD5	I/O	Z	PU/PD	4 mA	VCC-PD
D11	PD6	I/O	Z	PU/PD	4 mA	VCC-PD
B12	PD7	I/O	Z	PU/PD	4 mA	VCC-PD
B10	PD8	I/O	Z	PU/PD	4 mA	VCC-PD
D9	PD9	I/O	Z	PU/PD	4 mA	VCC-PD
A11	PD10	I/O	Z	PU/PD	4 mA	VCC-PD
B9	PD11	I/O	Z	PU/PD	4 mA	VCC-PD
A10	PD12	I/O	Z	PU/PD	4 mA	VCC-PD
B11	PD13	I/O	Z	PU/PD	4 mA	VCC-PD
A13	PD14	I/O	Z	PU/PD	4 mA	VCC-PD
C9	PD15	I/O	Z	PU/PD	4 mA	VCC-PD
C11	PD16	I/O	Z	PU/PD	4 mA	VCC-PD
D7	PD17	I/O	Z	PU/PD	4 mA	VCC-PD
A8	PD18	I/O	Z	PU/PD	4 mA	VCC-PD
B8	PD19	I/O	Z	PU/PD	4 mA	VCC-PD
A7	PD20/GPADC2	I/O	Z	PU/PD	4 mA	VCC-PD/AVCC
B7	PD21/GPADC3	I/O	Z	PU/PD	4 mA	VCC-PD/AVCC
C7	PD22	I/O	Z	PU/PD	4 mA	VCC-PD

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
F9	VCC-PD	P	N/A	N/A	N/A	N/A

4.1.2.4 Port E

Table 4-5 Port E Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
R4	PE0	I/O	Z	PU/PD	4 mA	VCC-PE
W1	PE1	I/O	Z	PU/PD	4 mA	VCC-PE
R2	PE2	I/O	Z	PU/PD	4 mA	VCC-PE
R3	PE3	I/O	Z	PU/PD	4 mA	VCC-PE
P2	PE4	I/O	Z	PU/PD	4 mA	VCC-PE
P1	PE5	I/O	Z	PU/PD	4 mA	VCC-PE
U1	PE6	I/O	Z	PU/PD	4 mA	VCC-PE
T1	PE7	I/O	Z	PU/PD	4 mA	VCC-PE
V2	PE8	I/O	Z	PU/PD	4 mA	VCC-PE
U2	PE9	I/O	Z	PU/PD	4 mA	VCC-PE
W3	PE10	I/O	Z	PU/PD	4 mA	VCC-PE
W2	PE11	I/O	Z	PU/PD	4 mA	VCC-PE
T2	PE12	I/O	Z	PU/PD	4 mA	VCC-PE
U3	PE13	I/O	Z	PU/PD	4 mA	VCC-PE
U4	PE14	I/O	Z	PU/PD	4 mA	VCC-PE
N1	PE15	I/O	Z	PU/PD	4 mA	VCC-PE
N5	PE16	I/O	Z	PU/PD	4 mA	VCC-PE
N3	PE17	I/O	Z	PU/PD	4 mA	VCC-PE
R6	VCC-PE	P	N/A	N/A	N/A	N/A

4.1.2.5 Port F

Table 4-6 Port F Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
N23	PF0	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
N22	PF1	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
M22	PF2	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
L22	PF3	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
L23	PF4	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
K23	PF5	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
L21	PF6	I/O	Z	PU/PD	4 mA	VCC33-PF-USB/VCC18-PF
J19	VCC18-PF	P	N/A	N/A	N/A	N/A
J18	VCC33-PF-USB	P	N/A	N/A	N/A	N/A

4.1.2.6 Port G

Table 4-7 Port G Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
K2	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
K1	PG1	I/O	Z	PU/PD	4 mA	VCC-PG
L1	PG2	I/O	Z	PU/PD	4 mA	VCC-PG
L2	PG3	I/O	Z	PU/PD	4 mA	VCC-PG
M2	PG4	I/O	Z	PU/PD	4 mA	VCC-PG
N2	PG5	I/O	Z	PU/PD	4 mA	VCC-PG
L3	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
L4	PG7	I/O	Z	PU/PD	4 mA	VCC-PG

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
N6	VCC-PG	P	N/A	N/A	N/A	N/A

4.1.2.7 Port H

Table 4-8 Port H Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
N21	PH0	I/O	Z	PU/PD	4 mA	VCC-IO
L18	PH1	I/O	Z	PU/PD	4 mA	VCC-IO
P22	PH2	I/O	Z	PU/PD	4 mA	VCC-IO
R19	PH3	I/O	Z	PU/PD	4 mA	VCC-IO
L19	PH4	I/O	Z	PU/PD	4 mA	VCC-IO
R22	PH5	I/O	Z	PU/PD	4 mA	VCC-IO
T22	PH6	I/O	Z	PU/PD	4 mA	VCC-IO
R21	PH7	I/O	Z	PU/PD	4 mA	VCC-IO
P23	PH8	I/O	Z	PU/PD	4 mA	VCC-IO
U19	PH9	I/O	Z	PU/PD	4 mA	VCC-IO
U18	PH10	I/O	Z	PU/PD	4 mA	VCC-IO
U21	PH11	I/O	Z	PU/PD	4 mA	VCC-IO
V22	PH12	I/O	Z	PU/PD	4 mA	VCC-IO
U22	PH13	I/O	Z	PU/PD	4 mA	VCC-IO
U23	PH14	I/O	Z	PU/PD	4 mA	VCC-IO
T23	PH15	I/O	Z	PU/PD	4 mA	VCC-IO
R18	VCC-IO	P	N/A	N/A	N/A	N/A

4.1.2.8 Port L

Table 4-9 Port L Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
D1	PL0/PWR-EN0	I/O	Z	PU/PD	4 mA	VCC-RTC
D2	PL1/PWR-EN1	I/O	Z	PU/PD	4 mA	VCC-RTC

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
B3	PL2/PWR-EN2	I/O	Z	PU/PD	4 mA	VCC-RTC
A2	PL3/X32KIN	I/O	Z	PU/PD	4 mA	VCC-RTC
B2	PL4/X32KOUT	I/O	Z	PU/PD	4 mA	VCC-RTC
B1	PL5/NMI1	I/O	Z	PU/PD	4 mA	VCC-RTC
C2	PL6	I/O	Z	PU/PD	4 mA	VCC-RTC

4.1.3 System Control

Table 4-10 System Control Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
N18	FEL	I	PU	PU/PD	N/A	VCC-IO
N19	JTAG-SEL	I	PU	PU/PD	N/A	VCC-IO
G5	TEST	I	PD	PU/PD	N/A	VCC-RTC
J5	TEST-ALT	I	N/A	N/A	N/A	VCC-RTC
G18	VCC-EFUSE	P	N/A	N/A	N/A	N/A

4.1.4 PMC

Table 4-11 PMC Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
F2	RESET	I/O,OD	N/A	N/A	N/A	VCC-RTC
G3	PWRON	I, OD	N/A	N/A	N/A	VCC-RTC
E1	PWR-STARTUP	I	N/A	N/A	N/A	VCC-RTC
E3	PMC-BYP	I	PU	PU/PD	N/A	VCC-RTC

4.1.5 RTC

Table 4-12 RTC Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
J8	VCC-RTC	P	N/A	N/A	N/A	N/A

4.1.6 DCXO

Table 4-13 DCXO Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
G1	DXIN	AI	N/A	N/A	N/A	VCC-RTC
H1	DXOUT	AO	N/A	N/A	N/A	VCC-RTC
J2	REFCLK-OUT	AO	N/A	N/A	N/A	VCC-RTC

4.1.7 PLL

Table 4-14 PLL Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
J3	PLLTEST	AO, OD	N/A	N/A	N/A	VCC-PLL
L5	VCC-PLL	P	N/A	N/A	N/A	N/A

4.1.8 USB

Table 4-15 USB Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
B16	USB0-DM	A I/O	N/A	N/A	N/A	VCC33-PF-USB
B15	USB0-DP	A I/O	N/A	N/A	N/A	VCC33-PF-USB

4.1.9 ADC

Table 4-16 ADC Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
B6	GPADC0	AI	N/A	N/A	N/A	AVCC
B5	GPADC1	AI	N/A	N/A	N/A	AVCC

4.1.10 Audio Codec

Table 4-17 Audio Codec Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
A4	MICIN1P	AI	N/A	N/A	N/A	AVCC
A5	MICIN2P	AI	N/A	N/A	N/A	AVCC
D5	VRA1	AO	N/A	N/A	N/A	N/A
E5	AVCC	P	N/A	N/A	N/A	N/A
B4	LINEOUTP	AO	N/A	N/A	N/A	AVCC
C5	AGND	G	N/A	N/A	N/A	N/A

4.1.11 Power

Table 4-18 Power Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]	Ball Reset State ^[4]	Pull Up/Down ^[5]	Default Buffer Strength ^[6]	I/O Power Supply ^[7]
M12, L15, M15, M16, N16, N17	VDD-SYS	P	N/A	N/A	N/A	N/A
L16	VDD-SYSFB	P	N/A	N/A	N/A	N/A

4.1.12 Ground

Table 4-19 Ground Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]
A1, AC1, G2, H2, AB3, E4, G4, J4, N4, R5, W5, AC5, G6, J6, L6, E7, F7, G7, U7, Y7, AB7, H8, K8, L8, M8, N8, P8, E9, H9, J9, K9, L9, N9, P9, R9, U9, W9, H10, J10, L10, N10, AC10, F11, H11, J11, K11, L11, N11, P11, U11, Y11, H12, J12, F13, H13, J13, K13, L13, N13, P13, Y13, AB13, B14, H14, N14, P14, F15, H15, K15, P15, V15, Y15, A16, H16, J16, P16, E17, U17, Y17, AB17, D19, AC19, L20, N20, R20, U20, J21, W21, W22, A23, AC23	GND	G

4.1.13 NC

Table 4-20 NC Pin Characteristics

Ball# ^[1]	Pin Name ^[2]	Type ^[3]
AA2, Y2, AB1, AB2, AC2, W4, Y1, U5, U6, E2	NC	N/A

4.2 GPIO Multiplex Function

The following tables provide a description of the GPIO multiplex function.



NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function10 to Function13 are reserved.

4.2.1 Port A

Table 4-21 Port A Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PA0	I/O	MCSIA-CKP	NCSI-D8							PA-EINT0
PA1	I/O	MCSIA-CKN	NCSI-D9							PA-EINT1
PA2	I/O	MCSIA-D0P	NCSI-D10							PA-EINT2
PA3	I/O	MCSIA-D0N	NCSI-D11							PA-EINT3
PA4	I/O	MCSIA-D1P/MCSIC-D0P	NCSI-D12							PA-EINT4
PA5	I/O	MCSIA-D1N/MCSIC-D0N	NCSI-D13							PA-EINT5
PA6	I/O	MCSIB-D1P/MCSIC-CKP/MCSIA-D2P	NCSI-D14	TWI1-SCK	PWM-0		SQPI-CLK			PA-EINT6
PA7	I/O	MCSIB-D1N/MCSIC-CKN/MCSIA-D2N	NCSI-D15	TWI1-SDA	PWM-1		SQPI-CS0			PA-EINT7
PA8	I/O	MCSIB-D0P/MCSIA-D3P	TWI2-SCK	TWI3-SCK	PWM-2	UART2-TX	SQPI-MOSI-IO0			PA-EINT8
PA9	I/O	MCSIB-D0N/MCSIA-D3N	TWI2-SDA	TWI3-SDA	PWM-3	UART2-RX	SQPI-MISO-IO1			PA-EINT9
PA10	I/O	MCSIB-CKP	NCSI-HSYNC	PWM-13	TWI0-SCK	CLK-FANOUT0	SQPI-WP-IO2			PA-EINT10
PA11	I/O	MCSIB-CKN	NCSI-VSYNC	PWM-14	TWI0-SDA	CLK-FANOUT1	SQPI-HOLD-IO3			PA-EINT11
PA12	I/O		NCSI-D0	MCSI0-MCLK	UART0-TX					PA-EINT12
PA13	I/O	CSI0-XVS-FSYNC	NCSI-D1	MCSI1-MCLK	UART0-RX					PA-EINT13
PA14	I/O	CSI1-XVS-FSYNC	NCSI-D2	MCSI2-MCLK	CLK-FANOUT0					PA-EINT14
PA15	I/O		NCSI-D3	TWI1-SCK	CLK-FANOUT1					PA-EINT15
PA16	I/O		NCSI-D4	TWI1-SDA	UART3-TX					PA-EINT16
PA17	I/O	CSI0-XVS-FSYNC	NCSI-D5	TWI0-SCK	UART3-RX					PA-EINT17
PA18	I/O		NCSI-D6	TWI0-SDA	UART3-RTS					PA-EINT18
PA19	I/O		NCSI-D7		UART3-CTS					PA-EINT19
PA20	I/O		NCSI-MCLK		TCON-FSYNC					PA-EINT20

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PA21	I/O		NCSI-PCLK							PA-EINT21

4.2.2 Port C

Table 4-22 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PC0	I/O	SPIF-CLK	SDC2-CLK	SPI0-CLK			SQPI-CLK			PC-EINT0
PC1	I/O	SPIF-CS0	SDC2-CMD	SPI0-CS0			SQPI-CS0			PC-EINT1
PC2	I/O	SPIF-MOSI	SDC2-D2	SPI0-MOSI	BOOT-SEL0		SQPI-MOSI-IO0			PC-EINT2
PC3	I/O	SPIF-MISO	SDC2-D1	SPI0-MISO	BOOT-SEL1		SQPI-MISO-IO1			PC-EINT3
PC4	I/O	SPIF-WP	SDC2-D0	SPI0-WP	PWM-4	TWI1-SCK	SQPI-WP-IO2			PC-EINT4
PC5	I/O	SPIF-HOLD	SDC2-D3	SPI0-HOLD	PWM-5	TWI1-SDA	SQPI-HOLD-IO3			PC-EINT5
PC6	I/O	SPIF-D4	SDC2-D4	SPI0-CS1						PC-EINT6
PC7	I/O	SPIF-D5	SDC2-D5							PC-EINT7
PC8	I/O	SPIF-D6	SDC2-D6							PC-EINT8
PC9	I/O	SPIF-D7	SDC2-D7							PC-EINT9
PC10	I/O	SPIF-DQS	SDC2-DS							PC-EINT10
PC11	I/O		SDC2-RST							PC-EINT11

4.2.3 Port D

Table 4-23 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PD0	I/O	LCD-D2								PD-EINT0
PD1	I/O	LCD-D3	PWM-0	RMII-RXD1		SPI1-CS0/DBI-CSX	RMII-TXD0			PD-EINT1
PD2	I/O	LCD-D4	PWM-1	RMII-RXD0		SPI1-CLK/DBI-SCLK	RMII-TXD1			PD-EINT2
PD3	I/O	LCD-D5	PWM-2	RMII-CRS-DV		SPI1-MOSI/DBI-SDO	RMII-RXER			PD-EINT3
PD4	I/O	LCD-D6	PWM-3	RMII-RXER		SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	RMII-CRS-DV			PD-EINT4
PD5	I/O	LCD-D7	PWM-4	RMII-TXD1		SPI1-HOLD/DBI-DCX/DBI-WRX	RMII-RXD1			PD-EINT5
PD6	I/O	LCD-D10	PWM-5	RMII-TXD0		SPI1-WP/DBI-TE	RMII-RXD0			PD-EINT6
PD7	I/O	LCD-D11	PWM-6	RMII-TXCK		SPI1-CS1	RMII-MDC			PD-EINT7
PD8	I/O	LCD-D12	PWM-7	RMII-TXEN						PD-EINT8
PD9	I/O	LCD-D13	PWM-8				RMII-MDIO			PD-EINT9

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PD10	I/O	LCD-D14	I2S0-MCLK				RMII-TXEN			PD-EINT10
PD11	I/O	LCD-D15	I2S0-BCLK				RMII-TXCK			PD-EINT11
PD12	I/O	LCD-D18	I2S0-LRCK				PWM-11			PD-EINT12
PD13	I/O	LCD-D19	I2S0-DOUT0							PD-EINT13
PD14	I/O	LCD-D20	I2S0-DOUT1	I2S0-DIN1						PD-EINT14
PD15	I/O	LCD-D21	I2S0-DOUT2	I2S0-DIN2						PD-EINT15
PD16	I/O	LCD-D22	I2S0-DOUT3	I2S0-DIN3						PD-EINT16
PD17	I/O	LCD-D23	I2S0-DIN0							PD-EINT17
PD18	I/O	LCD-CLK	PWM-12	RMII-EPHY-25M	SPI1-CLK	TWI3-SCK	UART2-TX			PD-EINT18
PD19	I/O	LCD-DE	PWM-9	TCON-FSYNC	SPI1-MOSI	TWI3-SDA	UART2-RX			PD-EINT19
PD20/GPADC2	I/O	LCD-HSYNC	TWI0-SCK	RMII-MDC	SPI1-MISO	TWI2-SCK	UART2-RTS			PD-EINT20
PD21/GPADC3	I/O	LCD-VSYNC	TWI0-SDA	RMII-MDIO	SPI1-CS0	TWI2-SDA	UART2-CTS			PD-EINT21
PD22	I/O	TCON-FSYNC	PWM-9							PD-EINT22

4.2.4 Port E

Table 4-24 Port E Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PE0	I/O	NCSI-PCLK	RMII-RXD1	LCD-D0	PWM-0	SDC1-D1	SPI2-CLK	TWI3-SCK	SQPI-CLK	PE-EINT0
PE1	I/O	NCSI-MCLK	RMII-TXCK	LCD-D1	PWM-1	SDC1-D0	SPI2-MOSI	TWI3-SDA	SQPI-CS0	PE-EINT1
PE2	I/O	NCSI-HSYNC	RMII-CRS-DV	LCD-D8	PWM-2	SDC1-CLK	SPI2-MISO	TWI1-SCK	SQPI-MOSI-IO0	PE-EINT2
PE3	I/O	NCSI-VSYNC	RMII-RXD0	LCD-D9	PWM-3	SDC1-CMD	SPI2-CS0	TWI1-SDA	SQPI-MISO-IO1	PE-EINT3
PE4	I/O	NCSI-D0	RMII-TXD0	LCD-D16	PWM-4	SDC1-D3	TWI3-SCK	TWI0-SCK	SQPI-WP-IO2	PE-EINT4
PE5	I/O	NCSI-D1	RMII-TXD1	LCD-D17	PWM-5	SDC1-D2	TWI3-SDA	TWI0-SDA	SQPI-HOLD-IO3	PE-EINT5
PE6	I/O	NCSI-D2	RMII-TXEN		PWM-6	UART3-TX		TWI2-SCK		PE-EINT6
PE7	I/O	NCSI-D3	RMII-RXER		PWM-7	UART3-RX	I2S0-DOUT0	TWI2-SDA		PE-EINT7
PE8	I/O	NCSI-D4	RMII-MDC	SPI2-CLK	PWM-8	UART1-TX	I2S0-DIN0	TWI1-SCK		PE-EINT8
PE9	I/O	NCSI-D5	RMII-MDIO	SPI2-MOSI	PWM-9	UART1-RX	I2S0-LRCK	TWI1-SDA		PE-EINT9
PE10	I/O	NCSI-D6	RMII-EPHY-25M	SPI2-MISO	PWM-10	UART2-RTS	I2S0-BCLK	TWI2-SCK		PE-EINT10
PE11	I/O	NCSI-D7		SPI2-CS0	CSI0-XVS-FSYNC	UART2-CTS	I2S0-MCLK	TWI2-SDA		PE-EINT11
PE12	I/O	NCSI-D8	PWM-12	CSI1-XVS-FSYNC	MCSI0-MCLK	UART2-TX	UART3-TX	TWI3-SCK		PE-EINT12
PE13	I/O	NCSI-D9	PWM-13		MCSI1-MCLK	UART2-RX	UART3-RX	TWI3-SDA		PE-EINT13
PE14	I/O	NCSI-D10	PWM-14							PE-EINT14

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PE15	I/O	NCSI-D11	PWM-15							PE-EINT15
PE16	I/O	TWI0-SCK	TWI2-SCK							PE-EINT16
PE17	I/O	TWI0-SDA	TWI2-SDA							PE-EINT17

4.2.5 Port F

Table 4-25 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PF0	I/O	SDC0-D1	E907-JTAG-MS	SPI0-CLK		C907-JTAG-MS				PF-EINT0
PF1	I/O	SDC0-D0	E907-JTAG-DI	SPI0-MOSI		C907-JTAG-DI				PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX	SPI0-MISO						PF-EINT2
PF3	I/O	SDC0-CMD	E907-JTAG-DO	SPI0-CS0		C907-JTAG-DO				PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX	SPI0-CS1						PF-EINT4
PF5	I/O	SDC0-D2	E907-JTAG-CK			C907-JTAG-CK				PF-EINT5
PF6	I/O									PF-EINT6

4.2.6 Port G

Table 4-26 Port G Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PG0	I/O	SDC1-D1	LCD-D0	UART3-TX						PG-EINT0
PG1	I/O	SDC1-D0	LCD-D1	UART3-RX						PG-EINT1
PG2	I/O	SDC1-CLK	LCD-D8	UART3-CTS						PG-EINT2
PG3	I/O	SDC1-CMD	LCD-D9	UART3-RTS						PG-EINT3
PG4	I/O	SDC1-D3	LCD-D16	UART1-RTS						PG-EINT4
PG5	I/O	SDC1-D2	LCD-D17	UART1-CTS						PG-EINT5
PG6	I/O	TWI3-SCK	CLK-FANOUT0	UART1-TX						PG-EINT6
PG7	I/O	TWI3-SDA	CLK-FANOUT1	UART1-RX						PG-EINT7

4.2.7 Port H

Table 4-27 Port H Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PH0	I/O	PWM-0	I2S0-MCLK	PWM-12	UART3-TX					PH-EINT0
PH1	I/O	PWM-1	I2S0-BCLK	PWM-13	UART3-RX					PH-EINT1
PH2	I/O	PWM-2	I2S0-LRCK	PWM-14	UART3-CTS					PH-EINT2
PH3	I/O	PWM-3	I2S0-DOUT0	PWM-15	UART3-RTS					PH-EINT3
PH4	I/O	PWM-4	I2S0-DIN0		CLK-FANOUT2					PH-EINT4
PH5	I/O	PWM-5	RMII-RXD1	TWI2-SCK	UART2-TX					PH-EINT5
PH6	I/O	PWM-6	RMII-RXD0	TWI2-SDA	UART2-RX	I2S0-MCLK				PH-EINT6

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PH7	I/O	PWM-7	RMII-CRS-DV	UART0-TX	UART2-RTS	I2S0-BCLK				PH-EINT7
PH8	I/O	PWM-8	RMII-RXER	UART0-RX	UART2-CTS	I2S0-LRCK				PH-EINT8
PH9	I/O	E907-JTAG-MS	RMII-TXD1	TWI3-SCK	UART0-TX	I2S0-DIN0	C907-JTAG-MS	PWM-4		PH-EINT9
PH10	I/O	E907-JTAG-CK	RMII-TXD0	TWI3-SDA	UART0-RX	I2S0-DOUT0	C907-JTAG-CK	PWM-5		PH-EINT10
PH11	I/O	E907-JTAG-DO	RMII-TXCK	SPI2-CLK	TWI2-SCK	CLK-FANOUT0	C907-JTAG-DO	PWM-6		PH-EINT11
PH12	I/O	E907-JTAG-DI	RMII-TXEN	SPI2-MOSI	TWI2-SDA	CLK-FANOUT1	C907-JTAG-DI	PWM-7		PH-EINT12
PH13	I/O	PWM-9	RMII-MDC	SPI2-MISO	TWI3-SCK	UART0-TX		PWM-8		PH-EINT13
PH14	I/O	PWM-10	RMII-MDIO	SPI2-CS0	TWI3-SDA	UART0-RX		PWM-14		PH-EINT14
PH15	I/O	CLK-FANOUT2	RMII-EPHY-25M	SPI2-CS1				PWM-15		PH-EINT15

4.2.8 Port L

Table 4-28 Port L Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function8	Function 9	Function14
PL0/PWR_EN0	I/O	TWI1-SCK								PL-EINT0
PL1/PWR_EN1	I/O	TWI1-SDA								PL-EINT1
PL2/PWR_EN2	I/O	CSI0-XVS-FSYNC								PL-EINT2
PL3/X32KIN	I/O	TWI2-SCK	UART0-TX	UART2-CTS	CSI0-XVS-FSYNC					PL-EINT3
PL4/X32KOUT	I/O	TWI2-SDA	UART0-RX	UART2-RTS	CSI1-XVS-FSYNC					PL-EINT4
PL5/NMI1	I/O	TWI0-SCK	UART3-TX	UART2-TX	CSI1-XVS-FSYNC					PL-EINT5
PL6	I/O	TWI0-SDA	UART3-RX	UART2-RX						PL-EINT6

4.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name:** The name of every signal.

[2] **Description:** The detailed function description of every signal.

[3] **Type:** Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

4.3.1 SDRAM

Table 4-29 SDRAM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
DDR3-SZQ1	DDR3 SZQ Calibration Resistor	AO
SRST	DRAM Reset Signal	O
SWE	DRAM Write Enable	O
SA0	DRAM Address Signal 0	O
SA1	DRAM Address Signal 1	O
SA2	DRAM Address Signal 2	O
SA3	DRAM Address Signal 3	O
SA4	DRAM Address Signal 4	O
SA5	DRAM Address Signal 5	O
SA6	DRAM Address Signal 6	O

Signal Name ^[1]	Description ^[2]	Type ^[3]
SA7	DRAM Address Signal 7	O
SA8	DRAM Address Signal 8	O
SA9	DRAM Address Signal 9	O
SA10	DRAM Address Signal 10	O
SA11	DRAM Address Signal 11	O
SA12	DRAM Address Signal 12	O
SA13	DRAM Address Signal 13	O
SA14	DRAM Address Signal 14	O
SA15	DRAM Address Signal 15	O
SBA0	DRAM Bank Address Signal 0	O
SBA1	DRAM Bank Address Signal 1	O
SBA2	DRAM Bank Address Signal 2	O
SRAS	DRAM Row Address Strobe	O
SCAS	DRAM Column Address Strobe	O
SCKE0	DRAM Clock Enable Signal to the Memory Device 0	O
SCKE1	DRAM Clock Enable Signal to the Memory Device 1	O
SCKN	DRAM Differential Clock (Negative)	O
SCKP	DRAM Differential Clock (Positive)	O
SCS0	DRAM Chip Select Signal to the Memory Device for RANK 0	O
SCS1	DRAM Chip Select Signal to the Memory Device for RANK 1	O
SDQ0	DRAM Bidirectional Data Line 0	I/O
SDQ1	DRAM Bidirectional Data Line 1	I/O
SDQ2	DRAM Bidirectional Data Line 2	I/O
SDQ3	DRAM Bidirectional Data Line 3	I/O
SDQ4	DRAM Bidirectional Data Line 4	I/O
SDQ5	DRAM Bidirectional Data Line 5	I/O
SDQ6	DRAM Bidirectional Data Line 6	I/O
SDQ7	DRAM Bidirectional Data Line 7	I/O
SDQ8	DRAM Bidirectional Data Line 8	I/O
SDQ9	DRAM Bidirectional Data Line 9	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
SDQ10	DRAM Bidirectional Data Line 10	I/O
SDQ11	DRAM Bidirectional Data Line 11	I/O
SDQ12	DRAM Bidirectional Data Line 12	I/O
SDQ13	DRAM Bidirectional Data Line 13	I/O
SDQ14	DRAM Bidirectional Data Line 14	I/O
SDQ15	DRAM Bidirectional Data Line 15	I/O
SDQS0P	DRAM Bidirectional Data Strobe 0 (Active High)	I/O
SDQS0N	DRAM Bidirectional Data Strobe 0 (Active Low)	I/O
SDQS1P	DRAM Bidirectional Data Strobe 1 (Active High)	I/O
SDQS1N	DRAM Bidirectional Data Strobe 1 (Active Low)	I/O
SDQM0	DRAM Data Mask Signal 0	I/O
SDQM1	DRAM Data Mask Signal 1	I/O
SODT0	DRAM On-Die Termination Output Signal 0	O
SODT1	DRAM On-Die Termination Output Signal 1	O
SVREF	DRAM Reference Voltage	P
VCC-DRAM	IO Power Supply for DRAM PHY	P
VDD18-DRAM	SDRAM Controller 1.8V Power Supply	P

4.3.2 Boot

Table 4-30 Boot Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
FEL	Boot Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process.	I
BOOT-SEL0	Boot Media Select 0	I
BOOT-SEL1	Boot Media Select 1	I

4.3.3 RTC

Table 4-31 RTC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
TEST	Test Mode Signal, valid only when TEST-ALT is high.	I

Signal Name ^[1]	Description ^[2]	Type ^[3]
TEST-ALT	Test System Selection Signal	I
RESET	SoC Reset Signal (Active Low)	I/O, OD
PWRON	Power-on key	I, OD
PWR-STARTUP	VBUS Detection Signal	I
PMC-BYP	PMC Bypass Control Signal	I
PL0/PWR-EN0	Wake-up IO0; LDO/DCDC Enable For pin mode select, see RTC register in User Manual.	I/O
PL1/PWR-EN1	Wake-up IO1; LDO/DCDC Enable For pin mode select, see RTC register in User Manual.	I/O
PL2/PWR-EN2	Wake-up IO2; LDO/DCDC Enable For pin mode select, see RTC register in User Manual.	I/O
PL3/X32KIN	Wake-up IO3; Clock Input of 32.768 kHz Crystal Before using external 32K crystal oscillator, the function of PL3 must be configured as disabled.	I/O
PL4/X32KOUT	Wake-up IO4; Clock Output of 32.768 kHz Crystal Before using external 32K crystal oscillator, the function of PL4 must be configured as disabled.	I/O
PL5/NMI	Wake-up IO5; Non-Maskable Interrupt For pin mode select, see RTC register in User Manual.	I/O
PL6	Wake-up IO6	I/O
VCC-RTC	RTC Power Supply	P

4.3.4 PLL

Table 4-32 PLL Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
PLLTEST	PLL Test Signal	AO, OD
VCC-PLL	PLL Power Supply	P

4.3.5 DCXO

Table 4-33 DCXO Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI

Signal Name ^[1]	Description ^[2]	Type ^[3]
DXOUT	Digital Compensated Crystal Oscillator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO

4.3.6 Clock Fanout

Table 4-34 Clock Fanout Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
CLK-FANOUT0	Internal Clock Fanout 0 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, and so on	O
CLK-FANOUT1	Internal Clock Fanout 1 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, and so on	O
CLK-FANOUT2	Internal Clock Fanout 2 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, and so on	O

4.3.7 SD Card/SDIO/eMMC

Table 4-35 SD Card/SDIO/eMMC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SDC0-CMD	SD Card Command Output/Response Input	I/O, OD
SDC0-CLK	SD Card Clock Output	O
SDC0-D0	SD Card Data Input/ Output 0	I/O
SDC0-D1	SD Card Data Input/ Output 1	I/O
SDC0-D2	SD Card Data Input/ Output 2	I/O
SDC0-D3	SD Card Data Input/ Output 3	I/O
SDC1-CMD	SDIO WIFI Command Output/Response Input	I/O, OD
SDC1-CLK	SDIO WIFI Clock Output	O
SDC1-D0	SDIO WIFI Data Input/ Output 0	I/O
SDC1-D1	SDIO WIFI Data Input/ Output 1	I/O
SDC1-D2	SDIO WIFI Data Input/ Output 2	I/O
SDC1-D3	SDIO WIFI Data Input/ Output 3	I/O
SDC2-CMD	eMMC Command Output/Response Input	I/O, OD

Signal Name ^[1]	Description ^[2]	Type ^[3]
SDC2-CLK	eMMC Clock Output	O
SDC2-D0	eMMC Data Input/ Output 0	I/O
SDC2-D1	eMMC Data Input/ Output 1	I/O
SDC2-D2	eMMC Data Input/ Output 2	I/O
SDC2-D3	eMMC Data Input/ Output 3	I/O
SDC2-D4	eMMC Data Input/ Output 4	I/O
SDC2-D5	eMMC Data Input/ Output 5	I/O
SDC2-D6	eMMC Data Input/ Output 6	I/O
SDC2-D7	eMMC Data Input/ Output 7	I/O
SDC2-RST	eMMC Reset	O
SDC2-DS	eMMC Data Strobe	I

4.3.8 Audio Codec

Table 4-36 Audio Codec Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
MICIN1P	Microphone Positive Input 1	AI
MICIN2P	Microphone Positive Input 2	AI
LINEOUTP	Lineout Positive Output	AO
VRA1	Internal Reference Voltage	AO
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G

4.3.9 I2S/PCM

Table 4-37 I2S/PCM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S0-DIN0	I2S0/PCM0 Serial Data Input 0	I
I2S0-DIN1	I2S0/PCM0 Serial Data Input 1	I
I2S0-DIN2	I2S0/PCM0 Serial Data Input 2	I

Signal Name ^[1]	Description ^[2]	Type ^[3]
I2S0-DIN3	I2S0/PCM0 Serial Data Input 3	I
I2S0-DOUT0	I2S0/PCM0 Serial Data Output 0	O
I2S0-DOUT1	I2S0/PCM0 Serial Data Output 1	O
I2S0-DOUT2	I2S0/PCM0 Serial Data Output 2	O
I2S0-DOUT3	I2S0/PCM0 Serial Data Output 3	O

4.3.10 SPI&SPI_DBI

Table 4-38 SPI&SPI_DBI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SPI0-CS0	SPI0 Chip Select 0 (Active Low)	I/O
SPI0-CS1	SPI0 Chip Select 1 (Active Low)	I/O
SPI0-CLK	SPI0 Clock	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0-HOLD	SPI0 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-CS0	SPI1 Chip Select 0 (Active Low)	I/O
SPI1-CS1	SPI1 Chip Select 1 (Active Low)	I/O
SPI1-CLK	SPI1 Clock	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-HOLD	SPI1 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
DBI-CSX	Chip Select Signal (Active Low)	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge.	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O
SPI2-CS0	SPI2 Chip Select 0 (Active Low)	I/O
SPI2-CS1	SPI2 Chip Select 1 (Active Low)	I/O
SPI2-CLK	SPI2 Clock	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O

4.3.11 SPI_Flash

Table 4-39 SPI_Flash Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SPIF-CS0	SPIF Peripheral Chip Select Signal 0, Low Active	O
SPIF-D4	SPIF Master Mode Data 4 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF-D5	SPIF Master Mode Data 5 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF-D6	SPIF Master Mode Data 6 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF-D7	SPIF Master Mode Data 7 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF-CLK	SPIF Master Mode Clock Output	O
SPIF-MOSI	SPIF Master Data Out, Slave Data In	I/O
SPIF-MISO	SPIF Master Data In, Slave Data Out	I/O
SPIF-DQS	SPIF Data Strobe Signal	I
SPIF-WP	SPIF Write Protection (Active Low)	I/O
SPIF-HOLD	SPIF Hold Signal	I/O

4.3.12 SQPI PSRAM

Table 4-40 SQPI PSRAM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
SQPI-CLK	SQPI Clock	I/O
SQPI-CS0	SQPI Chip Select 0 (Active Low)	I/O
SQPI-MOSI-IO0	SQPI Master Data Out, Slave Data In	I/O
SQPI-MISO-IO1	SQPI Master Data In, Slave Data Out	I/O
SQPI-WP-IO2	SQPI Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SQPI-HOLD-IO3	SQPI Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O

4.3.13 MIPI CSI

Table 4-41 MIPI CSI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
MCSI0-MCLK	MIPI CSI A Master Clock	O
MCSIA-CKN	MIPI CSI A Differential Receive Clock Signal (Negative)	AI
MCSIA-CKP	MIPI CSI A Differential Receive Clock Signal (Positive)	AI
MCSIA-D0N	MIPI CSI A Data Line 0 Input (Negative)	AI
MCSIA-D0P	MIPI CSI A Data Line 0 Input (Positive)	AI
MCSIA-D1N/MCSIC-D0N	MIPI CSI A Data Line 1 Input (Negative)/MIPI CSI C Data Line 0 Input (Negative)	AI
MCSIA-D1P/MCSIC-D0P	MIPI CSI A Data Line 1 Input (Positive)/MIPI CSI C Data Line 0 Input (Positive)	AI
MCSI1-MCLK	MIPI CSI B Master Clock	O
MCSIB-CKN	MIPI CSI B Differential Receive Clock Signal (Negative)	AI
MCSIB-CKP	MIPI CSI B Differential Receive Clock Signal (Positive)	AI
MCSIB-D0N/MCSIA-D3N	MIPI CSI B Data Line 0 Input (Negative)/MIPI CSI A Data Line 3 Input (Negative)	AI

Signal Name ^[1]	Description ^[2]	Type ^[3]
MCSIB-D0P/MCSIA-D3P	MIPI CSI B Data Line 0 Input (Positive)/MIPI CSI A Data Line 3 Input (Positive)	AI
MCSIB-D1N/MCSIC-CKN/MCSIA-D2N	MIPI CSI B Data Line 1 Input (Negative)/MIPI CSI C Differential Receive Clock Signal (Negative)/MIPI CSI A Data Line 2 Input (Negative)	AI
MCSIB-D1P/MCSIC-CKP/MCSIA-D2P	MIPI CSI B Data Line 1 Input (Positive)/MIPI CSI C Differential Receive Clock Signal (Positive)/MIPI CSI A Data Line 2 Input (Positive)	AI
MCSI2-MCLK	MIPI CSI C Master Clock	O
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC 0	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC 1	I/O
VCC18-MCSI	MIPI CSI Power Supply	P

4.3.14 Parallel CSI

Table 4-42 Parallel CSI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
NCSI-PCLK	Parallel CSI Pixel Clock Input	I
NCSI-MCLK	Parallel CSI Master Clock Output	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous Input	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous Input	I
NCSI-D0	Parallel CSI Pixel Data 0	I
NCSI-D1	Parallel CSI Pixel Data 1	I
NCSI-D2	Parallel CSI Pixel Data 2	I
NCSI-D3	Parallel CSI Pixel Data 3	I
NCSI-D4	Parallel CSI Pixel Data 4	I
NCSI-D5	Parallel CSI Pixel Data 5	I
NCSI-D6	Parallel CSI Pixel Data 6	I
NCSI-D7	Parallel CSI Pixel Data 7	I
NCSI-D8	Parallel CSI Pixel Data 8	I

Signal Name ^[1]	Description ^[2]	Type ^[3]
NCSI-D9	Parallel CSI Pixel Data 9	I
NCSI-D10	Parallel CSI Pixel Data 10	I
NCSI-D11	Parallel CSI Pixel Data 11	I
NCSI-D12	Parallel CSI Pixel Data 12	I
NCSI-D13	Parallel CSI Pixel Data 13	I
NCSI-D14	Parallel CSI Pixel Data 14	I
NCSI-D15	Parallel CSI Pixel Data 15	I

4.3.15 LCD

Table 4-43 LCD Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
LCD-CLK	LCD Clock	O
LCD-VSYNC	LCD Vertical Synchronization	O
LCD-HSYNC	LCD Horizontal Synchronization	O
LCD-DE	LCD Data Enable	O
TCON-FSYNC	Frame Synchronization Signal for TCON and Sensor	O
LCD-D0	LCD Data Input/Output 0	I/O
LCD-D1	LCD Data Input/Output 1	I/O
LCD-D2	LCD Data Input/Output 2	I/O
LCD-D3	LCD Data Input/Output 3	I/O
LCD-D4	LCD Data Input/Output 4	I/O
LCD-D5	LCD Data Input/Output 5	I/O
LCD-D6	LCD Data Input/Output 6	I/O
LCD-D7	LCD Data Input/Output 7	I/O
LCD-D8	LCD Data Input/Output 8	I/O
LCD-D9	LCD Data Input/Output 9	I/O
LCD-D10	LCD Data Input/Output 10	I/O
LCD-D11	LCD Data Input/Output 11	I/O
LCD-D12	LCD Data Input/Output 12	I/O
LCD-D13	LCD Data Input/Output 13	I/O
LCD-D14	LCD Data Input/Output 14	I/O

Signal Name ^[1]	Description ^[2]	Type ^[3]
LCD-D15	LCD Data Input/Output 15	I/O
LCD-D16	LCD Data Input/Output 16	I/O
LCD-D17	LCD Data Input/Output 17	I/O
LCD-D18	LCD Data Input/Output 18	I/O
LCD-D19	LCD Data Input/Output 19	I/O
LCD-D20	LCD Data Input/Output 20	I/O
LCD-D21	LCD Data Input/Output 21	I/O
LCD-D22	LCD Data Input/Output 22	I/O
LCD-D23	LCD Data Input/Output 23	I/O

4.3.16 USB

Table 4-44 USB Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
USB0-DM	USB2.0 DRD Data Signal DM	AI/O
USB0-DP	USB2.0 DRD Data Signal DP	AI/O

4.3.17 GMAC

Table 4-45 GMAC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
RMII-RXD0	RMII Receive Data 0	I
RMII-TXD0	RMII Transmit Data 0	O
RMII-RXD1	RMII Receive Data 1	I
RMII-TXD1	RMII Transmit Data 1	O
RMII-TXCK	RMII Reference Clock	I
RMII-RXER	RMII Receive Error	I
RMII-CRS-DV	RMII Carrier Sense Receive Data Valid	I
RMII-TXEN	RMII Transmit Enable	O
RMII-MDC	RMII Management Data Clock	O
RMII-MDIO	RMII Management Data Input/ Output	I/O
RMII-EPHY-25M	PHY 25 MHz Clock Output	O

4.3.18 UART

Table 4-46 UART Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
UART0-RX	UART0 Data Receiver	I
UART0-TX	UART0 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART1-CTS	UART1 Clear to Send	I
UART1-RTS	UART1 Request to Send	O
UART2-RX	UART2 Data Receiver	I
UART2-TX	UART2 Data Transmitter	O
UART2-CTS	UART2 Clear to Send	I
UART2-RTS	UART2 Request to Send	O
UART3-RX	UART3 Data Receiver	I
UART3-TX	UART3 Data Transmitter	O
UART3-CTS	UART3 Clear to Send	I
UART3-RTS	UART3 Request to Send	O

4.3.19 TWI

Table 4-47 TWI Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O

4.3.20 PWM

Table 4-48 PWM Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
PWM-0	PWM Wave Output /Capture Wave Input 0	I/O
PWM-1	PWM Wave Output /Capture Wave Input 1	I/O
PWM-2	PWM Wave Output /Capture Wave Input 2	I/O
PWM-3	PWM Wave Output /Capture Wave Input 3	I/O
PWM-4	PWM Wave Output /Capture Wave Input 4	I/O
PWM-5	PWM Wave Output /Capture Wave Input 5	I/O
PWM-6	PWM Wave Output /Capture Wave Input 6	I/O
PWM-7	PWM Wave Output /Capture Wave Input 7	I/O
PWM-8	PWM Wave Output /Capture Wave Input 8	I/O
PWM-9	PWM Wave Output /Capture Wave Input 9	I/O
PWM-10	PWM Wave Output /Capture Wave Input 10	I/O
PWM-11	PWM Wave Output /Capture Wave Input 11	I/O
PWM-12	PWM Wave Output /Capture Wave Input 12	I/O
PWM-13	PWM Wave Output /Capture Wave Input 13	I/O
PWM-14	PWM Wave Output /Capture Wave Input 14	I/O
PWM-15	PWM Wave Output /Capture Wave Input 15	I/O

4.3.21 GPADC

Table 4-49 GPADC Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
GPADC0	General Purpose ADC Input Channel 0	AI
GPADC1	General Purpose ADC Input Channel 1	AI
GPADC2	General Purpose ADC Input Channel 2	AI
GPADC3	General Purpose ADC Input Channel 3	AI

4.3.22 JTAG

Table 4-50 JTAG Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
C907-JTAG-MS	C907 JTAG Mode Selection	I

Signal Name ^[1]	Description ^[2]	Type ^[3]
C907-JTAG-DI	C907 JTAG Data Input	I
C907-JTAG-DO	C907 JTAG Data Output	O
C907-JTAG-CK	C907 JTAG Clock Signal	I
E907-JTAG-MS	E907 JTAG Mode Selection	I
E907-JTAG-DI	E907 JTAG Data Input	I
E907-JTAG-DO	E907 JTAG Data Output	O
E907-JTAG-CK	E907 JTAG Clock Signal	I
JTAG-SEL	JTAG mode select =1: Force JTAG function to port H. =0: Software-selectable JTAG function (Port F or Port H), only one port can be selected (Default port F).	I

4.3.23 Power

Table 4-51 Power Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
VCC-PA	Digital Port A Power Supply	P
VCC-PC	Digital Port C Power Supply	P
VCC-PD	Digital Port D Power Supply	P
VCC-PE	Digital Port E Power Supply	P
VCC-PG	Digital Port G Power Supply	P
VCC-PL	Digital Port L Power Supply	P
VCC33-PF-USB	Digital Port F&USB 3.3V Power Supply	P
VCC18-PF	Digital Port F 1.8V Power Supply	P
VCC-IO	GPIO Power Supply	P
VDD-SYS	System Power Supply	P
VDD-SYSFB	System Power Supply Feedback	P
VCC-EFUSE	Power Supply for eFuse	P

4.3.24 Interrupt

Table 4-52 Interrupt Signal Description

Signal Name ^[1]	Description ^[2]	Type ^[3]
PA-EINT [21:0]	Port A Interrupt	I
PC-EINT [11:0]	Port C Interrupt	I
PD-EINT [22:0]	Port D Interrupt	I
PE-EINT [17:0]	Port E Interrupt	I
PF-EINT [6:0]	Port F Interrupt	I
PG-EINT [7:0]	Port G Interrupt	I
PH-EINT [15:0]	Port H Interrupt	I
PL-EINT [6:0]	Port L Interrupt	I

5 Electrical characteristics

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.



CAUTION

Stresses beyond those listed under Table 5-1 Absolute Maximum Ratings may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 5.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Supply Name	Description	Min ⁽¹⁾	Max ⁽¹⁾	Unit
For TFBGA 317 and TFBGA194				
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-DRAM	DRAM IO Power Supply	-0.3	VDDQ+0.3	V
VCC18-MCSI	MIPI CSI Power Supply	-0.3	2.16	V
VCC-PA	Digital Port A Power	-0.3	3.96	V
VCC-PC	Digital Port C Power	-0.3	3.96	V
VCC-PD	Digital Port D Power	-0.3	3.96	V
VCC-PE	Digital Port E Power	-0.3	3.96	V
VCC18-PF	Digital Port F Power	-0.3	2.16	V
VCC33-PF-USB	Digital Port F&USB Power	-0.3	3.96	V
VCC-PG	Digital Port G Power	-0.3	3.96	V
VCC-PG-PE	Digital Port G&E Power	-0.3	3.96	V
VCC-IO	GPIO Power Supply	-0.3	3.96	V
VCC-EFUSE	eFuse Power Supply	-0.3	2.16	V
VCC-RTC	RTC Power Supply	-0.3	2.16	V
VCC-PLL	System PLL Supply	-0.3	2.16	V

Supply Name	Description	Min ⁽¹⁾	Max ⁽¹⁾	Unit
VDD-SYS	System Power Supply	-0.3	1.08	V
VDD18-DRAM	SDRAM Controller Power Supply	-0.3	2.16	V
VCCIO-WIFI	Wi-Fi GPIO Power	-0.3	3.96	V
VCC33-WIFI	Supply Voltage for Wi-Fi System	-0.3	3.96	V
AVDD33-TX	Supply Voltage for RF_PA+LNA	-0.3	3.96	V
For QFN128				
AVCC-PLL	Power Supply for Analog Part & PLL & GPADC	-0.3	2.16	V
VCC-DRAM	DRAM IO Power Supply	-0.3	VDDQ+0.3	V
VCC18-PA-EFUSE	PA & eFuse Power Supply	-0.3	2.16	V
VCC-PE-PC-USB	PC & PE & USB Power Supply	-0.3	3.96	V
VDD18-DRAM&VCC18-PF	SDRAM Controller Power Supply& Digital Port F Power Supply	-0.3	2.16	V
VCC-PD	Digital Port D Power	-0.3	3.96	V
VCC-PG	Digital Port G Power	-0.3	3.96	V
VCC-IO	PF & PH Power Supply	-0.3	3.96	V
VCC-RTC	RTC Power Supply	-0.3	2.16	V
VDD-SYS	System Power Supply	-0.3	1.08	V

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

5.2 ESD and Latch-up Ratings

Table 5-2 ESD and Latch-up Ratings

Parameter	Value	Conditions	Unit
V _{ESD} ⁽¹⁾	Human Body Model (HBM)	±2000	ESDA/JEDEC JS-001-2024
	Charged Device Model (CDM)	±250	ESDA/JEDEC JS-002-2025
Latch up	I-test performance current-pulse injection on each IO pin	±200 mA	JESD78F.02; room temperature

Parameter	Value	Conditions	Unit
Over-voltage performance voltage injection on each IO pin	1.5 x Vddmax	JESD78F.02; room temperature	V

- (1) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

5.3 Recommended Operating Conditions

The following table describes operating conditions of the device.



NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-3 Recommended Operating Conditions

Supply Name	Description	Min	Typ	Max	Unit
For TFBGA 317 and TFBGA194					
AVCC	Power Supply for Analog Part	1.764	1.8	1.836	V
VCC-DRAM	Power Supply for DRAM IO and DDR3/DDR3L	1.2825	1.35	1.4175	V
	Power Supply for DRAM IO and DDR3/DDR2	1.425	1.5	1.575	V
	Power Supply for DRAM IO and DDR2	1.71	1.8	1.89	V
VCC18-MCSI	MIPI CSI Power Supply	1.71	1.8	1.98	V
VCC-PA	Digital Port A Power 1.8 V Voltage	1.71	1.8	1.98	V
	3.3 V Voltage	2.97	3.3	3.63	
VCC-PC	Digital Port C Power 1.8 V Voltage	1.71	1.8	1.98	V
	3.3 V Voltage	2.97	3.3	3.63	
VCC-PD	Digital Port D Power 1.8 V Voltage	1.71	1.8	1.98	V
	3.3 V Voltage	2.97	3.3	3.63	
VCC-PE	Digital Port E Power 1.8 V Voltage	1.71	1.8	1.98	V
	3.3 V Voltage	2.97	3.3	3.63	

Supply Name	Description	Min	Typ	Max	Unit
VCC18-PF	Digital Port F Power 1.8 V Voltage	1.71	1.8	1.98	V
VCC33-PF-USB	Digital Port F&USB Power 3.3 V Voltage	2.97	3.3	3.63	V
VCC-PG	Digital Port G Power 1.8 V Voltage 3.3 V Voltage	1.71 2.97	1.8 3.3	1.98 3.63	V
VCC-PG-PE	Digital Port G&E Power 1.8 V Voltage 3.3 V Voltage	1.71 2.97	1.8 3.3	1.98 3.63	V
VCC-IO	GPIO Power Supply	2.97	3.3	3.63	V
VCC-EFUSE	eFuse Power Supply	1.71	1.8	1.89	V
VCC-RTC	RTC Power Supply	1.71	1.8	1.89	V
VCC-PLL	System PLL Supply	1.746	1.8	1.854	V
VDD-SYS	System Power Supply	0.9	-	1.00	V
VDD18-DRAM	SDRAM Controller Power Supply	1.71	1.8	1.89	V
VCCIO-WIFI	Wi-Fi GPIO Power	1.71 2.97	1.8 3.3	1.98 3.63	V
VCC33-WIFI	Supply Voltage for Wi-Fi System	3	3.3	3.6	V
AVDD33-TX	Supply Voltage for RF_PA+LNA	3	3.3	3.6	V
For QFN128					
AVCC-PLL	Power Supply for Analog Part & PLL & GPADC	1.764	1.8	1.836	V
VCC-DRAM	Power Supply for DRAM IO and DDR3/DDR3L	1.2825	1.35	1.4175	V
	Power Supply for DRAM IO and DDR3	1.425	1.5	1.575	V
VCC-PE-PC-USB	PC & PE & USB Power Supply	2.97	3.3	3.63	V
VDD18-DRAM&VCC18-PF	SDRAM Controller Power Supply& Digital Port F Power Supply	1.71	1.8	1.89	V
VCC-PD	Digital Port D Power 1.8 V Voltage 3.3 V Voltage	1.71 2.97	1.8 3.3	1.98 3.63	V

Supply Name	Description	Min	Typ	Max	Unit
VCC-PG	Digital Port G Power 1.8 V Voltage 3.3 V Voltage	1.71 2.97	1.8 3.3	1.98 3.63	V
VCC-IO	PF & PH Power Supply	2.97	3.3	3.63	V
VCC18-PA-MCSI-EFUSE	PA & MIPI CSI & eFuse Power Supply	1.71	1.8	1.89	V
VCC-RTC	RTC Power Supply	1.71	1.8	1.89	V
VDD-SYS	System Power Supply	0.9	-	1.00	V

5.4 PLL Electrical Characteristics

The following table describes PLL Electrical Characteristics.

Table 5-4 PLL Electrical Characteristics

PLL Type	Frequency of VCO's Output	Linear FM	Lock Time
PLL_CPU	480 MHz - 2.016 GHz	Yes	500us
PLL_DDR	1.8 GHz - 3.6 GHz	No	500us
PLL_PERI	1.26 GHz - 2.52 GHz	No	500us
PLL_VIDEO	1.26 GHz - 2.52 GHz	No	500us
PLL_CSI	1.26 GHz - 2.52 GHz	No	500us
PLL_AUDIO	1.536 GHz - 3.12 GHz	No	500us
PLL_NPU	1.26 GHz - 2.52 GHz	No	500us

5.5 GPIO DC Electrical Characteristics

Table 5-5 summarizes the GPIO DC electrical characteristics of the device.

Table 5-5 GPIO DC Electrical Characteristics⁽¹⁾

(VCC: VCC-IO/VCC-PA/VCC-PC/VCC-PD/VCC-PE/VCC33-PF-USB/VCC18-PF/VCC-PG/VCC-RTC/VCC-PE-PC-USB)

Symbol	Parameter		Min	Typ	Max	Unit
V _{IH}	High-Level Input Voltage		0.7 * VCC	-	1.1*VCC	V
V _{IL}	Low-Level Input Voltage		-0.3	-	0.3 * VCC	V
R _{PU}	Output Pull-up Resistance	PC1-PC11, PF3	9	15	21	kΩ
		PG0, PG1, PG3, PG4, PG5	19.8	33	46.2	kΩ

Symbol	Parameter		Min	Typ	Max	Unit
		Other GPIOs	60	100	140	kΩ
R _{PD}	Output Pull-down Resistance	PC1-PC11, PF3	9	15	21	kΩ
		PG0, PG1, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
		Other GPIOs	60	100	140	kΩ
I _{IH}	High-Level Input Current		-	-	10	uA
I _{IL}	Low-Level Input Current		-	-	10	uA
V _{OH}	High-Level Output Voltage		VCC - 0.3	-	VCC	V
V _{OL}	Low-Level Output Voltage		0	-	0.2	V
I _{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C _{IN}	Input Capacitance		-	-	5	pF
C _{OUT}	Output Capacitance		-	-	5	pF

(1) Guaranteed by design.

5.6 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 5-1 SMHC Voltage Waveform

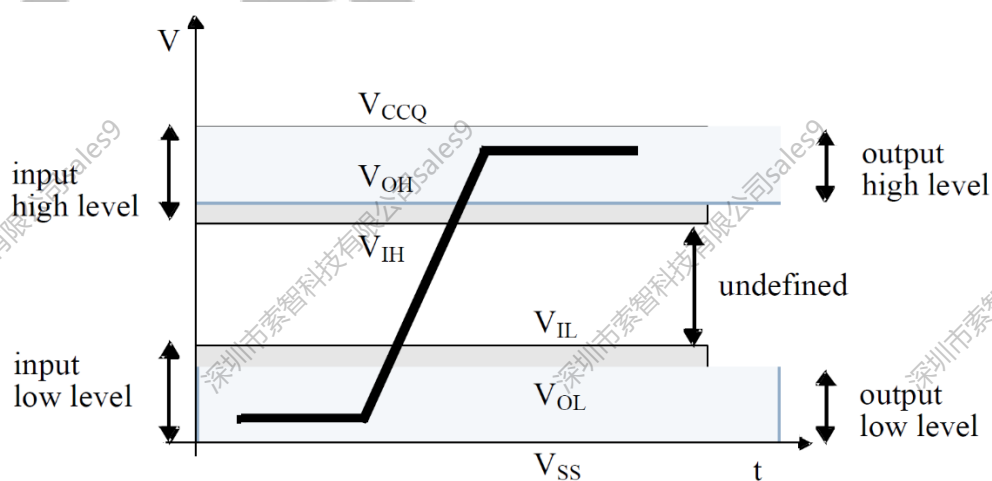


Table 5-6 shows 3.3 V SMHC electrical parameters.

Table 5-6 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V _{CCQ}	I/O voltage	2.7		3.6	V

Symbol	Parameter	Min	Typ	Max	Unit
V _{OH}	Output high-level voltage	0.75 * V _{CCQ}	-	-	V
V _{OL}	Output low-level voltage	-	-	0.125 * V _{CCQ}	V
V _{IH}	Input high-level voltage	0.625 * V _{CCQ}	-	V _{CCQ} + 0.3	V
V _{IL}	Input low-level voltage	V _{SS} - 0.3	-	0.25 * V _{CCQ}	V

Table 5-7 shows 1.8 V SMHC electrical parameters.

Table 5-7 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7		3.6	V
V _{CCQ}	I/O voltage	1.7		1.95	V
V _{OH}	Output high-level voltage	V _{CCQ} - 0.45	-	-	V
V _{OL}	Output low-level voltage	-	-	0.45	V
V _{IH}	Input high-level voltage	0.65 * V _{CCQ} ⁽¹⁾	-	V _{CCQ} + 0.3	V
V _{IL}	Input low-level voltage	V _{SS} - 0.3	-	0.35 * V _{CCQ} ⁽²⁾	V
(1).0.7 * V _{CCQ} for MMC4.3 or lower.					
(2).0.3 * V _{CCQ} for MMC4.3 or lower.					

5.7 GPADC Electrical Characteristics

Table 5-8 lists the GPADC electrical characteristics.

Table 5-8 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	AVCC	V
Absolute Maximum Input Voltage	0	-	3.3	V
Sampling Rate	-	-	1	MHz
Conversion Time	0.5	-	-	us

5.8 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz, ADC fs = 16 kHz, input gain = 0 dB, 16-bit audio data unless otherwise stated.

Table 5-9 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTP					
	Full-scale	0dBFS 1kHz	-	540	-	mVrms
	SNR(A-weighted)	0data	-	90	-	dB
	THD+N	0dBFS 1kHz	-	-85	-	dB
ADC Path	MICIN via ADC					
	Output Level	MICP=3.3Vpp/2, MICN=3.3Vpp/2, 1kHz, 0dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	95	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=1.65Vpp/2, MICN=1.65Vpp/2, 1kHz, 6dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	90	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=0.414Vpp/2, MICN=0.414Vpp/2, 1kHz, 18dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	80	-	dB
	THD+N		-	-80	-	dB
	Output Level	MICP=0.208Vpp/2, MICN=0.208Vpp/2, 1kHz, 24dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	74	-	dB
	THD+N		-	-69	-	dB
	Output Level	MICP=0.053Vpp/2, MICN=0.053Vpp/2, 1kHz, 36dB Gain	-	880	-	mFFS
	SNR(A-weighted)		-	61	-	dB
	THD+N		-	-54	-	dB

5.9 External Clock Source Electrical Characteristics

5.9.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-10 High-speed 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C ⁽¹⁾	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance ⁽²⁾	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of the device. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 5-11 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1 , C_2 , and C_{shunt} .

The total load capacitance is $C_L = [(C_1 * C_2) / (C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.

- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{\text{pkg}} + C_{\text{PCB}}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

5.9.2 Low-speed Crystal/Ceramic Resonator Characteristics

This device contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.

This device also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-12 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
$f_{\text{X32K_IN}}$	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C ⁽¹⁾	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance ⁽²⁾	-	1.35	-	pF

This device has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.

The 1.35 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

5.10 Interface Timing Characteristics

5.10.1 SMHC Interface Timing

5.10.1.1 HS-SDR Mode



NOTE

IO voltage is 1.8V or 3.3V.

Figure 5-2 SMHC HS-SDR Mode Output Timing Diagram

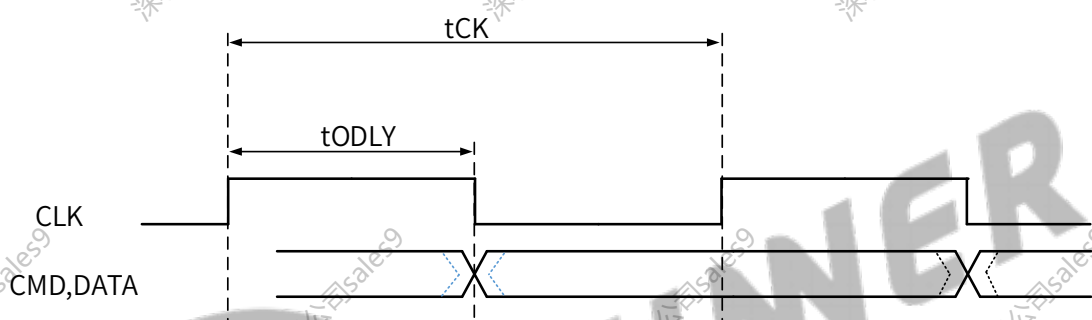


Table 5-13 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	30	50	70	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz.					
(2) The driver strength level of GPIO is 2 for test.					

Figure 5-3 SMHC HS-SDR Mode Input Timing Diagram

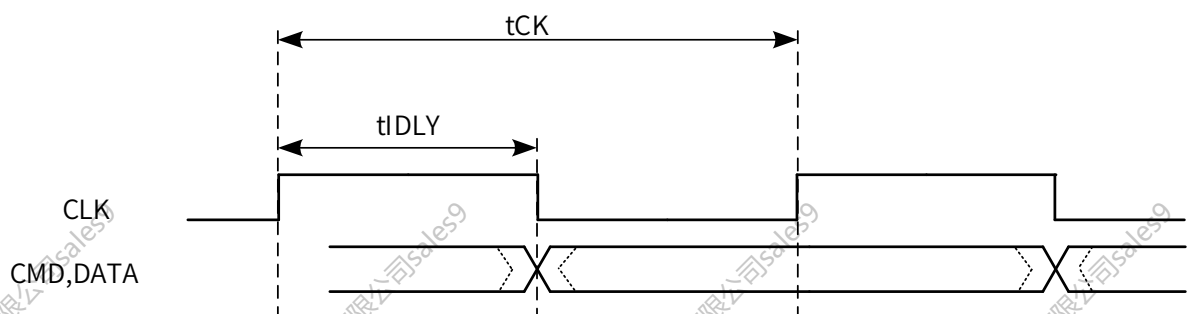


Table 5-14 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	30	50	70	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
The driver strength level of GPIO is 2 for test.					

5.10.1.2 HS-DDR Mode

Figure 5-4 SMHC HS-DDR Mode Output Timing Diagram

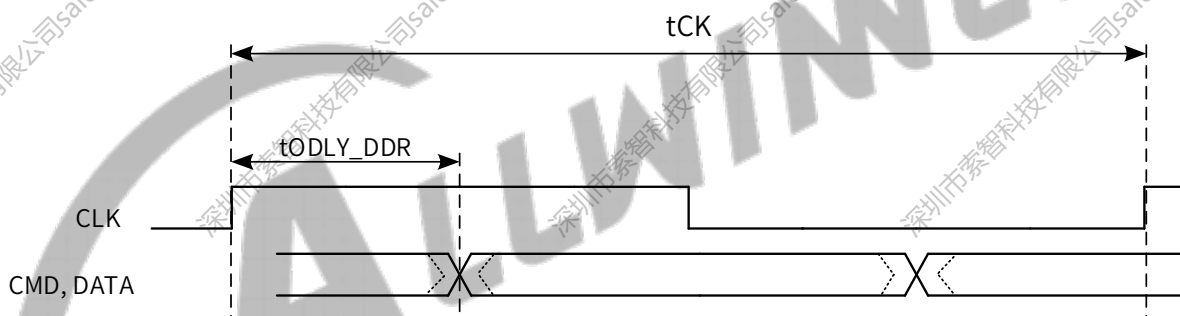


Table 5-15 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-5 SMHC HS-DDR Mode Input Timing Diagram

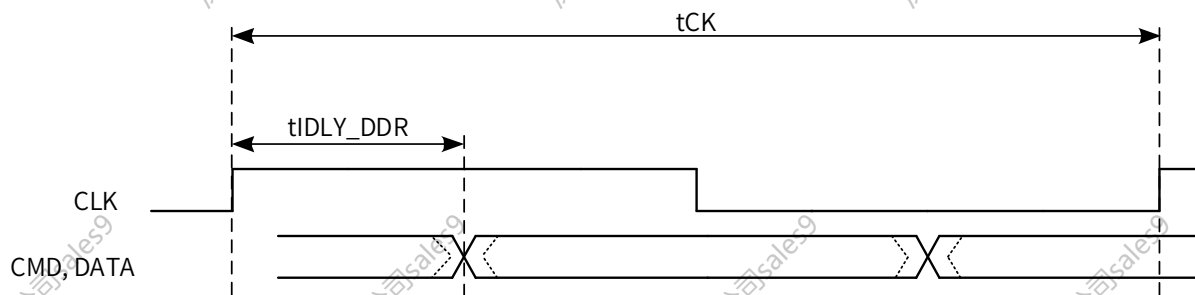


Table 5-16 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	t_{CK}	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
The driver strength level of GPIO is 2 for test.					

5.10.1.3 HS200/SDR104 Mode

Figure 5-6 SMHC HS200/SDR104 Mode Host Output and Device Input Timing Diagram

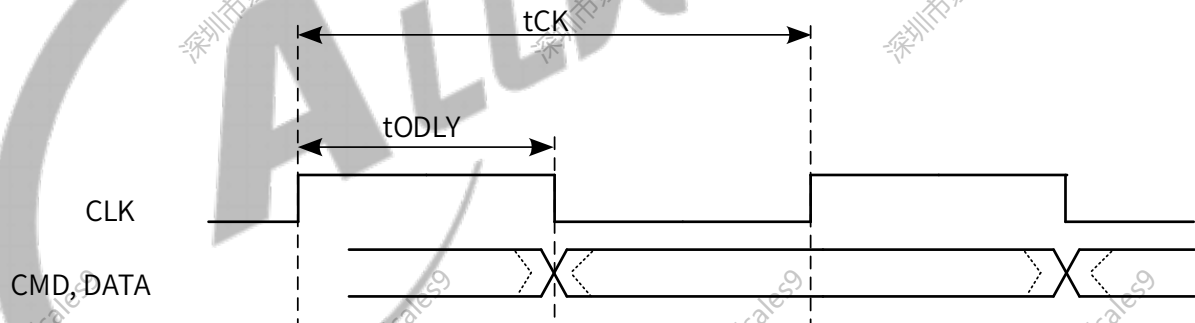


Table 5-17 SMHC HS200/SDR104 Mode Host Output and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	t_{CK}	-	-	150	MHz
Duty Cycle	DC	30	50	70	%
Rise time, fall time	t_{TLH} , t_{THL}	-	-	0.2	UI
Host Output CMD, DATA (referenced to CLK)					
Host CMD, Data output delay time	t_{ODLY}	-	0.25	0.5	UI

Parameter	Symbol	Min	Typ	Max	Unit
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.					

Figure 5-7 SMHC HS200/SDR104 Mode Host Input and Device Output Timing Diagram

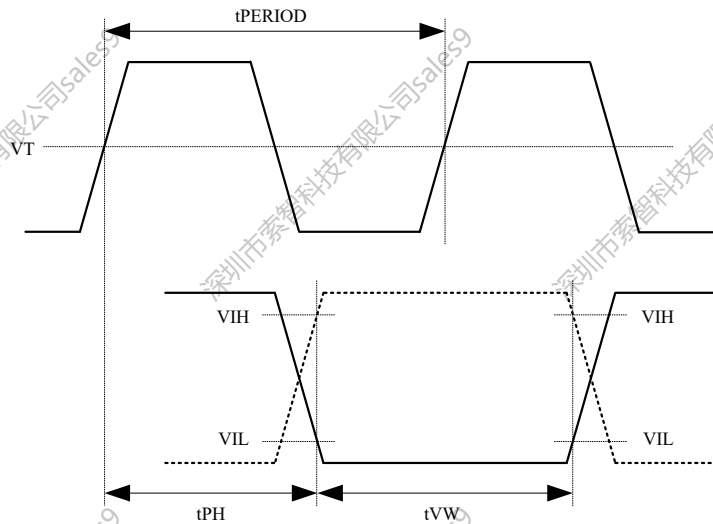


Table 5-18 SMHC HS200/SDR104 Mode Host Input and Device Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	6.66	-	-	ns	Max: 150 MHz
Duty Cycle	DC	30	50	70	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Host Input CMD, DATA (referenced to CLK)						
Device Output delay	tPH	0	-	2	UI	
Device Output delay variation due to temperature change after tuning	dPH	-350 ⁽³⁾	-	1550 ⁽⁴⁾	ps	
Device CMD, Data valid window	tVW	0.575	-	-	UI	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test. (3) Temperature variation: -20 °C. (4) Temperature variation: 90 °C.						

5.10.1.4 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 5-8 SMHC HS400 Mode Host Output Timing and Device Input Timing Diagram

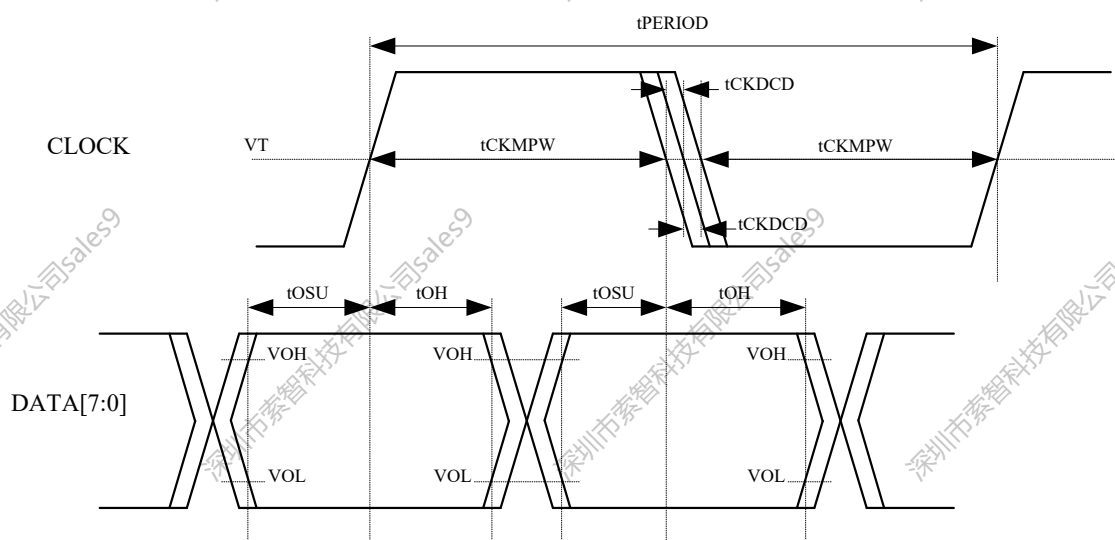


Table 5-19 SMHC HS400 Mode Host Output Timing and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	t_{PERIOD}	6.66	-	-	ns	Max: 150 MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	t_{CKDCD}	0	-	0.5	ns	
Clock minimum pulse width	t_{CKMPW}	2.2	-	-	ns	
Output DATA (referenced to CLK)						
Data output setup time	t_{OSU}	0.4	-	-	ns	
Data output hold time	t_{OH}	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.						
(2) The driver strength level of GPIO is 3 for test.						

Figure 5-9 SMHC HS400 Mode Host Input Timing and Device Output Timing Diagram

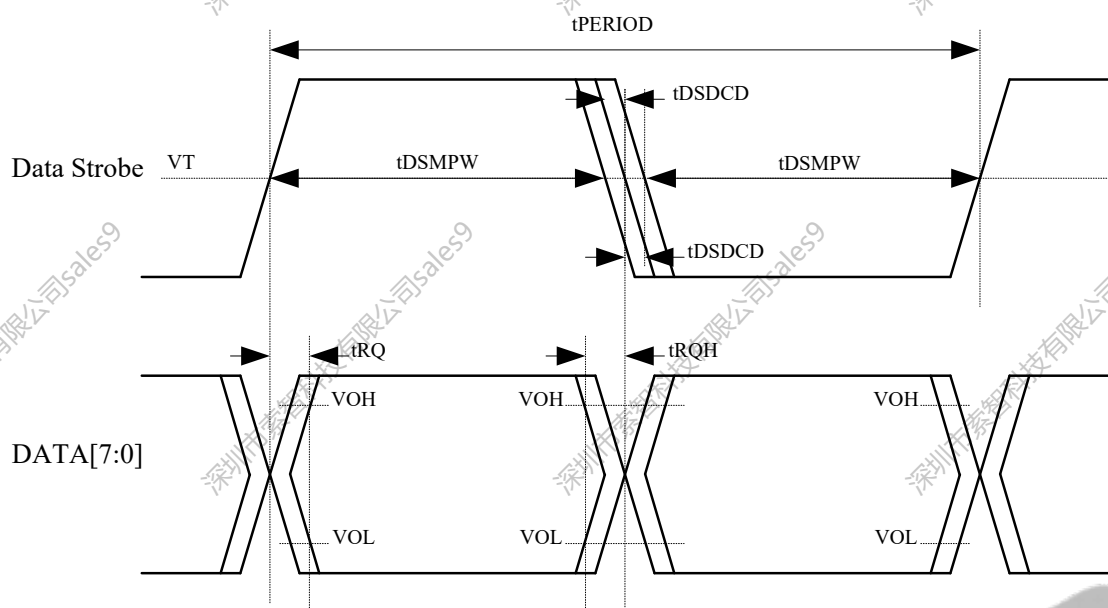


Table 5-20 SMHC HS400 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS (Data Strobe)						
DS period	t_{PERIOD}	6.66	-	-	ns	Max: 150 MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	t_{DSDCD}	0.0	-	0.4	ns	
DS minimum pulse width	t_{DSMPW}	2.0	-	-	ns	
Input DATA (referenced to DS)						
Data input skew	t_{RQ}	-	-	0.4	ns	
Data input hold skew	t_{RQH}	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

5.10.2 LCD Interface Timing

Figure 5-10 HV_IF Vertical Timing

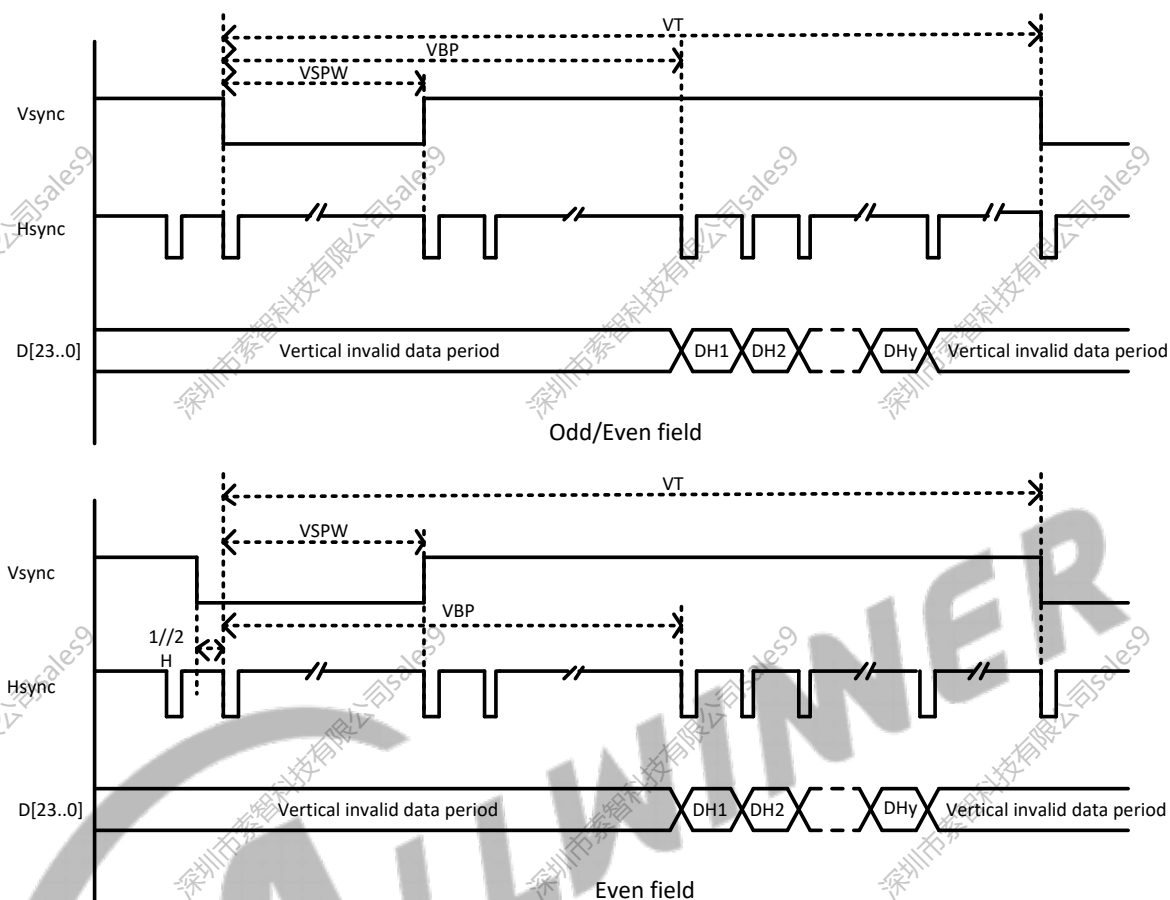


Figure 5-11 HV_IF Horizontal Timing

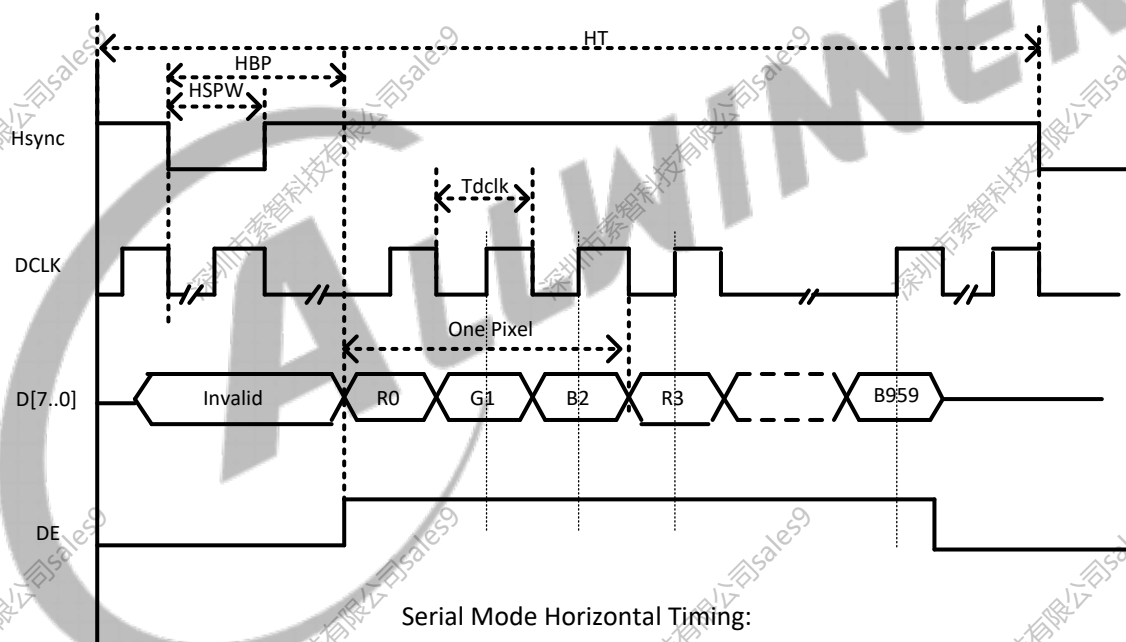
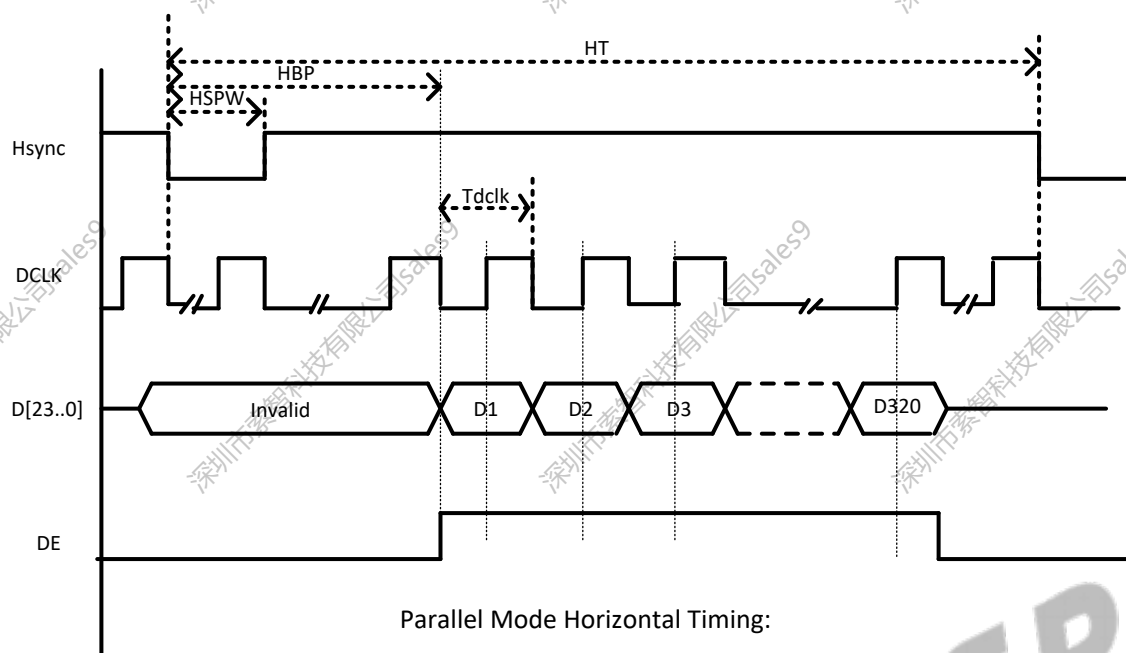


Table 5-21 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5.9	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

- (1) Vsync: Vertical sync, indicates one new frame.
- (2) Hsync: Horizontal sync, indicate one new scan line.
- (3) DCLK: Dot clock, pixel data are sync by this clock.
- (4) LDE: LCD data enable.
- (5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

Figure 5-12 Parallel CSI Data Sample Timing

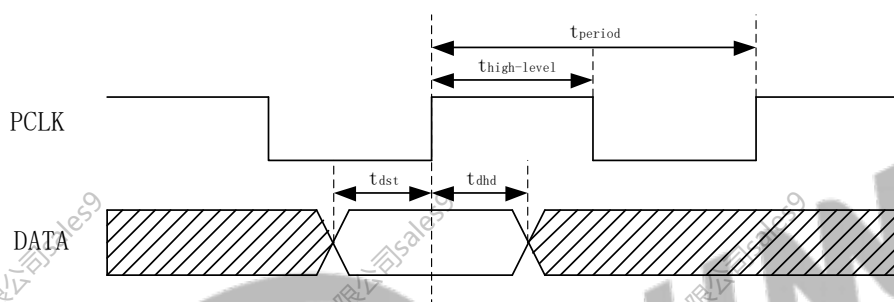


Table 5-22 Parallel CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.73	-	-	ns
Pclk frequency	$1/t_{\text{period}}$	-	-	148.5	MHz
Pclk duty	$t_{\text{high-level}}/t_{\text{period}}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.10.4 MIPI CSI Interface Timing

Figure 5-13 MIPI CSI Interface Timing

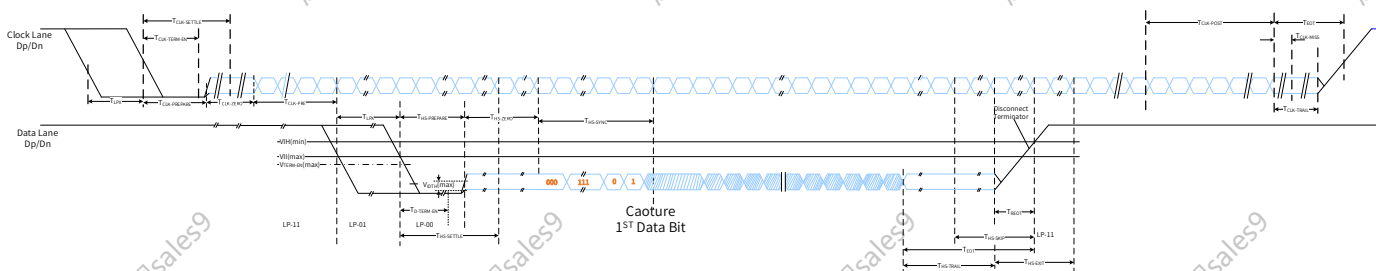


Table 5-23 MIPI CSI Interface Timing Constants

Parameter	Description	Min	Typ	Max	Unit	Notes
T _{CLK-MISS}	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	1, 6
T _{CLK-POST}	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of T _{CLK-TRAIL} .	60ns + 52*UI			ns	5
T _{CLK-PRE}	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	5
T _{CLK-PREPARE}	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	5
T _{CLK-SETTLE}	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns	6,7
T _{CLK-TERM-EN}	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V _{IL,MAX} .	Time for Dn to reach V _{TERM-EN}		38	ns	6
T _{CLK-TRAIL}	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	5
T _{CLK-PREPARE} + T _{CLK-ZERO}	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	5
T _{D-TERM-EN}	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses V _{IL,MAX} .	Time for Dn to reach V _{TERM-EN}		35ns + 4*UI		6
T _{EOT}	Transmitted time interval from the start of T _{HS-TRAIL} or T _{CLK-TRAIL} , to the start			105ns + n*12*UI		3,5

Parameter	Description	Min	Typ	Max	Unit	Notes
	of the LP-11 state following a HS burst.					
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	5
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	$40ns + 4*UI$		$85ns + 6*UI$	ns	5
$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	$145ns + 10*UI$			ns	5
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	$85ns + 6*UI$		$145ns + 10*UI$	ns	6
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40			ns	6
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	$\max(n*8*UI, 60ns + n*4*UI)$			ns	2, 3, 5
T_{INIT}		100			ns	5
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	4,5
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2	ns	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns	5

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4 \cdot T_{LPX}$			ns	5
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2 \cdot T_{LPX}$	ns	5
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	5



NOTE

1. The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.
2. If $a > b$ then $\max(a, b) = a$ otherwise $\max(a, b) = b$.
3. Where $n = 1$ for Forward-direction HS mode and $n = 4$ for Reverse-direction HS mode.
4. T_{LPX} is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.
5. Transmitter-specific parameter.
6. Receiver-specific parameter.
7. The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

5.10.5 GMAC Interface Timing

Figure 5-14 RMII Receive Timing

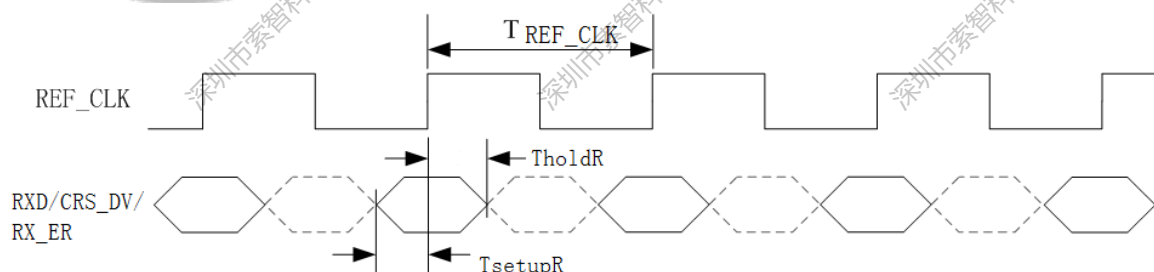


Figure 5-15 RMII Transmit Timing

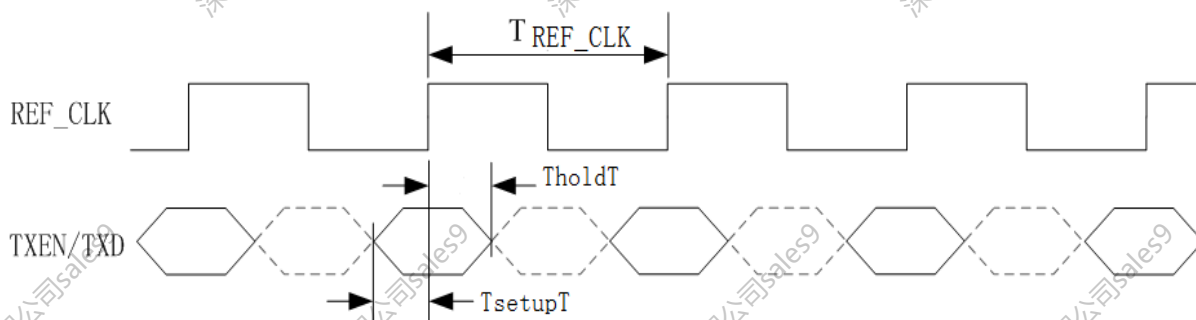


Table 5-24 RMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
T_{duty}	REF_CLK duty cycle	35		65	%
T_{setupT}	TXD/TXEN to REF_CLK setup time	4			ns
T_{holdT}	TXD/TXEN to REF_CLK hold time	2			ns
T_{setupR}	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
T_{holdR}	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

5.10.6 SPI Interface Timing

Figure 5-16 SPI Writing Timing

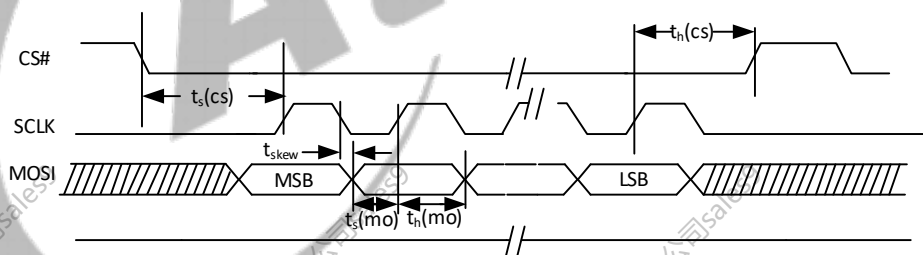


Figure 5-17 SPI Reading Timing

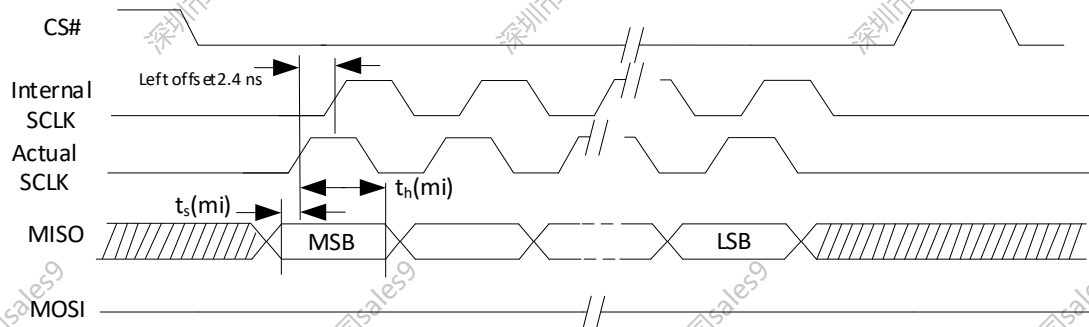


Table 5-25 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	$t_s(cs)$	$2T^{(1)}$	-	-	ns
CS# Active Hold Time	$t_h(cs)$	$2T^{(1)}$	-	-	ns
CLK/Data output skew time	$t_{skew}^{(2)}$	-	-	1	ns
Data output Delay Time	$t_s(mo)$	$T^{(1)}/2 - t_{skew}$	-	$T^{(1)}/2 + t_{skew}$	ns
Data output Hold Time	$t_h(mo)$	$T^{(1)}/2 - t_{skew}$	-	$T^{(1)}/2 + t_{skew}$	ns
Data In Setup Time	$t_s(mi)$	0.2(master mode) 4.5(slave mode)	-	-	ns
Data In Hold Time	$t_h(mi)$	0.2(master mode) 2(slave mode)	-	-	ns

(1) T is the cycle of clock.

(2) t_{skew} is the output skew time between SCLK and MOSI. SCLK may be either faster or slower than MOSI.

5.10.7 SPI-DBI Interface Timing

Figure 5-18 DBI 3-line Serial Interface Timing

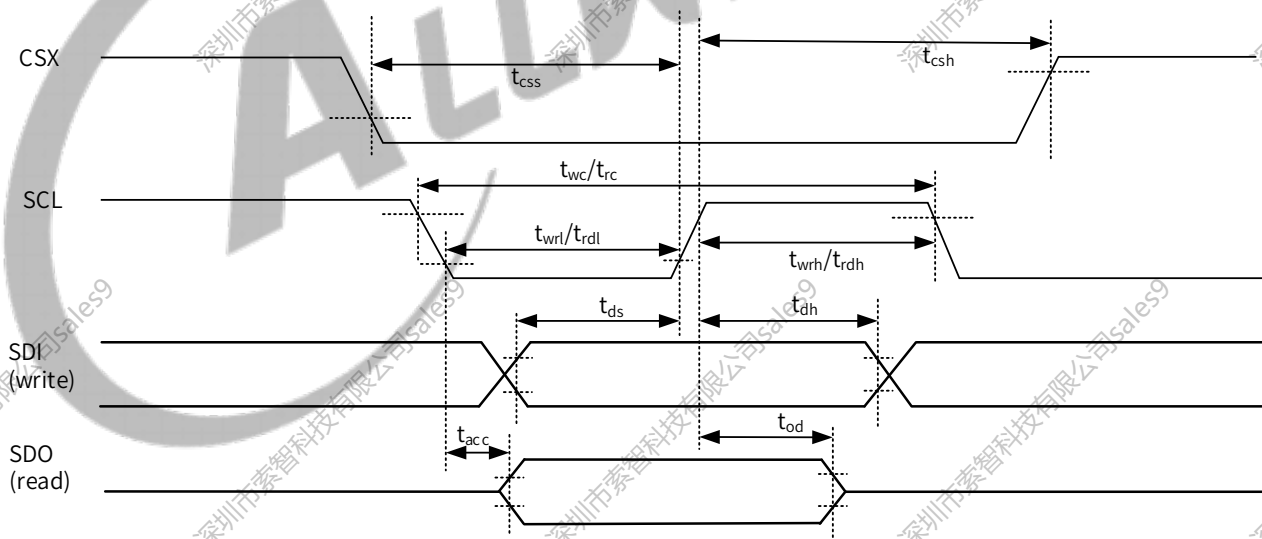


Table 5-26 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse "H" duration	t_{wrh}	7		ns
	Control pulse "L" duration	t_{wrl}	7		ns

Signal	Parameter	Symbol	Min	Max	Unit
SDI/SDO	Data setup time	t_{ds}	7 ⁽¹⁾		ns
	Data hold time	t_{dt}	7 ⁽¹⁾		ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-27 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10 ⁽¹⁾	50	ns
	Output disable time	t_{od}	15 ⁽¹⁾	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 5-19 DBI 4-line Serial Interface Timing

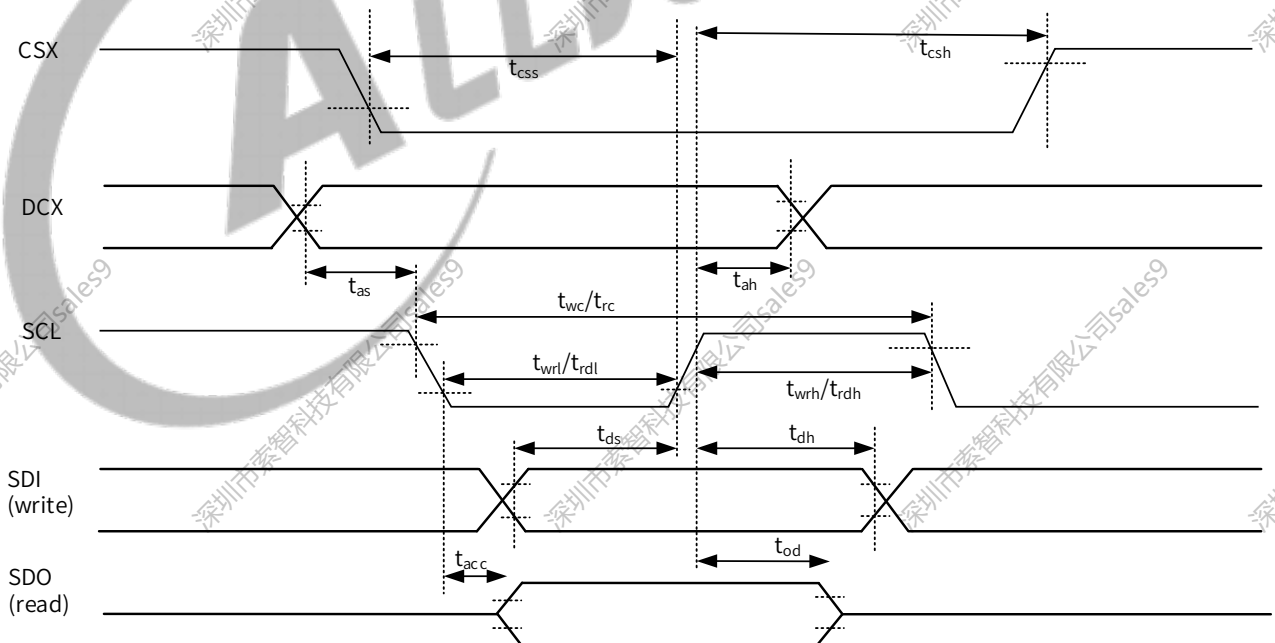


Table 5-28 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns

Signal	Parameter	Symbol	Min	Max	Unit
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7 ⁽¹⁾		ns
	Data hold time	t_{dt}	7 ⁽¹⁾		ns
	Output disable time	t_{od}	15 ⁽¹⁾	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-29 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15 ⁽¹⁾	50	ns

Signal	Parameter	Symbol	Min	Max	Unit
Note: Range of required clock frequency: 0-6.67 MHz.					

5.10.8 SPI Flash Interface Timing

5.10.8.1 Controller Output to Target Input Timing

Figure 5-20 xSPI Target Data Input Timing

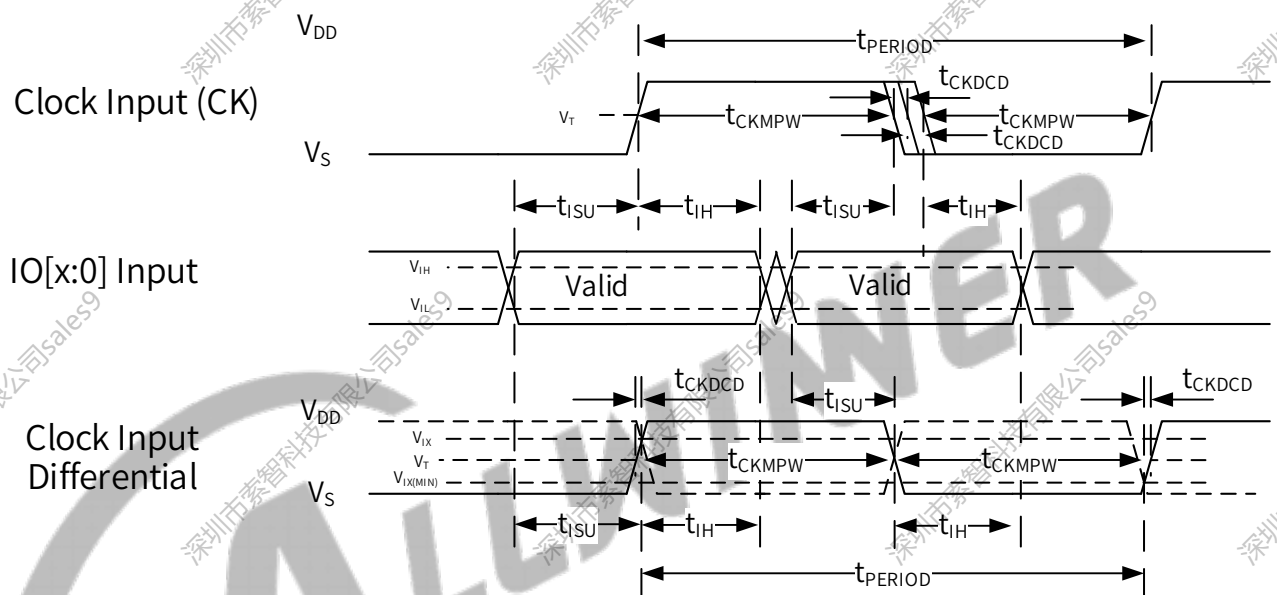


Table 5-30 Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	$V_{T(AC)}$	$0.50 * V_{DD}$	$0.50 * V_{DD}$	V
Input differential crossing (AC)	$V_{IX(AC)}$	$0.4 * V_{DD}$	$0.60 * V_{DD}$	V

Table 5-31 xSPI Device Input Timing

Parameter	Symbol	xSPI-333 ⁽¹⁾		xSPI-266 ⁽²⁾		xSPI-200 ⁽³⁾		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Input CK									
Cycle Time Data Transfer Mode	t _{PERIOD}	6.66	-	7.5	-	10	-	ns	150 MHz (max) between the rising edges with respect to V _T .
Slew Rate	SR	0.94	-	0.75	-	0.56	-	V/ns	With respect to V _{IH} /V _{IL} .

Parameter	Symbol	xSPI-333 ⁽¹⁾		xSPI-266 ⁽²⁾		xSPI-200 ⁽³⁾		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Duty Cycle Distortion	t_{CKDCD}	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to V_T . Includes jitter and phase noise.
Minimum Pulse Width	t_{CKMPW}	2.7	-	3.375	-	4.5	-	ns	With respect to V_T .
Input Signals (Referenced to CK)									
Input Setup Time (DTR)	t_{ISUddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL} .
Input Hold Time (DTR)	t_{IHddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL} .
Input Setup Time (STR)	t_{ISU}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL} .
Input Hold Time (STR)	t_{IH}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL} .
Slew Rate @ 1.8 V	SR	0.94	--	0.75	-	0.56	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 3.0 V	SR	1.72	-	1.37	-	1.03	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.

Parameter	Symbol	xSPI-333 ⁽¹⁾		xSPI-266 ⁽²⁾		xSPI-200 ⁽³⁾		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Note: (1) xSPI-333: Up to 166 MHz; up to 333 MT/s. (2) xSPI-266: Up to 133 MHz; up to 266 MT/s. (3) xSPI-200: Up to 100 MHz; up to 200 MT/s.									

5.10.8.2 Target Output to Controller Input Timing

Figure 5-21 xSPI Target Data Output Timing

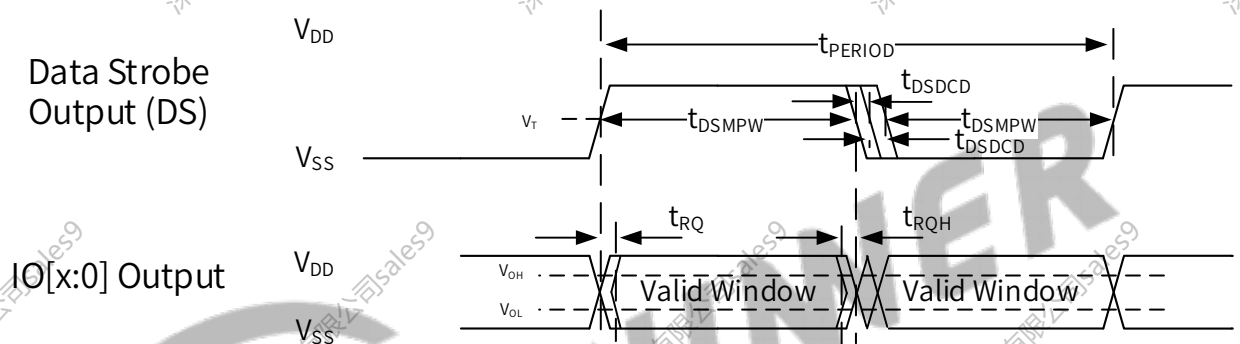


Table 5-32 xSPI Device Output Timing

Parameter	Symbol	xSPI-200 ⁽¹⁾		Unit	Comments
		Min	Max		
Data Strobe ⁽²⁾					
Cycle Time Data Transfer Mode	t _{PERIOD}	10	-	ns	100 MHz (max) between the rising edges with respect to V _T .
Duty Cycle Distortion	t _{DSDCD}	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (t _{CKDCD}) with respect to V _T . Includes jitter and phase noise.
Minimum Pulse Width	t _{DMPW}	4.1	-	ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With respect to V _T .
Output DATA (Referenced to DS)					
Output skew	t _{RQ}	-	0.8	ns	With respect to V _{OH} /V _{OL} and xSPI reference load.

Parameter	Symbol	xSPI-200 ⁽¹⁾		Unit	Comments
		Min	Max		
Output hold skew	t_{RQH}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Note: (1) xSPI-200: Up to 100 MHz; up to 200 MT/s. (2) Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their related (triggering) CK edges.					

5.10.9 UART Interface Timing

Figure 5-22 UART RX Timing

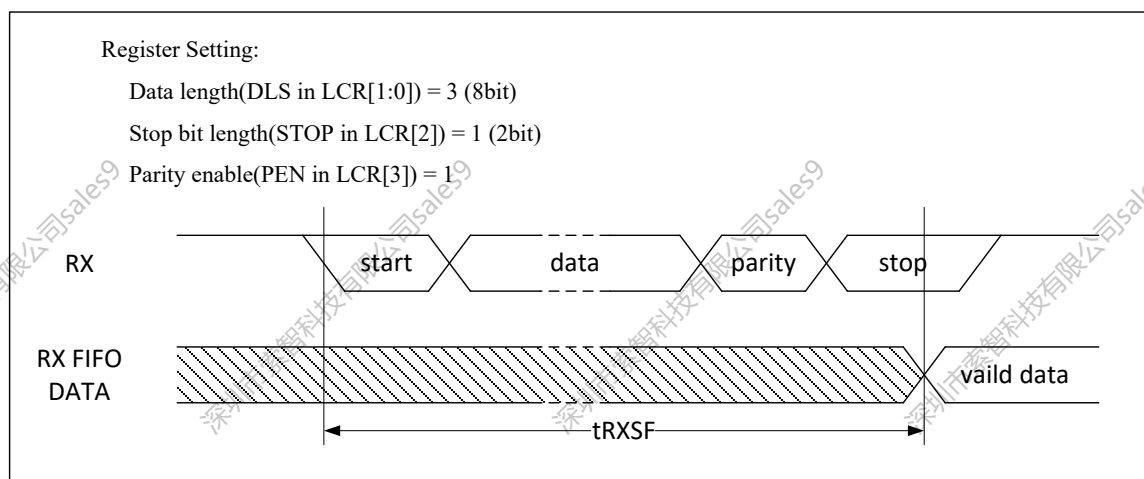


Figure 5-23 UART nCTS Timing

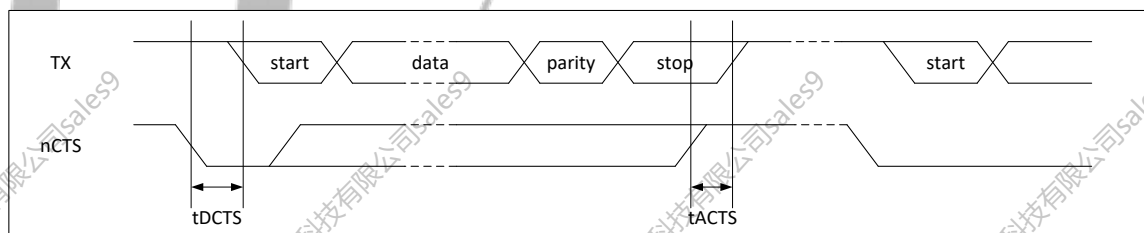


Figure 5-24 UART nRTS Timing

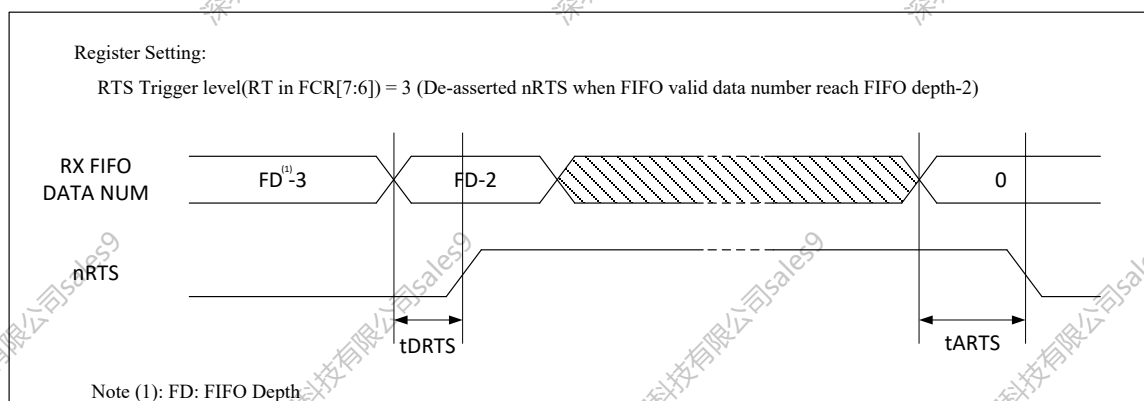


Table 5-33 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5*BRP ⁽¹⁾	-	11*BRP ⁽¹⁾	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	BRP ⁽¹⁾	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP ⁽¹⁾ / 4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP ⁽¹⁾	ns
Delay time of asserted nRTS	tARTS	-	-	BRP ⁽¹⁾	ns

(1) BRP: Baud-Rate Period.

5.10.10 TWI Interface Timing

Figure 5-25 TWI Timing

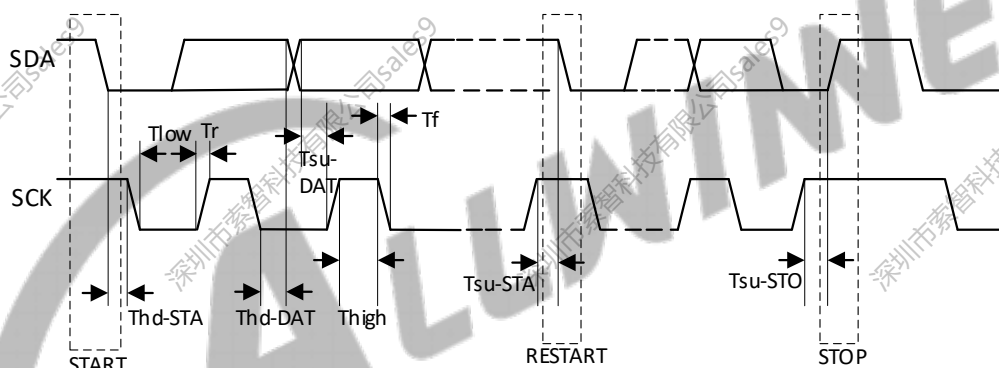


Table 5-34 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data (I2C-bus devices)	Thd-DAT	0	-	0	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.10.11 I2S/PCM Interface Timing

Figure 5-26 I2S/PCM Timing in Master Mode

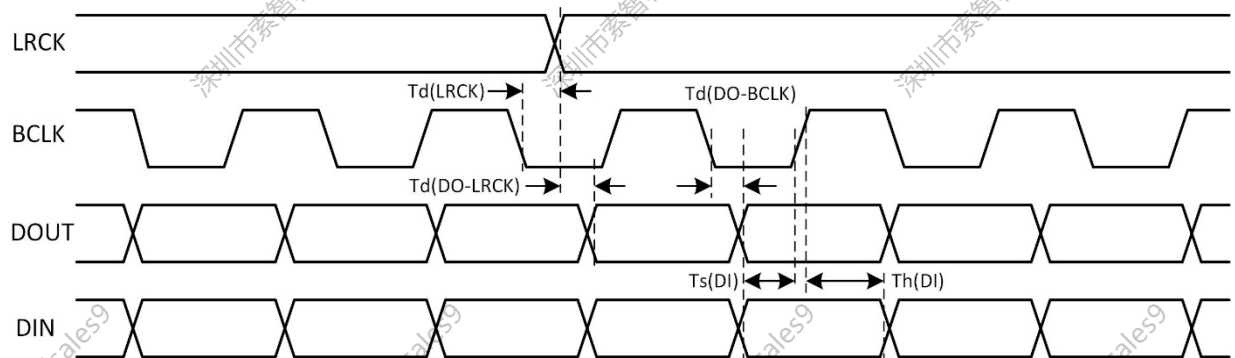


Table 5-35 I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	$T_d(LRCK)$	-	-	10	ns
LRCK to DOUT delay (For LJF)	$T_d(DO-LRCK)$	-	-	10	ns
BCLK to DOUT delay	$T_d(DO-BCLK)$	-	-	10	ns
DIN setup	$T_s(DI)$	4	-	-	ns
DIN hold	$T_h(DI)$	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

Figure 5-27 I2S/PCM Timing in Slave Mode

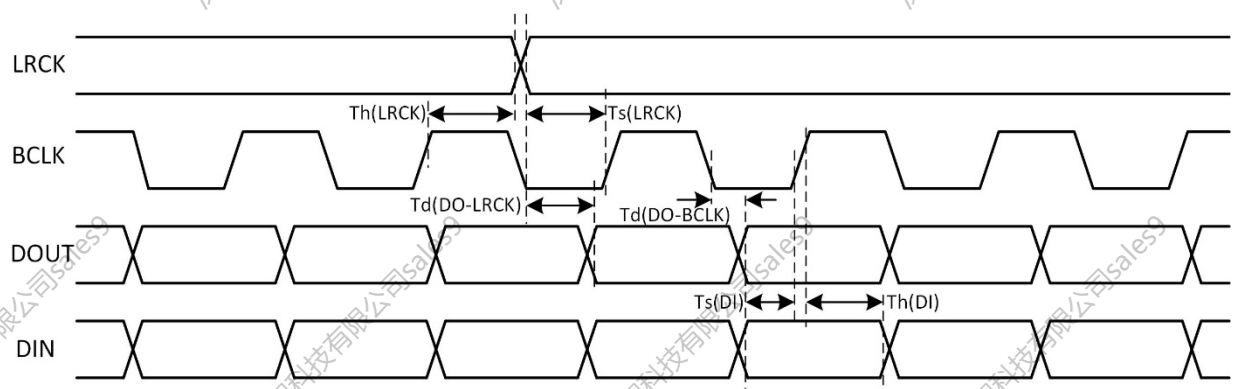


Table 5-36 Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	$T_s(\text{LRCK})$	4	-	-	ns
LRCK hold	$T_h(\text{LRCK})$	4	-	-	ns
LRCK to DOUT delay (For LJF)	$T_d(\text{DO-LRCK})$	-	-	10	ns
BCLK to DOUT delay	$T_d(\text{DO-BCLK})$	-	-	10	ns
DIN setup	$T_s(\text{DI})$	4	-	-	ns
DIN hold	$T_h(\text{DI})$	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.11 Power-Up and Power-Down Sequence



NOTE

- All “Tn” markers represent different steps during power-on and power-down process and show the minimum time interval between current step and previous step.
- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90%-110% of their nominal voltage, unless stated otherwise.
- Different power rails at the same Tn step should become stable within 1ms.

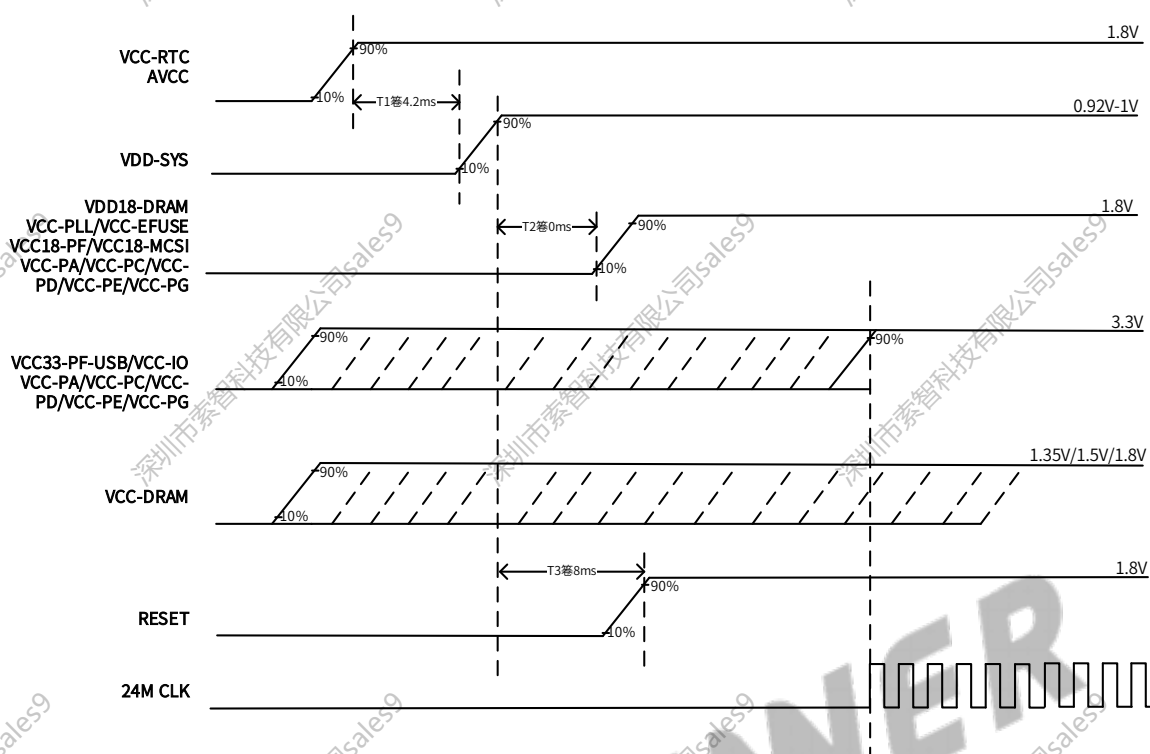
5.11.1 V881MX-XXX

5.11.1.1 Power-Up Sequence

Figure 5-28 shows an example of the power-up sequence. The description of the power-up sequence is as follows.

- After VCC-RTC power-on, delay $\geq 4.2\text{ms}$ before powering on VDD-SYS.
- Once VDD-SYS becomes valid, delay $\geq 8\text{ms}$ before the SOC releases RESET.
- 3.3V power supplies are allowed to power up simultaneously with VCC-RTC or before VCC-RTC, but must complete power-up before the 24MHz clock oscillation starts.
- VCC-DRAM must be powered on before software DRAM initialization.

Figure 5-28 Power-Up Sequence



5.11.1.2 Power-Down Sequence

No specific restrictions on the sequence of power down.

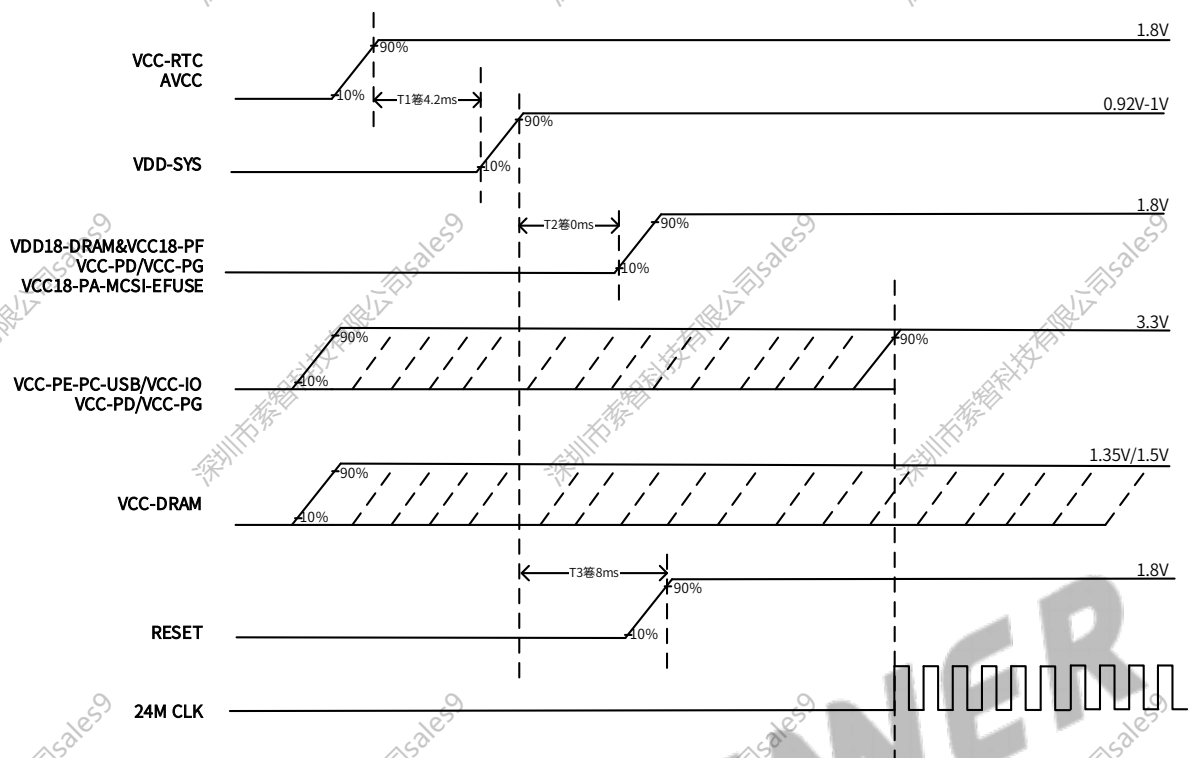
5.11.2 V881M3-XXX

5.11.2.1 Power-Up Sequence

The following figure shows an example of the power-up sequence. The description of the power-up sequence is as follows.

- After VCC-RTC power-on, delay $\geq 4.2\text{ms}$ before powering on VDD-SYS.
- Once VDD-SYS becomes valid, delay $\geq 8\text{ms}$ before the SOC releases RESET.
- 3.3V power supplies are allowed to power up simultaneously with VCC-RTC or before VCC-RTC, but must complete power-up before the 24MHz clock oscillation starts.
- VCC-DRAM must be powered on before software DRAM initialization.

Figure 5-29 Power-Up Sequence



5.11.2.2 Power-Down Sequence

No specific restrictions on the sequence of power down.

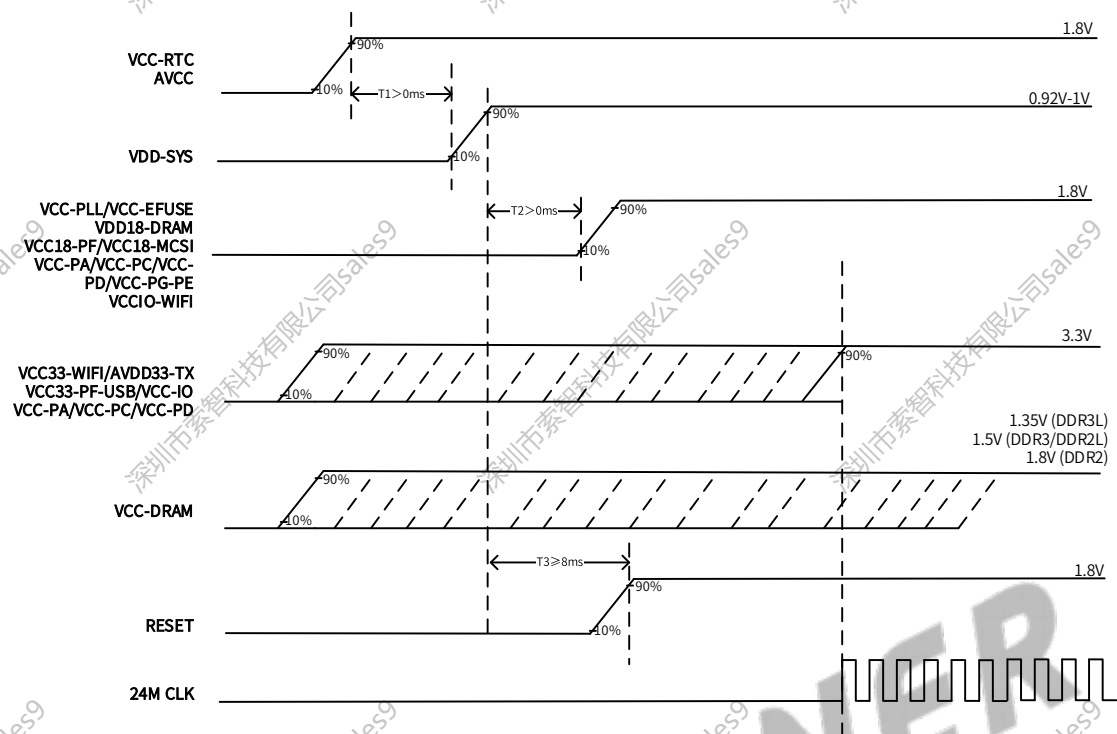
5.11.3 V881M2-WB2/V881M3-WB2

5.11.3.1 Power-Up Sequence

Figure 5-28 shows an example of the power-up sequence. The description of the power-up sequence is as follows.

- After the VCC-RTC is powered on and stabilized, the VDD-SYS is powered on.
- Once VDD-SYS becomes valid, delay $\geq 8ms$ before the SOC releases RESET.
- 3.3V power supplies are allowed to power up simultaneously with VCC-RTC or before VCC-RTC, but must complete power-up before the 24MHz clock oscillation starts.
- VCC-DRAM must be powered on before software DRAM initialization.

Figure 5-30 Power-Up Sequence



5.11.3.2 Power-Down Sequence

No specific restrictions on the sequence of power down.

6 Temperature and Thermal Characteristics

6.1.1 Temperature

The following tables describe the temperature of the device

Table 6-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
T _a	Ambient Operating Temperature ⁽¹⁾	-25	75	°C
T _{STG}	Storage Temperature	-40	125	°C

(1) Ambient Temperature: the temperature of the surrounding environment.

Table 6-2 Junction Temperature⁽¹⁾

Chip	Recommended Operating Temperature ⁽²⁾ (T _J)		Absolute Maximum Junction Temperature ⁽³⁾	Unit
	Min	Max		
V881	-25	115	125	°C

(1) Junction Temperature— the hottest temperature of the silicon chip inside the package.

(2) Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

(3) Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.

6.1.2 Package Thermal Characteristics

The maximum chip junction temperature (T_{J max}) must never exceed the values given in Table 6-2.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-3 Package Thermal Characteristics (TFBGA 12 mm x 12 mm)

Symbol	Parameter	Min	Typ ⁽¹⁾⁽²⁾	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	37.23	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	19.96	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	4.85	-	°C/W

Table 6-4 Package Thermal Characteristics (TFBGA 11.9 mm x 6.9 mm)

Symbol	Parameter	Min	Typ ⁽¹⁾⁽²⁾	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	62.76	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	27.92	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	1.43	-	°C/W

Table 6-5 Package Thermal Characteristics (QFN 12.3 mm x 12.3 mm)

Symbol	Parameter	Min	Typ ⁽¹⁾⁽²⁾	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	23.19	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	9.45	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	2.25	-	°C/W

- (1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.
- (2) The testing PCB is 4 layers, 114.5 mm x 76.2 mm body, and 1.6 mm thickness. Ambient temperature is 25 °C.

7 Pin Assignment

7.1.1 Pin Map

7.1.1.1 TFBGA 12 mm x 12 mm

The following shows the 317 balls, 12 mm x 12 mm, 0.5 mm ball pitch, 0.3 mm ball size pin map.

Figure 7-1 TFBGA 12 mm x 12 mm Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND	PL3/X32K IN		MICIN1P	MICIN2P		PD20/GP ADC2	PD18		PD12	PD10		PD14	PD0		GND	PA0		PA6	PA7		PA3	GND	A
B	PL5/NMI	PL4/X32K OUT	PL2/PWR-EN2	LINEOUT P	GPADC1	GPADC0	PD21/GP ADC3	PD19	PD11	PD8	PD13	PD7	PD4	GND	USB0-DP	USB0-DM	PA1	PA8	PA9	PA4	PA5	PA2	PA11	B
C		PL6			AGND		PD22		PD15		PD16		PD3		PA13		PA15		PA19			PA10		C
D	PL0/PWR-EN0	PL1/PWR-EN1			VRA1		PD17		PD9		PD6		PD2		PA14		PA16		GND			PA18	PA17	D
E	PWR-STARTUP	NC	PMC-BYP	GND	AVCC		GND		GND		PD5		PD1		PA12		GND		VCC-PA	PA21	PA20	PC2	PC9	E
F		RESET					GND		VCC-PD		GND		GND		GND		VCC18-MCSI					PC8		F
G	DXIN	GND	PWRON	GND	TEST	GND	GND											VCC-EFUSE	PC11	PC10	PC1	PC3	PC7	G
H	DXOUT	GND						GND	GND	GND	GND	GND	GND	GND	GND	GND						PC6	PC4	H
J		REFCLK-OUT	PLLTEST	GND	TEST-ALT	GND		VCC-RTC	GND	GND	GND	GND	GND			GND		VCC33-PF-USB	VCC18-PF	VCC-PC	GND	PC5		J
K	PG1	PG0						GND	GND		GND		GND		GND							PC0	PF5	K
L	PG2	PG3	PG6	PG7	VCC-PLL	GND		GND	GND	GND	GND		GND		VDD-SYS	VDD-SYSFB		PH1	PH4	GND	PF6	PF3	PF4	L
M		PG4						GND				VDD-SYS			VDD-SYS	VDD-SYS						PF2		M
N	PE15	PG5	PE17	GND	PE16	VCC-PG		GND	GND	GND	GND		GND	GND		VDD-SYS	VDD-SYS	FEL	JTAG-SEL	GND	PH0	PF1	PF0	N
P	PE5	PE4						GND	GND		GND		GND	GND	GND	GND						PH2	PH8	P
R		PE2	PE3	PE0	GND	VCC-PE			GND	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM	VCC-DRAM				VCC-IO	PH3	GND	PH7	PH5		R
T	PE7	PE12														VDD18-DRAM						PH6	PH15	T
U	PE6	PE9	PE13	PE14	NC	NC	GND		GND		GND		SVREF		SA7		GND	PH10	PH9	GND	PH11	PH13	PH14	U
V		PE8					SDQM1		SDQ6		SDQ3		DDR3-SZQ1		GND		SCKE1					PH12		V
W	PE1	PE11	PE10	NC	GND		SDQ8		GND		SDQ1		SZQ		SBA1		SA14		SA15	SODT1	GND	GND	SA3	W
Y	NC	NC			SDQ14		GND		SDQM0		GND		GND		GND		GND		SCS1			SA13	SA5	Y
AA		NC			SDQ11		SDQ15		SDQ4		SDQ0		SWE		SA10		SA11		SA8			SRST		AA
AB	NC	NC	GND	SDQ12	SDQ1P	SDQS1N	GND	SDQS0P	SDQS0N	SDQ7	SDQ2	SCKE0	GND	SCS0	SCAS	SA12	GND	SODT0	SA2	SA4	SA6	SA1	SA9	AB
AC	GND	NC		SDQ9	GND		SDQ10	SDQ13		GND	SDQ5		SCKN	SCKP		SBA0	SRAS		GND	SBA2		SA0	GND	AC
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

7.1.1.2 TFBGA 11.9 mm x 6.9 mm

The following shows the 194 balls, 11.9 mm x 6.9 mm, 0.5 mm ball pitch, 0.3 mm ball size pin map.

Figure 7-2 TFBGA 11.9 mm x 6.9 mm Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	
A	GND		GND		PL2/PWR-EN2		MICIN1P		PD21/GP ADC3		PD2		PD5		USB0-DP		PA2		PA7		PA10		GND	A
B		GPIOA8	GPIOA9	PL4/X32K OUT	PL1/PWR-EN1	LINEOUT P	MICIN2P	GPADC1	PD18	PD3	PD8	PD7	PD4	GND	USB0-DM	PA0	PA3	PA5	PA6	PA9	PA11	PA12		B
C	NC	PWRON	VCCIO-WIFI	PL5/NMI	PL3/X32K IN	PL0/PWR-ENO	GPADC0	PD19	PD20/GP ADC2	PD6	GND	PD1	GND	GND	GND	PA1	GND	PA4	PA8	PA13	PA15	PA14	PA16	C
D		VCC33-WIFI	TEST	PWR-STARTUP	VCORE	VCORE	VRA1	AGND	AVCC	GND	VCC-RTC	GND	VCC-PD	GND	GND	GND	GND	VCC-PA	VCC18-MCSI	VCC-PC	GND	VCC-EFUSE		D
E	AVDD13	SW	TEST-ALT	PMC-BYP																	PC10	PC11		E
F		RESET	GND			AVDD18	AVDD13-DECAP2	RF-XTAL-IN	GND	DXOUT	DXIN	GND			GND			GND		VCC33-PF-USB	PC7	PC8	PC9	F
G	AVDD33-TX	AVDD13-DECAP0	GND	GND	GND				GND			GND	GND	GND	GND	GND	GND			VCC18-PF	PC5	PC6		G
H		PWR-WF																			PC2	PC4	PC0	H
J	GND	GND	GND	GND	GND	GND	VCC-PG-PE	GND	GND	GND	GND	VCC-PLL	GND		VDD-SYS		VCC-IO	PH7			PC1	PC3		J
K	WF-RF5G	GND	GND	GND	GND	GND	AVDD13-DECAP1	GND	GND	GND	CONFIG1-PG1	GND	GND	GND	VDD-SYS	VDD-SYS	GND	PH10	PH6	PF5	PF3	PF6	PH1	K
L		WF-BT-RF24G	GND	GND	BT-RFGND	GND	BT-DVDD		GND	RESERVE	CONFIG0-PG0	VCC-DRAM	GND	GND	VDD-SYS	VDD-SYS	GND	PH9	PH8	PF4	PF2	PF0		L
M	GND		WF-RFGND-24G		BT-RF-CONFIG	GND			GND			VCC-DRAM	VCC-DRAM		VDD-SYS		VDD18-DRAM		PH15		PF1		GND	M
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	

The following shows the QFN 128 pins, 12.3 mm x 12.3 mm pin map.

Figure 7-3 QFN 12.3 mm x 12.3 mm Pin Map

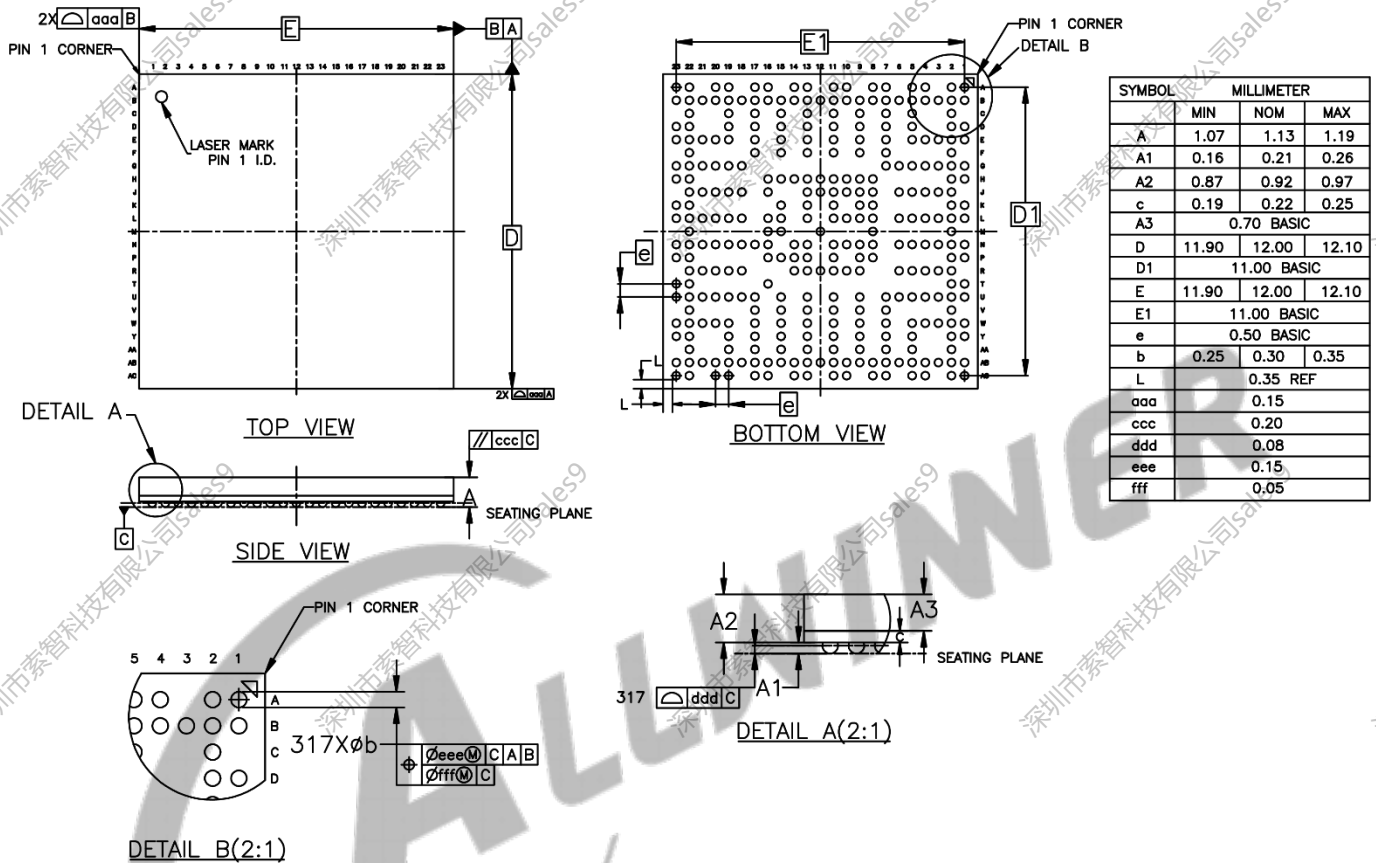
[illegible]

7.1.2 Package Dimension

7.1.2.1 TFBGA 12 mm x 12 mm

The following figure shows the top, bottom, and side views of the package.

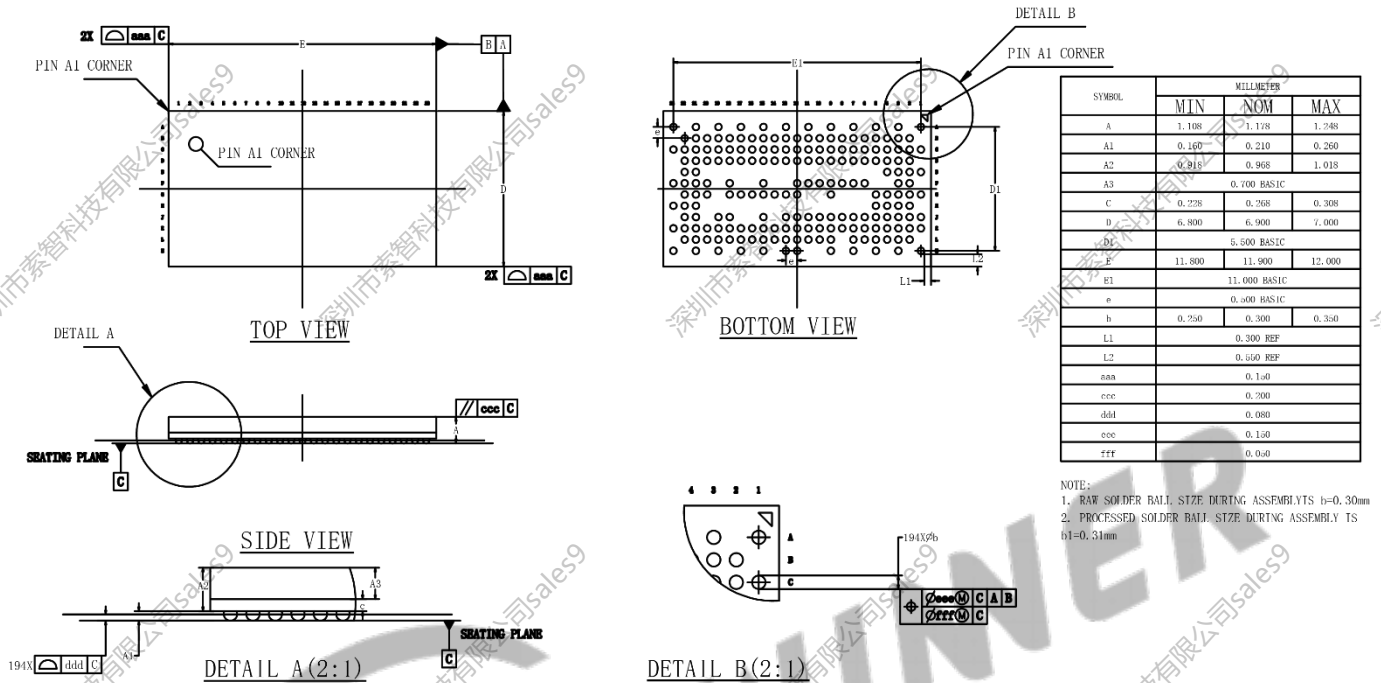
Figure 7-4 TFBGA 12 mm x 12 mm Package Dimension



7.1.2.2 TFBGA 11.9 mm x 6.9 mm

The following figure shows the top, bottom, and side views of the package.

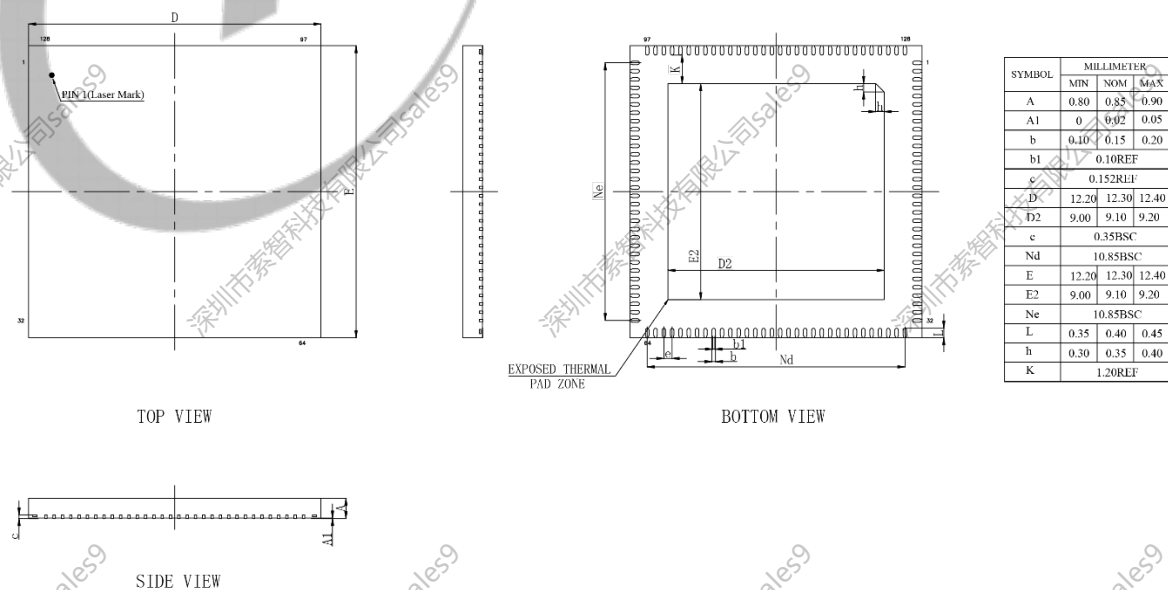
Figure 7-5 TFBGA 11.9 mm x 6.9 mm Package Dimension



7.1.2.3 QFN 12.3 mm x 12.3 mm

The following figure shows the top, bottom, and side views of the package.

Figure 7-6 QFN 12.3 mm x 12.3 mm Package Dimension



8 Carrier, Storage and Backing Information

8.1 Carrier

The following table shows matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	- TFBGA 12 mm x 12 mm: 168 Qty/Tray - TFBGA 11.9 mm x 6.9 mm: 208 Qty/Tray - QFN 12.3 mm x 12.3 mm: 152 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

The following table shows packing quantity.

Table 8-2 Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V881MX-XXX	12 mm x 12 mm	168	10	1680	6	10080

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
V881M2-WB2 V881M3-WB2	11.9 mm x 6.9 mm	208	10	2080	6	12480
V881M3-XXX	12.3 mm x 12.3 mm	152	10	1520	6	9120

The following figures show tray dimension drawing.

Figure 8-1 Tray Dimension Drawing for TFBGA 12 mm x 12 mm Size

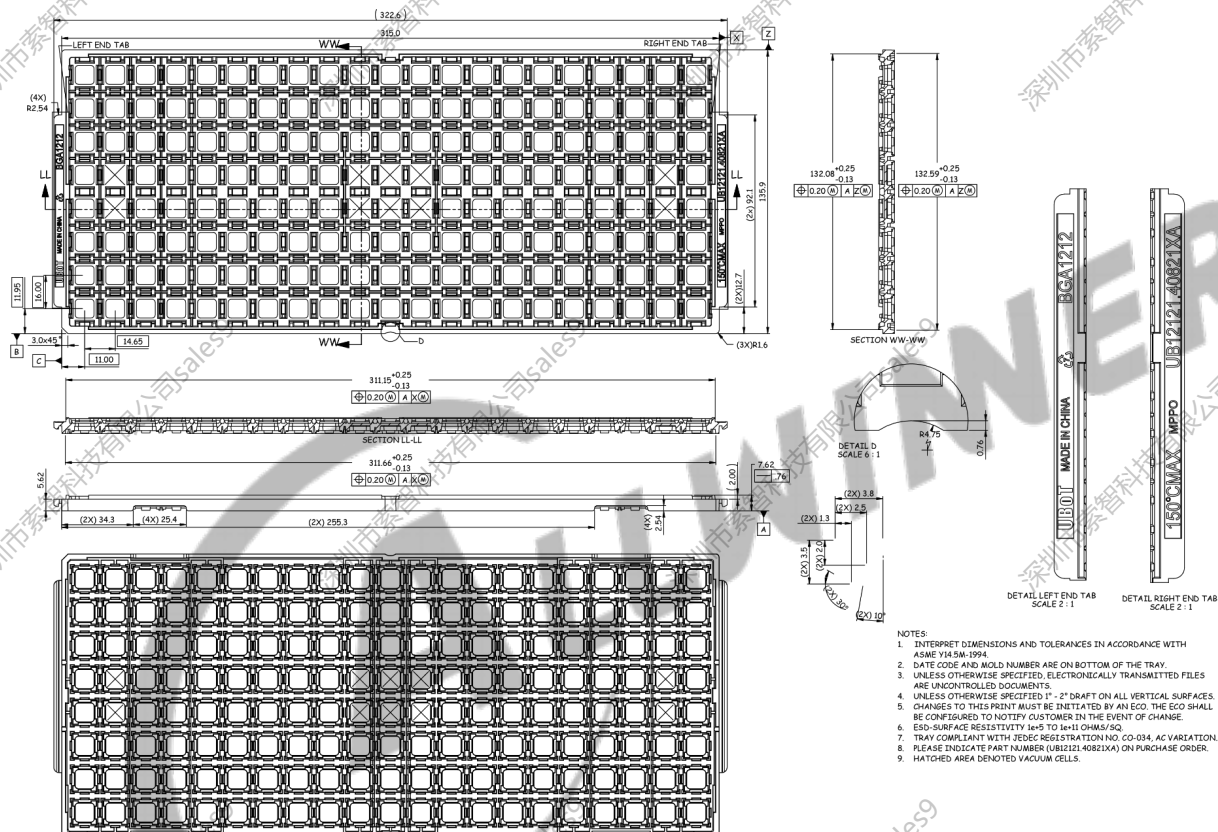


Figure 8-2 Tray Dimension Drawing for TFBGA 11.9 mm x 6.9 mm Size

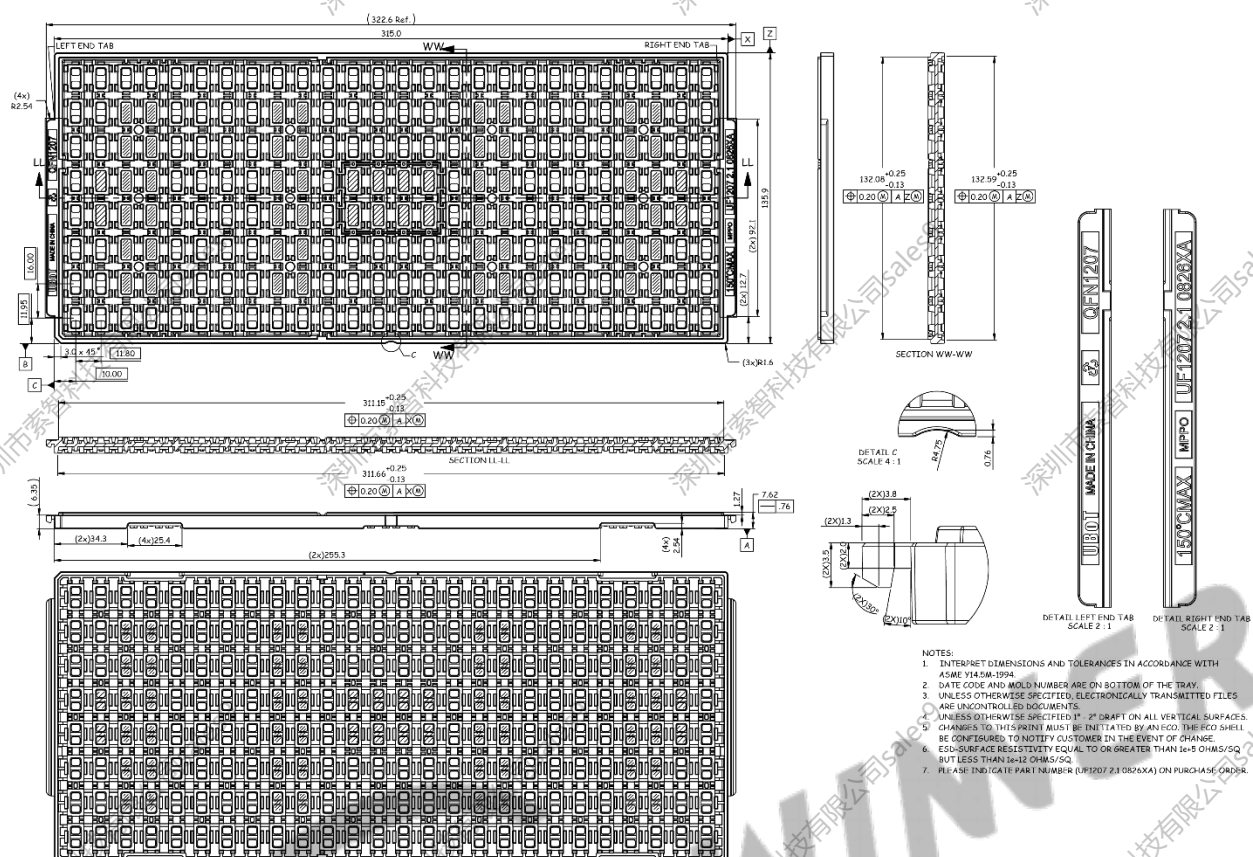
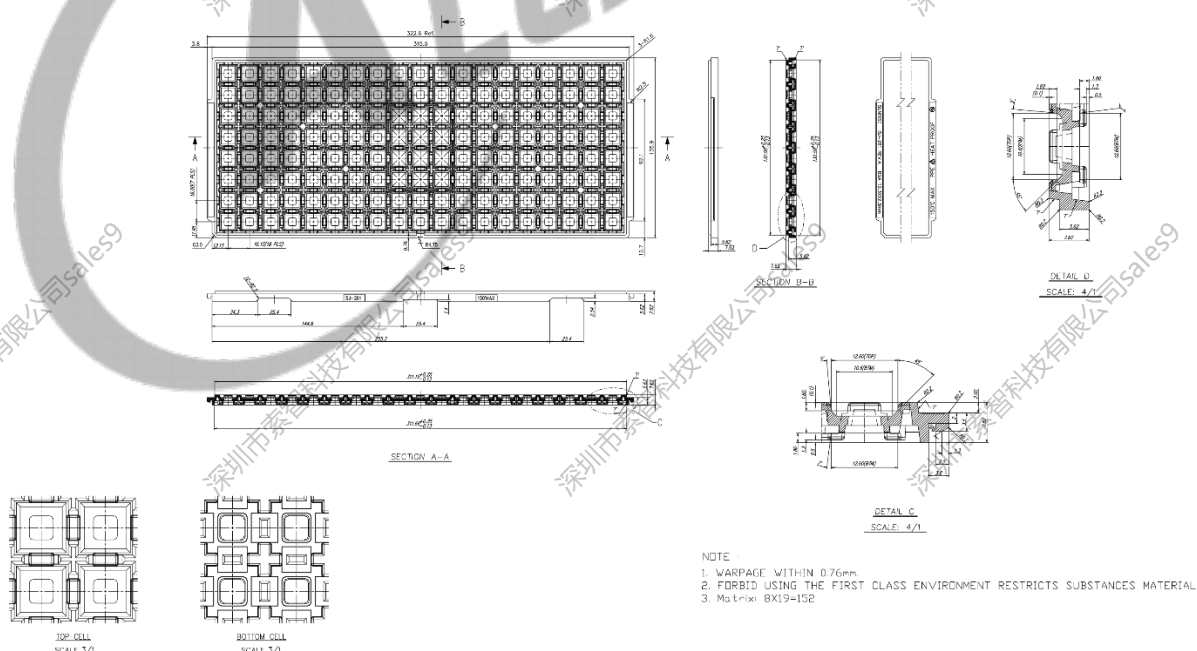


Figure 8-3 Tray Dimension Drawing for QFN 12.3 mm x 12.3 mm Size



8.2 Storage

Reliability is affected if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-3 defines all MSL.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	$\leq 30^{\circ}\text{C}$ / 85%RH
2	1 year	$\leq 30^{\circ}\text{C}$ / 60%RH
2a	4 weeks	$\leq 30^{\circ}\text{C}$ / 60%RH
3	168 hours	$\leq 30^{\circ}\text{C}$ / 60%RH
4	72 hours	$\leq 30^{\circ}\text{C}$ / 60%RH
5	48 hours	$\leq 30^{\circ}\text{C}$ / 60%RH
5a	24 hours	$\leq 30^{\circ}\text{C}$ / 60%RH
6	Time on Label (TOL)	$\leq 30^{\circ}\text{C}$ / 60%RH



NOTE

The V881 device samples are classified as MSL3.

8.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 8-4 Bagged Storage Conditions

Packing Mode	Vacuum packing
Storage Temperature	20-26°C
Storage Humidity	40%-60%RH
Shelf Life	12 months

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 8-5 Out-of-bag Duration

Storage Temperature	20-26°C
---------------------	---------

Storage Humidity	40%-60%RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake chips if the conditions specified in section 8.2.2 and section 8.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology or lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

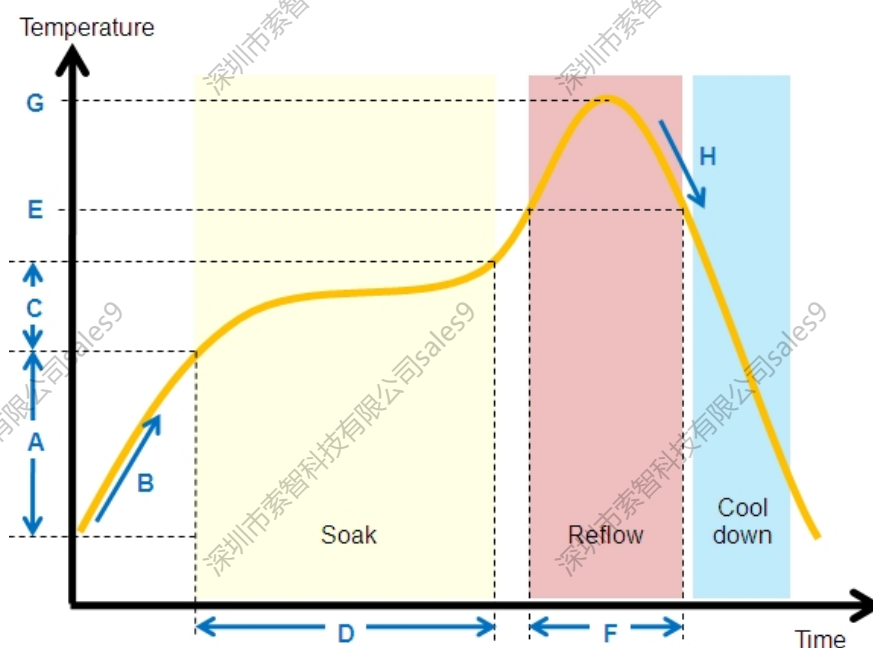


Table 9-1 Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5-2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80-110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 s
G	Peak temperature	240-250 °C

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
H	Cool down temperature rate	$\leq 4^{\circ}\text{C/s}$

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe.

Figure 9-2 Measuring the Reflow Soldering Process for BGA Package

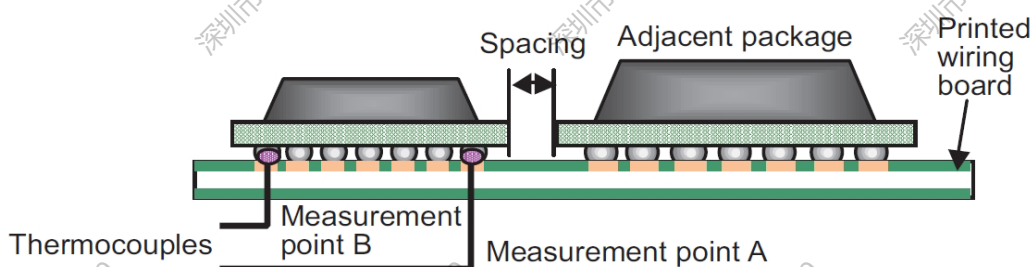
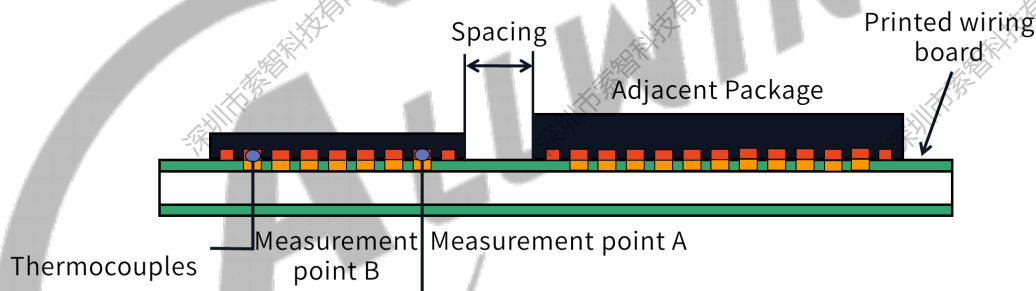


Figure 9-3 Measuring the Reflow Soldering Process for QFN Package



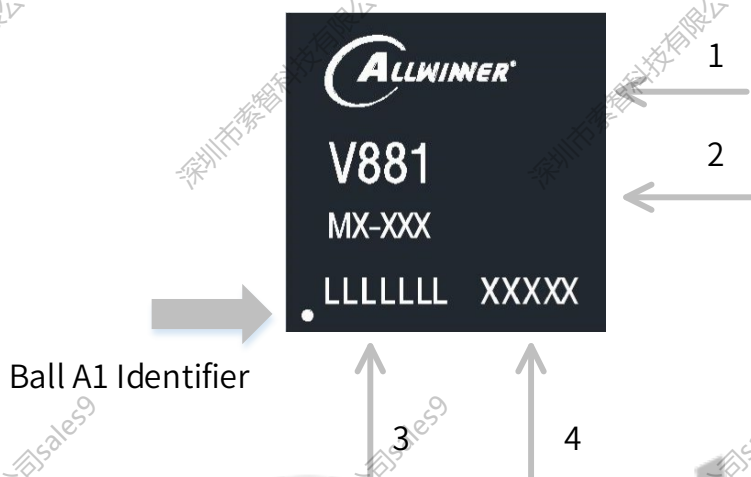
If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 Part Marking

10.1 V881MX-XXX

The following figure shows the V881MX-XXX marking.

Figure 10-1 V881MX-XXX Marking



The following table describes the V881MX-XXX marking definitions.

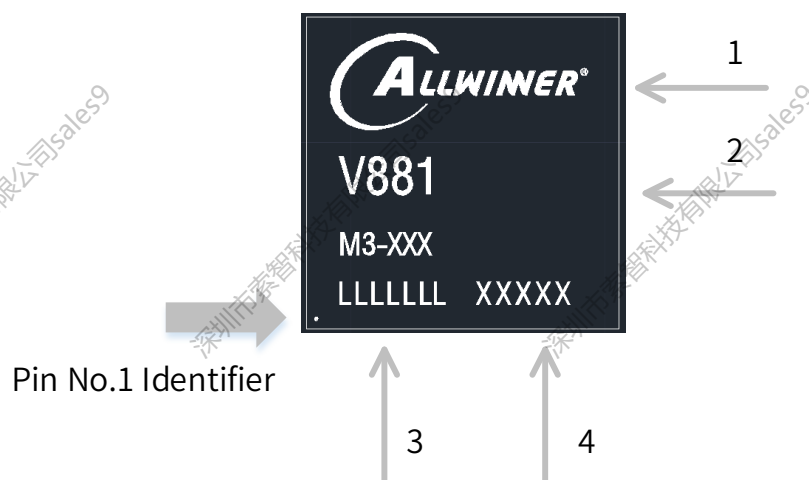
Table 10-1 V881MX-XXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V881MX-XXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.2 V881M3-XXX

The following figure shows the V881M3-XXX marking.

Figure 10-2 V881M3-XXX Marking



The following table describes the V881M3-XXX marking definitions.

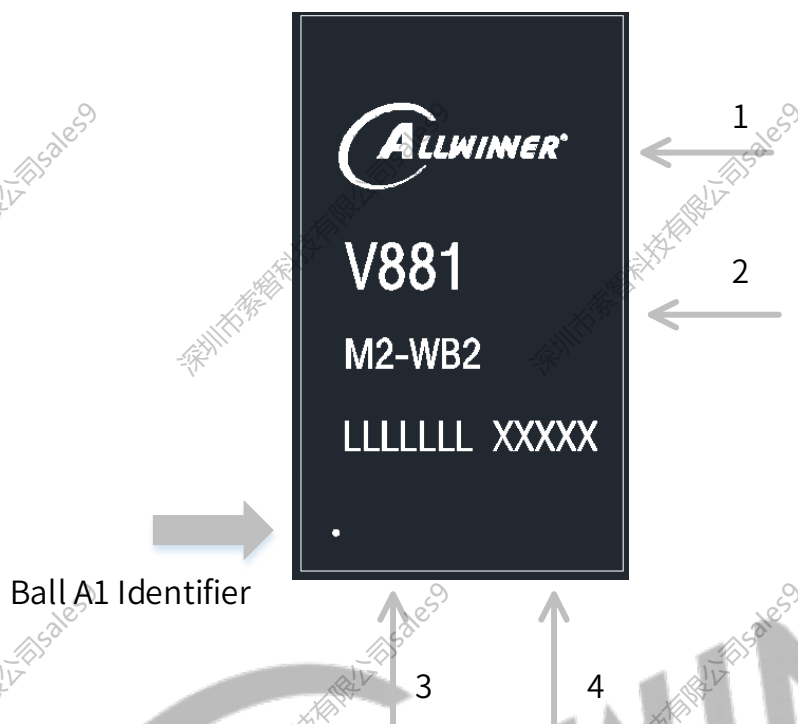
Table 10-2 V881M3-XXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V881M3-XXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.3 V881M2-WB2

The following figure shows the V881M2-WB2 marking.

Figure 10-3 V881M2-WB2 Marking



The following table describes the V881M2-WB2 marking definitions.

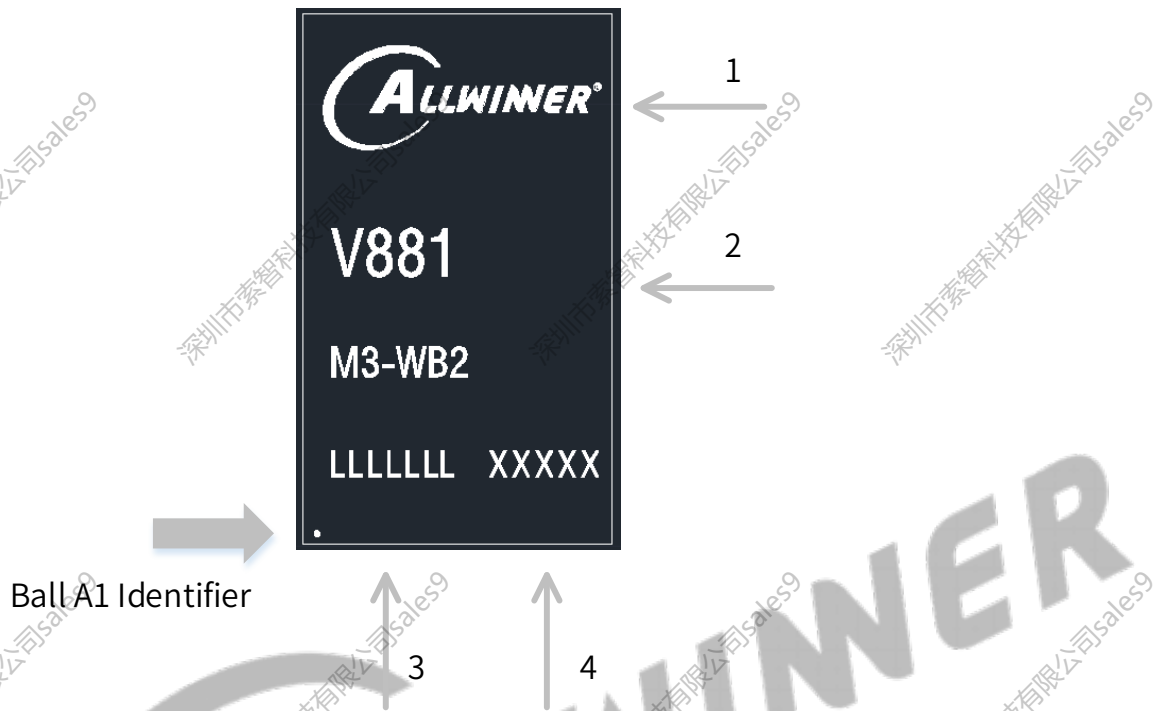
Table 10-3 V881M2-WB2 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V881M2-WB2	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.4 V881M3-WB2

The following figure shows the V881M3-WB2 marking.

Figure 10-4 V881M3-WB2 Marking



The following table describes the V881M3-WB2 marking definitions.

Table 10-4 V881M3-WB2 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	V881M3-WB2	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

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