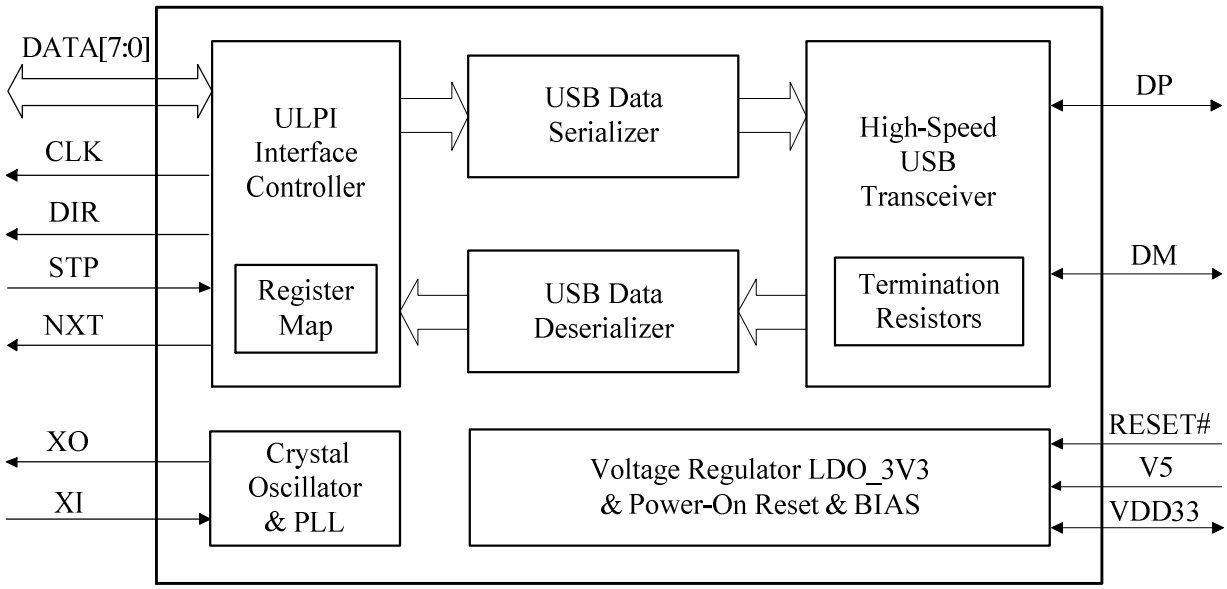
CH132 Datasheet

V1.2

Overview

The CH132 is a UTMI+ Low Pin Interface (ULPI) Hi-Speed Universal Serial Bus (USB) transceiver that is compliant with USB Specification Rev. 2.0, and UTMI+ Low Pin Interface (ULPI) Specification Rev. 1.1. The CH132 can transmit and receive data at high speed (480 Mbps), full speed (12 Mbps) and low speed (1.5 Mbps). It is ideal for use in MCU or FPGA which has ULPI Interface.



Features

- Complies with USB Specification Rev. 2.0
- Complies with UTMI+ Low Pin Interface (ULPI) Rev 1.1
- 12-pin ULPI interface with 3.3V I/O voltage, 60MHz clock signal output
- Support USB host and USB device
- Support USB High Speed, Full Speed and Low Speed
- Support 3-pin or 6-pin Full-Speed or Low-Speed serial mode
- Internal voltage regulator supplies 3.3 V to 5.0 V Power Input
- Built-in power-on reset circuit, built-in clock oscillator and PLL
- Built-in termination resistors, built-in oscillation capacitors, peripheral circuitry streamlined
- 6KV enhanced ESD performance
- Industrial grade temperature range: -40 to 85°C
- Packages: QFN24, QFN32 and the others

Chapter 1 Pinning information

1.1 Pinouts

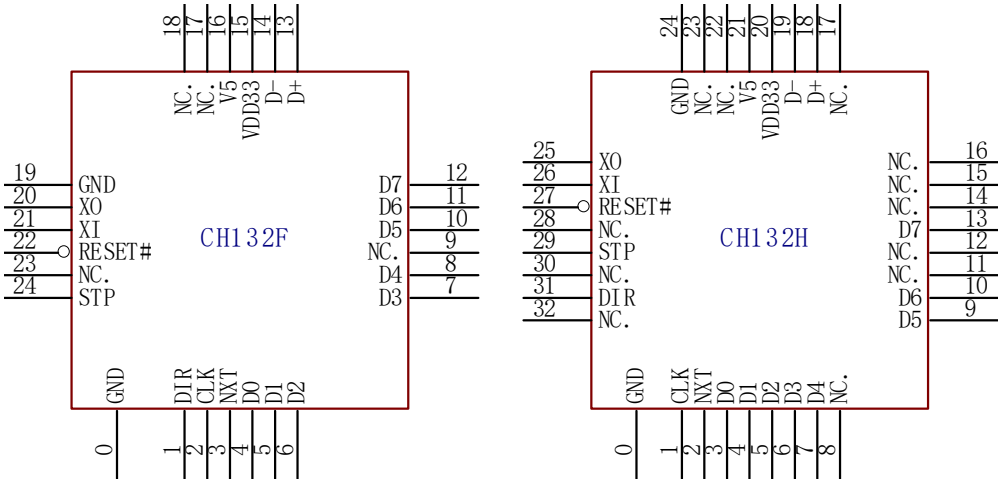


Figure 1-1 CH132F and CH132H pinouts

Note: Pin 0# is the EPAD of QFN package

Smaller packages such as the QFN20_3*3 are also available for volume orders.

1.2 Packages

Table 1-1 CH132 package information

Package	Body size		Lead pitch		Description	Part No.
QFN24_4*4	4.0mm		0.5mm	19.7mil	Quad flat no-lead 24-pin	CH132F
QFN32_5*5	5.0mm		0.5mm	19.7mil	Quad flat no-lead 32-pin	CH132H

1.3 Pin definitions

Table 1-2 CH132 pin definitions

Pin No.		Pin Name	Pin Type	Function Description
CH132F	CH132H			
13	18	D+	USB	USB2.0 high-speed differential signal lines DP
14	19	D-	USB	USB2.0 high-speed differential signal lines DM
2	1	CLK	O	ULPI 60 MHz clock signal output
3	2	NXT	O	ULPI Next signal output
1	31	DIR	O	ULPI Direction signal output
24	29	STP	I	ULPI Stop signal input, built-in controlled pull-up current

4	3	D0	I/O	Bidirectional ULPI DATA Pin 0, built-in weak pull-down resistor
5	4	D1	I/O	Bidirectional ULPI DATA Pin 1, built-in weak pull-down resistor
6	5	D2	I/O	Bidirectional ULPI DATA Pin 2, built-in weak pull-down resistor
7	6	D3	I/O	Bidirectional ULPI DATA Pin 3, built-in weak pull-down resistor
8	7	D4	I/O	Bidirectional ULPI DATA Pin 4, built-in weak pull-down resistor
10	9	D5	I/O	Bidirectional ULPI DATA Pin 5, built-in weak pull-down resistor
11	10	D6	I/O	Bidirectional ULPI DATA Pin 6, built-in weak pull-down resistor
12	13	D7	I/O	Bidirectional ULPI DATA Pin 7, built-in weak pull-down resistor
21	26	XI	I	Crystal input, external 12MHz crystal end required or external clock input
20	25	XO	O	Inverted output of crystal oscillator, external 12MHz crystal to be connected to the other end
22	27	RESET#	I	Reset signal input, active low, built-in pull-up resistor
16	21	V5	P	5V or 3.3V power input, external 1uF decoupling capacitor
15	20	VDD33	P	LDO output and 3.3V power input, external 1uF decoupling capacitor
19	24	GND	P	Common ground, optional but recommended connection to GND
0	0	GND	P	Common ground (QFN EPAD), necessary connection
9,17, 18,23	8,11,12, 14,15,16 17,22,23 28,30,32	NC.	-	Empty or reserved pins, connection prohibited

Pin Type:

(1) I: 3.3V signal input

(2) O: 3.3V signal output

(3) P: Power or ground

(4) USB: USB signal

Chapter 2 Basic functions

2.1 Clock and reset

2.1.1 Clock source

The CH132 requires a 12 MHz clock source, either by inputting the clock from pin XI and leaving XO suspended, or by connecting an external 12MHz crystal to pins XI and XO to generate the clock source via an internal oscillator. The CH132 then generates the multiple clocks required by the chip via a PLL:

- 1.5MHz clock for USB low-speed data transfer
- 12MHz clock for USB full-speed data transfer
- 480MHz clock for USB high-speed data transfer
- 60MHz clock for ULPI Controller
- Other clocks required for internal data processing

2.1.2 Power-on reset

The CH132 has a built-in power-on reset module, which generally does not require an external reset signal. When the power supply is powered on, the chip's internal POR power-on reset module will generate a power-on reset timing and delay Trpor for about 15-25mS to wait for the power supply to stabilize. During operation, when the power supply voltage falls below V_{lvr}, the chip's internal low voltage reset module generates a low voltage reset until the voltage rises back up and delays for the power supply to stabilize. Figure 3-1 shows the power-on reset process as well as the low-voltage reset process.

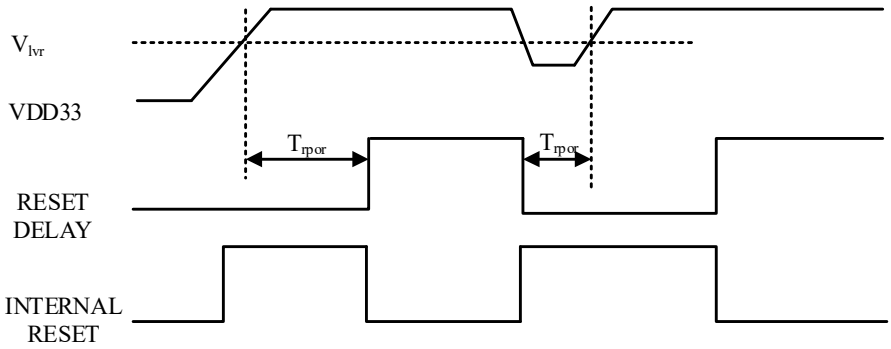


Fig 2-1 Power-on reset

2.1.3 External reset

The external reset input pin RESET# has a built-in pull-up resistor of approximately 24KΩ and can be driven low if an external reset of the chip is required, with a recommended low-level pulse width of at least 5us for the reset. It is recommended that no further pull-up resistors be connected externally.

2.2 Power supply

The CH132 has a built-in low dropout linear regulator LDO. 3.3V supply by default, 5V supply is also supported. For 3.3V powered systems, the 3.3V supply is fed to both VDD33 pin and V5 pin for internal

analogue and I/O circuits. For 5V supply systems, the 5V supply is input to V5 pin and the internal LDO generates a 3.3V supply at VDD33 pin for internal analogue and I/O circuits. In both cases, the VDD33 pin and the V5 pin require external decoupling capacitors. When 5V power supply is selected, the general-purpose CH132 with a letter in the 4th digit from last of the batch number supports 4.5V to 5.25V, while the special-purpose CH132 with a number in the 4th digit from last of the batch number supports 3.7V to 4.5V.

Avoid feeding the 5V power from VBUS directly into V5 pin. It is recommended that an overvoltage protection circuit be added between VBUS pin and V5 pin.

2.3 USB transceiver

The CH132 USB transceiver takes on USB high speed, full speed and low speed data transceiver tasks. The Transceiver includes the differential driver circuitry necessary for USB high speed, full speed and low speed data transmission, the differential and single ended receivers for USB high speed, full speed and low speed data reception, the circuitry to detect high speed bus activity and the circuitry to detect high speed bus disconnection.

The USB port has a variety of built-in matching resistors, including impedance matching resistors, device pull-up resistors, host pull-down resistors, etc.

A detailed relationship between the registers and the USB port mode can be found in Table 2-1 below.

Table 2-1 Register settings and port mode relationships

USB signaling mode	Register settings				
	XCVR SELECT[1:0]	TERM SELECT	OP MODE[1:0]	DP_ PULLDOWN	DM_ PULLDOWN
3-state drivers	xxb	xb	01b	xb	xb
Host Chirp	00b	0b	10b	1b	1b
Host High-speed	00b	0b	00b	1b	1b
Host Full-speed	x1b	1b	00b	1b	1b
Host High-speed or Full-speed suspend	01b	1b	00b	1b	1b
Host High-speed or Full-speed resume	01b	1b	10b	1b	1b
Host Low-speed	10b	1b	00b	1b	1b
Host Low-speed suspend	10b	1b	00b	1b	1b
Host Low-speed resume	10b	1b	10b	1b	1b
Host Test J or Test K	00b	0b	10b	1b	1b

Peripheral Chirp	00b	1b	10b	0b	0b
Peripheral High-speed	00b	0b	00b	0b	0b
Peripheral Full-speed	01b	1b	00b	0b	0b
Peripheral High-speed or Full-speed suspend	01b	1b	00b	0b	0b
Peripheral High-speed or Full-speed resume	01b	1b	10b	0b	0b
Peripheral Test J or Test K	00b	0b	10b	0b	0b

2.4 ULPI controller

The CH132 provides a 12 Pin interface compatible with the ULPI (UTMI+ Low Pin Interface) 1.1 protocol. This interface should be connected to the ULPI connector of the ULPI linker, which has a USB controller at the other end. This ULPI interface controller has the following functions:

- ULPI protocol compatible interface and register settings
- Allows functional control via USB host or peripheral devices
- Parses data sent or received by USB
- Determines USB Data transmission and receipt, interrupts and register operations
- 3-pin serial mode
- 6-pin serial mode
- Maskable interrupts

2.5 3-pin and 6-pin serial mode

The CH132 is available in either 3-pin or 6-pin serial mode. The serial mode of the 3-pin or 6-pin interface is selected as required to transmit full-speed or low-speed USB packets. Interface mapping for the 3-pin serial mode is shown in Table 2-2 and for the 6-pin serial mode is shown in Table 2-3. Entering or exiting the 3-pin or 6-pin serial mode can be described in the R8_INTF_CTRL register regarding the 3PIN_FSLS_SERIAL or 6PIN_FSLS _SERIAL bit is described.

Table 2-2 Signal mapping for 3-pin serial

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	Transmit enable. Active high. 0: Receive data; 1: Transmit data.
DAT	DATA1	I/O	When TX_ENABLE = 1, transmit differential data on DP and DM.

Signal	Maps to	Direction	Description
			When TX_ENABLE = 0, receive differential data from DP and DM.
SE0	DATA2	I/O	When TX_ENABLE = 1, transmit single-ended zero on DP and DM. When TX_ENABLE = 0, receive single-ended zero from DP and DM.
INT	DATA3	O	Interrupt request flag. Active high. It will be asserted and latched whenever any unmasked interrupt occurs
Reserved[7:4]	DATA[7:4]	O, PD	Reserved. The CH132 drives these pins to LOW through pull-down resisters.

Table 2-3 Signal mapping for 6-pin serial

Signal	Maps to	Direction	Description
TX_ENABLE	DATA0	I	Transmit enable. Active high.
TX_DAT	DATA1	I	Transmit differential data on DP and DM
TX_SE0	DATA2	I	transmit single-ended zero on DP and DM
INT	DATA3	O	Interrupt request flag. Active high. It will be asserted and latched whenever any unmasked interrupt occurs
RX_DP	DATA4	O	single-ended receive data from DP
RX_DM	DATA5	O	single-ended receive data from DP
RX_RCV	DATA6	O	single-ended receive data from DP
Reserved	DATA7	O, PD	Reserved. The CH132 drives this pin to LOW through a pull-down resister

Chapter 3 ULPI register

3.1 Register description

The following abbreviations may be used in this datasheet when describing registers:

Register Bit Attributes	Description
RO	Read-only. Data is generated and changed by hardware.
WO	Write-only (This bit cannot be read, and the read value is uncertain)
RW	Readable and writable.

Description of registers related to the operation of the ULPI interface on CH132

Table 3-1 CH132 ULPI registers

Name	Address (6 bit)				Description	Reset Value
	Read	Write	Set	Clear		
ID	0x00–0x03				ID register. Reserved	0x00000000
R8_FUNC_CTRL	0x04–0x06	0x04	0x05	0x06	ULPI function control register	0x4D
R8_INTF_CTRL	0x07–0x09	0x07	0x08	0x09	ULPI interface control register	0x00
R8_OTG_CTRL	0x0A–0x0C	0x0A	0x0B	0x0C	OTG control register	0x00
R8_USB_INTR_EN_R	0x0D–0x0F	0x0D	0x0E	0x0F	USB rising interrupt enable register	0x00
R8_USB_INTR_EN_F	0x10–0x12	0x10	0x11	0x12	USB falling interrupt enable register	0x00
R8_USB_INTR_STAT	0x13	-	-	-	USB interrupt status register	0x00
R8_USB_INTR_L	0x14	-	-	-	USB interrupt latch register	0x00
R8_SCRATCH	0x16–0x18	0x16	0x17	0x18	Scratch register	0x00
	Other				Reserved	0x00

（1）R: Read. A register can be read. Read-only if this is the only mode given.

（2）W: Write. The pattern on the data bus will be written over all bits of a register.

（3）S: Set. The pattern on the data bus is OR-ed with and written to a register.

（4）C: Clear. The pattern on the data bus is a mask. If a bit in the mask is set, then the corresponding register bit will be set to zero (cleared).

ULPI function control register (R8_FUNC_CTRL, Address R = 04h/05h/06h, W = 04h, S = 05h, C = 06h)

Bit	Symbol	Access	Description	Reset Value
7	Reserved	RW	Reserved	0b
6	SUSPEND	RW	**Suspend:**	1b

			Enter low-power mode. Active low. The ULPI linker can exit low power mode through STP. This bit is automatically set to 1 when the CH132 exits low power mode. **0**: Low power mode. The device does not support it yet, and it is recommended to write 1. **1**: Normal.	
5	RESET	RW	**Reset:** Active high. This does not reset the ULPI interface or the ULPI register. When the reset is completed, the CH132 will desert DIR and automatically clear this bit. **0**: Not reset **1**: Reset	0b
[4:3]	OP MODE	RW	**Operation Mode:** Selects the required bit-encoding style during transmit **00**: Normal **01**: Not drive **10**: Disable bit-stuffing and NRZI encoding **11**: Do not automatically add SYNC and EOP when transmitting (only for high-speed packets)	01b
2	TERM SELECT	RW	**Termination select:** Controls the pull-up/pull-down resistor and high-speed terminations, depending on XCVR SELECT, OP MODE, DP_PULLDOWN and DM_PULLDOWN, as shown in Table 2-1	1b
[1:0]	XCVR SELECT	RW	**Transceiver select:** Selects the required transceiver speed. **00**: Enable the high-speed transceiver **01**: Enable the full-speed transceiver **10**: Enable the low-speed transceiver **11**: Enable the full-speed transceiver for low-speed packets (full-speed preamble is automatically prefixed)	01b

ULPI interface control register (R8_INTF_CTRL, Address R = 07h/08h/09h, W = 07h, S = 08h, C = 09h)

Bit	Symbol	Access	Description	Reset Value
7	INTF_PROT_DIS	RW	**Disable interface protect:** The ULPI interface protection circuitry built into the control chip when the ULPI linker is not output to STP and	0b

			DATA[7:0] **0**: Enable ULPI interface protection circuitry, enable STP weak pull-ups; **1**: Close the ULPI protection circuit and disable STP weak pull-ups.	
[6:2]	Reserved	RW	Reserved	00000b
1	3PIN_FSLS_SERIAL	RW	**3-Pin full-speed and low-speed serial mode:** Changes the ULPI interface into a 3-pin serial interface. The CH132 automatically clears this bit when the mode is exited. **0**: Disables 3-pin serial mode, full-speed low-speed packet transfer via ULPI parallel port; **1**: Enables 3-pin serial mode, full-speed low-speed packet transmission over 3-pin interface	0b
0	6PIN_FSLS_SERIAL	RW	**6-Pin full-speed and low-speed serial mode:** Changes the ULPI interface into a 3-pin serial interface. The CH132 will automatically clear this bit when the mode is exited. **0**: Disables 6-pin serial mode, full-speed low-speed packet transfer via ULPI parallel port; **1**: Enables 6-pin serial mode, full-speed low-speed packet transmission over 6-pin interface	0b

OTG control register (R8_OTG_CTRL, Address R = 0Ah/0Bh/0Ch, W = 0Ah, S = 0Bh, C = 0Ch)

Bit	Symbol	Access	Description	Reset Value
[7:3]	Reserved	RW	Reserved	00000b
2	DM_PULLDOWN	RW	**DM pull-down enable:** **0:** DM pull-down resistor disabled **1:** DM pull-down resistor enabled	0b
1	DP_PULLDOWN	RW	**DP pull-down enable:** **0:** DP pull-down resistor disabled **1:** DP pull-down resistor enabled	0b
0	Reserved	RW	Reserved	0b

USB rising interrupt enable register (R8_USB_INTR_EN_R, Address R = 0Dh/0Eh/0Fh, W = 0Dh, S = 0Eh, C = 0Fh)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RW	Reserved	0000000b

0	HOST_DISCON_R	RW	**Host disconnect rise:** Enable Interrupts for logic 0 to logic 1 transitions on HOST_DISCON	0b

USB falling interrupt enable register (R8_USB_INTR_EN_F, Address R = 10h/11h/12h, W = 10h, S = 11h, C = 12h)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RW	Reserved	0000000b
0	HOST_DISCON_F	RW	**Host disconnect rise:** Enable Interrupts for logic 1 to logic 0 transitions on HOST_DISCON	0b

USB interrupt status register (R8_USB_INTR_STAT, Address R = 13h)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RO	Reserved	0000000b
0	HOST_DISCON	RO	**Host disconnect:** Reflects the current value of the host disconnect detector **0**: Connected, USB device detected on host port; **1**: Disconnected, no USB device connection detected	0b

USB interrupt latch register (R8_USB_INTR_L, Address R = 14h)

Bit	Symbol	Access	Description	Reset Value
[7:1]	Reserved	RO	Reserved	0000000b
0	HOST_DISCON	RO	**Host disconnect latch:** Automatically set when an unmasked event occurs on HOST_DISCON. CLEARED when this register is READ	0b

SCARTCH register (R8_SCARTCH, Address R = 16h)

Bit	Symbol	Access	Description	Reset Value
[7:0]	SCARTCH	RW	Registers used for testing, readable and writable, without affecting chip functionality	00000000b

Chapter 4 Parameters

4.1 Absolute maximum ratings

Stresses at or above the absolute maximum ratings listed in the table below may cause permanent damage to the device.

Symbol	Conditions	Min.	Max.	Unit
TA	Operating ambient temperature	-40	85	℃
TS	Storage ambient temperature	-55	150	℃
V5	LDO input voltage (pin V5 to power, pin GND to ground)	-0.4	5.5	V
VDD33	3.3V source voltage (pin VDD33 to power, pin GND to ground)	-0.4	4.0	V
VUSB	Voltage on USB signal pins	-0.4	VDD33+0.4	V
VIO	Voltage on other input or output pins (excluding XI and XO)	-0.4	VDD33+0.4	V
VESD	HBM ESD withstand voltage on I/O pins	5K	7K	V

4.2 Electrical characteristics

Test conditions: TA=25°C, V5=5V or V5=VDD33=3.3V

Symbol	Conditions		Min.	Typ.	Max.	Unit
V5	LDO input power voltage@V5	LDO enabled	4.5	5.0	5.25	V
	For those with a number in the 4th digit from last of the batch number	LDO enabled	3.7	4.2	4.5	
	External input power voltage@V5	LDO bypassed	3.15	3.3	3.45	
VDD33	LDO output voltage @VDD33	LDO enabled	3.15	3.3	3.45	V
	3.3V external input power source@VDD33	LDO bypassed	3.15	3.3	3.45	
ILDO	Internal power regulator LDO external load capability				30	mA
ICC	Operating current during high-speed USB transfers			27		mA
ICC0	Operating current in the idle state			19		mA

VIL	Low level input voltage	0		0.8	V
VIH	High level input voltage	1.9		VDD33	V
VOL	Low level output voltage @ 8mA current sunk		0.4	0.6	V
VOH	High level output voltage @ 8mA current sourced	VDD33-0.6	VDD33-0.4		V
IPU	Pull-up current on the STP pin	20	40	80	uA
RPD	Pull-down resistors for pins Date[7:0]	50	70	90	KΩ
Vlvr	Low voltage reset threshold	2.4	2.8	3.1	V

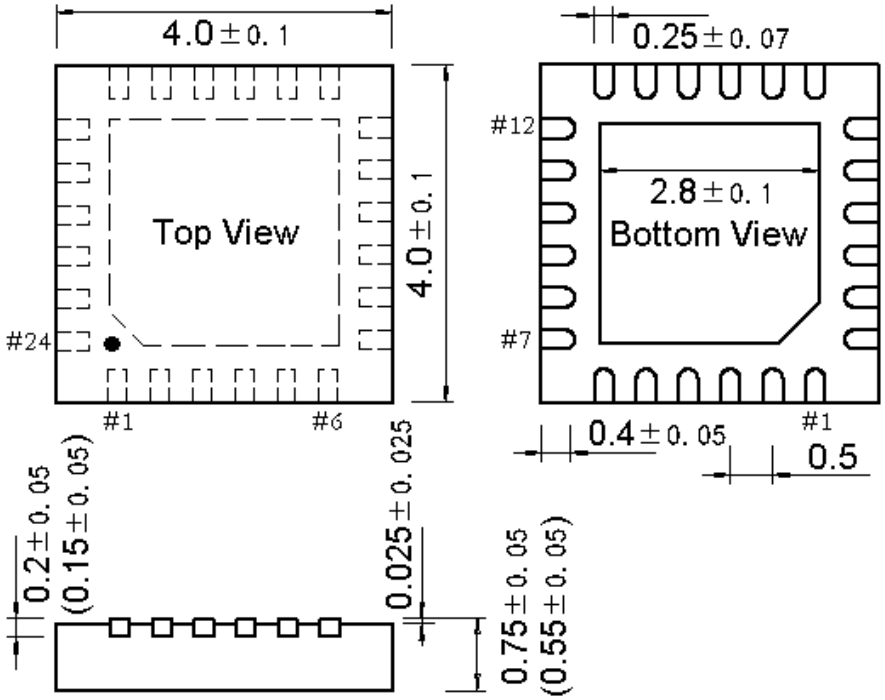
Chapter 5 Package information

Description:

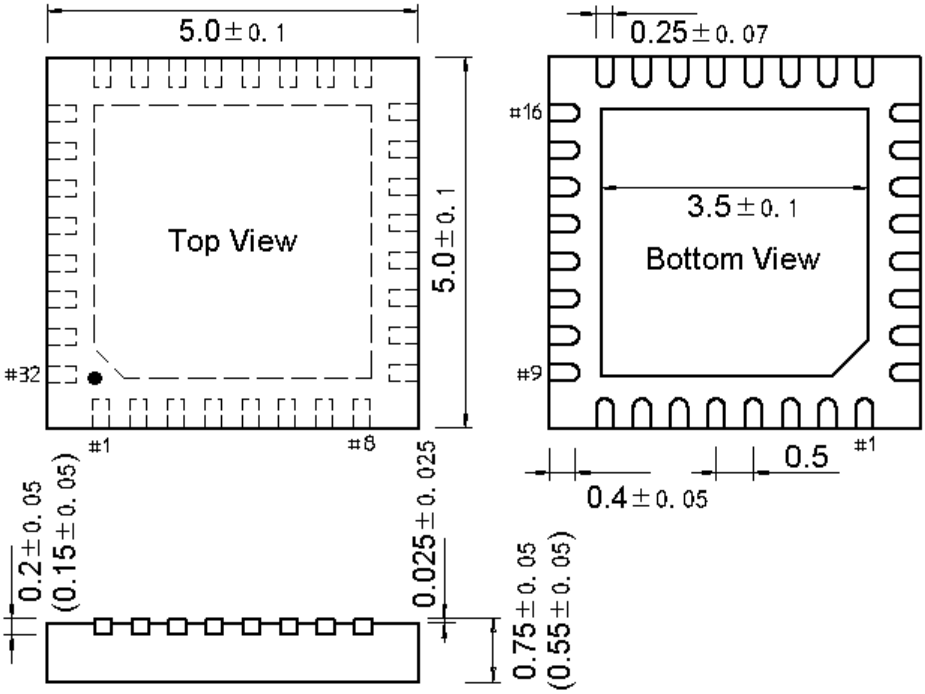
All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

5.1 QFN24_4x4 outline

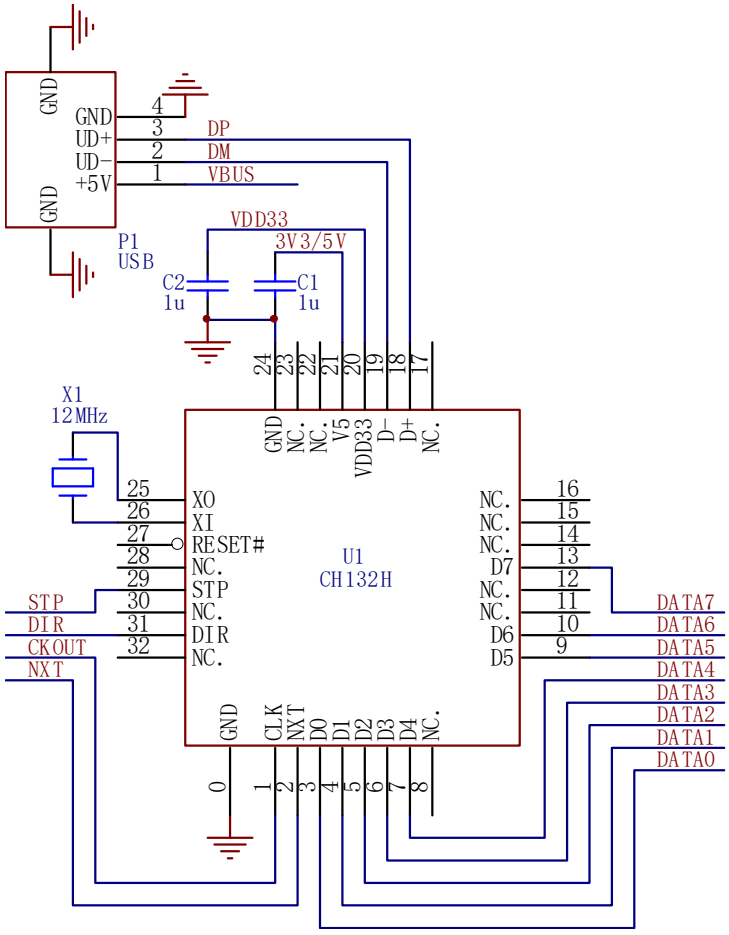


5.2 QFN32_5x5 outline



Chapter 6 Applications

6.1 Connected with an MCU or FPGA



The CH132 acts as a USB PHY for the microcontroller and requires 12 signal lines to be connected. The crystal in the diagram can be replaced by the 12MHz clock provided by the microcontroller or FPGA. The RESET# pin is an optional connection and is left dangling by default. The C1 and C2 capacitors (MLCC) are optional in the 1uF to 4.7uF range.

It is recommended that CH132 and the MCU or FPGA use the same 3.3V supply, which is fed from both V5 and VDD33 pins.

For USB host applications, it is also necessary to provide 5V power to the VBUS and it is recommended to consider VBUS overcurrent protection. Select the CH217 or a similar USB current-limit power switch, which can be controlled by MCU or FPGA for VBUS overcurrent protection. The dynamic load may cause the voltage on VBUS to drop instantaneously when a USB device is hot-plugged. If the internal LDO of the CH132 is enabled, it is recommended to replace the C2 capacitor with a 0.1uF capacitor and a 10uF capacitor in parallel, to avoid 5V drop to affect VDD33 and cause CH132 to reset.

For USB device applications, 5V power can be obtained from VBUS, three cases are as follows: ①,If no VBUS power is used, if needed, VBUS can also be connected to the MCU pins through a 10KΩ resistor for detection; ②, VBUS can be stepped down to 3.3V by an external LDO for use by the MCU and CH132; ③,

If the power consumption of the MCU is small, then it can be powered after stepped down by the internal LDO of the CH132, but it is recommended to increase the capacitance of C2 and add an overvoltage protection device for VBUS. In addition, for the CH132 with a number in the 4th digit from last of the batch number, the voltage on V5 needs to be limited (Connect a diode in series between VBUS and V5 pins to step down the voltage).