NOVOSENSE
纳芯微电子

NSD8381

Bipolar Stepper Motor Driver with Micro-step Dual H-Bridge or Quad Half Bridge

Preliminary Datasheet (EN) 0.2 **Subject to change without notice**

Product Overview

The NSD8381 is a bipolar stepper motor driver, supporting up to max 1.35A full-scale current, for wide range automotive applications including headlight position, projector adjustment actuator in HUD and other valves or BDC motors used in thermal management application.

The device includes current chopping regulation, internal up to 1/32 micro-step translator and multiple decay modes selection to enable stepper motor smooth motion. Furthermore, configurable full-scale current, external pin as simple STEP / DIR input and HOLD mode, all these functions easy customer management of stepper motor operation.

The device is fully protected from faults and short circuits, including undervoltage, overcurrent and overtemperature. Also, open load diagnosis and stall detection can be individually requested to perform during system running. Both SPI interface and dedicated DOUT1/DOUT2 pins are provided to indicate these fault status & alert to microcontroller.

With the different connection of half bridge outputs and HBMODE control, the device can also work as 4x independent half bridges and support other various load as BDC motor, relay etc.

The device features sleep mode with low quiescent current when EN input is low or VDD falls below POR threshold.

Applications

- Headlight adjustment
- HUD
- Actuator control in thermal management

Device information

Part Number	*Package*	*Body Size*
NSD8381-Q1QAIR	VQFN40	6mm × 6mm
NSD8381-Q1QANR	VQFN32	5mm × 5mm

Key Features

- AEC-Q100 Compliant Grade1: -40°C to 125°C
- Bipolar stepper motor driver with max 1.35A full scale current or 4x independent half bridge driver
  - Wide 4.5-V to 36-V Operating Voltage
  - 1200mΩ Typical $R_{DS(ON)}$ (HS + LS), per leg
- Programmable input IOs for STEP / DIR / HOLD or direct half bridge control
- Programmable step mode:

  Full step, half step, mini step, 1/8 micro step, 1/16 micro step, 1/32 micro step
- Programmable output stage slew rate / dead time
- Selectable decay mode:

  Slow decay, mixed decay, auto decay 1, auto decay 2
- Current regulation loop with fully integrated PWM controller and internal current sensing
  - 4bit programmable full scale current and 4-bit programmable HOLD current
  - Internal DAC for reference current generation
  - Spread spectrum function on PWM for EMC reduction
- Very low power consumption in sleep mode
- SPI Interface (24-bit, 4 MHz)
- VQFN40 or VQFN32, wettable flank with exposed pad
- Integrated Protection Features
  - VS Undervoltage Lockout (VS UV)
  - Overcurrent Protection (OCP)
  - Thermal Warning (OTW/UTW) and Shutdown (OTSD)
  - Open load detection
  - Stall detection based on BEMF sensing
  - Fault indicating (FAULT)

1. Pin Configuration and Functions

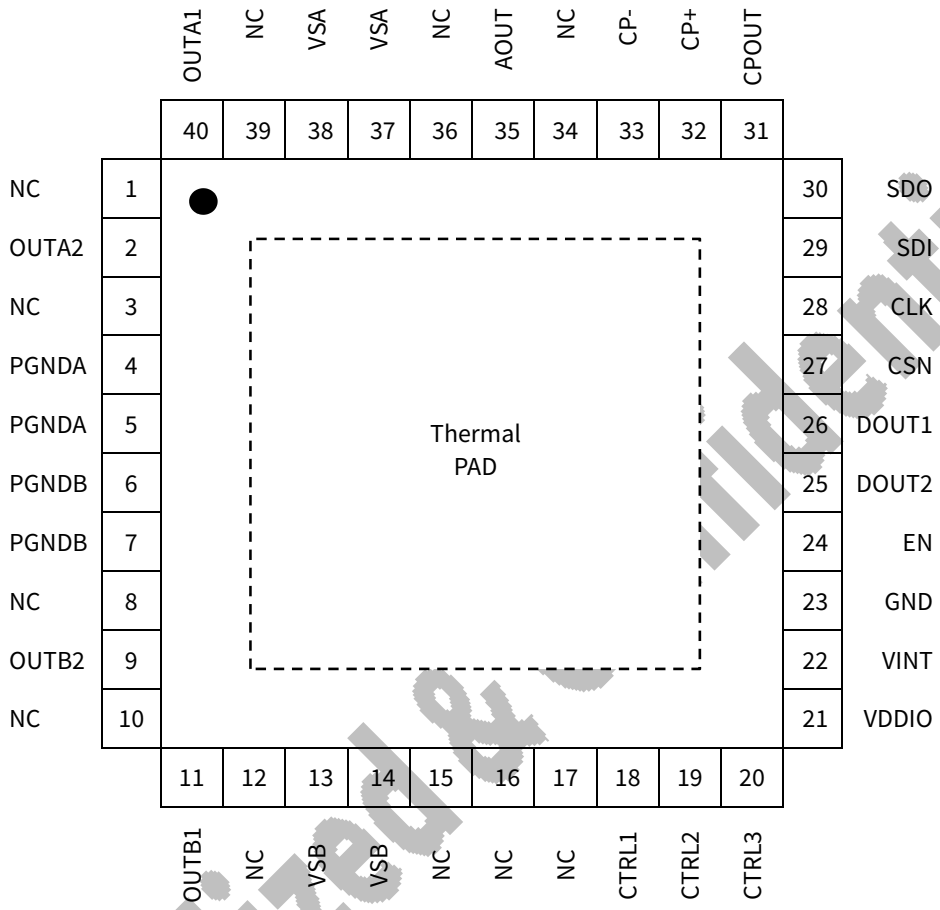


Figure 1 NSD8381 VQFN40 Pinout (top view)

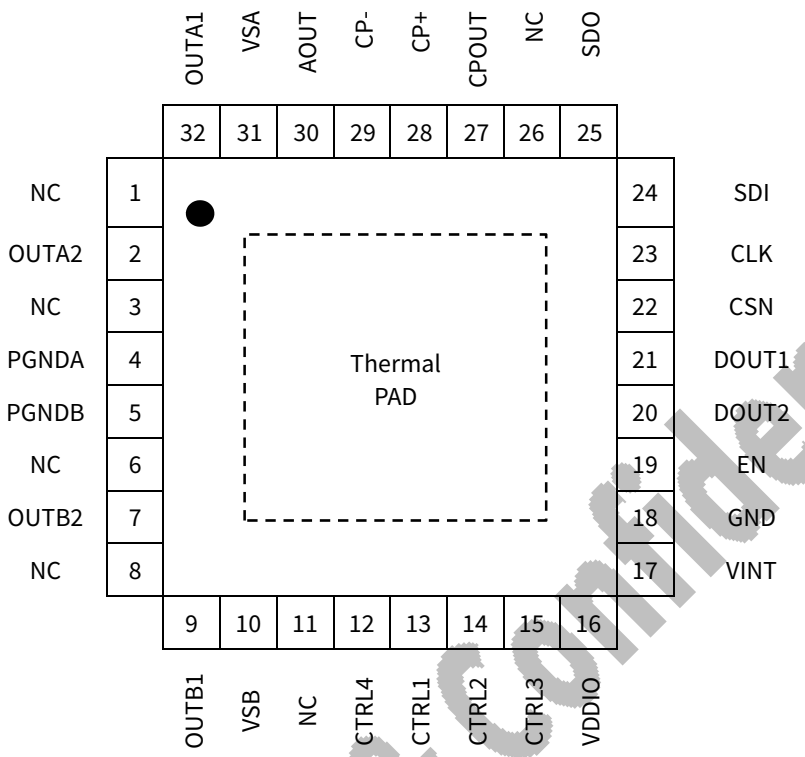


Figure 2 NSD8381 VQFN32 Pinout (top view)

Table 1. NSD8381 Pin Configuration and Description

NAME	NSD8381 PIN		TYPE	DESCRIPTION
	VQFN40 NO.	VQFN32 NO.		
CTRL4	-	12	I	Logic inputs 4. It has internal pull downs. In bipolar stepper mode, no function associated with CTRL4. In half bridge mode, CTRL4 pin controls the OUTB2 output as PWM input.
CTRL1	18	13	I	Logic inputs 1. It has internal pull downs. In bipolar stepper mode, CTRL1 pin are configured as STEP input function in default. In half bridge mode, CTRL1 pin controls the OUTA1 output as PWM input.
CTRL2	19	14	I	Logic inputs 2. It has internal pull downs. In bipolar stepper mode, CTRL2 pin are configured as DIR input function in default.

				In half bridge mode, CTRL2 pin controls the OUTA2 output as PWM input.
CTRL3	20	15	I	Logic inputs 3. It has internal pull downs. In bipolar stepper mode, no function associated with CTRL3 in default. HOLD or SMODE input function through CTRL3 pin can be active by SPI setting after device powers up. In half bridge mode, CTRL3 pin controls the OUTB1 output as PWM input.
VDDIO	21	16	PWR	Digital I/Os supply. Suggest 100nF X7R decoupling capacitor closed to VDDIO pin.
VINT	22	17	PWR	Internal regulator decoupling output. Connect 100nF X7R ceramic capacitor to ground, the capacitor shall be closed to VINT pin.
GND	23	18	PWR	Device ground. Connect to system ground.
EN	24	19	I	Device-enable input pin with internal pull down (active HIGH). If EN input pin is pulled low, all OUTAx/OUTBx go to tri-state and device move to low-power sleep state.
DOUT2	25	20	O	Push-pull output DOUT2 for fault indication or internal PWM signal or fault check indication, selected by SPI setting.
DOUT1	26	21	O	Push-pull output DOUT1 for coil voltage conversion status signals, selected by SPI setting.
CSN	27	22	I	SPI chip select input pin.
SCK	28	23	I	SPI clock input pin.
SDI	29	24	I	SPI data input pin.
SDO	30	25	O	SPI data output pin.
CPOUT	31	27	PWR	Charge pump output. Put 100nF X7R capacitor between VCP and VM pins.
CP+	32	28	PWR	Charge pump high side pin, connect a 100nF X7R capacitor between CPH and CPL pins.
CP-	33	29	PWR	Charge pump low side pin, connect a 100nF X7R capacitor between CPH and CPL pins.
AOUT	35	30	O	Internal analog voltage or reference mux output.
VSA	37,38	31	O	5V to 36V power supply. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitor (>10uF) needs to guarantee VSx pin voltage in maximum range. Put the 0.1uF and bulk capacitor (>10uF) close to the VSx pin. Two VSA and VSB pins should be externally connected together.
OUTA1	40	32	O	Half-bridge output OUTA1 pin. Connect directly to the motor or other inductive load.

OUTA2	2	2	O	Half-bridge output OUTA2 pin. Connect directly to the motor or other inductive load.
PGNDA	4,5	4	PWR	High-current ground path. Connect PGND directly to board ground.
PGNDB	6,7	5	PWR	High-current ground path. Connect PGND directly to board ground.
OUTB2	9	7	O	Half bridge output OUTB2 pin. Connect directly to the motor or other inductive load.
OUTB1	11	9	O	Half bridge output OUTB1 pin. Connect directly to the motor or other inductive load.
VSB	13,14	10	PWR	5V to 36V power supply. Connect a 0.1-µF bypass capacitor to ground, as well as sufficient bulk capacitor (>10uF) needs to guarantee VSx pin voltage in maximum range. Put the 0.1uF and bulk capacitor (>10uF) close to the VSx pin. Two VSA and VSB pins should be externally connected together.
NC	1,3,8,10, 12,15,16,17, 34,36,39	1,3,6,8, 11,26,30	-	Not connected
Exposed PAD	-	-	-	Exposed pad. Connect to board ground. For good thermal dissipation, use large ground planes on multiple layers, and multiple nearby vias connecting those planes.

2. Absolute Maximum Rating

ITEMS	MIN	MAX	UNIT
Power supply voltage (VSA, VSB)	–0.3	40	V
VDDIO voltage	–0.3	5.75	V
VINT voltage	–0.3	5.75	V
Logic input/ouput voltage (SDI, SDO, NCS, SCK, EN, CTRL1, CTRL2, CTRL3, CTRL4, DOUT1, DOUT2)	–0.3	VDDIO+0.3	V
Analog output (AOUT)	–0.3	40	V
VCP, CPH charge pump voltage	VS-0.3	VS+6	V
CPL, charge pump negative pin voltage	-0.3	VS	V
Output voltage (OUTA1, OUTA2, OUTB1, OUTB2) DC condition	–0.3	VS+0.3	V
Output voltage (OUTA1, OUTA2, OUTB1, OUTB2) AC condition, Iout=1A for t<500ms, voutx < VPS+1V	-1	VS+1	V

3. ESD Ratings

SYMBOL	DESCRIPTION	VALUE	UNIT
VESD_HBM	Human Body Model(HBM), VSx & OUTx pins per ANSI/ESDA/JEDEC JS-001	±4000	V
	Human Body Model(HBM), other pins per ANSI/ESDA/JEDEC JS-001	±2000	V
VESD_CDM	Charged device model(CDM), Corner pin, per JEDEC specification JS-002	±750	V
	Charged device model(CDM), other pins, per JEDEC specification JS-002	±500	V

4. Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VM	VM Power supply voltage	4.5		36	V
VDDIO	VDD supply voltage	3		5.5	V
EN, NCS, SCK, SDO, SDI, CTRL1, CTRL2, CTRL3, CTRL4, DOUT1, DOUT2	Logic input / output voltage	0		5.5	V

AOUT	Analog output voltage	0		5.5	V
CTRL1	STEP signal low or high timing	2			us
IFS	Motor full scale current			IFSR (MAX 1.35)	A
IRMS	Motor RMS current			IFSR*0.707 (MAX 1.06)	A

(1) When the maximum allowable output load current is considered during application scenario, both power dissipation and thermal condition, including ambient temperature, application board thermal condition etc., shall also be evaluated.

5. Thermal Information

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
Ta	Ambient operating ambient temperature	-40		125	°C
Tj	Junction temperature	-40		150	°C
Tstg	Storage temperature	-65		150	°C
Rthjc	VQFN40, Thermal resistance, junction to case		5 (TBD)		°C/W
Rthjc	VQFN32, Thermal resistance, junction to case		5 (TBD)		°C/W
Rthja	VQFN40, Thermal resistance, junction to ambient, on 4-layer PCB based on JEDEC standard		56 (TBD)		°C/W
	VQFN40, Thermal resistance, junction to ambient, on 2-layer PCB based on JEDEC standard		23 (TBD)		°C/W
Rthja	VQFN32, Thermal resistance, junction to ambient, on 4-layer PCB based on JEDEC standard		60 (TBD)		°C/W
	VQFN32, Thermal resistance, junction to ambient, on 2-layer PCB based on JEDEC standard		30 (TBD)		°C/W

6. Functional description

6.1. VSA, VSB Input

VS is the supply voltage used for internal H-bridge outputs and change pump; it ranges from 4.5v to 36v with typical case 13.5v power supply. VSA and VSB pins must be shorted together externally on PCB.

During motor operation, electrical energy is stored in the motor coils, and then fed back to the supply voltage VS once motor shut down. Thus, it is required to put at both 100nF ceramic and >10uF bulk electrolytic capacitor closed to VSA, VSB pin to avoid electrical spike / overstress on VSA and VSB pins.

6.1.1.VS UV, VS RST

When VS power supply pin voltage falls below the undervoltage threshold (VUV_LOW) over 10us typ. undervoltage deglitch time,

- The corresponding VS undervoltage flag (*VSUV bit* in STA1 register) is set to '1';
- half bridge outputs *OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off*.

When VS rise above the V_{UV_HIGH} longer than 10us typ. undervoltage deglitch time, then

- If FLT_LATCH bit = 1, device works in fault latch mode, to recovery normal operation, VSUV bit shall be read & clear to re-enable charge pump and DRV_EN (ME) bit shall remain unchanged '1' status.
- If FLT_LATCH bit = 0, device automatically resumes operation when DRV_EN (ME) bit remains unchanged '1' status and charge pump voltage exit CP_UV. The VSUV bit keeps '1' until read & clear command is received.

When VS power supply pin voltage falls below the undervoltage threshold ($V_{UV\_RST\_LOW}$) over 5us typ. undervoltage reset deglitch time,

- SPI unavailable.
- half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When VS rise above the $V_{UV\_RST\_HIGH}$ longer than 5us typ. undervoltage deglitch time, then

- *Device is reset and all SPI registers are reset to default value.*

POWERUP _NMASK internal digital signal = 0, it masks the VS and charge pump UV detection until VS rising over V_{UV_HIGH} (charge pump enable) plus charge pump operating timing (TBD us). After the timing elapses, POWERUP_NMASK internal signal = 1, VS UV and CP UV detection works in normal.

6.1.2. VS OV protection

When OVP_DIS bit =0 and VS power supply pin voltage rises above the overvoltage threshold (V_{OV_HIGH}) over 10us typ. overvoltage deglitch time,

- The corresponding VS overvoltage flag (VSOV bit in STA1 register) is set to '1';
- half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2 becomes OFF and charge pump is switched off.

When OVP_DIS bit =0 and VS decrease under the V_{OV_LOW} longer than 10us typ. overvoltage deglitch time, then

- If FLT_LATCH bit = 1, device works in fault latch mode, to recovery normal operation, VSOV bit shall be read & clear and DRV_EN (ME) bit remains unchanged '1' status
- If FLT_LATCH bit = 0, device automatically resumes operation when DRV_EN (ME) bit remains unchanged '1' status. The VSOV bit keeps '1' until read & clear command is received.

When OVP_DIS bit = 1, overvoltage protection function is disabled, no reaction on VSOV status and DRV_EN (ME) bit, half bridge outputs OUTA1, OUTA2, OUTB1, OUTB2, charge pump; in consequence, no need for overvoltage recovery.

6.1.3.VS power supply electrical specifications

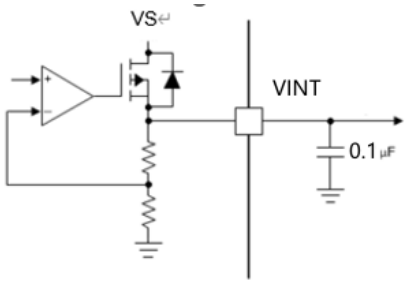
Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

VS power supply electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY (VSA, VSB)						
VS	VS operating voltage		4.5		36	V
I_{VS}	VS operating supply current	VSA = VSB = 13.5V, EN=HIGH, all output off		3	7	mA
		VSA = VSB = 13.5V, EN=HIGH, half bridge driver working, no load			10	mA
I_{VS_SLEEP}	VS sleep current	VSA= VSB = 13.5V, -40≤Tj≤85°C EN=LOW, I(VSA)+I(VSB)			10	μA
VS_UV_L	VS undervoltage threshold	VSx falls until VSUV triggers	4.25	4.5	4.75	V
VS_UV_H		VSx rises until operation recovers	4. 5	4.75	5	V
V_{UV_HYS}	VS undervoltage hysteresis			200		mV
t_{UV}	VS undervoltage deglitch time	Guaranteed by digital scan	7	10	13	us
V_{UV_RST}	VS undervoltage reset	VSx fall until reset triggers	2.9	3.3	3.7	V
		VSx rise until reset	3.1	3.5	3.9	V
$V_{UV\_RST\_HYS}$	VS undervoltage reset hysteresis			200		mV
V_{OV}	VS overvoltage	VSx increasing, OVP_DIS = 0	28		32	V
		VSx decreasing, OVP_DIS = 0	27		31	V
V_{OV_HYS}	VS overvoltage hysteresis			1		V
t_{OV}	VS overvoltage deglitch time	Test by digital scan		10		us
C_{VS}	Capacitor on VSA, VSB pin	Application information	100			nF
C_{VS_BULK}	Bulk Capacitor on VSx pin	Application information	10			uF

6.2. VINT internal regulator

A linear voltage regulator is integrated into the device. For proper operation, bypass the VINT pin to GND using a ceramic capacitor which values from 47nF~470nF.



The internal regulator can be used to supply internal blocks and provide a maximum of 2 mA load current for on board load for example external reference.

During sleep state, the internal regulator is disabled.

6.2.1. VINT internal regulator electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

VINT internal regulator electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Internal regulator (VINT)						
V_{VINT}	VINT internal regulator voltage	Load current 0~2mA	4.65	5	5.35	V
C_{VINT}	Capacitor on VINT pin	Application information	47	100	470	nF

6.3. VDDIO Supply Input

VDDIO pin accepts wide supply range from 3v to max 5.5v which intends for the compatibility with both 3.3v and 5v system supply. 100nF X7R ceramic capacitor is suggested to put closed to VDDIO pin.

SPI interface, digital output will be inactive when VDDIO drops below VDDIO_RST_L, so including charge pump and all half bridge drivers are switched off. Once VDDIO > VDDIO_RST_H, internal digital is reset.

6.3.1. VDDIO internal regulator electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

VDDIO electrical parameters

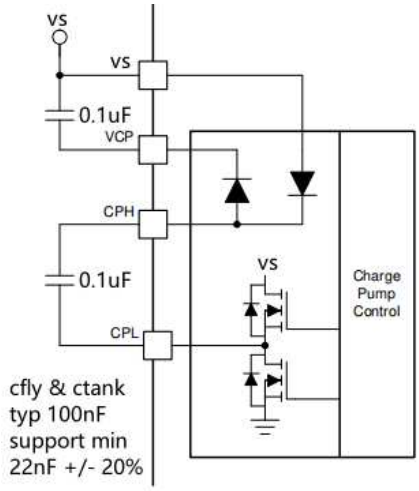
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDIO supply input (VDDIO)						
I_{VDDIO}	Input current of VDDIO	EN=High, outputs off			3(TBD)	mA

I_{VDDIO_SLEEP}	Input current of VDD in sleep mode	EN=LOW, SPI inactive -40≤Tj≤85 °C		5	10	uA
VDDIO_RST_H	VDDIO reset high threshold,	VDDIO increasing	2	2.5	3	V
VDDIO_RST_L	VDDIO reset low threshold	VDDIO decreasing	1.8	2.3	2.8	V

6.4. Charge pump

The charge pump is integrated to support internal high side driving.

It requires external fly capacitor between CPH and CPL, also external tank capacitor between VS and VCP.



It also has the possibility to vary instantaneous frequency for spread spectrum capability (CP_SS_CONFIG bit in CONFIG_8 register)

6.4.1.VCP charge pump electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

VCP electrical parameters

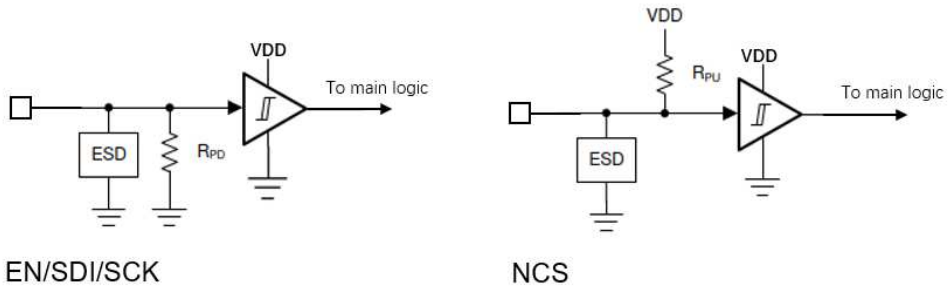
SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Charge pump (VCP)						
VCP	Charge pump output voltage	VSx >=9V, ICP=3mA		VS+5 (TBD)		V
		6v<VSx <9V, ICP=3mA		VS+4 (TBD)		V
VCP_UV	charge pump undervoltage	VCP falling		VS+3		V
VCP_UV_HYS	Charge pump undervoltage hysteresis			200		mV

tCP_UV	Charge pump undervoltage digital deglitch filter	Test by digital scan		10		us
Fcp	charge pump frequency	spread spectrum disable		400		kHz
		spread spectrum enable		+/- 10%		kHz

6.5. Digital Input EN & CTRL1/2/3/4 & SPI SDI/SCK/NCS

NCS / SDI / SCK is the typical CMOS schmitt trigger as SPI inputs.

EN, SCK, SDI and CTRL1/2/3/4 input pins has typ. 100kohm internal pull-down resistance, while 100kohm internal pull up is applied on NCS pin.



6.5.1. EN Function

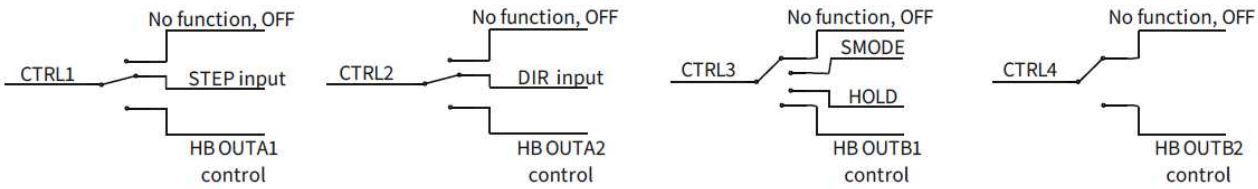
The EN pin is sleep / active mode control signal.

When it is driven low, internal logic / register is reset, charge pump / all outputs OUTA1/A2, OUTB1/OUTB2 are disabled, and device enter sleep mode.

After EN transition from low to high at VDDIO>VDDIO_POR & VS>Vuv_rst, device come out sleep mode at finishing internal POR and RSTB=1. A TWAKE time shall be wait for SPI ready for write/read operation and charge pump reach regulated voltage once device move from sleep to normal operation.

6.5.2. CTRL1/2/3/4 Function

Some of the functions in the NSD8381, such as stepper mode – STEP / DIR / HOLD or independent half bridge control, can be controlled directly by microcontroller I/Os (without using SPI) through the CTRL1/2/3/4 digital input pins. The action to be executed by these CTRLx pins is defined by selection bits in CONFIG_1 and CONFIG_8 registers.



CTRL1/2/34 pin selection function are defined as below table.

Pin	Function	Register configuration		Comment
		CONFIG_1 (Address 0x03)	CONFIG_8 (Address 0x11)	
CTRL1	Stepper mode - no function	Bit D5, CTRL1_SEL='0'	Bit D3, HBMODE ='0'	STEP signal is not related to CTRL1 under these register bits setting.It is controlled by SPI CONFIG_3 PH[5:0] or CONFIG_7 APH[6:0] if CONFIG_8 bit D7, 1/32_STEP_EN=1
	Stepper mode - STEP input	Bit D5, CTRL1_SEL='1'	Bit D3, HBMODE ='0'	**Default setting, after power up.** CTRL1 pin as stepper mode - STEP signal input.
	Half bridge - OUTA1 control input	Don't care	Bit D3, HBMODE ='1'	See details in section 'Independent half bridge mode'
CTRL2	Stepper mode - no function	Bit D3, CTRL2_SEL='0'	Bit D3, HBMODE ='0'	DIR signal is not related to CTRL2 under these register bits setting.It is controlled by SPI CONFIG_3 DIR bit.
	Stepper mode - DIR input	Bit D3, CTRL2_SEL='1'	Bit D3, HBMODE ='0'	**Default setting, after power up** CTRL2 pin as stepper mode - DIR signal input.
	Half bridge - OUTA1 control input	Don't care	Bit D3, HBMODE ='1'	See details in section 'Independent half bridge mode'
CTRL3	**Stepper mode - no function**	Bits D2&D1, CTRL3_SEL[1:0]= '00'	Bit D3, HBMODE ='0'	**Default setting, after power up**. Changing stepper mode or switching into HOLD are not related to CTRL3 pin under these register bits setting. Device into HOLD operation mode is controlled by CONFIG_3 HOLD_EN bit.
	Stepper mode - SMODE input	Bits D2&D1, CTRL3_SEL[1:0]= '01'	Bit D3, HBMODE ='0'	CTRL3 pin controls stepper operation mode switching between ASM[2:0] and SM[2:0] under these register bits setting
	Stepper mode - HOLD input	Bits D2&D1, CTRL3_SEL[1:0]= '10'	Bit D3, HBMODE ='0'	CTRL3 pin directlly controls HOLD operation mode switching under these register bits setting
	Half bridge - OUTB1 control input	Don't care	Bit D3, HBMODE ='1'	See details in section 'Independent half bridge mode'
CTRL4	**Stepper mode - no function**	No bit in CONFIG_1 related CTRL4	Bit D3, HBMODE ='0'	**Default setting, after power up**
	Half bridge - OUTB2 control input	Don't care	Bit D3, HBMODE ='1'	See details in section 'Independent half bridge mode'

6.5.3. Logical control input pins electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

Logic inputs electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Logic Control Input (EN, NCS, SDI, SCK, CTRL1, CTRL2, CTRL3, CTRL4)						
V_{IL}	Input logic low voltage				0.8	V
V_{IH}	Input logic high voltage		2			V
V_{HYS}	Input logic hysteresis			0.5		V
R_{PD}	Pulldown resistance	EN, SDI, SCK, CTRL1, CTRL2, CTRL3, CTRL4	50	100	150	kΩ
R_{PU}	Pullup resistance	NCS	50	100	150	kΩ
C_{IN}	Input capacitance	NCS, SDI, SCK, CTRL1, CTRL2, CTRL3, CTRL4 pin Specified by design			15	pF
$T_{Deglitch\_EN}$	Deglitch filter on EN falling and rising			10(TBD)	20	us
T_{WAKE}	wake-up time	From EN low to high transition until SPI ready			150(TBD)	us
		From EN low to high transition until Output transition			1.5(TBD)	ms

6.6. Digital output SDO and DOUT1 / DOUT2

SDO is push-pull structure, which transfers internal register values to microcontroller. It also features SDO tristate at NCS high when device SPI interface is not selected.

The two DOUT pins, DOUT1 & DOUT2, are also push-pull structure with tristate when EN=0.

6.6.1. DOUT1 / DOUT2 functions

The device drives DOUT1, DOUT2 pins upon detecting internal status, trigger or faults signals as shown in below table.

CONFIG_2 register DOUT1[1:0] setting	DOUT1 Function
2b'00'	OFF, tri-state (EN=0), LOW(EN=1)
2b'01'	Coil voltage conversion ready signal (CVRDY) output
2b'10'	Coil voltage conversion under low limit (CVLL) output
2b'11'	Coil voltage conversion out of range (CVOOR) output / replace CVRUN runaway Name

CONFIG_2 register DOUT2[1:0] setting	DOUT2 Function
2b'00'	OFF, tri-state (EN=0), LOW(EN=1)
2b'01'	Internal PWM signal (PWM)
2b'10'	Fault (Fault) output
2b'11'	Fault Check Indicator (FCI)

6.6.2. Digital output pins electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

digital output electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DOUT1, DOUT2, SDO output (push-pull)						
V_{OL}	DOUT DOUT1 & DOUT2 & SDO output low voltage	I_O = 5 mA		0.2	0.5	V
V_{OH}	VOH_DOUT DOUT1 & DOUT2 & SDO Output high	I_O = 5 mA	VDDIO-0.5			V
Ileak_DOUT	Ileak_DOUT DOUT1 & DOUT2 & SDO Output leakage current	DOUT1, DOUT2 function selection OFF, EN=0, 0<V_{DOUT}<VDDIO NCS high, 0<V_{SDO}<VDDIO	-1		1	uA
Cout	Cout Output capacitance	Specified by design			60	pF

6.7. Analog output AOUT

The device integrates an analog output channel, which can be selectable among embedded sensor output, internal bandgap voltage reference or test mode voltage/reference mux, see **CONFIG_1** register ***AOUT_SEL*** bits setting.

CONFIG_1 register AOUT_SEL[1:0] setting	AOUT Function
2b'00' or 2b'11'	Disabled
2b'01'	Voltage proportional to junction temperature
2b'10'	Bandgap voltage

6.7.1. Analog output pins electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

Analog output electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Analog output (Bandgap)						
V_{AOUT_BG}	V_{AOUT_BG} Bandgap output voltage			1.2		V
$V_{AOUT\_BG\_ERR}$	$V_{AOUT\_BG\_ERR}$ Bandgap output voltage accuracy		-2.5		2.5	%
Analog output (TSENSE)						
V_{AOUT_TSENSE}	Output voltage proportional to junction temperature			1.32(TBD)		V
K_{AOUT_TSENSE}	Thermal coefficient of output proportional to junction temperature			-4.24(TBD)		mv/℃
Analog output						
Cout	Output capacitance				100	pF
I_{AOUT}	Output current				10	uA

6.8. Stepper mode / Step mode selection & Coil current translator

6.8.1. Step mode selection

Six different step modes, full step (4steps), half step (8 steps), 1/4 mini step (16 steps), 1/8 micro step (32 steps), 1/16 micro step (64 steps), 1/32 micro step (128 steps), can be selected depending on application required step resolution.

CONFIG_3 register SM[2:0] / ASM[2:0] bits set the step mode from full step to 1/16 micro step, while CONFIG_8 register 1/32 STEP_EN bit control 1/32 micro step enable or not, CONFIG_8 FULL_STEP_IFS bit selects 71% or 100% full scale current.

After device POWER ON RESET (caused by VSx, EN, VDDIO), the internal step mode is reset to default 1/16 micro step and coil current translator moves to the position 0 degree.

6.8.2. Coil current translator

[Coil current translator] The translator starts from position 0 of corresponding step mode, and the next position is increased or decreased with 1 of the same columns. As shown in below table, the relative coil A current and coil B current vs. step modes / phase counter are listed.

Positive current is defined as current flowing from OUTA1 to OUTA2 or OUTB1 to OUTB2, in contrast, current from OUTA2 to OUTA1 or OUTB2 to OUTB1 is considered as negative.

Internal translator of start position 0°

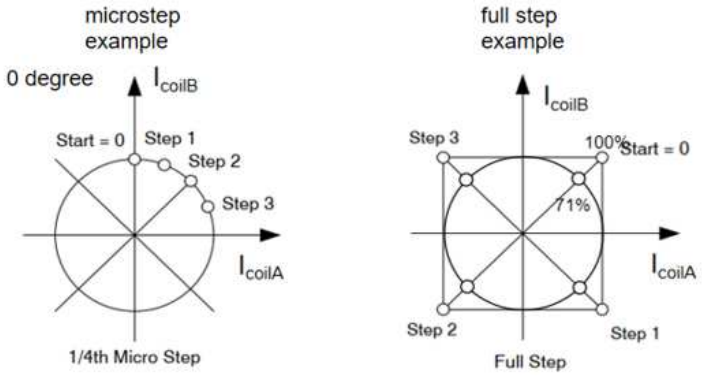
APH[6:0]	PH[5:0]	1/32 micro step	1/16 micro step	1/8 micro step	1/4 mini step	1/2 half step	coil A % of IFS	coil B % of IFS
0000000	000000	0	0	0	0	0	0	100
0000001		1					4.91	99.88
0000010	000001	2	1				9.8	99.52
0000011		3					14.67	98.92
0000100	000010	4	2	1			19.51	98.08
0000101		5					24.3	97
0000110	000011	6	3				29.03	95.69
0000111		7					33.69	94.15
0001000	000100	8	4	2	1		38.27	92.39
0001001		9					42.76	90.4
0001010	000101	10	5				47.14	88.19
0001011		11					51.41	85.77
0001100	000110	12	6	3			55.56	83.15
0001101		13					59.57	80.32
0001110	000111	14	7				63.44	77.3
0001111		15					67.16	74.1
0010000	001000	16	8	4	2	1	70.71	70.71
0010001		17					74.1	67.16
0010010	001001	18	9				77.3	63.44
0010011		19					80.32	59.57
0010100	001010	20	10	5			83.15	55.56
0010101		21					85.77	51.41
0010110	001011	22	11				88.19	47.14
0010111		23					90.4	42.76
0011000	001100	24	12	6	3		92.39	38.27
0011001		25					94.15	33.69
0011010	001101	26	13				95.69	29.03
0011011		27					97	24.3

0011100	001110	28	14	7			98.08	19.51
0011101		29					98.92	14.67
0011110	001111	30	15				99.52	9.8
0011111		31					99.88	4.91
0100000	010000	32	16	8	4	2	100	0
0100001		33					99.88	-4.91
0100010	010001	34	17				99.52	-9.8
0100011		35					98.92	-14.67
0100100	010010	36	18	9			98.08	-19.51
0100101		37					97	-24.3
0100110	010011	38	19				95.69	-29.03
0100111		39					94.15	-33.69
0101000	010100	40	20	10	5		92.39	-38.27
0101001		41					90.4	-42.76
0101010	010101	42	21				88.19	-47.14
0101011		43					85.77	-51.41
0101100	010110	44	22	11			83.15	-55.56
0101101		45					80.32	-59.57
0101110	010111	46	23				77.3	-63.44
0101111		47					74.1	-67.16
0110000	011000	48	24	12	6	3	70.71	-70.71
0110001		49					67.16	-74.1
0110010	011001	50	25				63.44	-77.3
0110011		51					59.57	-80.32
0110100	011010	52	26	13			55.56	-83.15
0110101		53					51.41	-85.77
0110110	011011	54	27				47.14	-88.19
0110111		55					42.76	-90.4
0111000	011100	56	28	14	7		38.27	-92.39
0111001		57					33.69	-94.15

0111010	011101	58	29				29.03	-95.69
0111011		59					24.3	-97
0111100	011110	60	30	15			19.51	-98.08
0111101		61					14.67	-98.92
0111110	011111	62	31				9.8	-99.52
0111111		63					4.91	-99.88
1000000	100000	64	32	16	8	4	0	-100
1000001		65					-4.91	-99.88
1000010	100001	66	33				-9.8	-99.52
1000011		67					-14.67	-98.92
1000100	100010	68	34	17			-19.51	-98.08
1000101		69					-24.3	-97
1000110	100011	70	35				-29.03	-95.69
1000111		71					-33.69	-94.15
1001000	100100	72	36	18	9		-38.27	-92.39
1001001		73					-42.76	-90.4
1001010	100101	74	37				-47.14	-88.19
1001011		75					-51.41	-85.77
1001100	100110	76	38	19			-55.56	-83.15
1001101		77					-59.57	-80.32
1001110	100111	78	39				-63.44	-77.3
1001111		79					-67.16	-74.1
1010000	101000	80	40	20	10	5	-70.71	-70.71
1010001		81					-74.1	-67.16
1010010	101001	82	41				-77.3	-63.44
1010011		83					-80.32	-59.57
1010100	101010	84	42	21			-83.15	-55.56
1010101		85					-85.77	-51.41
1010110	101011	86	43				-88.19	-47.14
1010111		87					-90.4	-42.76

1011000	101100	88	44	22	11		-92.39	-38.27
1011001		89					-94.15	-33.69
1011010	101101	90	45				-95.69	-29.03
1011011		91					-97	-24.3
1011100	101110	92	46	23			-98.08	-19.51
1011101		93					-98.92	-14.67
1011110	101111	94	47				-99.52	-9.8
1011111		95					-99.88	-4.91
1100000	110000	96	48	24	12	6	-100	0
1100001		97					-99.88	4.91
1100010	110001	98	49				-99.52	9.8
1100011		99					-98.92	14.67
1100100	110010	100	50	25			-98.08	19.51
1100101		101					-97	24.3
1100110	110011	102	51				-95.69	29.03
1100111		103					-94.15	33.69
1101000	110100	104	52	26	13		-92.39	38.27
1101001		105					-90.4	42.76
1101010	110101	106	53				-88.19	47.14
1101011		107					-85.77	51.41
1101100	110110	108	54	27			-83.15	55.56
1101101		109					-80.32	59.57
1101110	110111	110	55				-77.3	63.44
1101111		111					-74.1	67.16
1110000	111000	112	56	28	14	7	-70.71	70.71
1110001		113					-67.16	74.1
1110010	111001	114	57				-63.44	77.3
1110011		115					-59.57	80.32
1110100	111010	116	58	29			-55.56	83.15
1110101		117					-51.41	85.77

1110110	111011	118	59				-47.14	88.19
1110111		119					-42.76	90.4
1111000	111100	120	60	30	15		-38.27	92.39
1111001		121					-33.69	94.15
1111010	111101	122	61				-29.03	95.69
1111011		123					-24.3	97
1111100	111110	124	62	31			-19.51	98.08
1111101		125					-14.67	98.92
1111110	111111	126	63				-9.8	99.52
1111111		127					-4.91	99.88

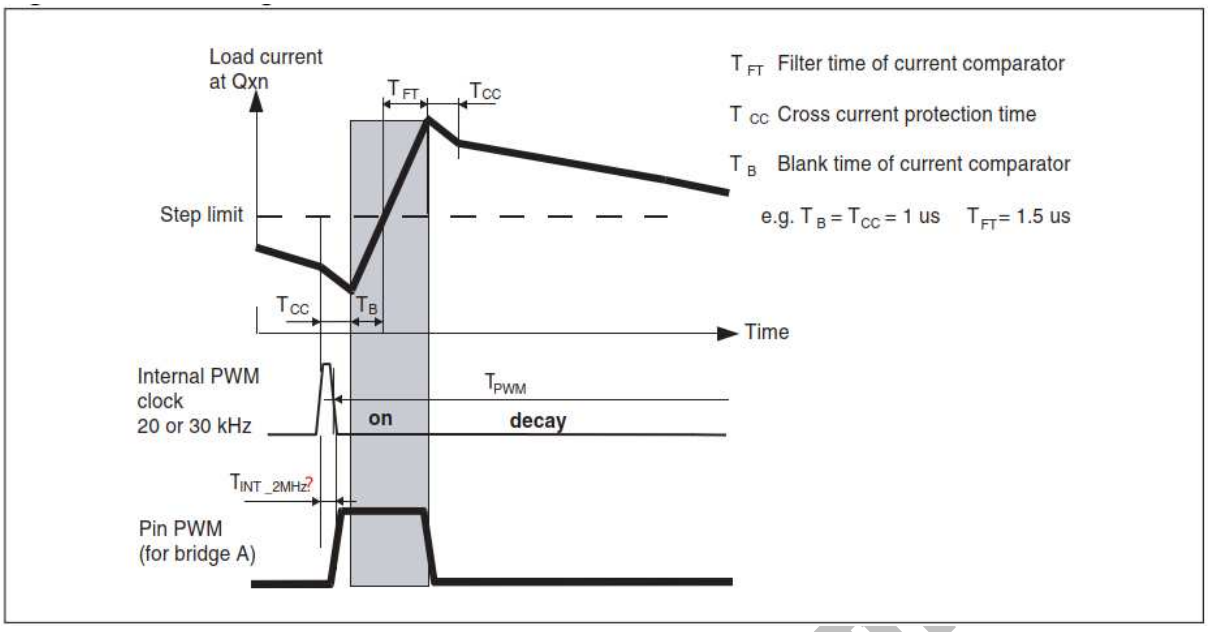


6.8.3. PWM current regulation

An internal current monitor output of each low-side sources a current image which has a fixed ratio of the instantaneous load current. These current images are compared with the current limit in current regulation loop. This loop comparator generates the PWM control signal which turns on or off the output H-bridge stage. The switching on points of PWM control signal are synchronized to internal PWM clock. The bridges are switched on until the load current sensed at low side exceeds the limit over t_{FT}. The current comparator signal is used to detect open load condition also.

Before enabling the current regulation, the current monitor output is ignored for a programmable period (T_B) which related on output slew rate and additional extended (See CONFIG_4 register TBLANK_EXT bit) or reduction setting (See CONFIG_8 register TBLANK_RED bit). The blanking time also sets the minimum driving ON time of PWM.

The frequency of internal PWM clock can be select among 20khz, 30khz, and 40khz. High frequency can reduce the overall current ripple amplitude. To reduce the PWM emission, the spread spectrum function can be enabled. (See CONFIG_1 register PWM_SS bit).

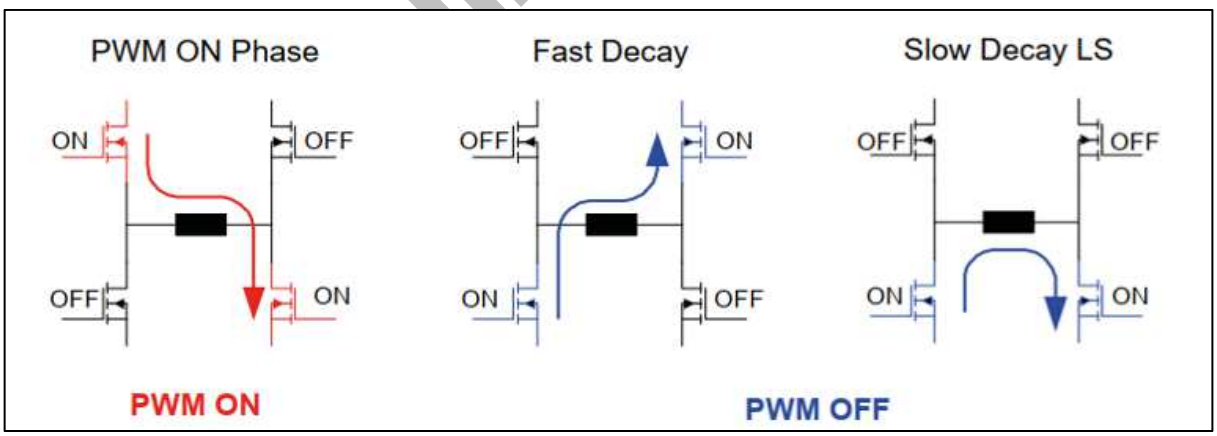


Range of limit can reach from programmed full scale value (CONFIG_6 register IFSR[3:0]) down belonging LSB value of 9-bit internal DAC. The data of the internal DACs comes from the 33 current profiles shown in coil current translator.

If signal changes to logic high at pin CTRL1(STEP function), then next current profiles are moved in DAC Phase A and B. The index of profile depends on phase counter reading, direction, and step mode.

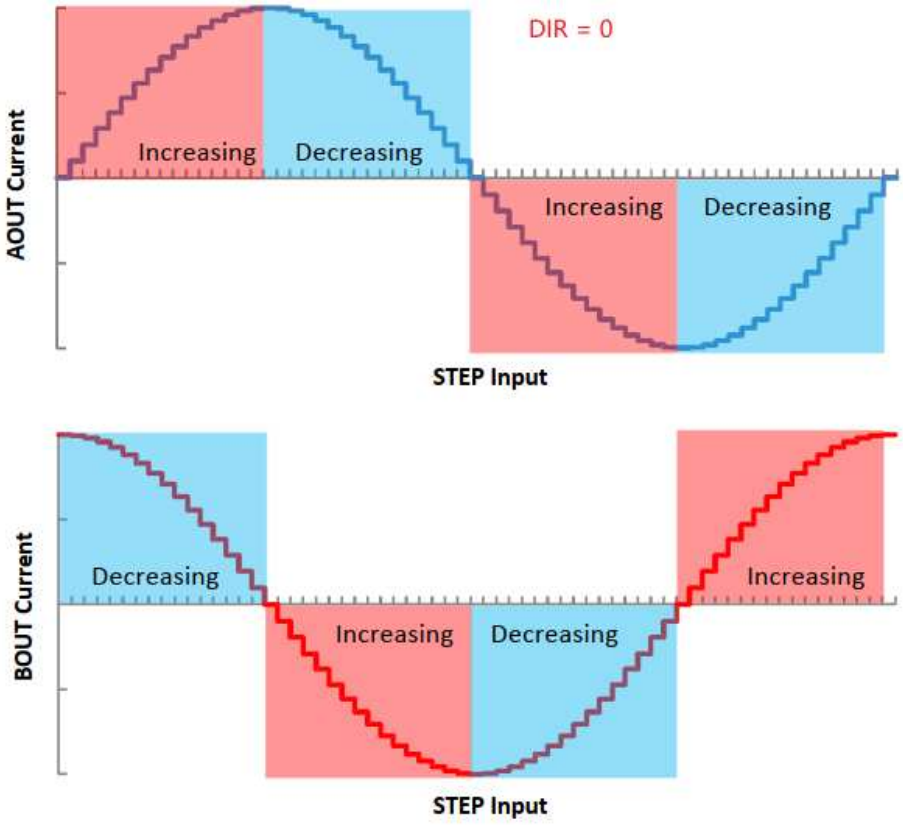
6.8.4. Decay modes

During PWM current regulation, once the current limit is reached over t_{FT}, the H-bridge operates in two different states, mixed decay, or slow decay. In mixed decay mode, the H-bridge first turns on the opposite HS and LS to reduce the current in fast decay; as the load current drop and cross the limit for t_{FT}, then the bridge output stage is changed to slow decay to avoid large current ripple. In the contrast, if the slow decay mode is selected, both low side FETs will be turn on until next PWM cycle



In order to provide the low current ripple of entire steps, the device features four decay selection, especially auto decay1 and auto decay 2, which combine the advantage of low current ripple in slow decay and fast response in fast decay for both increasing current steps and decreasing current steps. Figure below shows an example of increasing and decreasing current step at DIR=0.

CONFIG_4 register DECAY_SEL1:0] setting	Increasing current steps	Decreasing current steps
2b'00' auto decay 1	Slow decay	Mixed decay
2b'01' slow decay always	Slow decay	Slow decay
2b'10' mixed decay always	Mixed decay	Mixed decay
2b'11' auto decay 2	Slow decay	Slow/mixed decay combination



During slow decay, it allows the current to be recirculated through the two turned on low-side FETs of the H-bridge.

Note: Slow decay features the smallest current ripple of the decay modes. However, during decreasing current steps, current decreases very slowly and takes longer time to settle to the new current step. If the current at the end of the PWM off time is still above the current step level, slow decay will be extended for another PWM off time duration and so on, till the current reach the current step during the off time.

So slow decay may not properly regulate current where motor works very low stepping speeds, because quite small back-EMF is present across the motor coil in this state, motor current can rise very quickly, and may require a large off-time. Also

in some cases (long tblank and tFT timing, but low current limit), this may cause a loss of current regulation, and a more aggressive decay mode is recommended.

Mixed decay begins as fast decay for a time, followed by slow decay for the remainder. In this mode, mixed decay occurs for both increasing and decreasing current steps.

The current ripple of mixed decay always mode is larger than slow decay. On decreasing current steps, mixed decay settles to the new current limit level faster than slow decay.

In cases motor at very low stepping speeds, or low current limit with long tblank and tFT timing,

mixed decay mode allows the current level to stay in regulation.

6.8.5. Run mode and Hold mode

The driver has two stepper modes, RUN mode and HOLD mode, and the full scale current of each mode can be set by SPI (CONFIG_6 register, IFSR[3:0] and IFSH[3:0] bits).

The percentage of full-scale current for each register value is shown as below

CONFIG_6 register IFSR[3:0] setting	RUN mode, full scale current (mA)	[%]
’0000’	176	13%
’0001’	198	14.65%
’0010’	220	16.22%
’0011’	302	22.3%
’0100’	323	23.83%
’0101’	329	24.3%
’0110’	375	27.7%
’0111’	396	29.2%
’1000’	465	34.3%
’1001’	571	42.7%
’1010’	679	50.18%
’1011’	812	60%
’1100’	920	68%
’1101’	1051	77.68%
’1110’	1160	85.7%
’1111’	1350	100%

CONFIG_6 register IFSH[3:0] setting	RUN mode, full scale current (mA)	[%]
’0000’	28	8.6%
’0001’	50	15.34%
’0010’	62	19.02%
’0011’	73	22.39%
’0100’	79	24.23%
’0101’	84	25.76%
’0110’	95	29.14%
’0111’	101	30.98%
’1000’	118	36.19%
’1001’	140	42.94%
’1010’	168	51.53%
’1011’	202	61.96%
’1100’	230	70.55%
’1101’	264	80.98%
’1110’	292	89.57%
’1111’	326	100%

The driver HOLD mode is determined by SPI CONFIG_3 register HOLD_EN bit or CTRL3 pin status if CTRL3_SEL bit HOLD function enable & HB_MODE bit function not active.

If the coil voltage measurement function is enabled (see SPI CONFIG_5 register CV_EN bit), the sampled coil voltage is out of the range [CVLLA, CVUL] for the consecutive conversion number over CONFIG_5 register CV_STALL_NUM[2:0] bits and CONFIG_5 register STALL_HOLD_EN bit is set, then the STALL bit flag in STA_1 register is asserted and the HOLD_EN bit is also automatically set to enter HOLD mode. In this condition, STALL bit flag must be cleared before HOLD_EN bit can be configured or reset to 0.

If CTRL3 pin is configuration as HOLD function and CTRL3 is low, but coil voltage measurement and STALL bit still can trigger HOLD_EN bit automatically enable.

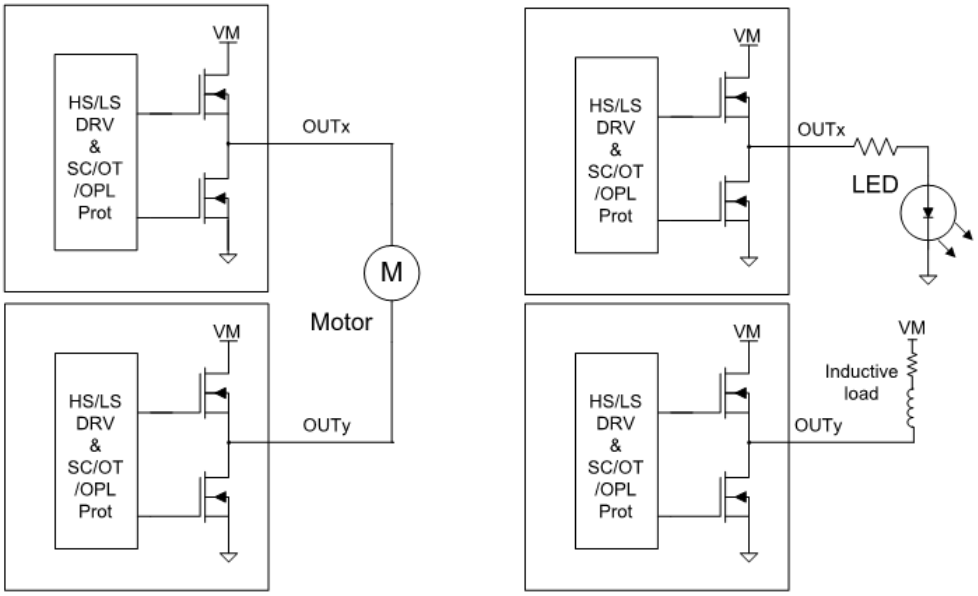
6.9. Independent half bridge mode

When CONFIG_7 register HB_MODE bit is set, the device is latched into independent half bridge mode. This mode allows four half bridge drivers, OUTA1/OUTA2 & OUTB1/OUTB2, can be directly control for independent loads, such as general used inductive/resistive load, BDC motor, LED etc.

The CTRL1/2/3/4 & OUTA1/OUTA2/OUTB1/OUTB2 relationship is defined as section CTRL1/2/3/4 function description. And the truth table for independent half bridge mode is shown as below table.

In independent half bridge mode, over current protection are still available, but internal current regulation is disabled.

CONFIG_7 register HB_MODE bit shall be cleared to exit independent half bridge control.



EN pin	DRV_EN bit	OUTxx_HIZ bit	CTRLx pin	OUTx	Description
0	x	x	X	HIZ	Sleep, half bridge output HIZ
1	0	x	X	HIZ	Half bridge output not enable, HIZ
1	0	1	x	HIZ	Half bridge output not enable, HIZ
1	1	0	0	LOW	Output low side on, high side off
1	1	0	1	HIGH	Output low side off, high side on

6.10. output stage, OUTA1/OUTA2, OUTB1/OUTB2

Each half bridge is built by an internally connected high side and a low-side power LDMOS. Due to the integrated body diodes of the HS/LS output stage, inductive loads can be directly driven without external freewheeling diodes. To reduce the power dissipation during freewheeling condition, the internal PWM controller will switch-on the output low side as synchronous rectification.

The half bridges are cross-current protected by an internal delay timing depends on slew rate configuration (see CONFIG_4 register SR_SEL[1:0])

6.10.1. Output stage electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

Output stage electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output (OUTA1, OUTA2, OUTB1, OUTB2)						
$R_{DS(ON)}$	HS/LS FET on resistance	I = 0.5 A, Tj=25		0.6		Ω
		I = 0.5 A, Tj=150			1.2	Ω
Ileak_hs	HS OFF-state leakage	VOUT = 0V, EN=1	-100(TBD)	-60(TBD)	-	uA
		VOUT = 0V, EN=0	-100(TBD)	-60(TBD)	-	uA
Ileak_ls	LS OFF-state leakage	VOUT = 13.5V, EN=1	-	60(TBD)	100(TBD)	uA
		VOUT = 13.5V, EN=0	-	60(TBD)	100(TBD)	uA
t_{RISE}, t_{FALL},	Output rise time Output fall time High side or low side	VS = 13.5 V, resistive load 100 ohm, SR_SEL=00		10		V/µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=01		40		V/µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=10		70		V/µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=11		100		V/µs
t_{PD}	Propagation delay (high side / low side ON/OFF) (Independent half bridge)	VS = 13.5 V, resistive load 100 ohm, SR_SEL=00		(TBD)		µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=01		(TBD)		µs

		VS = 13.5 V, resistive load 100 ohm, SR_SEL=10		(TBD)		µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=11		(TBD)		µs
t_{CC}	Cross protection time, high to low / low to high	VS = 13.5 V, resistive load 100 ohm, SR_SEL=00		4.8		µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=01		1.8		µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=10		1.2		µs
		VS = 13.5 V, resistive load 100 ohm, SR_SEL=11		0.9		µs

6.11. Protection and diagnosis function

6.11.1. Overcurrent protection

The integrated overcurrent protection function provides the half bridge high side against short to ground or half bridge low side against short to battery.

When the current pass the half bridge high side (VS->highside->OUTx) or flow into the half bridge low side (OUTx->low side->GND), once I_{OC} overcurrent threshold is exceeded, an overcurrent deglitch filter t_{OC} starts and internal circuit limits current at I_{LIM}.

Upon the overcurrent condition last until t_{OC} expiration, if half bridge mode is enabled, the particular half bridge (including high side and low side) is disabled, on the contrary, under stepper mode all four half bridge outputs are disabled on the same time for OC. No matter stepper or independent half bridge, the OC status bit shall report the corresponding HS or LS which trigger OC, see STA_1 & STA_2 register description. DOUT2 pin also asserts high if FAULT (OR of fault/warning flag in GSB) is selected and mux.

For example, if only OUTA1 LS is short to battery and detected, STA_2 register OC_OUTA1_LS bit and STA_1 register OC bit is asserted while other independent OC status bits OC_OUTA1_HS or corresponding OUTA2/OUTB1/OUTB2 bits not affected, for output stage, only OUTA1 half bridge, HS and LS, are disabled in half bridge mode while all OUTA1/A2/B1/B2 are disabled in stepper mode.

Note:

1. Even the half bridge output is disabled due to overcurrent protection mechanism, the DRV_EN remains previous state, unless user change the value through SPI.
2. Charge pump remains active during overcurrent protection.
3. The output stage turn-off slew rate caused by OC protection is same as normal driving configuration.
4. When device operate in high voltage > 28v, short t_{OC} is automatically used, even TOC_SEL bit in CONFIG_8 register is set to select long filter in normal VSx operating range (5.5~18V).

Anyhow if overcurrent condition short than t_{OC} deglitch filter, the OC event is not confirmed, and HB / stepper driver keeps normal status.

The output stage is latched off, to resume normal driving, besides the overcurrent condition disappear, it is also required to clear the OC status bit in STA1 & STA2 register by SPI reading (RD_CLR_EN=1) or send READ&CLEAR command (SPI frame OP code '10') to trigger clear fault command.

6.11.2. Overcurrent protection electrical specifications

Valid for automotive version at T_j = -40 to 150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

Overcurrent protection electrical parameters

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Overcurrent protection						
I_{OC}	Over current threshold	Half bridge low side	1.9	2.3	2.75	A
		Half bridge high side	-2.75	-2.3	-1.9	A
t_{OC}	OC deglitch filter time	TOC_SEL=0, TFLT_TOC_EXT=0		0.2		us
		TOC_SEL=0, TFLT_TOC_EXT=1		0.4		
		TOC_SEL=1, TFLT_TOC_EXT=0		3.2		
		TOC_SEL=0, TFLT_TOC_EXT=1		6.4		

6.11.3. Open load in ON state

The load current is monitored in each activated output stage for open load detection in ON state.

Under stepper mode,

Starting from any PWM cycle, if the load current is NOT reach the current reference for at least t_{OL} for consecutive PWM cycles, the corresponding open load bit is set in status register (STA2, OPL_OUTA or OPL_OUTB bit, STA1 OPL bit).

The open load is only as information flag andstepper operation not impacted.

DOUT2 (FAULT output function if selected) is also asserted high once open load detected, as WARN bit in GSB contains open load.

Note:

1. For stepper application, the open load detection is not asserted in below condition
   a) Output driver disabled (DRV_EN not able, TSD, OCP, CPUV, VSUV, VSOV if VSOV_DIS=0).
   b) When the stepper motor position is 0°/ 180 °(stop open load detection only in OUTA side), 90°/ 270 °(stop open load detection only in OUTB side)
2. ON state open load detection filter timing t_{OL} can be programmable (OPL_FLT bit in CONFIG_4 register)
3. ON state open load detection can be disabled by OPL_DIS bit in CONFIG_8 register, in case ON state open load not required.

The OL status bits (STA2 & STA1 corresponding bits) are latched until SPI reading (RD_CLR_EN=1) or SPI READ&CLEAR fault command when open load condition is disappeared.

Table 1. open load electrical characteristics

T_j = -40~150°C, VSx = 5.5 to 18V, VDDIO = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ON state open load protection						
t_{OL}	Open load filter time	OPL_FLT=0	15	30	45	ms
		OPL_FLT=1	30	60	90	ms

6.11.4. Over temperature warning and shut down

To protect power stage from overheat, dedicated thermal sensor is placed close to each half bridge power stage, if the temperature increases above the OTwarn, a temperature warning flag (OTWARN) is set in SPI STA_1 register, stepper / half bridge output operation is not impacted. Once the sensed temperature over the second OT_{SD} threshold, the corresponding OTSD flag is set and power MOSFET channel is automatically disabled.

DOUT2 pin can be configured for OTwarn and OTSD event report, which asserted DOUT2 to high.

If FLT_LATCH = 1, in order to reactive the output stage after OTSD and release DOUT2 pin, the temperature drops below OTSD-T_{HYS_OTSD}, and the thermal shutdown OTSD bit is latched until SPI READ&CLEAR command or SPI reading (RD_CLR_EN=1). In a similar way, the OTwarn flag is latched until temperature drops below OTwarn-T_{HYS_OTwarn} and SPI READ&CLEAR command or SPI reading (RD_CLR_EN=1).

If FLT_LATCH = 0, when the temperature drops below OTSD-T_{HYS_OTSD}, the output stage is automatically recovery, while the thermal shutdown OTSD bit is latched until SPI READ&CLEAR command or SPI reading (RD_CLR_EN=1). For OTwarn flag, it is automatically cleared once temperature drops below OTwarn-T_{HYS_OTwarn}.

Table 2. Thermal protection electrical characteristics

T_j = -40~150°C, VSx = 5.5 to 18V, VDD = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Thermal protection						
OT_{WARN}	Thermal warning temperature *		135	150	165	°C
T_{HYS_OTW}	Thermal warning hysteresis			20		°C
OT_{SD}	Thermal shutdown temperature *		150	165	180	°C
T_{HYS_OTSD}	Thermal shutdown hysteresis			20		°C

* OT_{WARN}, OT_{SD} threshold is not overlap.

6.11.5. Under temperature warning

If the device internal temperature falls below the under temperature warning threshold, the UTWARN flag is set in SPI register CONFIG_7. No other action is performed, and device operation is NOT impacted. When the temperature rises and exceeds the UTwarn + T_{HYS_UTW}, the UTW flag is automatically cleared.

UTW flag is not reported on STA_1 register, neither on DOUT2 pin.

T_j = -40~150°C, VSx = 5.5 to 18V, VDD = 3 to 5.5V, unless otherwise specified

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Under temperature protection						
OT_{WARN}	UT_{WARN} Under temperature warning temperature		135	150	165	°C
T_{HYS_OTW}	T_{HYS_UTW} Under temperature warning hysteresis			20		°C

6.11.6. Stall detection in stepper mode

As figure below shown, there is a clear relation between the coil current and stepper motor BEMF. When the motor load increases, the BEMF shifts and cause voltage difference when coil current equals 0. The NSD8381 takes advantage of this phenomenon. When the stepper motor position is 0°/ 180 °/ 90°/ 270 °, one coil current is typically programmed at zero amps, this makes it possible to measure the induced BEMF voltage through sampling the voltage across the motor terminal.

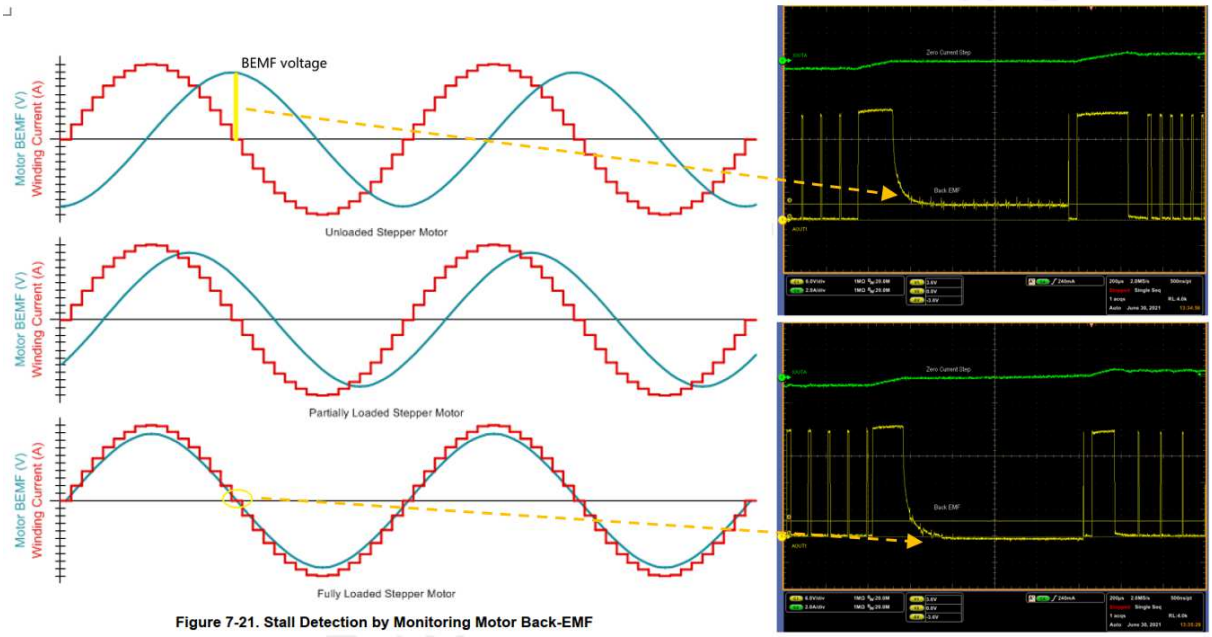
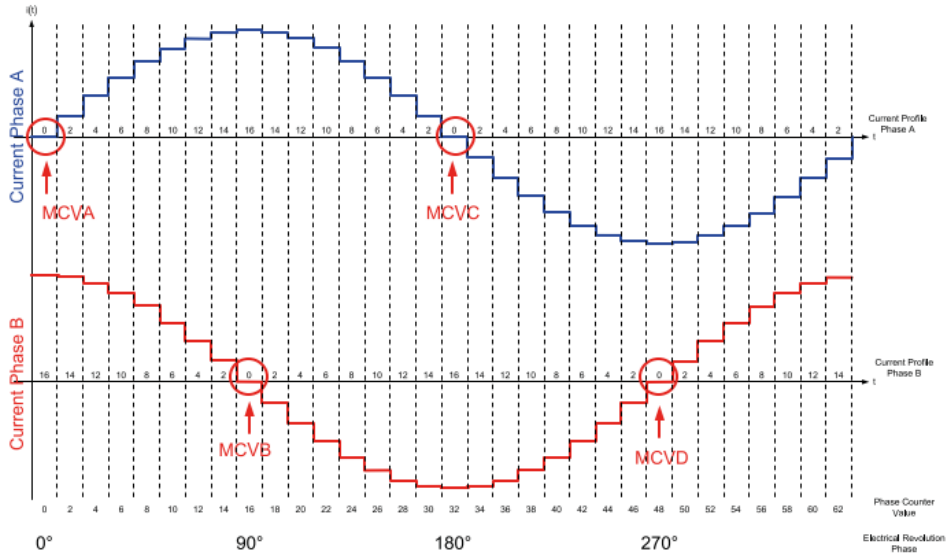


Figure 7-21. Stall Detection by Monitoring Motor Back-EMF

As soon as the zero current step (0°/ 180 °/ 90°/ 270 °) starts, the half bridge PWM driving signals are switched off. If coil voltage conversion is enabled by SPI CONFIG_5 register CV_EN bit, after the cross current protection timing, the opposite low side is additionally switched on to measure the motor terminal voltage difference refer to GND. The four corresponding digital values are stored into SPI register CVA, CVB, CVC, CVD, as table explained.

Step position	PHASE COUNTER APH[6:0]	PHASE COUNTER PH[5:0]	DIR=0		DIR=1		SPI store register
			Switch on low side	Sampling	Switch on low side	Sampling	
0°	0000000	000000	OUTA2	OUTA1	OUTA1	OUTA2	CVA
90°	0100000	010000	OUTB1	OUTB2	OUTB2	OUTB1	CVB

180°	1000000	100000	OUTA1	OUTA2	OUTA2	OUTA1	CVC
270°	1100000	110000	OUTB2	OUTB1	OUTB1	OUTB2	CVD

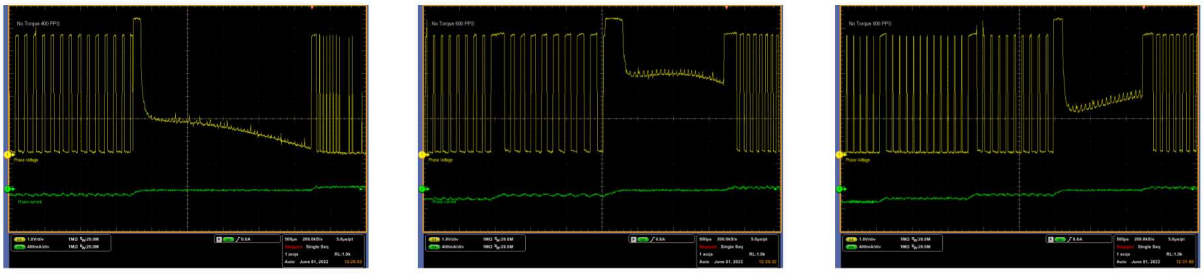


The full scale BEMF measurement is range from min 150mV to max 28v, and the converted BEMF is defined as below formula:

$$V_{BEMF} = \frac{10\text{bit register decimal value}}{1023} \times 28V$$

BEMF voltage measurement sample point

Motor related operating condition, like motor speed & load torque, has effect on BEMF voltage and timing. The key of right detecting the stall condition is to sample the BEMF at the proper point.



400 PPS 600 PPS 800 PPS

CONFIG_5 register CV_DELAY[4:0] bits allow user to adjust the BEMF sample point by the number of PWM periods after zero current step starts.

Default setting of CV_DELAY[4:0] is '00000', it is defined as sampling the BEMF at the end of zero current step. This is useful for detection at continuous movement in fast speeds. To detect the stall condition at low speed, the sample point shall be close to the beginning of zero current step, in hence, CV_DELAY[4:0] setting value shall be not too high.

In case the phase counter update command is given before the CV_DELAY[4:0] PWM periods expired, the zero current step is extended and next step movement is delayed, until coil voltage conversion ready.

BEMF voltage measurement averaging

The CV_AVG_SEL bit in CONFIG_8 register determines whether the average of 8~16 times conversion or the real time ADC data is updated to the corresponding CVx register.

BEMF voltage measurement indicator CV_RDY signal / CV_REG_IND[1:0] bits

CV_REG_IND[1:0] bits in CONFIG_5 register always report the last updated CVx register where the new conversion value stored.

Additionally, the device provides digital signal 'CV_RDY' output which indicates the coil voltage (BEMF) measurement is ready and available the respective CVx register. When the new conversion triggers, the CV_RDY signal goes from high to low, then it returns to high once the voltage measurement is updated.

BEMF voltage measurement comparison and stall detection

Three different thresholds can be configured by SPI registers.

CVUL (coil voltage / BEMF upper limit)

CVLLB (coil voltage / BEMF low limit B)

CVLLA (coil voltage / BEMF low limit A) -> recommend for the lowest threshold

Depending on the comparison result between coil voltage measurement value and the three thresholds, the device asserts and reports the corresponding flag bit.

CVULF bit is set if the coil conversion voltage is higher than CVUL threshold. It is automatically cleared when new value is lower.

CVLLBF bit is set if the coil conversion voltage is lower than CVLLB threshold. It is automatically cleared when new value exceeds CVLLB.

CVLLAF bit is set if the coil conversion voltage is lower than CVLLA threshold. It is automatically cleared when new value exceeds CVLLA.

If the conversion value is out of range [CVLLA; CVUL] for lasting over the number of consecutive conversions in zero current step, which equals the CV_STALL_NUM[2:0] bits value, then the STALL flag bit in STA_1 is set. For example, if the conversion value is quite low and below CVLLA threshold over the stall counter number, the device reports both CVLLAF and STALL flag, similar case for conversion value higher than CVUL, CVULF and STALL flag is set.

Both CVULF / CVLLBF / CVLLAF and STALL flag NOT impact device operating state.

Additionally, two digital signals related with BEMF measurement comparison, CVLL and CVOOR, can be mux on DOUT1 pin. CVOOR signals is set to high if conversion value out of range and fall to low once conversion value is within the two setting thresholds. CVLL signal is set if conversion value is below CVLLB threshold.

6.11.7. Fault table summary

FAULT EVENT	Condition	Configuration	ERR indicator	Output status	Charge pump	Digital logic	SPI Comm	Recovery action
VSx UV	VS < Vuv	FLT_LATCH=0	a.VS UV bit in STA1 b. DOUT2 if fault function is set	OFF	OFF	Normal	Normal	power stage output, charge pump and internal translator automatically recovery when VS>VUV rising edge. VSUV flag keeps latch until Read&clear or read command if RD_CLR_EN=1
		FLT_LATCH=1		OFF	OFF	Normal	Normal	VSUV flag keeps latch until Read&clear or read command if RD_CLR_EN=1. power stage output, charge pump and internal translator recovery when VS>VUV rising edge and VSUV flag clears by read&clear or read command if RD_CLR_EN=1
VSx POR	VS < Vuv_rst	NA	RSTB =1 in GSB byte of SDO frame	OFF	OFF	RESET	OFF	NA
VSx OV	VS > V_{OV_H}	OVP_DIS=0 & FLT_LATCH=0	a.VS OV in STA1 b. DOUT2 if fault function is set	OFF	OFF	Normal	Normal	power stage output and charge pump automatically recovery when VS < V_{OV_L}. VSOV flag keeps latch until Read&clear or read command if RD_CLR_EN=1
		OVP_DIS=0 & FLT_LATCH=1		OFF	OFF	Normal	Normal	VSOV flag keeps latch until Read&clear or read command if RD_CLR_EN=1. Power stage output and charge pump also keeps latch until VS < VOV_L and flags clear by read&clear or read command if RD_CLR_EN=1
		OVP_DIS=1, FLT_LATCH= x	NA (not report)	Normal	Normal	Normal	Normal	NA
VDDIO POR	VDDIO < V_{UV_VDDIO}	NA	RSTB =1 in GSB byte of SDO frame	OFF	OFF	RESET	OFF	NA
CP UV	VCP < VCP_UV	FLT_LATCH=0	a. CPUV bit in STA1 b. DOUT2 if fault function is set	OFF	Normal	Normal	Normal	output stage automatically recovery if VCP > VCP_UV with tcp_uv. CPUV flag keeps latch until Read&clear or read command if RD_CLR_EN=1
		FLT_LATCH=1		OFF	Normal	Normal	Normal	CPUV flag keep latch until Read&clear or read command if RD_CLR_EN=1, and also output stage remains latch until CPUV flag clear and VCP>VCP_UV with tcp_uv
OCP	IOUT > Iocp	NA	a. OC bit in STA1 b. OCP_OUTA1_HS or OCP_OUTA1_LS or OCP_OUTA2_HS or OCP_OUTA2_LS or OCP_OUTB1_HS or OCP_OUTB1_LS or OCP_OUTB2_HS or OCP_OUTB2_LS bits in STA2 b. DOUT2 if fault function is set	HIZ	Normal	Normal	Normal	OCP flags, all four output stages off are latched until Read&clear or read command if RD_CLR_EN=1

OPEN LOAD (ON MODE)[1]	Load open / not connected	NA	a. OPL bit in STA1 b. OPL_OUTA or OPL_OUTB bits in STA2 b. DOUT2 if fault function is set	Normal	Normal	Normal	Normal	NA
STALL[1]	Motor stuck	NA	a. STALL bit in STA1 b. CVLLA or CVUL bits in STA2 b. DOUT2 if nfault function is set	Normal	Normal	Normal	Normal	Read&clear doesn't clear STALL bit. STALL bit depends on coil voltage conversion vs. CVUL / CVLLA threshold with CV_STALL_NUM bits
OTSD	Tj > OTSD	FLT_LATCH=0	a. OTSD bit in STA1 b. DOUT2 if fault function is set	OFF	OFF	Normal	Normal	Automatically recovery of output and charge pump after Tj < OT_{SD} - T_{HYS_OTSD}. OTSD flag keep latch until Read&clear or read command if RD_CLR_EN=1
		FLT_LATCH=1		OFF	OFF	Normal	Normal	OTSD flag, output stage off and charge pump off are latched until Read&clear or read command if RD_CLR_EN=1
OTWARN	Tj > Twarn	FLT_LATCH=0	a. OTWARN bit in STA1 b. DOUT2 if fault function is set	Normal	Normal	Normal	Normal	Automatically clear of OTWARN bit when Tj < OTwarn - T_{HYS_OTW}
		FLT_LATCH=1		Normal	Normal	Normal	Normal	OTWARN flag are latched until Read&clear or read command if RD_CLR_EN=1 when Tj < OTwarn - T_{HYS_OTW}
UTWARN	Tj < UTW	NA	a. UTWARN bit in CONFIG_REG7	Normal	Normal	Normal	Normal	Automatically clear of UTWARN bit Tj > UTwarn + T_{HYS_UTW}

Note:

1. OPEN LOAD and stall detection are NOT available in half bridge mode (OPL_OUTA, OPL_OUTB in half bridge mode).

6.12. SPI interface

The following table summarizes the SPI interface designed.

SPI Interface quick look

Parameter	Description
Protocol	in frame
Single Frame Length	24 bit, MSB first
Frame protection	frame length & odd parity check
Max. Frequency	4 MHz
CPOL	0
CPHA	0
Master/Slave configuration	Slave

The falling edge of NCS defines the start of the SPI frames. It samples the SDI line at the rising edge of SCK, while the output data is shifted out on SDO line at the falling edge of SCK (CPOL='0' CPHA = '0'). The end of SPI frame is defined by a rising edge of NCS.

6.12.1. SPI Frame structure

Each SDI input frame has 24 bits with the following structure:

- 2 operation command bit C1 / C0

  '00' for write operation, '01' for read operation, '10' for read & clear operation
- 6 ADDRESS bits
- 16 DATA bits

	MSB								LSB
BIT	23	22	21	20	19	18	17	16	[15:0]
SDI	C1	C0	A[5]	A[4]	A[3]	A[2]	A[1]	A[0]	DATA

Register frame SDO responses the selected address and register content bit values. It has with the following structure:

- 8bits GSB, represents global status / failure / warning
- 16 bits data, two bytes

	MSB							LSB
BIT	23	22	21	20	19	18	17	16	[15:0]
SDO	Global status byte								DATA

6.12.2. Global status byte definition

Every bit of global status byte in SDO frame

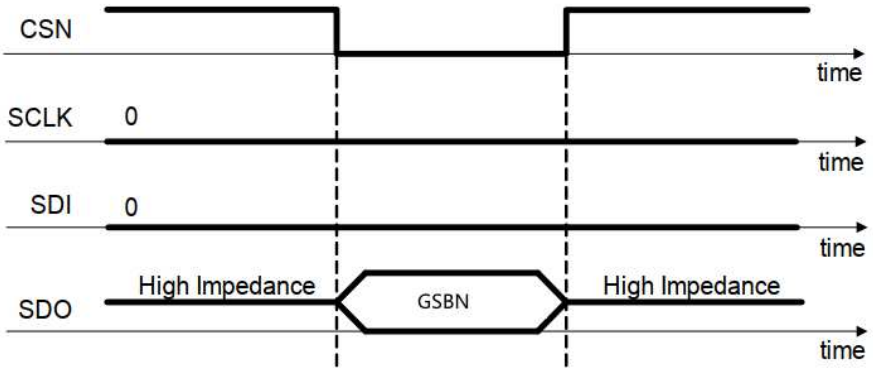
	Global status byte							
BIT	23	22	21	20	19	18	17	16
SDO	GSBN	RSTB	SPI_ERR	0	Function_ERR	DEVICE_ERR	WARN	0

Bit name	Description Function
GSBN	The GSBN bit is a logical NOR combination of SDO Global status byte bit 17 to bit 23. GSBN = 1 (No Error) GSBN = 0 (Error)
RSTB	The RSTB bit is set to 1 after any POR (VS POR or VDDIO POR), it is reset after first valid SPI frame
SPI_ERR	The SPI_ERR is a logical OR combination of SPI communication related error: frame length, ODD parity, SDI stuck, CPOL check.
FUNCTION_ERR	The FUNCTION_ERR is a logical OR combination of application specific function flags: • Overcurrent status bit (OC) • Stall detection (STALL)
DEVICE ERR	The DEVICE_ERR is a logical OR combination of device specific block flags: • Overvoltage status bit (VSOV) • Undervoltage status bit (VSUV) • Charge pump status bit (CPUV) • Overtemperature shutdown bit (OTSD)
WARN	The WARN is a logical OR combination of warning flags: • Thermal warning (TW) • Open Load (OL)

6.12.3. GSBN flag

A logic OR combination between GSBN and the signal present on SDI is reported on SDO between a CSN falling edge and the first SCLK rising edge. GSBN is set if a fault condition is detected or if the device comes from a Power On Reset (POR).

It is possible to check if the device has detected a fault by reading the GSBN without SPI clock pulse.



6.12.4. Parallel and multi-devices communication

SPI communication between microcontroller (SPI master) and multiple these devices (slave) can be operated only in parallel.

Parallel operation: several slave devices are connected to one SPI channel, which share communication lines SDI, SDO and SCK, but every slave connects dedicated own NCS.

Daisy chain operation: multi devices shared one NCS and SCK and each device SDI and SDO daisy-chain connected are NOT supported.

6.12.5. Frame Length Check

For each command received, the SPI peripheral checks the number of clock edges at SCK pin. If the total number of edges is not 16 plus a multiple of 8, which means 24, 32, 40…, the frame content is discarded and an SPI_ERR bit will be returned upon next iteration.

6.12.6. ODD parity check

An ODD parity is used in NSD8381 for SPI data consistency check. The ODD parity bit is allocated in bit0, LSB, and the value is calculated based on the number of '1' from bit 23 to bit 1. If the count number is even, the LSB odd parity bit value shall be inserted using '1', otherwise, '0' shall be used.

6.12.7. CSN timeout

An internal timer is started when CSN pin is tied down from high to low, the SPI frame shall be within the timer window, as the SDO is internally set to tristate (HIZ) after the timer ends. It avoids one device abnormal occupancy on SDO, in case CSN is stuck at low of multi devices communication on the same SPI bus.

6.12.8. SDI stuck

When the 24-bit values of one SPI command are all '0', it is considered as SDI stuck at low, all '0' SPI frame is discarded and an SPI_ERR will be returned on next iteration. The mechanism means a SPI write command to register address '000000' with all data bit in '0' is rejected.

In the similar way, for SDI stuck at high, the frame with 24-bit all '1' is also rejected and SPI_ERR flag is set.

6.12.9. SDO stuck

The GSBN bit is logic NOR of other bits in GSB. It means the normal SDO frame always contains both '0' and '1', otherwise, SDO returns all '1' can be recognized as SDO stuck at high and all '0' means SDO stuck at low. This fault detection can be handled by microcontroller.

6.12.10. CPOL check

Providing the first SCK edge is falling after CSN low or last SCK edge is rising before CSN goes high, the NSD8381 detects the input SPI frame CPOL abnormal, ignores the wrong SPI frame and reports SPI_ERR on next SDO frame.

6.12.11. CPHA check (TBD)

An internal CPHA test register (TBD) is implemented. If the register read return 16-bit data is 0x55, the SPI CPHA meets the NSD8381 requirement, while read return 16-bit data is 0xAA, the SPI CPHA setting shall be changed.

6.12.12. SPI error flag

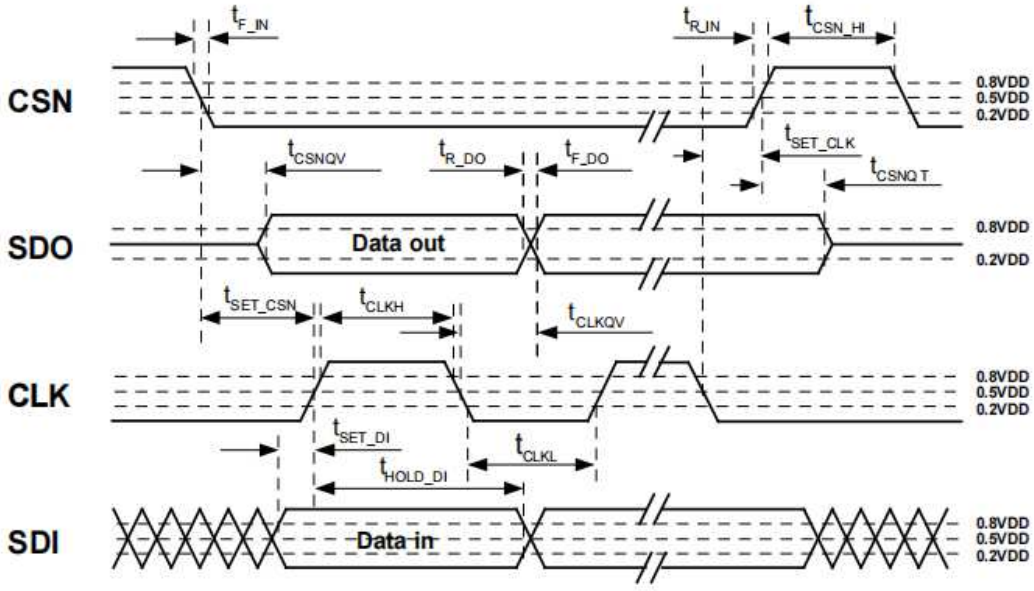
As the above SPI protection described, the SPI_ERR diagnosis bit in GSB will be returned upon next communication iteration for the following error occurs:

- Frame Length error
- ODD parity
- SDI stuck
- CPOL check

6.12.13. SPI Physical Layer

It implements an SPI Slave with the following timing requirements:

Figure 3 – SPI Timing Diagram



SPI AC Characteristics

Symbol	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	Type
T_{CLKL}	Minimum time CLK = LOW	Application info	100			ns	
T_{CLKH}	Minimum time CLK = HIGH	Application info	100			ns	

T_{CSNQV}	CSN falling until SDO valid	Cload=50pF			100	ns	
T_{SET_CSN}	CSN setup timing before CLK rising	Application info	100			ns	
T_{CLKQV}	CLK falling until SDO valid	Cload=50pF			60	ns	
T_{SET_DI}	SDI input setup time (CLK change low to high after SDI data valid)	Application info	25			ns	
T_{HOLD_DI}	SDI input hold time (SDI data hold after CLK change high to low)	Application info	25			ns	
T_{SET_CLK}	CLK low timing before CSN rising		100			ns	
T_{CSNQT}	CSN high timing to SDO tri-state	Cload=50pF			100	ns	
T_{F_IN}	CLK, CSN, SDI falling timing	Application info			25	ns	
T_{R_IN}	CLK, CSN, SDI rising timing	Application info			25	ns	
T_{F_DO}	SDO falling timing	Cload=50pF			25	ns	
T_{R_DO}	SDO rising timing	Cload=50pF			25	us	
T_{CSN_HI}	CSN high timing between two SPI frame		6			us	
T_{CSN_TO}	CSN low time out		20	35	50	ms	
F_{CLK_SPI}	CLK frequency (50% duty cycle)	Application info			4	MHz	

6.12.14. Registers map

SECT	REG_NAME	REG_ADDR	Bits															
			D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Status register	STA_1	0x01	VSOV	VSUV	Reserved	Reserved	Reserved	CPUV	Reserved	Reserved	Reserved	OTWARN	OTSD	OPL	OC	STALL	Reserved	Parity
	STA_2	0x02	OC_OUTA1_HS	OC_OUTA1_LS	OC_OUTA2_HS	OC_OUTA2_LS	OC_OUTB1_HS	OC_OUTB1_LS	OC_OUTB2_HS	OC_OUTB2_LS	OPL_OUTA	OPL_OUTB	Reserved	Reserved	CVULF	CVLLAF	CVLLBF	Parity
Control register	CONFIG_1	0x03	CP_SS	PWM_SS	Reserved	AOUT_SEL[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	CTRL1_SEL	Reserved	CTRL2_SEL	CTRL3_SEL[1:0]		Parity
	CONFIG_2	0x04	Reserved	Reserved	Reserved	Reserved	DOUT1_SEL[1:0]		Reserved	DOUT2_SEL[1:0]		Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Parity
	CONFIG_3	0x05	DRV_EN	HOLD_EN	ASM[2:0]			SM[2:0]			DIR	PH[5:0]						Parity
	CONFIG_4	0x06	PWM_FREQ_SEL[1:0]		TFILT_TOC_EXT	TBLANK_EXT	TFILT_SEL[1:0]		SR_SEL[1:0]		DECAY_SEL[1:0]		Reserved	Reserved	OPL_FILT	DECAY_SEL_HOLD	Reserved	Parity
	CONFIG_5	0x07	CV_EN	Reserved	CV_DELAY[4:0]				CV_STALL_NUM[2:0]				CV_REG_IND[1:0]		STALL_HOLD_EN	Reserved	Reserved	Parity
	CONFIG_6	0x08	IFSH[3:0]				Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	IFSR[3:0]				Parity
	CVA	0x09	Reserved	Reserved	Reserved	Reserved	Reserved	CVA[9:0]										Parity
	CVB	0x0A	Reserved	Reserved	Reserved	Reserved	Reserved	CVB[9:0]										Parity
	CVC	0x0B	Reserved	Reserved	Reserved	Reserved	Reserved	CVC[9:0]										Parity
	CVD	0x0C	Reserved	Reserved	Reserved	Reserved	Reserved	CVD[9:0]										Parity
	CVLLB	0x0D	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLB[9:0]										Parity
	CVLLA	0x0E	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLA[9:0]										Parity
	CVUL	0x0F	Reserved	Reserved	Reserved	Reserved	Reserved	CVUL[9:0]										Parity
	CONFIG_7	0x10	OUTA1_HIZ	OUTA2_HIZ	OUTB1_HIZ	OUTB2_HIZ	Version[1:0]		Device_ID	UTWARN	APH[6:0]							Parity
	CONFIG_8	0x11	CP_SS_CONFIG	HOLDM_CONFIG	TOC_SEL	OPL_ON_DIS	CV_AVG_SEL	TCC_INC	TCC_RED	TBLANK_RED	1/32 STEP_EN	DIS_SLOPE_BLANK	FULL_STEP_IFS	RD_CLR_EN	HB_MODE	FLT_LATCH	OVP_DIS	Parity
	CONFIG_9	0x12	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Unlock	Parity

6.12.15. SPI – status and control registers

Table 7.6.1 STA_1 status register (REG_ADDR = 0x01)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	VSOV	VSUV	Reserved	Reserved	Reserved	CPUV	Reserved	Reserved
Operation Type	RLR	RLR	RO	RO	RO	RLR	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	OTWARN	OTSD	OPL	OC	STALL	Reserved	Parity
Operation Type	RO	RLR	RLR	RLR	RLR	RLR	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 STA_1 status register description

Bit	Field Name	Description
15	VSOV	0: No VS overvoltage detected (default value) 1: VS overvoltage detected. Error flag latched,
14	VSUV	0: No VS undervoltage detected (default value) 1: VS undervoltage detected. Error flag latched,
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CPUV	0: No charge pump undervoltage detected (default value) 1: Charge pump undervoltage detected. Error flag latched,
9	Reserved	0: reversed (default value).
8	Reserved	0: reversed (default value).
7	Reserved	0: reversed (default value).
6	OTWARN	0: No over temperature warning (default value) 1: over temperature warning detected. Error flag latched,
5	OTSD	0: No over tempearture shut down (default value) 1: Over temperature shut down detected. Error flag latched,
4	OPL	0: No open load in OUTA / OUTB detected (default value) 1: Open load detected. Error flag latched,
3	OC	0: No overcurrent in OUTA / OUTB high/low side detected (default value) 1: overcurrent detected in OUTA/OUTB. Error flag latched,
2	STALL	0: No stall detected in HB2 low side detected (default value) 1: Stall detected. Error latched,
1	Reserved	0: reversed (default value).
0	Parity	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 7.6.1 STA_2 status register (REG_ADDR = 0x02)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	OC_OUTA1_HS	OC_OUTA1_LS	OC_OUTA2_HS	OC_OUTA2_LS	OC_OUTB1_HS	OC_OUTB1_LS	OC_OUTB2_HS	OC_OUTB2_LS
Operation Type	RLR	RLR	RLR	RLR	RLR	RLR	RLR	RLR
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	OPL_OUTA	OPL_OUTB	Reserved	Reserved	CVULF	CVLLAF	CVLLBF	Parity

Operation Type	RLR	RLR	RO	RO	RLR	RLR	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 STA_2 status register description

Bit	Field Name	Description
15	OC_OUTA1_HS	0: No overcurrent in OUTA1 high side detected (default value) 1: Overcurrent detected in OUTA1 high side. Error flag latched,
14	OC_OUTA1_LS	0: No overcurrent in OUTA1 low side detected (default value) 1: Overcurrent detected in OUTA1 low side. Error flag latched,
13	OC_OUTA2_HS	0: No overcurrent in OUTA2 high side detected (default value) 1: Overcurrent detected in OUTA2 high side. Error flag latched,
12	OC_OUTA2_LS	0: No overcurrent in OUTA2 low side detected (default value) 1: Overcurrent detected in OUTA2 low side. Error flag latched,
11	OC_OUTB1_HS	0: No overcurrent in OUTB1 high side detected (default value) 1: Overcurrent detected in OUTB1 high side. Error flag latched,
10	OC_OUTB1_LS	0: No overcurrent in OUTB1 low side detected (default value) 1: Overcurrent detected in OUTB1 low side. Error flag latched,
9	OC_OUTB2_HS	0: No overcurrent in OUTB2 high side detected (default value) 1: Overcurrent detected in OUTB2 high side. Error flag latched,
8	OC_OUTB2_LS	0: No overcurrent in OUTB2 low side detected (default value) 1: Overcurrent detected in OUTB2 low side. Error flag latched,
7	OPL_OUTA	0: No open load in OUTA detected (default value) 1: Open load in OUTA detected. Error flag latched,
6	OPL_OUTB	0: No open load in OUTB detected (default value) 1: Open load in OUTB detected. Error flag latched,
5	Reserved	0: reversed (default value).
4	Reserved	0: reversed (default value).
3	CVULF	0: No conversion voltage CVA / CVB / CVC / CVD over CVUL upper limit detected (default value) 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, over CVUL upper limit detected.
2	CVLLAF	0: No conversion voltage CVA / CVB / CVC / CVD under CVLLA low limit A detected (default value) 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, under CVLLA low limit A detected.
1	CVLLBF	0: No conversion voltage CVA / CVB / CVC / CVD under CVLLB low limit B detected (default value) 1: Conversion voltage CVA or CVB or CVC or CVD, one or multiple, under CVLLB low limit detected.
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 7.6.1 CONFIG_1 control register (REG_ADDR = 0x03)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	CP_SS	PWM_SS	Reserved	AOUT_SEL[1:0]		Reserved	Reserved	Reserved
Operation Type	RW	RW	RO	RW	RW	RW	RO	RO
Default	0	0	0	0	0	1	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	Reserved	CTRL1_SEL	Reserved	CTRL2_SEL	CTRL3_SEL[1:0]		Parity
Operation Type	RO	RO	RW	RO	RW	RW	RW	-
Default	0	0	1	0	1	0	0	-

Table 7.6.2 CONFIG_1 register description

Bit	Field Name	Description
15	CP_SS	0: fix charge pump frequency (default value) 1: enable charge pump spread spectrum function
14	PWM_SS	0: fix current regulation PWM frequency (default value) 1: enable current regulation PWM spread spectrum function

13	Reserved	0: reversed (default value).
12 11	AOUT_SEL[1:0]	00: disabled (default value) 01: voltage proportional to junction temperature 10: bandgap voltage 11: Disable in normal mode or Internal voltage/reference mux in test mode
10	Reserved	1: reversed (default value).
9	Reserved	0: reversed (default value).
8	Reserved	0: reversed (default value).
7	Reserved	0: reversed (default value).
6	Reserved	0: reversed (default value).
5	CTRL1_SEL	0: No function selected on CTRL1 pin, stepper mode phase counter PH[5:0] or APH[6:0] updated only by SPI 1: CTRL1 as stepper mode STEP input control signal, a rising edge on CTRL1 pin cause phase counter updated, while PH[5:0] bits can only be read (default value)
4	Reserved	0: reversed (default value).
3	CTRL2_SEL	0: No function selected on CTRL2 pin, stepper mode DIR signal updated by SPI CONFIG_3 register DIR bit 1: CTRL2 as stepper mode DIR input control signal, CTRL2 pin status LOW, DIR bit '0', phase counter increment, while CTRL2 pin status HIGH, DIR bit '1', phase counter decrement (default value)
2 1	CTRL3_SEL[1:0]	00: No function selected on CTRL3 pin, stepper mode HOLD or SMODE selection are achieved by CONFIG3 HOLD bit and SM[2:0] bits (default value) 01: CTRL3 as stepper mode SMODE (ASM[2:0] / SM[2:0]) select pin 10: CTRL3 as stepper mode HOLD select pin 11: No function selected on CTRL3 pin, stepper mode HOLD or SMODE selection are achieved by CONFIG3 HOLD bit and SM[2:0] bits
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 7.6.1 CONFIG_2 control register (REG_ADDR = 0x04)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	DOUT1_SEL[1:0]		Reserved	DOUT2_SEL1
Operation Type	RO	RO	RO	RO	RW	RW	RO	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	DOUT2_SEL0	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Parity
Operation Type	RW	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_2 register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).

11	DOUT1_SEL1	00: No function available on DOUT1 pin, tristate 01: Coil voltage conversion ready signal (CVRDY) output 10: Coil voltage conversion under low limit (CVLL) output 11: Coil voltage conversion out of range (CVOOR) output / replace CVRUN name
10	DOUT1_SEL0	
9	Reserved	0: reversed (default value).
8	DOUT2_SEL1	00: No function available on DOUT2 pin, tristate 01: Internal current regulation PWM signal output 10: Fault output 11: Fault check indicator
7	DOUT2_SEL0	
6	Reserved	0: reversed (default value).
5	Reserved	0: reversed (default value).
4	Reserved	0: reversed (default value).
3	Reserved	0: reversed (default value).
2	Reserved	0: reversed (default value).
1	Reserved	0: reversed (default value).
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 7.6.1 CONFIG_3 control register (REG_ADDR = 0x05)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	DRV_EN	HOLD_EN	ASM[2:0]			SM[2:0]		
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	DIR	PH[5:0]						Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_3 register description

Bit	Field Name	Description
15	DRV_EN	0: Output stage disable, HIZ state (default value) 1: Enable output OUTA, OUTB stage
14	HOLD_EN	0: HOLD mode disabled (default value) 1: HOLD mode enable If CTRL3_SEL[1:0] = 2b'10' & stepper mode, the bit is read only and reflects CTRL3 pin status, HOLD_EN bit is set to '0' when CTRL3 pin is low , on the contray, HOLD_EN bit is asserted to '1' while CTRL3 pin is high.
13	ASM[2:0]	Alternative step mode, used only when CTRL3_SEL bits = 2b'01' && CTRL3 = HIGH && HB_MODE=0 000,101, 110, 111: 1/16th microstep 001: 1/8 th microstep 010: ministep 011: half step 100: full step
12		
11		
10	SM[2:0]	default step mode, used in stepper mode CTRL3_SEL bits = 2b'01' && CTRL3 = LOW && HB_MODE=0 or CTRL3_SEL bits != 2b'01' && HB_MODE=0 000,101, 110, 111: 1/16th microstep 001: 1/8 th microstep 010: ministep
9		
8		

		011: half step 100: full step
7	DIR	0: No open load in OUTA detected (default value) 1: Open load in OUTA detected. Error flag latched,
6 5 4 3 2 1	PH[5:0]	Phase counter values in stepper mode, it determine the current profile applied on OUTA / OUTB and reports the step position. If CTRL1_SEL is '0', the phase counter bits PH[5:0] can be read and write with fully SPI step position control, no matter CTRL1 /CTRL2 pin status and DIR bit. While CTRL1_SEL is '1', the phase counter bits PH[5:0] is read only, CTRL1 pin rise edge cause phase counter updated according to DIR bit status, after new PWM period begins.
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

Table 7.6.1 CONFIG_4 control register (REG_ADDR = 0x06)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	PWM_FREQ_SEL[1:0]		TFILT_TOC_EXT	TBLANK_EXT	TFILT_SEL[1:0]		SR_SEL[1:0]	
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	1	1	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	DECAY_SEL[1:0]		Reserved	Reserved	OPL_FILT	DECAY_SEL_HOLD	Reserved	Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_4 register description

Bit	Field Name	Description
15 14	PWM_FREQ_SEL[1:0]	Current regulation PWM 00: 20khz 01: 30khz 10: 40khz 11: 40khz
13	TFILT_TOC_EXT	Current regulation tfilter and overcurrent toc filter timing extended selection 0: no extended timing on tfilter and toc 1: two system clock cycles (system clock 1/10MHZ, 100ns, two clock cycle 200ns)
12	TBLANK_EXT	Current regulation tblank timing extended selection 0: no extended on tblank timing 1: extend tblank to 4us independently from SR_SEL[1:0] settings
11 10	TFILT_SEL[1:0]	Current regulation tfilter selection 00: 0.5us 01: 1us 10: 2us 11: 3us
9 8	SR_SEL[1:0]	OUTA, OUTB slew rate selection 00: 10v/us

		01: 40v/us 10: 70v/us 11: 100v/us
7	DECAY_SEL[1:0]	Decay mode selection 00: auto decay mode 1 01: slow decay always 10: mixed decay 11: auto decay mode 2
6		
5	Reserved	0: reversed (default value).
4	Reserved	0: reversed (default value).
3	OPL_FILT	Open load detection filter timing 0: 30ms 1: 60ms
2	DECAY_SEL_HOLD	Decay mode selection during HOLD mode 0: slow decay used in HOLD mode 1: mix decay used in HOLD mode
1	Reserved	0: reversed (default value).
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CONFIG_5 control register (REG_ADDR = 0x07)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	CV_EN	Reserved	CV_DELAY[4:0]					CV_STALL_NUM BIT2
Operation Type	RW	RO	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CV_STALL_NUM BIT1	CV_STALL_NUM BIT0	CV_REG_IND[1:0]		STALL_HOLD_EN	Reserved	Reserved	Parity
Operation Type	RW	RW	RO	RO	RW	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_5 register description

Bit	Field Name	Description
15	CV_EN	Coil voltage conversion enable 0: Coil voltage conversion not start 1: Coil voltage starts according to trigger sequence
14	Reserved	0: reversed (default value).
13	CV_DELAY[4:0]	Coil voltage conversion delay timing configuration For the value from 1 to max 31, it sets the number of PWM periods between the beginning of zero current step and coil voltage conversion starts. If the value is 0, it sample the coil voltage at the end of zero current step
12		
11		
10		
9		
8	CV_STALL_NUM[2:0]	Coil voltage conversion number configuration for stall detection It sets the required number of coil voltage consecutive conversion which out of range [CVLLA, CVUL], CVOOR until stall detection asserted. The minimum value is 1, even CV_STALL_NUM[2:0] is configured to 0.
7		
6		
5	CV_REG_IND[1:0]	Last coil voltage conversion store register 00: CVA 01: CVB 10: CVC
4		

		11: CVD
3	STALL_HOLD_EN	Automatic hold mode enable configuration during stall event detected 0: Not automatically enter HOLD mode when stall event detected 1: Automatically enter HOLD mode when CONFIG_3 HOLD_EN bit =1 and stall event detected
2	Reserved	0: reversed (default value).
1	Reserved	0: reversed (default value).
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CONFIG_6 control register (REG_ADDR = 0x08)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	IFSH[3:0]				Reserved	Reserved	Reserved	Reserved
Operation Type	RW	RW	RW	RW	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	Reserved	Reserved	IFSR[3:0]				Parity
Operation Type	RO	RO	RO	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_6 register description

Bit	Field Name	Description
15	IFSH[3:0]	Full scale current setting in HOLD mode 1111: typ 326mA 1110: typ 292mA 1101: typ 264mA 1100: typ 230mA 1011: typ 202mA 1010: typ 168mA 1001: typ 140mA 1000: typ 118mA 0111: typ 101mA 0110: typ 95mA 0101: typ 84mA 0100: typ 79mA 0011: typ 73mA 0010: typ 62mA 0001: typ 50mA 0000: typ 28mA
14		
13		
12		
11	Reserved	0: reversed (default value).
10	Reserved	0: reversed (default value).
9	Reserved	0: reversed (default value).
8	Reserved	0: reversed (default value).
7	Reserved	0: reversed (default value).
6	Reserved	0: reversed (default value).
5	Reserved	0: reversed (default value).
4	IFSR[3:0]	Full scale current setting in normal running mode 1111: typ 1353mA 1110: typ 1160mA 1101: typ 1051mA 1100: typ 920mA 1011: typ 812mA
3		
2		
1		

		1010: typ 679mA 1001: typ 571mA 1000; typ 465mA 0111: typ 396mA 0110: typ 375mA 0101: typ 329mA 0100: typ 323mA 0011: typ 302mA 0010: typ 220mA 0001: typ 198mA 0000: typ 176mA
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVA register (REG_ADDR = 0x09)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVA[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVA[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CVA register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVA[9:0]	Coil voltage conversion digital value at phase counter 0°
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVB register (REG_ADDR = 0x0A)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVB[9:7]		

Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVB[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CVB register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVB[9:0]	Coil voltage conversion digital value at phase counter 90°
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVC register (REG_ADDR = 0x0B)

	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVC[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVC[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CVC register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVC[9:0]	Coil voltage conversion digital value at phase counter 180°

9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVD register (REG_ADDR = 0x0C)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVD[9:7]		
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVD[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CVD register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVD[9:0]	Coil voltage conversion digital value at phase counter 270°
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVLLB register (REG_ADDR = 0x0D)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLB[9:7]		

Operation Type	RO	RO	RO	RO	RO	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVLLB[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CVLLB register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVLLB[9:0]	Coil voltage low limit B threshold setting CVLLBF flag is asserted, if the last conversion voltage below CVLLB[9:0] setting. otherwise, CVLLBF flag is cleared
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVLLA register (REG_ADDR = 0x0E)

	D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVLLA[9:7]		
Operation Type	RO	RO	RO	RO	RO	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVLLA[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CVLLA register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVLLA[9:0]	Coil voltage low limit A threshold setting

9		CVLLAF flag is asserted, if the last conversion voltage below CVLLA[9:0] setting. otherwise, CVLLAF flag is cleared
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CVUL register (REG_ADDR = 0x0F)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	CVUL[9:7]		
Operation Type	RO	RO	RO	RO	RO	RW	RW	RW
Default	0	0	0	0	0	1	1	1
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	CVUL[6:0]							Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	1	1	1	1	1	1	1	-

Table 7.6.2 CVUL register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	CVUL9:0]	Coil voltage upper limit threshold setting CVULF flag is asserted, if the last conversion voltage over CVUL[9:0] setting. otherwise, CVULF flag is cleared
9		
8		
7		
6		
5		
4		
3		
2		
1		
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CONFIG_7 control register (REG_ADDR = 0x10)

	D15	D14	D13	D12	D11	D10	D9	D8

Field Name	OUTA1_HIZ	OUTA2_HIZ	OUTB1_HIZ	OUTB2_HIZ	Version[1:0]		Device_ID	UTWARN
Operation Type	RW	RW	RW	RW	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	APH[6:0]							Parity
Operation Type	RO	RO	RO	RO	RO	RO	RO	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_7 register description

Bit	Field Name	Description
15	OUTA1_HIZ	Only valid under half bridge mode （HB_EN=1) 0: half bridge OUTA1 enable 1: half bridge OUTA1 disable （HIZ)
14	OUTA2_HIZ	Only valid under half bridge mode （HB_EN=1) 0: half bridge OUTA2 enable 1: half bridge OUTA2 disable （HIZ)
13	OUTB1_HIZ	Only valid under half bridge mode （HB_EN=1) 0: half bridge OUTB1 enable 1: half bridge OUTB1 disable （HIZ)
12	OUTB2_HIZ	Only valid under half bridge mode （HB_EN=1) 0: half bridge OUTB2 enable 1: half bridge OUTB2 disable （HIZ)
11 10	Version[1:0]	00: version A 01: version B 10: version C 11: version D
9	Device_ID	0: NSD8381 stepper 1: NSD8304 4x half bridge
8	UTWARN	0: under temperature not happen 1: under temperature happens
7 6 5 4 3 2 1	APH[6:0]	Phase counter values only works in stepper mode 1/32 stepper mode. Similar as PH[5:0] bit, if CTRL1_SEL is '0', the phase counter bits APH[6:0] can be read and write with fully SPI step position control, no matter CTRL1 /CTRL2 pin status and DIR bit. While CTRL1_SEL is '1', the phase counter bits APH[6:0] is read only, CTRL1 pin rise edge cause phase counter updated according to DIR bit status, after new PWM period begins.
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CONFIG_8 control register (REG_ADDR = 0x11)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	CP_SS_CONFIG	HOLDM_CONFIG	TOC_SEL	OPL_ON_DIS	CV_AVG_SEL	TCC_INC	TCC_RED	TBLANK_RED
Operation Type	RW	RW	RW	RW	RW	RW	RW	RW
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**

Field Name	1/32 STEP_EN	DIS_SLOPE_ BLANK	FULL_STEP _IFS	RD_CLR_E N	HB_MOD E	FLT_LATCH	OVP_DIS	Parity
Operation Type	RW	RW	RW	RW	RW	RW	RW	-
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_8 register description

Bit	Field Name	Description
15	CP_SS_CONFIG	0: 16.5khz (default value). 1: 33khz
14	HOLDM_CONFIG	0: reversed (default value).
13	TOC_SEL	0: short OC filter, 0.2us if TFIT_OC_EX=0, 0.4us if TFIT_OC_EX=1 (default value). 1: long OC filter, 3.2us if TFIT_OC_EX=0, 6.4us if TFIT_OC_EX=1
12	OPL_ON_DIS	0: ON state OPL for stepper detection is available (default value). 1: ON state OPL function is disabled
11	CV_AVG_SEL	0: average of 8~16 times conversion (default value). 1: real time ADC data of BEMF voltage conversion
10	TCC_INC	0: Tcc, cross current protection timing no change (default value). 1: Tcc, cross current protection, dead time increase + tfilter
9	TCC_RED	0: Tcc, cross current protection timing no change (default value). 1: Tcc, cross current protection, dead time decrease down to 1/2 ratio
8	TBLANK_RED	Current regulation tblank timing reduction selection 0: no reduce on TBLANK 1: reduce tblank to 0.5us independently from SR_SEL[1:0] settings
7	1/32 STEP_EN	1/32 microstep mode enable 0: Not enable 1/32 microstep 1: Enable 1/32 microstep
6	DIS_SLOPE_BLA NK	Only works under mixed decay 0: slope&blank compenstation active under mixed decay (default value). 1: disable slope & blank in mixed decay
5	FULL_STEP_IFS	0: full step 100% full scale current (default value). 1: full step 71% full scale current
4	RD_CLR_EN	0: read to clear function not enable (default value). 1: spi read command to clear the STA_1, STA_2 flag bit
3	HB_MODE	Half bridge mode enable 0: default stepper mode 1: Enable independent 4x half bridge mode (OUTA1, OUTA2, OUTB1, OUTB2)
2	FLT_LATCH	FAULT latch configuration 0: auto recovery on VSUV, CPUV 1: fault latch on VSUV, CPUV
1	OVP_DIS	OVP protection disable configuation 0: overvoltage protection enable 1: overvoltage protection disable
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

CONFIG_9 register (REG_ADDR = 0x12)

	D15	D14	D13	D12	D11	D10	D9	D8
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
Operation Type	RO	RO	RO	RO	RO	RO	RO	RO
Default	0	0	0	0	0	0	0	0
	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
Field Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Unlock	Parity
Operation Type	RO	RO	RO	RO	RO	RO	RW	-

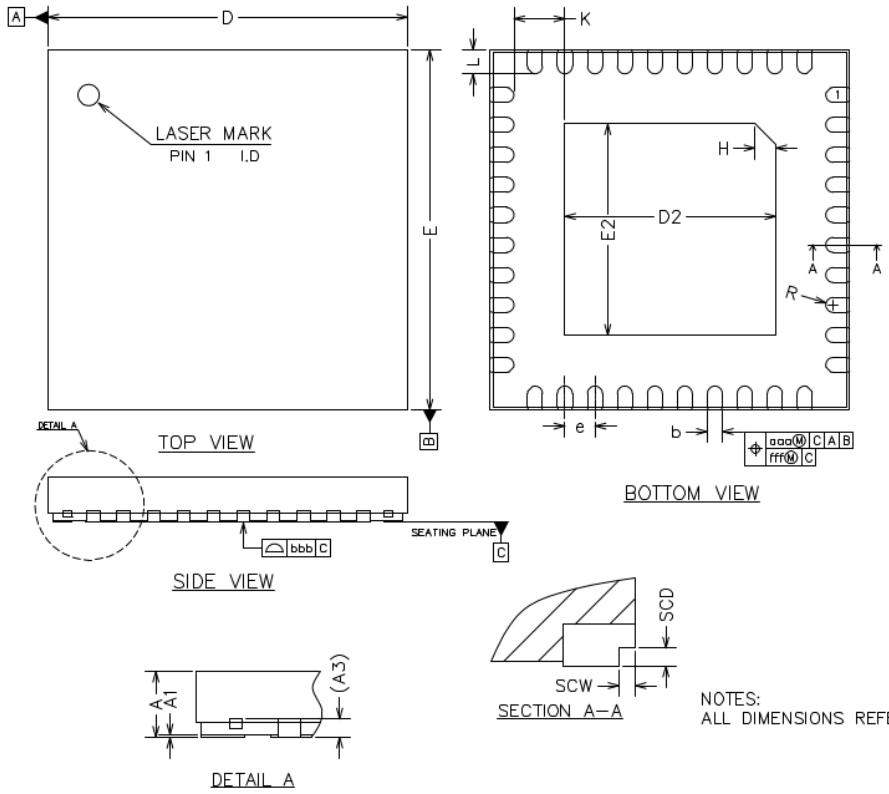
Default	0	0	0	0	0	0	0	-

Table 7.6.2 CONFIG_9 register description

Bit	Field Name	Description
15	Reserved	0: reversed (default value).
14	Reserved	0: reversed (default value).
13	Reserved	0: reversed (default value).
12	Reserved	0: reversed (default value).
11	Reserved	0: reversed (default value).
10	Reserved	0: reversed (default value).
9	Reserved	0: reversed (default value).
8	Reserved	0: reversed (default value).
7	Reserved	0: reversed (default value).
6	Reserved	0: reversed (default value).
5	Reserved	0: reversed (default value).
4	Reserved	0: reversed (default value).
3	Reserved	0: reversed (default value).
2	Reserved	0: reversed (default value).
1	Unlock	0: CONFIG_8 bit1~bit7 is lock (OVP_DIS, FLT_LATCH, HB_MODE, RD_CLR_EN, Full_Step_IFS, DIS_SLOPE_BLANK, 1/32 STEP_EN), write command ignore. 1: write 1 to unlock CONFIG_8 bit1~bit7 (OVP_DIS, FLT_LATCH, HB_MODE, RD_CLR_EN, Full_Step_IFS, DIS_SLOPE_BLANK,1/32 STEP_EN)bit
0	PARITY	bit 0 Parity bit, ODD parity check used of entire frame from bit 23~bit 1, except bit 0 parity bit. If the number of value '1' is odd, the value of last bit 0 shall be '0', otherwise, value '1' shall be inserted to complete the odd parity.

7. Package information

7.1. VQFN40 package information

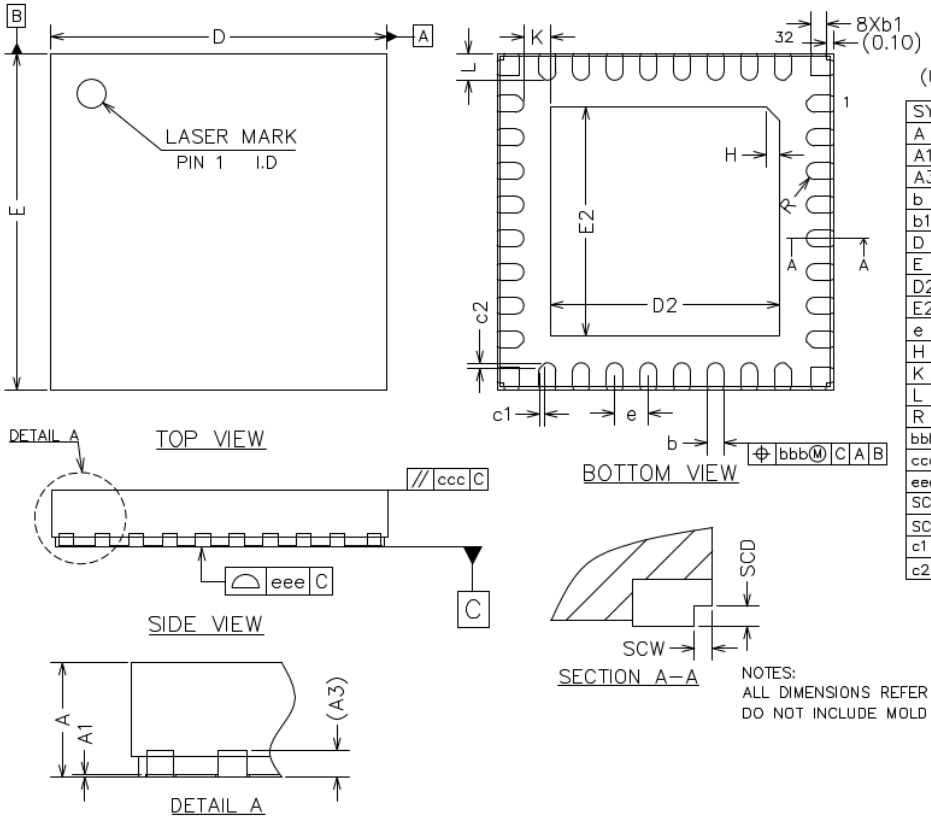


COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
D	5.90	6.00	6.10
E	5.90	6.00	6.10
D2	3.42	3.52	3.62
E2	3.42	3.52	3.62
e		0.50BSC	
H		0.35REF	
K	0.40	–	–
L	0.30	0.40	0.50
R	0.10	–	–
aaa		0.10	
bbb		0.08	
fff		0.05	
SCW	0.01	–	0.09
SCD	0.08	–	0.18

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDRAD MO–220 WJJD–5.

7.2. VQFN32 package information



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20REF	
b	0.20	0.25	0.30
b1	0.18	0.23	0.28
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.30	3.40	3.50
E2	3.30	3.40	3.50
e		0.50 BSC	
H		0.20 REF	
K	0.20	–	–
L	0.30	0.40	0.50
R	0.09	–	–
bbb		0.10	
ccc		0.10	
eee		0.08	
SCW	0.01	–	0.09
SCD	0.08	–	0.18
c1	–	0.08	–
c2	–	0.08	–

NOTES:
ALL DIMENSIONS REFER TO JEDEC STANDARD MO–220 VHHD–4
DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.

8. Ordering Information

Part Number	Automotive / Industrial	Package Type	MSL
NSD8381-Q1QAIR	Automotive	VQFN40	MSL3
NSD8381-Q1QANR	Automotive	VQFN32	MSL3

9. Revision History

Revision	Description	Date
0.1	Initial version	2023/4/5
0.2	Revise the description of CTRL1/2/3/4 pin function and fault table summary.	2023/6/25

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