Key Features

Processor

- Quad-core ARM Cortex™-A55
- Single-core E907 RISC-V MCU
- Embedded E902 RISC-V
- Up to 3 TOPS NPU

Memory

- 32-bit DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X interface with inline ECC, up to 8 GB
- SD3.0/eMMC5.1 interface
- 8-bit parallel NAND flash interface with maximum 80-bit/1KB BCH
- One octal SPI interface for flash devices

Video Engine

- Video decoding
  - MJPEG decoder, up to 3840x2160@15fps
  - JPEG Baseline decoder, up to 1080P@60fps
- Video encoding
  - H.264 BP/MP/HP, up to 3840x2160@25fps
  - MJPEG, up to 3840x2160@15fps
  - JPEG, up to 8192 x 8192 resolution
- Video decoder and video encoder are time-multiplexed

Video Input

- Parallel CSI
  - 8/10/12/16-bit
  - supporting BT.656 up to 4*720P@30fps and BT.1120 up to 4*1080P@30fps
- 4+4-lane/4+2+2-lane/2+2+2+2-lane MIPI CSI
  - Compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.2
  - Up to 2.0 Gbit/s per lane
  - Maximum video capture resolution of 8M@30fps (4-lane performance)

Video Output

- One dual-link LVDS interfaces, up to 1920 x 1080@60fps
- One RGB interfaces with DE/SYNC mode, up to 1920 x 1200@60fps (reduced blanking)
- 4-lane MIPI-DSI output interface up to 1920 x 1200@60fps (reduced blanking)

Audio

- 1 DAC
- 1 x audio output: LINEOUTP/N
- 4x I2S/PCM external interfaces
- Maximum 8 digital PDM microphones (DMIC)
- One OWA RX and one OWA TX, compliance with S/PDIF interface

Peripherals Interfaces

- 1 x USB2.0 Host, 1 x USB2.0 DRD, 1 x USB3.1 DRD&PCIe2.1 Combo
- 2 x GMAC (10/100/1000 Mbps port with RGMII and RMII interfaces)
- 5 x IR RX, 1 x IR TX, 9 x TWI, 6 x SPI, 17 x UART, 4 x CAN-FD, 1 x Local Bus
- 4-ch TPADC, 34-ch PWM, 21-ch GPADC, 1-ch LRADC
- SDIO 3.0, LEDC

Security Subsystem

- AES, DES, 3DES, and SM4 encryption and decryption algorithms
- MD5, SHA, and SM3 tamper proofing
- RSA, ECC, SM2 signature and verification algorithms

Device Summary

Orderable Device(s)	Package
T536MX-CEN3 T536MX-CEN2 T536MX-CEX T536MX-CXX	ED-FCCSP 533 balls Body size: 15 mm x 15 mm Maximum height: 1.056 mm Ball pitch: 0.5 mm Ball size: 0.3 mm

See Table 2-1 Ordering Information for details.

Revision History

Revision	Date	Author	Description
0.90	November 14, 2024	AWA1896	Initial Release Version

Content

Figures

Tables

About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the T536 family. For details about register descriptions of each module, see the *T536_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting https://open.allwinnertech.com/.

Revision Number Definition

Revision 0.90-0.9x

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

Test Item	Description
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

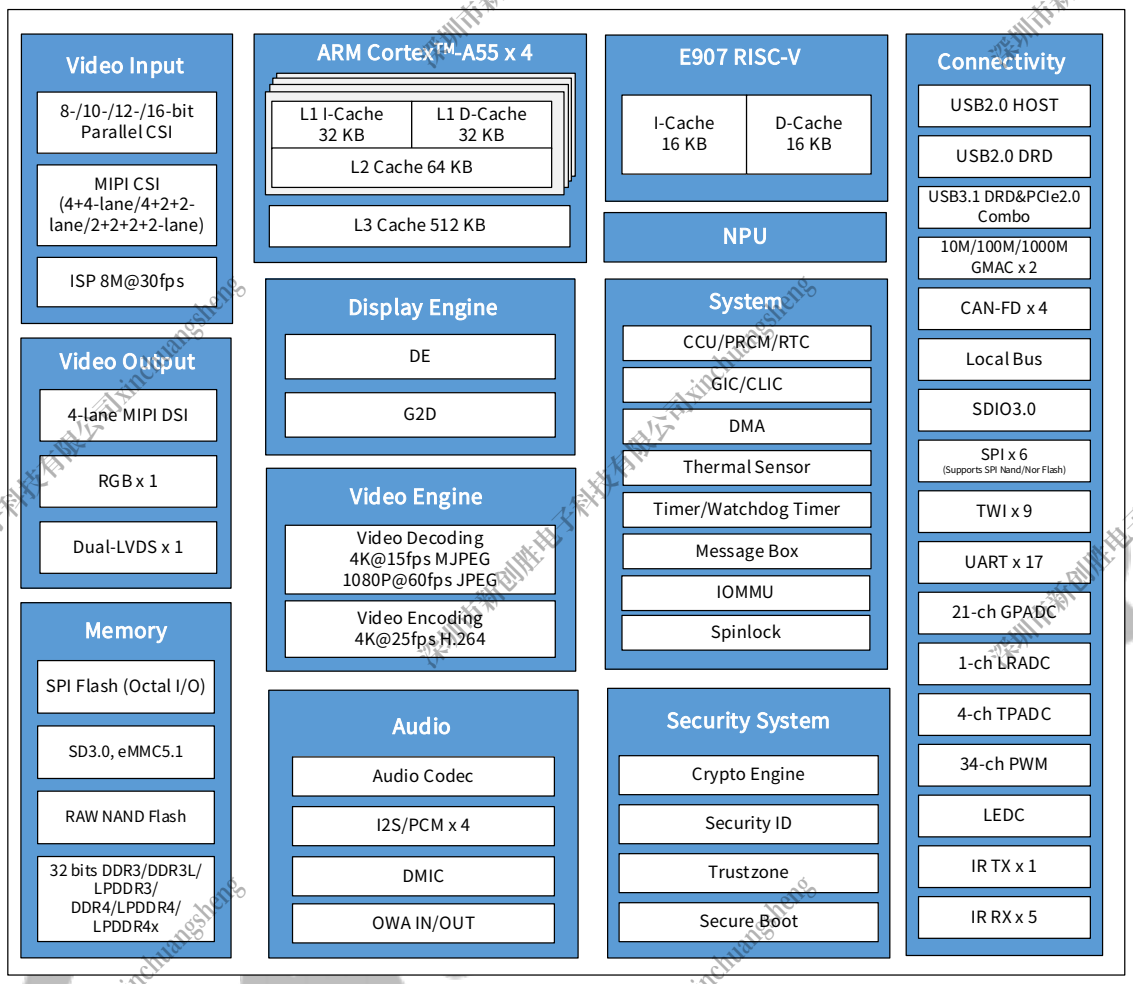
T536 family features high-performance quad-core Cortex™-A55 platform SoCs for the Industrial and intelligent hardware fields, which can be applied in interactive terminals, smart manufacturing, and other intelligent hardware and Industrial devices.

The T536 integrates a quad-core Cortex™-A55 CPU with independent L2 cache per core and a single-core E907 RISC-V with computing power scalability. T536 also has a neural processing unit (NPU) delivering up to 3 TOPS. With multiple heterogeneous expansion modes and multiple OS architectures. This processor family can meet the requirements of different application scenarios.

Besides, T536 family supports the combination of RGB/MIPI DSI/LVDS interfaces. The T536 also supplies high-speed interfaces for connectivity with 2 x GMAC and 1 x USB3.1 Gen1&PCIe2.1 Combo. In addition, the T536 processors contain 4 x CAN-FD and 1 x Local Bus for industrial application and expansion.

The following figure shows the system block diagram for the device.

Figure 1-1 System Block Diagram



(1) Video decoder and video encoder are time-multiplexed.

NOTE

Some modules shown in this block diagram are not offered on all devices, please refer to Table 2-1 Ordering Information for details.

2 Ordering Information

The following table provides the differences of orderable device(s) covered by this document.

Table 2-1 Ordering Information

Features	T536MX-CEN3	T536MX-CEN2	T536MX-CEX	T536MX-CXX
NPU	Up to 3 TOPS	Up to 2 TOPS	/	/
ECC Protection	Support	Support	Support	/
Qualification Level	Industrial	Industrial	Industrial	Industrial
Package	ED-FCCSP 533 balls, 15 mm x 15 mm	ED-FCCSP 533 balls, 15 mm x 15 mm	ED-FCCSP 533 balls, 15 mm x 15 mm	ED-FCCSP 533 balls, 15 mm x 15 mm

3 Features

3.1 Processors

- DynamIQ Architecture quad-core ARM Cortex™-A55
  - 32 KB L1 I/D-cache + 64 KB L2 cache per core
  - 512 KB L3 cache
  - ECC protection on L1 cache, L2 cache, and L3 cache
- E907 RISC-V MCU
- E902 RISC-V for low-power management
- NPU
  - Up to 3 TOPS
  - Supports INT8, UINT8, and INT16
  - Built-in 512 KB SRAM, and it can be shared with system

3.2 Memory

3.2.1 Boot ROM (BROM)

- On-chip memory
- Supports system boot from the following devices:
  - SD Card
  - eMMC
  - RAW NAND Flash

- SPI NOR Flash (Quad Mode and Single Mode)
- SPI NAND Flash

- Supports mandatory upgrade process through USB or SD card
- Supports GPADC pin and eFuse module to select the boot media type
- Supports normal booting and secure booting

3.2.2 Raw NAND Flash (NDFC)

- Up to 80-bit BCH per 1024 bytes
- 1K/2K/4K/8K/16K/32K bytes page size
- Up to 8-bit data bus width
- Supports SLC/MLC flash and EF-NAND
- Supports SDR, ONFI DDR1.0, Toggle DDR1.0, ONFI DDR2.0, and Toggle DDR2.0 Raw NAND flash

3.2.3 SDRAM

- 32-bit DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X interface with inline ECC
  - Not supports 6GB (4 GB +2 GB) LPDDR3 address space when inline ECC is enabled
  - Not supports inline ECC when the DQ width of BL8 DDR(DDR3, DDR4, LPDDR3 and BL8 mode LPDDR4) is 16bits
- 2 ranks
- Memory capacity up to 8 GB
- Clock frequency up to 1066 MHz for DDR3, DDR3L, and LPDDR3
- Clock frequency up to 1400 MHz for DDR4, LPDDR4, and LPDDR4X

3.2.4 SD/MMC Host Controller (SMHC)

- Three SD/MMC Host Controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (up to SD3.0)
  - SMHC1, compliant with the protocol Secure Digital I/O (up to SDIO3.0)
  - SMHC2, compliant with the protocol Multimedia Card (up to eMMC5.1)
- The SMHC0 and the SMHC1 support the following:
  - 1-bit or 4-bit data width
  - ECC protection for SMHC0
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 supports the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Supports ECC protection
  - Supports HS400 mode and HS200 mode

- Maximum performance:
  - SDR mode 200 MHz@1.8V IO pad
  - DDR mode 150 MHz@1.8V IO pad
  - SDR mode 50 MHz@3.3V IO pad
  - DDR mode 50 MHz@3.3V IO pad
- Supports block size of 1 to 65535 bytes
- Supports hardware CRC generation and error detection

3.2.5 SPI Flash Controller (SPIF)

- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI, and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports STR mode and DTR mode, and DTR mode supports DQS signal
- Supports prefetch mode to execute code from the Flash memory and to significantly reduce read time
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Supports mode0, mode1, mode2 and mode3
- Supports control signal configuration
  - One chip select to support multiple peripherals
  - Polarity and phase of the Chip Select (SPIF_CS) and SPI Clock (SPIF_CLK) are configurable

3.3 Image Processing

3.3.1 Image Signal Processor (ISP)

- Supports multiple sensor (up to 4) inputs
- Supports raw8/10/12/14/16
- Maximum resolution:
  - Online: 2688 x 4224
  - Offline: 4800 x 4224
- Performance of one sensor:
  - Online: 5M@30fps (linear), 5M@30fps(2f-wdr)
  - Offline: 8M@30fps (linear), 8M@30fps (2f-wdr)
- Supports multiple data stream outputs
  - Crop

  - 1 to 1/16 scaling for height and width
  - Up to 16 rectangle boxes
  - YUV422/YUV420/RGB888/RGB565 output
  - graphics mirror and flip
- Supports algorithm features
  - Crop
  - 2F-WDR
  - Dynamic Range Compression (DRC)
  - Local Tone Mapping
  - Black Level Correction
  - Digital Gain
  - White Balance
  - Len Shading Correction (LSC)
  - Gamma Correction
  - Defect Pixel Correction (DPC)
  - Cross Talk Correction (CTC)
  - Chromatic Aberration Correction (CAC)
  - Noise Reduction (2D/3D)
  - Bayer Interpolation
  - Sharpness
  - Color Enhancement (3D-LUT)
  - Adjustable 3A functions: Automatic White Balance (AWB), Automatic Exposure (AE), and Automatic Focus (AF)
  - Supports Anti-Flick Detection Statistics
  - Histogram Statistics

3.3.2 Encoder Pre-Processor (ENCPP)

- Geometric Distortion Correction (GDC), including Lens Distortion Correction (LDC) and Fish Eye Correction (FEC)
- Input data format: 8-bit image, YUV420/YUV422/ARGB8888
- Input resolution
  - Minimum: 64 x 64
  - Maximum: 8192 x8192
- Output resolution
  - Minimum: 64 x 64
  - Maximum: 8192 x 8192
- Rotation of 90/180/270 degrees clockwise and horizontal flip
- Watermark images overlaying
- Pixel-level cropping and virtual zoom

- Maximum unlimited 8x horizontal and vertical zoom-out
- Scaled image write back

3.4 Graphics Processing

3.4.1 Display Engine (DE)

- One display output, size up to 2048 x 2048
- Three alpha blending channels optional
- Four overlay layers in each channel, and has an independent scaler.
- Supports potter-duff compatible blending operation
- Input format
  - Semi-planar of YUV422/YUV420/YUV411
  - Planar of YUV422/YUV420/ YUV411
  - ARGB8888/XRGB8888/RGB888/ARGB4444/ ARGB1555/RGB565
- Supports input format palette only for UI channel to save image buffer memory
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- SmartColor2.0 for excellent display experience
  - Flesh tone protection
  - Hue gain, saturation gain, and value gain controller
  - Fully programmable color matrix
  - Dynamic gamma
- Supports write back for verification

3.4.2 Graphic 2D (G2D)

- Mixer supports layer size up to 2K pixels, and rotation supports layer size up to 4K pixels
- Mixer contains the following functions:
  - Multiple video formats and format conversion
    - YUV 4:2:0, YUV4:2:2, and YUV4:1:1
    - Supports conversion between any two of the above formats
  - Multiple pixel formats and 8/16/24/32-bit graphic layer
  - 1/16x to 32x resize ratio
  - Pre-multiplied alpha
  - Color key
  - Window clip
  - Porter-duff alpha blending
  - 32-phase 8-tap horizontal anti-alias filter and 2-phase 4-tap vertical anti-alias filter
  - FillRectangle, BitBlit, StretchBlit, and MaskBlit.
- Multiple rotation types
  - Horizontal flip and vertical flip

- 0, 90, 180, or 270 degrees' rotation in clockwise direction

3.5 Video Engine

NOTE

Video decoder and video encoder are time-multiplexed.

3.5.1 Video Decoder

- Motion JPEG, up to 3840 x 2160@15fps
- JPEG baseline
  - Supports 1920x1080@60fps
  - Maximum decoding resolution: 16384x16384
  - Supports two channels for output, the prior channel and the second channel.
    - The prior channel supports online scale-down: 1/2, 1/4, 1/8, 1/16, 1/32
    - The second channel supports online scale-down: 1/2, 1/4, 1/8
    - The second can be enabled when the prior channel output format is YUV420 and scale ratio is 1/1, 1/2 or 1/4. The prior channel scale ratio shall be larger than the second channel scale ratio.
  - Supports translation: YUVV444 to YUV420, YUV422 to YUV420, YUV420T to YUV420, YUV to RGB
  - Supports tile decoding (ROI Decoding, random rectangle region in the JPEG Picture. If tile decoding mode is enabled, the second shall be disabled)

3.5.2 Video Encoder

- H.264 BP/MP/HP encoding
  - Supports 3840x2160@25fps
  - Supports I/P frame type
  - Supports CBR, VBR and FIXEDQP modes
  - Supports region of interest(ROI) encoding, a maximum of eight ROIs
  - Maximum resolution: 4096x4096
- JPEG baseline encoding
  - Supports 3840x2160@15fps
  - Supports YUV420, YUV422 and YUV444 format
  - Maximum resolution: 8192x8192
- MJPEG baseline encoding up to 3840x2160@15fps

3.6 Video Input Interfaces

3.6.1 MIPI CSI

- Complaint with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.2
- Up to 2.0 Gbit/s per lane, 8M@30fps RAW12 2F-WDR (4-lane performance), size up to 3264(H) x 2448(V)
- Configurable number of data lanes and sequence of data lanes for MIPI interface:
  - 4+4-lane
  - 4+2+2-lane
  - 2+2+2+2-lane
- Pixel formats
  - RAW8, RAW10, RAW12, RAW14, and RAW16
  - 8-bit YUV420 and YUV422
  - RGB888 and RGB565

3.6.2 Parallel CSI

- Supports 8/10/12/16-bit width
- Supports BT.656, BT.601, BT.1120, and Digital Camera (DC) protocol
- Supports ITU-R BT.656 up to 4*720P@30fps
- Supports ITU-R BT.1120 up to 4*1080P@30fps
- Supports BT.656 2/4-channel time-multiplexed format
- Dual Data Rate (DDR) sample mode with maximum pixel clock of 148.5MHz

3.7 Video Output Interfaces

3.7.1 RGB and LVDS

- One RGB/BT.656/i8080 interface
  - DE/SYNC RGB mode, up to1920 x 1200@60fps (reduced blanking)
  - Serial/dummy RGB mode, up to 800 x 480@60fps
  - Dither function for RGB888, RGB666 and RGB565
  - Support BT.656 interface for NTSC and PAL
  - i8080 interface, up to 800x480@60fps
- Dual-link LVDS interface
  - Up to 1920x1080@60fps for dual-link
  - Up to 1366x768@60fps for single-link

3.7.2 MIPI DSI

- Compliant with MIPI DSI specification v1.02 and MIPI D-PHY specification v1.0

- Up to 1.0 Gbit/s per lane
- Supports one 4-lane MIPI DSI display, up to 1920 x 1200@60fps (reduced blanking)

3.8 System Peripherals

3.8.1 Clock Controller Unit (CCU)

- Supports clock configuration and clock generation for corresponding modules
- Supports software-controlled clock gating and software-controlled reset for corresponding modules

3.8.2 Message Box (MSGBOX)

- Up to seven message boxes
  - Three message boxes for communication between A55 subsystem, E907 subsystem, and E902 subsystem through one way channels.
  - Four separate message boxes for priority adjustment in AMP mode among A55 cores through one way channels
  - Each MSGBOX has one receiver and two or three transmitters
- 4 channels between every 2 users
- The FIFO depth of a channel is 8
- The FIFO width of a channel is 32 bits
- Supports interrupts

3.8.3 Power Reset Clock Management (PRCM)

- CPUS domain clock configuration
- Bus gating, bus reset, and clock configuration
- VDD-SYS power interface control
- RAM configuration control

3.8.4 RTC

- One on-chip RC oscillator
- Supports one external 24 MHz DCXO and one external 32.768 kHz oscillator
- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Timer frequency is 1 kHz
- Configurable initial value by software anytime
- Supports fanout function of internal 32.768 kHz clock
- Supports timing alarm, and generates interrupt and wakeup the external devices
- 8 general purpose registers for storing power-off information in RTC domain

3.8.5 Spinlock

- Supports 32 lock units
- Two kinds of lock status: locked and unlocked
- Lock time of the processor is predictable

3.8.6 Thermal Sensor Controller (THS)

- Three thermal sensors
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Support ±3°C error limit from 60°C to 125°C, and ±5°C from -40°C to 60°C

3.8.7 Timer

- Sixteen programmable 56-bit down timers
- Configurable counting clock: 32KHz, 24MHz, 16MHz, or 200MHz
- Two working modes: periodic mode and single count mode
- Generates an interrupt when the count is decreased to 0

3.8.8 Watchdog Timer (WDT)

- Three watchdog timers
- Supports 12 initial values
- Supports the generation of timeout interrupts
- Supports the generation of reset signals
- Supports watchdog restart

3.9 Audio

3.9.1 Audio codec

- One audio differential lineout output: LINEOUTP/N
- One audio digital-to-analog converter (DAC) channel
  - 16-bit and 20-bit sample resolution
  - 8 kHz to 192 kHz DAC sample rate
  - 95 ± 3 dB SNR@A-weight, -85 ± 3 dB THD+N
- Supports Dynamic Range Controller adjusting the DAC playback
- One 128x20-bits FIFO for DAC data transmit
- Programmable FIFO thresholds
- Supports interrupts and DMA

3.9.2 I2S/PCM

- Four I2S/PCM interfaces (I2S0, I2S1, I2S2, and I2S3)
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and TDM format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and receive data FIFOs
  - Programmable FIFO thresholds
  - 128 x 32-bit TXFIFO, 64 x 32-bit RXFIFO
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode (Only if the IO PAD and peripheral I2S/PCM satisfy timing parameters)
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode (Only if the IO PAD and peripheral I2S/PCM satisfy timing parameters)
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8 bits to 32 bits
  - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width ⩽ 24.576 MHz)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

3.9.3 DMIC

- Supports maximum 8 digital PDM microphones
- Supports sample rate from 8 kHz to 48 kHz

3.9.4 One Wire Audio (OWA)

- One OWA TX and One OWA RX, compliant with S/PDIF interface
- Compatible with IEC-60958 and IEC-61937
  - IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- Supports sample rate: 8 kHz – 384 kHz
- Transmit and receive data FIFOs
  - Programmable FIFO thresholds
  - One 128x24bits TXFIFO and one 64x24bits RXFIFO for audio data transfer

3.10 Peripheral Interfaces

3.10.1 SerDes System

SerDes contains one PCIe2.1 & USB3.1 DRD combo PHY, one PCIe2.1 controller, one USB3.1 DRD controller, one USB2.0 DRD controller, and one USB2.0 Host controller.

3.10.1.1 PCIe2.1

- One 1-lane PCI Express 2.1 (PCIe) port
- Supports Gen1(2.5 Gbit/s), Gen2 (5.0 Gbit/s) speed
- Supports Dual Mode (DM) mode: Root Complex (RC) mode and EndPoint (EP) mode
- RAS DP (Data Protection) for RAMs using ECC
- 2 Virtual Channels (VCs)
- Multiple Functions: support 4 Functions for PCIe in EP Mode
- Configurable MAX_PAYLOAD_SIZE size and up to 256 bytes
- Embedded DMA with Hardware Flow Control. Support 4 Write/Read Channels
- Internal Address Translation Unit. Support 16 Inbound Address Translation regions and 16 Outbound Address Translation regions
- MSI with Per-Vector Masking (PVM), Extended message data for MSI
- PCIe and USB2_U3(USB3.1 GEN2) share one COMB0 PHY in SerDes
- PCI Express Active State Power Management (ASPM)

3.10.1.2 USB3.1 DRD

- One USB3.1 PIPE PHY (USB2_U3)
- One USB 2.0 UTMI+ PHY (USB2_U2). USB2_U2 has no separate physical PHY, and it share the PHY with USB2.0 DRD or USB2.0 Host.
- Compliant with USB 3.1 Gen1 Specification
- Compatible to the xHCI specification v1.1
- Static host and device operation
- USB device mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s) and Full-Speed (FS, 12-Mbit/s) for USB2.0 PHY
- USB host mode supports the following:
  - Super-Speed (SS, 5 Gbit/s) for USB3.1 PHY
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) for USB2.0 PHY
- 4 pairs of user endpoints share TX FIFO (22 KB) and RX FIFO (asynchronous transmission 8KB and periodic transmission 8 KB). The size of Endpoint 0 RX/TX FIFO is 64B.
- Supports device or host operation at a time

- Hardware handles all data transfer
- AXI interface for DMA operation
- Implements both static and dynamic power reduction techniques at multiple levels

3.10.1.3 USB2.0 DRD

- One USB2.0 DRD (USB0), with integrated USB 2.0 analog PHY
- Complies with USB2.0 Specification
- Static host and device mode
- USB host that supports the following:
  - Compatible with Enhanced Host Controller Interface (EHCI) specification, version 1.0
  - Compatible with Open Host Controller Interface (OHCI) specification, version 1.0a
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s), and Low-Speed (LS, 1.5 Mbit/s)
  - Supports only 1 USB Root Port shared between EHCI and OHCI
- USB device that supports the following:
  - High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s)
  - Up to 8KB+64Bytes FIFO for EPs (including EP0)
- Supports an internal DMA controller for data transfer with memory
- Device and Host controller share an 8KB SRAM and a physical PHY
- Link low power mode: supports L0(On)/L2(Suspend)/L3(Off)

3.10.1.4 USB2.0 Host

- One USB 2.0 Host (USB1), with integrated USB 2.0 analog PHY
- Compatible with Enhanced Host Controller Interface (EHCI) specification, version 1.0
- Compatible with Open Host Controller Interface (OHCI) specification, version 1.0a
- Supports High-Speed (HS, 480 Mbit/s), Full-Speed (FS, 12 Mbit/s) and Low-Speed (LS, 1.5 Mbit/s) Device
- An internal DMA Controller for data transfer with memory
- Supports only 1 USB Root Port shared between EHCI and OHCI
- Link low power mode: supports L0(On)/L2(Suspend)/L3(Off)

3.10.2 GMAC

- Two 10/100/1000 Mbit/s Ethernet ports with RGMII and RMII interfaces
- Compliant with IEEE 802.3-2015 standard
- IEEE 1588-2008 for precision networked clock synchronization
- Supports Ethernet packet timestamping described in IEEE 1588-2002 and IEEE 1588-2008
- Supports both full-duplex and half-duplex operations
- Supports Full-duplex flow control

- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Double VLAN for VLAN insertion or VLAN replacement
- Transmitting TCP/IP Checksum Offload
- 4 KB TXFIFO for transmission packets and 8 KB RXFIFO for reception packets.
- Supports the management data input/output (MDIO) interface
- Supports memory ECC

3.10.3 CAN-FD

- Four CAN-FD ports (up to 64 data bytes)
- Conforms with ISO 11898-1:2015
- Supports CAN 2.0A and 2.0B protocol specification
- Supports AUTomotive Open System ARchitecture (AUTOSAR)
- Supports SAE J1939 standards
- CAN error logging
- Improved acceptance filtering
- Two configurable receive FIFOs
- Separate signaling on reception of high priority messages
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO
- Configurable transmit queue
- Configurable transmit event FIFO
- Direct message RAM access for host CPU
- Supports DMA Master

3.10.4 Local Bus Controller (LBC)

- 8/16/32-bit wide transmission
- Address and data multiplexed access
- Supports parity check
- Synchronous read/write 128 x 8 FIFO (AHB clock domain)
- Read/write 16 x 8 buffer (local bus clock domain)
- Up to 400 MHz AHB clock and up to 100 MHz local bus clock
- Up to four chip selects, and the polarity is configurable
- Supports burst mode

3.10.5 UART

- Up to 17 UART controllers
  - UART0, UART1, UART2, UART3, UART4, UART5, UART6, UART7, UART8, UART9, UART10, UART11, UART12, UART13, and UART14
  - S_UART0 and S_UART1
- Compatible with industry-standard 16450/16550 UARTs
- 5-8 data bits, 1/1.5/2 stop bits, programmable parity (even, odd, or no parity)
- Programmable baud rates up to 10 Mbit/s (excluding S_UART0 and S_UART1)
- Two separate FIFOs: one is RX FIFO, and the other is TX FIFO
  - Each of them is 64 bytes for UART0, UART9, UART10, UART11, UART12, UART13, UART14, and S_UART0
  - Each of them is 128 bytes for UART1, UART2, UART3, UART4, UART5, UART6, UART7, UART8, and S_UART1
- Supports 9-bit/RS-485 format and RS-485 full duplex mode
- Supports Software/hardware flow control
- Supports interrupts and DMA mode
- Supports auto-flow by using CTS & RTS (excluding UART0)
- Supports LIN mode (UART1/S_UART1)

3.10.6 PWM

- Up to 30 PWM channels and 4 S-PWM channels
  - Supports PWM continuous mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz (when the clock source is DCXO)
    - 0 to 100 MHz (when the clock source is APB0 clock)
  - Various duty-cycle: 0% -100%
  - Minimum resolution: 1/65536
  - Up to 10-ch periodic counting of input pulses
- Maximum 5 complementary pairs output and the pairing methods are as follows:
  - PWM Channels

    PWM0-0+PWM0-1, PWM0-2+PWM0-3, PWM0-4+PWM0-5, PWM0-6+PWM0-7, PWM0-8+PWM0-9, PWM1-0+PWM1-1, PWM1-2+PWM1-3, PWM1-4+PWM1-5, PWM1-6+PWM1-7, PWM1-8+PWM1-9, PWM2-0+PWM2-1, PWM2-2+PWM2-3, PWM2-4+PWM2-5, PWM2-6+PWM2-7, PWM2-8+PWM2-9
  - S-PWM Channels

    S-PWM0-1 + S-PWM0-1, S-PWM0-2 + S-PWM0-3
  - Supports dead-zone generator, and the dead-zone time is configurable

- Maximum 4 group of PWM channel output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- Maximum 10 channels capture input
  - Supports rising edge detection and falling edge detection for input waveform pulse
  - Supports pulse-width measurement for input waveform pulse

3.10.7 SPI and SPI_DBI

- Up to 6 SPI controllers
  - SPI0, SPI2, SPI3, SPI4, and S_SPI0, supporting SPI mode
  - SPI1, supporting SPI mode and display bus interface (DBI) mode

SPI mode

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
  - Camera slave mode for Single-Output/Single-Input SPI (only SPI2 and SPI3)
  - Camera slave mode for Dual-Input SPI (only SPI2 and SPI3)
  - Camera slave mode for Quad-Input SPI (only SPI2 and SPI3)
  - Ordinary slave mode for Single-Output/Single-Input SPI
- Supports vertical synchronization and frame header detection for camera slave mode
- Supports mode0, mode1, mode2, and mode3 for master mode and both two slave modes
- TX/RX DMA Slave interface
- Transmit data FIFO with 8-bit wide and 64-entry
- Receive data FIFO with 8-bit wide and 64-entry
- Transmit data buffer with 8-bit wide and 128-entry
- Receive data buffer with 8-bit wide and 128-entry
- Supports control signal configuration for master mode and both two slave modes
  - Two chip selects for SPI0 and one chip select for SPI1, SPI2, SPI3, SPI4, S_SPI0 to support multiple peripherals
  - Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

DBI mode

- DBI Type C 3 Line/4 Line Interface Mode
- 2 Data Lane Interface Mode
- RGB111/444/565/666/888 video format
- Maximum resolution of RGB666 240 x 320@30Hz with single data lane

- Maximum resolution of RGB888 240 x 320@60Hz or 320 x 480@30Hz with dual data lane
- Tearing effect
- Software flexible control video frame rate

3.10.8 Two Wire Interface (TWI)

- Up to 9 TWI controllers
  - TWI0, TWI1, TWI2, TWI3, TWI4, TWI5, and TWI6
  - S_TWI0 and S_TWI1
- Compliant with I2C bus standard
- master mode and slave mode
- 7-bit and 10-bit device addressing modes
- Standard mode (up to 100 Kbit/s) and fast mode (up to 400 Kbit/s)
- Supports multi-master system

3.10.9 General Purpose ADC (GPADC)

- Two 10-ch ADCs and one 1-ch ADC, total 21 channels
- 12-bit sampling resolution
- Maximum sampling frequency up to 2 MHz
- Supports three operation modes: single conversion mode, continuous conversion mode, burst conversion mode
- Analog input range: 0 to 1.8 V

3.10.10 Low Rate ADC (LRADC)

- 1-ch LRADC with 6-bit resolution and maximum 2kHz sampling rate
- Supports hold key and general key
- Supports normal, continue and single work mode
- Power supply voltage:1.8 V; power reference voltage:1.35 V
- Voltage input range between 0 to 1.35 V

3.10.11 Touch Panel ADC (TPADC)

- 12-bit SAR type A/D converter
- 32x12 FIFO for storing A/D conversion result
- Supports DMA slave interface
- Supports AUX ADC, up to 4 channels
- 4-wire resistive touch panel input detection
  - Single touch detection
  - Dual touch detection
  - Touch pressure measurement with programmable threshold

- Pen down detection with programmable sensitivity
- Median and averaging filter for noise reduction
- X/Y coordinate exchange

- Maximum sampling rate of 750 kHz

3.10.12 LED Controller (LEDC)

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width and reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- Configurable interval time between data packets and frame data
- Configurable RGB display mode
- Configurable default level of non-data output

3.10.13Consumer Infrared Transmitter (IR_TX)

- One IR_TX interface
- NEC format infra data
- RLC encoding
- Arbitrary wave generator
- Configurable carrier frequency
- 64x8 bits FIFO for data buffer
- Supports Interrupts and DMA mode
- Supports DMA shake and wait mode

3.10.14Consumer Infrared Receiver (IR_RX)

- Five IR_RX interfaces
- NEC format infra data
- RLC encoding
- 64x8 bits FIFO for data buffer
- Sample clock up to 1 MHz

3.11 Security

3.11.1 Crypto Engine (CE)

- Symmetrical algorithm:
  - AES symmetrical algorithm
    - Key size: 128/192/256 bits
    - CFB mode includes: CFB1, CFB8, CFB64, and CFB128

  - CTR mode includes: CTR16, CTR32, CTR64, and CTR128
  - Supports ECB, CBC, CTS, OFB, CBC-MAC, GCM, and XTS modes
- Support XTS-AES symmetrical algorithm: key size: 256/512 bits
- DES symmetrical algorithm
  - CTR mode, includes: CTR16, CTR32, and CTR64
  - Supports ECB, CBC, and CBC-MAC mode
- 3DES, SM4 symmetrical algorithm

- Hash algorithms
  - Support MD5, SHA1, SHA224, SHA256, SHA384, SHA512, and SM3
  - Support HMAC-SHA1, HMAC-SHA256
- Random bit generator algorithms
  - Support PRNG, 175 bits seed width, and output with multiple of 5 words
  - Support TRNG, post-process by hardware with SHA256, output with multiple of 8 words
- Public key algorithms
  - Support RSA public key algorithms: 512/1024/2048/3072/4096-bit width
  - Support ECC public key algorithms: 160/224/256/384/521-bit width
  - Support SM2 algorithms

3.11.2 Security ID (SID)

- 2048-bit eFuse
- Supports secure and non-secure world in eFuse
- Backup eFuse information by using SID_SRAM
- One-time programming
- Selecting double-bit check by parameter definition
- Data scrambling
- Reading and writing protection
- Password for secure debug

3.11.3 Secure Memory Control (SMC)

- The SMC is always secure, only secure CPU can access the SMC
- Sets secure area of DRAM
- Supports Master and address protection
- Sets secure property that Master accesses to DRAM
- Maximum 16 regions and Master has access to each region

3.11.4 Secure Peripherals Control (SPC)

- The SPC is always secure, only secure CPU can access the SPC
- Sets secure property of peripherals

3.11.5 TrustZone Memory Access (TZMA)

- The TZMA is always secure and can only be accessed by secure CPU
- Sets the secure area of SRAM

3.12 Package

ED-FCCSP 533 balls, 15 mm x 15 mm body size, 1.056 mm height (maximum), 0.5 mm ball pitch, 0.3 mm ball size.

4 Pin Description

4.1 Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Ball#**: Package ball numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] **I/O Power Supply**: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

4.1.1 SDRAM

Table 4-1 SDRAM Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AC13	SRST	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
V18	SZQ	AI	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH12	SA0	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG12	SA1	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AC15	SA2	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH10	SA3	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH6	SA4	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH11	SA5	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AB11	SA6	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AB15	SA7	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AB9	SA8	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF13	SA9	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG13	SA10	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH13	SA11	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG11	SA12	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD11	SA13	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AC9	SA14	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD9	SA15	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG10	SA16	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF11	SA17	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AC11	SACT	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD7	SBA0	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG6	SBA1	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF9	SBG0	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD13	SBG1	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF7	SCKE0	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AH9	SCKN	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG9	SCKP	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG8	SCS0	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH8	SCS1	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF15	SDQM0	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH19	SDQM1	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH2	SDQM2	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AE2	SDQM3	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH14	SDQ0	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG14	SDQ1	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD15	SDQ2	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH16	SDQ3	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG16	SDQ4	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH17	SDQ5	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AB17	SDQ6	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AC17	SDQ7	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG17	SDQ8	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF17	SDQ9	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG19	SDQ10	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD17	SDQ11	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF19	SDQ12	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD19	SDQ13	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG20	SDQ14	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH20	SDQ15	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF3	SDQ16	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG1	SDQ17	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG2	SDQ18	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG3	SDQ19	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG4	SDQ20	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH4	SDQ21	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AG5	SDQ22	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH5	SDQ23	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AB2	SDQ24	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AC3	SDQ25	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AB3	SDQ26	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AC2	SDQ27	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AF2	SDQ28	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AE3	SDQ29	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AE5	SDQ30	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD5	SDQ31	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH15	SDQS0N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG15	SDQS0P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH18	SDQS1N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG18	SDQS1P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AJ3	SDQS2N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH3	SDQS2P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD3	SDQS3N	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AD2	SDQS3P	I/O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AG7	SODT0	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
AH7	SODT1	O	N/A	N/A	N/A	VCC-DRAM/VCC-DRAML
W9	VCC-DRAM	P	N/A	N/A	N/A	N/A
W12	VCC-DRAM	P	N/A	N/A	N/A	N/A
W13	VCC-DRAM	P	N/A	N/A	N/A	N/A
W14	VCC-DRAM	P	N/A	N/A	N/A	N/A
W15	VCC-DRAM	P	N/A	N/A	N/A	N/A
Y12	VCC-DRAM	P	N/A	N/A	N/A	N/A
V8	VCC-DRAML	P	N/A	N/A	N/A	N/A
V10	VCC-DRAML	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
V11	VCC-DRAML	P	N/A	N/A	N/A	N/A
V14	VCC-DRAML	P	N/A	N/A	N/A	N/A
Y15	VDD18-DRAM	P	N/A	N/A	N/A	N/A

4.1.2 System Control

Table 4-2 System Control Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AD21	FEL	I	N/A	PU	N/A	VCC-IO
AE21	JTAG-SEL	I	N/A	PU	N/A	VCC-IO
AE28	NMI	I/O, OD	N/A	N/A	N/A	VCC-RTC
AF27	RESET	I/O, OD	N/A	N/A	N/A	VCC-RTC

4.1.3 RTC&PLL

Table 4-3 RTC&PLL Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AF28	X32KFOUT	AO, OD	N/A	N/A	N/A	VCC-PM
AG29	X32KIN	AI	N/A	N/A	N/A	VCC-RTC
AG28	X32KOUT	AO	N/A	N/A	N/A	VCC-RTC
AA21	PLLTEST	AO, OD	N/A	N/A	N/A	VCC-PLL
R14	CPU-PLLTEST	AO, OD	N/A	N/A	N/A	VCC-CPU-PLL
R13	VCC-CPU-PLL	P	N/A	N/A	N/A	N/A
AB24	VCC-RTC	P	N/A	N/A	N/A	N/A
AA23	VCC-PLL	P	N/A	N/A	N/A	N/A

4.1.4 DCXO

Table 4-4 DCXO Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AJ27	DXIN	AI	N/A	N/A	N/A	VCC-PLL
AH27	DXOUT	AO	N/A	N/A	N/A	VCC-PLL
AH28	REFCLK-OUT	AO	N/A	N/A	N/A	VCC-PLL

4.1.5 GPIO Groups

4.1.5.1 Port A

Table 4-5 Port A Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
H24	PA0	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
H25	PA1	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
F27	PA2	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
E28	PA3	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
E29	PA4	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
F28	PA5	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
G29	PA6	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
G28	PA7	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
G27	PA8	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
H26	PA9	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
K22	VCC-PA	P	N/A	N/A	N/A	N/A

4.1.5.2 Port B

Table 4-6 Port B Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AC21	PB0	I/O	Z	PU/PD	4 mA	VCC-IO
AB21	PB1	I/O	Z	PU/PD	4 mA	VCC-IO

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AG24	PB2	I/O	Z	PU/PD	4 mA	VCC-IO
AF23	PB3	I/O	Z	PU/PD	4 mA	VCC-IO
AE23	PB4	I/O	Z	PU/PD	4 mA	VCC-IO
AD23	PB5	I/O	Z	PU/PD	4 mA	VCC-IO
AD24	PB6	I/O	Z	PU/PD	4 mA	VCC-IO
AH24	PB7	I/O	Z	PU/PD	4 mA	VCC-IO
AG25	PB8	I/O	Z	PU/PD	4 mA	VCC-IO
AH26	PB9	I/O	Z	PU/PD	4 mA	VCC-IO
AG26	PB10	I/O	Z	PU/PD	4 mA	VCC-IO
AF25	PB11	I/O	Z	PU/PD	4 mA	VCC-IO
AC23	PB12	I/O	Z	PU/PD	4 mA	VCC-IO
AJ25	PB13	I/O	Z	PU/PD	4 mA	VCC-IO
AH25	PB14	I/O	Z	PU/PD	4 mA	VCC-IO

4.1.5.3 Port C

Table 4-7 Port C Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
V4	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
V3	PC1	I/O	Z	PU/PD	4 mA	VCC-PC
V5	PC2	I/O	Z	PU/PD	4 mA	VCC-PC
Y3	PC3	I/O	Z	PU	4 mA	VCC-PC
Y4	PC4	I/O	Z	PU	4 mA	VCC-PC
V7	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
V6	PC6	I/O	Z	PU	4 mA	VCC-PC
Y7	PC7	I/O	Z	PU	4 mA	VCC-PC
V1	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
V2	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
W1	PC10	I/O	Z	PU/PD	4 mA	VCC-PC
W2	PC11	I/O	Z	PU/PD	4 mA	VCC-PC

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
Y5	PC12	I/O	Z	PU/PD	4 mA	VCC-PC
Y1	PC13	I/O	Z	PU/PD	4 mA	VCC-PC
Y2	PC14	I/O	Z	PU/PD	4 mA	VCC-PC
AA1	PC15	I/O	Z	PU/PD	4 mA	VCC-PC
AA2	PC16	I/O	Z	PU/PD	4 mA	VCC-PC
U8	VCC-PC	P	N/A	N/A	N/A	N/A

4.1.5.4 Port D

Table 4-8 Port D Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B5	PD0	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
A5	PD1	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
B4	PD2	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
A4	PD3	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
B3	PD4	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
A3	PD5	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
C1	PD6	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
C2	PD7	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
D1	PD8	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
D2	PD9	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
E1	PD10	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
E2	PD11	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
F1	PD12	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
F2	PD13	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
G1	PD14	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
G2	PD15	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
H1	PD16	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
H2	PD17	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
J1	PD18	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
J2	PD19	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
K6	PD20	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
H6	PD21	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
H5	PD22	I/O	Z	PU/PD	4 mA	VCC-PD
H4	PD23	I/O	Z	PU/PD	4 mA	VCC-PD
K8	VCC-PD	P	N/A	N/A	N/A	N/A
L9	VCC18-LVDS	P	N/A	N/A	N/A	N/A

4.1.5.5 Port E

Table 4-9 Port E Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B9	PE0	I/O	Z	PU/PD	4 mA	VCC-PE
G9	PE1	I/O	Z	PU/PD	4 mA	VCC-PE
F9	PE2	I/O	Z	PU/PD	4 mA	VCC-PE
G11	PE3	I/O	Z	PU/PD	4 mA	VCC-PE
F11	PE4	I/O	Z	PU/PD	4 mA	VCC-PE
E11	PE5	I/O	Z	PU/PD	4 mA	VCC-PE
D13	PE6	I/O	Z	PU/PD	4 mA	VCC-PE
E13	PE7	I/O	Z	PU/PD	4 mA	VCC-PE
E9	PE8	I/O	Z	PU/PD	4 mA	VCC-PE
D11	PE9	I/O	Z	PU/PD	4 mA	VCC-PE
D9	PE10	I/O	Z	PU/PD	4 mA	VCC-PE
C10	PE11	I/O	Z	PU/PD	4 mA	VCC-PE
A10	PE12	I/O	Z	PU/PD	4 mA	VCC-PE
C9	PE13	I/O	Z	PU/PD	4 mA	VCC-PE
B10	PE14	I/O	Z	PU/PD	4 mA	VCC-PE
H13	PE15	I/O	Z	PU/PD	4 mA	VCC-PE
G13	PE16	I/O	Z	PU/PD	4 mA	VCC-PE

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
F13	PE17	I/O	Z	PU/PD	4 mA	VCC-PE
K11	VCC-PE	P	N/A	N/A	N/A	N/A

4.1.5.6 Port F

Table 4-10 Port F Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AH21	PF0	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
AG21	PF1	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
AH22	PF2	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
AG22	PF3	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
AJ23	PF4	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
AH23	PF5	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
AF21	PF6	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
V19	VCC18-PF	P	N/A	N/A	N/A	N/A

4.1.5.7 Port G

Table 4-11 Port G Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
R29	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
T27	PG1	I/O	Z	PU/PD	4 mA	VCC-PG
R28	PG2	I/O	Z	PU/PD	4 mA	VCC-PG
R27	PG3	I/O	Z	PU/PD	4 mA	VCC-PG
U29	PG4	I/O	Z	PU/PD	4 mA	VCC-PG
U28	PG5	I/O	Z	PU/PD	4 mA	VCC-PG
T24	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
T25	PG7	I/O	Z	PU/PD	4 mA	VCC-PG
V27	PG8	I/O	Z	PU/PD	4 mA	VCC-PG
V28	PG9	I/O	Z	PU/PD	4 mA	VCC-PG

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
V26	PG10	I/O	Z	PU/PD	4 mA	VCC-PG
V25	PG11	I/O	Z	PU/PD	4 mA	VCC-PG
T26	PG12	I/O	Z	PU/PD	4 mA	VCC-PG
U27	PG13	I/O	Z	PU/PD	4 mA	VCC-PG
P24	PG14	I/O	Z	PU/PD	4 mA	VCC-PG
P23	VCC-PG	P	N/A	N/A	N/A	N/A

4.1.5.8 Port H

Table 4-12 Port H Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
G5	PH0	I/O	Z	PU/PD	4 mA	VCC-PH
F5	PH1	I/O	Z	PU/PD	4 mA	VCC-PH
E5	PH2	I/O	Z	PU/PD	4 mA	VCC-PH
D5	PH3	I/O	Z	PU/PD	4 mA	VCC-PH
B6	PH4	I/O	Z	PU/PD	4 mA	VCC-PH
A6	PH5	I/O	Z	PU/PD	4 mA	VCC-PH
C6	PH6	I/O	Z	PU/PD	4 mA	VCC-PH
B7	PH7	I/O	Z	PU/PD	4 mA	VCC-PH
G7	PH8	I/O	Z	PU/PD	4 mA	VCC-PH
F7	PH9	I/O	Z	PU/PD	4 mA	VCC-PH
E7	PH10	I/O	Z	PU/PD	4 mA	VCC-PH
D7	PH11	I/O	Z	PU/PD	4 mA	VCC-PH
C7	PH12	I/O	Z	PU/PD	4 mA	VCC-PH
B8	PH13	I/O	Z	PU/PD	4 mA	VCC-PH
C8	PH14	I/O	Z	PU/PD	4 mA	VCC-PH
A8	PH15	I/O	Z	PU/PD	4 mA	VCC-PH
K10	VCC-PH	P	N/A	N/A	N/A	N/A

4.1.5.9 Port I

Table 4-13 Port I Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B27	PI0	I/O	Z	PU/PD	4 mA	VCC-PI
B28	PI1	I/O	Z	PU/PD	4 mA	VCC-PI
C28	PI2	I/O	Z	PU/PD	4 mA	VCC-PI
C27	PI3	I/O	Z	PU/PD	4 mA	VCC-PI
C29	PI4	I/O	Z	PU/PD	4 mA	VCC-PI
D27	PI5	I/O	Z	PU/PD	4 mA	VCC-PI
A27	PI6	I/O	Z	PU/PD	4 mA	VCC-PI
B26	PI7	I/O	Z	PU/PD	4 mA	VCC-PI
D25	PI8	I/O	Z	PU/PD	4 mA	VCC-PI
E25	PI9	I/O	Z	PU/PD	4 mA	VCC-PI
D21	PI10	I/O	Z	PU/PD	4 mA	VCC-PI
E21	PI11	I/O	Z	PU/PD	4 mA	VCC-PI
F21	PI12	I/O	Z	PU/PD	4 mA	VCC-PI
D23	PI13	I/O	Z	PU/PD	4 mA	VCC-PI
E23	PI14	I/O	Z	PU/PD	4 mA	VCC-PI
A26	PI15	I/O	Z	PU/PD	4 mA	VCC-PI
B25	PI16	I/O	Z	PU/PD	4 mA	VCC-PI
K20	VCC-PI	P	N/A	N/A	N/A	N/A

4.1.5.10 Port J

Table 4-14 Port J Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
P1	PJ0	I/O	Z	PU/PD	4 mA	VCC-PJ
N3	PJ1	I/O	Z	PU/PD	4 mA	VCC-PJ
P3	PJ2	I/O	Z	PU/PD	4 mA	VCC-PJ
U3	PJ3	I/O	Z	PU/PD	4 mA	VCC-PJ

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
P4	PJ4	I/O	Z	PU/PD	4 mA	VCC-PJ
T3	PJ5	I/O	Z	PU/PD	4 mA	VCC-PJ
T7	PJ6	I/O	Z	PU/PD	4 mA	VCC-PJ
T6	PJ7	I/O	Z	PU/PD	4 mA	VCC-PJ
P5	PJ8	I/O	Z	PU/PD	4 mA	VCC-PJ
K5	PJ9	I/O	Z	PU/PD	4 mA	VCC-PJ
U2	PJ10	I/O	Z	PU/PD	4 mA	VCC-PJ
N2	PJ11	I/O	Z	PU/PD	4 mA	VCC-PJ
P2	PJ12	I/O	Z	PU/PD	4 mA	VCC-PJ
T2	PJ13	I/O	Z	PU/PD	4 mA	VCC-PJ
T4	PJ14	I/O	Z	PU/PD	4 mA	VCC-PJ
T5	PJ15	I/O	Z	PU/PD	4 mA	VCC-PJ
M1	PJ16	I/O	Z	PU/PD	4 mA	VCC-PJ
M3	PJ17	I/O	Z	PU/PD	4 mA	VCC-PJ
M2	PJ18	I/O	Z	PU/PD	4 mA	VCC-PJ
L1	PJ19	I/O	Z	PU/PD	4 mA	VCC-PJ
R3	PJ20	I/O	Z	PU/PD	4 mA	VCC-PJ
R2	PJ21	I/O	Z	PU/PD	4 mA	VCC-PJ
P7	PJ22	I/O	Z	PU/PD	4 mA	VCC-PJ
P6	PJ23	I/O	Z	PU/PD	4 mA	VCC-PJ
K4	PJ24	I/O	Z	PU/PD	4 mA	VCC-PJ
K3	PJ25	I/O	Z	PU/PD	4 mA	VCC-PJ
M5	PJ26	I/O	Z	PU/PD	4 mA	VCC-PJ
M4	PJ27	I/O	Z	PU/PD	4 mA	VCC-PJ
K1	PJ28	I/O	Z	PU/PD	4 mA	VCC-PJ
K2	PJ29	I/O	Z	PU/PD	4 mA	VCC-PJ
M7	PJ30	I/O	Z	PU/PD	4 mA	VCC-PJ
M6	PJ31	I/O	Z	PU/PD	4 mA	VCC-PJ
P8	VCC-PJ	P	N/A	N/A	N/A	N/A

4.1.5.11 Port K

Table 4-15 Port K Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B13	PK0	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A13	PK1	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B11	PK2	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A11	PK3	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B12	PK4	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A12	PK5	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B16	PK6	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A16	PK7	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B14	PK8	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A14	PK9	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B15	PK10	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A15	PK11	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B19	PK12	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A19	PK13	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B17	PK14	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A17	PK15	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
B18	PK16	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
A18	PK17	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
D19	PK18	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
E19	PK19	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
E15	PK20	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
D15	PK21	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
E17	PK22	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
D17	PK23	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-MCSI
J13	VCC-PK	P	N/A	N/A	N/A	N/A
H15	VCC18-MCSI	P	N/A	N/A	N/A	N/A

4.1.5.12 Port L

Table 4-16 Port L Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
W27	PL0	I/O	Z	PU	4 mA	VCC-PL
Y28	PL1	I/O	Z	PU	4 mA	VCC-PL
W28	PL2	I/O	Z	PU/PD	4 mA	VCC-PL
W29	PL3	I/O	Z	PU/PD	4 mA	VCC-PL
AA29	PL4	I/O	Z	PU/PD	4 mA	VCC-PL
Y27	PL5	I/O	Z	PU/PD	4 mA	VCC-PL
Y26	PL6	I/O	Z	PU/PD	4 mA	VCC-PL
Y25	PL7	I/O	Z	PU/PD	4 mA	VCC-PL
AB28	PL8	I/O	Z	PU/PD	4 mA	VCC-PL
AB27	PL9	I/O	Z	PU/PD	4 mA	VCC-PL
AA27	PL10	I/O	Z	PU/PD	4 mA	VCC-PL
AA28	PL11	I/O	Z	PU/PD	4 mA	VCC-PL
AB26	PL12	I/O	Z	PU/PD	4 mA	VCC-PL
AB25	PL13	I/O	Z	PU/PD	4 mA	VCC-PL
T21	VCC-PL	P	N/A	N/A	N/A	N/A

4.1.5.13 Port M

Table 4-17 Port M Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
AD27	PM0	I/O	Z	PU/PD	4 mA	VCC-PM
AE29	PM1	I/O	Z	PU/PD	4 mA	VCC-PM
AD28	PM2	I/O	Z	PU/PD	4 mA	VCC-PM
AC27	PM3	I/O	Z	PU/PD	4 mA	VCC-PM
AC29	PM4	I/O	Z	PU/PD	4 mA	VCC-PM
AC28	PM5	I/O	Z	PU/PD	4 mA	VCC-PM
V21	VCC-PM	P	N/A	N/A	N/A	N/A

4.1.6 SerDes

Table 4-18 SerDes Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
A24	PCIE-REF-CLKN	A I/O	N/A	N/A	N/A	VCC18-COMB
B24	PCIE-REF-CLKP	A I/O	N/A	N/A	N/A	VCC18-COMB
A25	PCIE-REXT	A I/O	N/A	N/A	N/A	VCC18-COMB
A23	PCIE-RX0-DN/USB2-U3-RXN	AI	N/A	N/A	N/A	VCC18-COMB
B23	PCIE-RX0-DP/USB2-U3-RXP	AI	N/A	N/A	N/A	VCC18-COMB
A22	PCIE-TX0-DN/USB2-U3-TXN	AO	N/A	N/A	N/A	VCC18-COMB
B22	PCIE-TX0-DP/USB2-U3-TXP	AO	N/A	N/A	N/A	VCC18-COMB
B20	USB0-DM	A I/O	N/A	N/A	N/A	VCC33-USB0-USB1
A20	USB0-DP	A I/O	N/A	N/A	N/A	VCC33-USB0-USB1
B21	USB1-DM	A I/O	N/A	N/A	N/A	VCC33-USB0-USB1
A21	USB1-DP	A I/O	N/A	N/A	N/A	VCC33-USB0-USB1
H19	VCC18-COMB	P	N/A	N/A	N/A	N/A
K16	VCC33-USB0-USB1	P	N/A	N/A	N/A	N/A
J18	VDD09-COMB	P	N/A	N/A	N/A	N/A
J16	VDD09-USB0-USB1	P	N/A	N/A	N/A	N/A

4.1.7 Audio Codec

Table 4-19 Audio Codec Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
D29	LINEOUTN	AO	N/A	N/A	N/A	AVCC
D28	LINEOUTP	AO	N/A	N/A	N/A	AVCC
H22	VRA1	AO	N/A	N/A	N/A	AVCC
K21	AVCC	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
H23	AGND	G	N/A	N/A	N/A	N/A

4.1.8 GPADC

Table 4-20 GPADC Pin Characteristics(1)

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
K28	BOOT-SEL-GPADC1-4	AI	N/A	N/A	N/A	VCC18-ADC
L29	DDR-PARA-SEL-GPADC1-5	AI	N/A	N/A	N/A	VCC18-ADC
K27	GPADC1-6	AI	N/A	N/A	N/A	VCC18-ADC
K26	GPADC1-7	AI	N/A	N/A	N/A	VCC18-ADC
L28	GPADC1-8	AI	N/A	N/A	N/A	VCC18-ADC
M24	GPADC1-9	AI	N/A	N/A	N/A	VCC18-ADC
H27	GPADC3-0	AI	N/A	N/A	N/A	VCC18-ADC
M23	VCC18-VCM-ADC	A I/O	N/A	N/A	N/A	VCC18-ADC
M21	VCC18-ADC	P	N/A	N/A	N/A	N/A
M22	AGND-ADC	G	N/A	N/A	N/A	N/A

(1) The signals of GPADC1-0, GPADC1-1, GPADC 1-2, GPADC1-3 are multiplexed with TPADC signals, see Table 4-21.

4.1.9 TPADC

Table 4-21 TPADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
J29	TP-X1/GPADC1-0	AI	N/A	N/A	N/A	VCC18-ADC
H28	TP-X2/GPADC1-1	AI	N/A	N/A	N/A	VCC18-ADC
J27	TP-Y1/GPADC1-2	AI	N/A	N/A	N/A	VCC18-ADC
J28	TP-Y2/GPADC1-3	AI	N/A	N/A	N/A	VCC18-ADC

4.1.10 LRADC

Table 4-22 LRADC Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
P28	LRADC	AI	N/A	N/A	N/A	VCC18-ADC

4.1.11 Power

Table 4-23 Power Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
W20	VCC18-EFUSE	P	N/A	N/A	N/A	N/A
V20	VCC-IO	P	N/A	N/A	N/A	N/A
N9	VDD-CPU	P	N/A	N/A	N/A	N/A
N10	VDD-CPU	P	N/A	N/A	N/A	N/A
P9	VDD-CPU	P	N/A	N/A	N/A	N/A
P11	VDD-CPU	P	N/A	N/A	N/A	N/A
T9	VDD-CPU	P	N/A	N/A	N/A	N/A
T10	VDD-CPU	P	N/A	N/A	N/A	N/A
T11	VDD-CPU	P	N/A	N/A	N/A	N/A
N11	VDD-CPU	P	N/A	N/A	N/A	N/A
T13	VDD-CPUFB	P	N/A	N/A	N/A	N/A
V23	VDD-CPUS	P	N/A	N/A	N/A	N/A
N18	VDD-NPU	P	N/A	N/A	N/A	N/A
N19	VDD-NPU	P	N/A	N/A	N/A	N/A
N20	VDD-NPU	P	N/A	N/A	N/A	N/A
P20	VDD-NPU	P	N/A	N/A	N/A	N/A
R19	VDD-NPU	P	N/A	N/A	N/A	N/A
R20	VDD-NPU	P	N/A	N/A	N/A	N/A
T18	VDD-NPUFB	P	N/A	N/A	N/A	N/A
L14	VDD-SYS	P	N/A	N/A	N/A	N/A
L15	VDD-SYS	P	N/A	N/A	N/A	N/A
N14	VDD-SYS	P	N/A	N/A	N/A	N/A

Ball#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
N15	VDD-SYS	P	N/A	N/A	N/A	N/A
R15	VDD-SYS	P	N/A	N/A	N/A	N/A
T15	VDD-SYS	P	N/A	N/A	N/A	N/A
L13	VDD-SYSFB	P	N/A	N/A	N/A	N/A
L19	VDD-VE	P	N/A	N/A	N/A	N/A

4.1.12 Ground

Table 4-24 Ground Pin Characteristics

Ball#[1]	Pin Name[2]	Type[3]
A1, A2, A28, A29, B1, B2, B29, C3, C5, C11, C13, C15, C17, C19, C21, C23, C25, D3, F3, F15, F17, F19, F23, F25, G15, G21, H3, H7, H9, H11, H17, H21, J15, J17, J19, J20, K7, K9, K13, K18, K19, K24, K25, L2, L11, L16, L17, L18, M8, M12, M16, N13, N16, N21, N22, P12, P16, P22, P25, R16, T1, T8, T17, T20, T22, T23, T28, U14, U15, U16, U18, U19, V22, V24, Y6, Y8, Y9, Y17, Y18, Y19, Y23, Y24, AA8, AA9, AA11, AA13, AA15, AA17, AA19, AB4, AB5, AB6, AB7, AB13, AB19, AB23, AC1, AC7, AC19, AD25, AE1, AE7, AE9, AE11, AE13, AE15, AE17, AE19, AE27, AF5, AF26, AG23, AG27, AH1, AH29, AJ1, AJ2, AJ5, AJ7, AJ9, AJ11, AJ13, AJ15, AJ17, AJ19, AJ21, AJ28, AJ29, L27, M25, M26, M27, M28, N27, N28, N29, P26, P27	GND	G

4.1.13 Others

Table 4-25 Unconnected Pin List

Ball#[1]	Pin Name[2]	Type[3]
G19, AD26	NC	N/A

4.2 GPIO Multiplex Function

The following tables provide a description of the GPIO multiplex function.

NOTE

For each GPIO, Function0 is input function; Function1 is output function; Function7 to Function13 are reserved.

4.2.1 Port A

Table 4-26 Port A Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PA0	I/O	GPADC0-0						PA-EINT0
PA1	I/O	GPADC0-1						PA-EINT1
PA2	I/O	GPADC0-2						PA-EINT2
PA3	I/O	GPADC0-3						PA-EINT3
PA4	I/O	GPADC0-4						PA-EINT4
PA5	I/O	GPADC0-5						PA-EINT5
PA6	I/O	GPADC0-6						PA-EINT6
PA7	I/O	GPADC0-7						PA-EINT7
PA8	I/O	GPADC0-8						PA-EINT8
PA9	I/O	GPADC0-9						PA-EINT9

4.2.2 Port B

Table 4-27 Port B Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PB0	I/O	UART2-TX	SPI4-CS0	JTAG-MS	PWM0-6		RJTAG-MS	PB-EINT0
PB1	I/O	UART2-RX	SPI4-CLK	JTAG-CK	PWM0-7		RJTAG-CK	PB-EINT1
PB2	I/O	UART2-RTS	SPI4-MOSI	JTAG-DO			RJTAG-DO	PB-EINT2
PB3	I/O	UART2-CTS	SPI4-MISO	JTAG-DI			RJTAG-DI	PB-EINT3
PB4	I/O	TWI1-SCK	I2S2-MCLK		PWM0-8	IR-RX0	UART8-TX	PB-EINT4
PB5	I/O	TWI1-SDA	I2S2-BCLK		PWM0-9	IR-RX1	UART8-RX	PB-EINT5
PB6	I/O		I2S2-LRCK		PWM1-0	IR-TX	UART8-RTS	PB-EINT6
PB7	I/O	OWA-IN	I2S2-DOUT0	I2S2-DIN1	PWM1-1	CAN1-TX0	UART8-CTS	PB-EINT7
PB8	I/O	OWA-OUT	I2S2-DIN0	I2S2-DOUT1	PWM0-0	CAN1-RX0	UART8-DCD	PB-EINT8
PB9	I/O	UART0-TX	I2S2-DIN2		I2S2-DOUT2	TWI0-SCK	UART8-DSR	PB-EINT9
PB10	I/O	UART0-RX	I2S2-DIN3	PWM0-1	I2S2-DOUT3	TWI0-SDA	UART8-DTR	PB-EINT10
PB11	I/O	TWI5-SCK	UART7-RTS	SPI1-CS0	PWM0-2		UART8-RI	PB-EINT11
PB12	I/O	TWI5-SDA	UART7-CTS	SPI1-CLK	PWM0-3			PB-EINT12
PB13	I/O	TWI4-SCK	UART7-TX	SPI1-MOSI	PWM0-4	IR-RX2		PB-EINT13
PB14	I/O	TWI4-SDA	UART7-RX	SPI1-MISO	PWM0-5	IR-RX3		PB-EINT14

4.2.3 Port C

Table 4-28 Port C Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PC0	I/O	NAND-WE	SDC2-DS					PC-EINT0
PC1	I/O	NAND-ALE	SDC2-RST					PC-EINT1
PC2	I/O	NAND-CLE		SPI0-MOSI	SPIF-MOSI			PC-EINT2
PC3	I/O	NAND-CE1		SPI0-CS0	SPIF-CS0			PC-EINT3

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PC4	I/O	NAND-CE0		SPI0-MISO	SPIF-MISO			PC-EINT4
PC5	I/O	NAND-RE	SDC2-CLK					PC-EINT5
PC6	I/O	NAND-RB0	SDC2-CMD					PC-EINT6
PC7	I/O	NAND-RB1		SPI0-CS1	SPIF-DQS			PC-EINT7
PC8	I/O	NAND-DQ7	SDC2-D3		SPIF-D7			PC-EINT8
PC9	I/O	NAND-DQ6	SDC2-D4		SPIF-D6			PC-EINT9
PC10	I/O	NAND-DQ5	SDC2-D0		SPIF-D5			PC-EINT10
PC11	I/O	NAND-DQ4	SDC2-D5		SPIF-D4			PC-EINT11
PC12	I/O	NAND-DQS		SPI0-CLK	SPIF-CLK			PC-EINT12
PC13	I/O	NAND-DQ3	SDC2-D1					PC-EINT13
PC14	I/O	NAND-DQ2	SDC2-D6					PC-EINT14
PC15	I/O	NAND-DQ1	SDC2-D2	SPI0-WP	SPIF-WP			PC-EINT15
PC16	I/O	NAND-DQ0	SDC2-D7	SPI0-HOLD	SPIF-HOLD			PC-EINT16

4.2.4 Port D

Table 4-29 Port D Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PD0	I/O	LCD-D2	LVDS0-D0P	DSI-D0P	PWM0-0		UART9-TX	PD-EINT0
PD1	I/O	LCD-D3	LVDS0-D0N	DSI-D0N	PWM0-1		UART9-RX	PD-EINT1
PD2	I/O	LCD-D4	LVDS0-D1P	DSI-D1P	PWM0-2		UART9-RTS	PD-EINT2
PD3	I/O	LCD-D5	LVDS0-D1N	DSI-D1N	PWM0-3		UART9-CTS	PD-EINT3
PD4	I/O	LCD-D6	LVDS0-D2P	DSI-CKP	PWM0-4		UART10-TX	PD-EINT4
PD5	I/O	LCD-D7	LVDS0-D2N	DSI-CKN	PWM0-5		UART10-RX	PD-EINT5
PD6	I/O	LCD-D10	LVDS0-CKP	DSI-D2P	PWM0-6		UART10-RTS	PD-EINT6
PD7	I/O	LCD-D11	LVDS0-CKN	DSI-D2N	PWM0-7		UART10-CTS	PD-EINT7
PD8	I/O	LCD-D12	LVDS0-D3P	DSI-D3P	PWM0-8		CAN1-TX0	PD-EINT8
PD9	I/O	LCD-D13	LVDS0-D3N	DSI-D3N	PWM0-9		CAN1-RX0	PD-EINT9
PD10	I/O	LCD-D14	LVDS1-D0P	SPI1-CS0/DBI-CSX	PWM1-0	TWI6-SCK	UART8-TX	PD-EINT10
PD11	I/O	LCD-D15	LVDS1-D0N	SPI1-CLK/DBI-SCLK	PWM1-1	TWI6-SDA	UART8-RX	PD-EINT11
PD12	I/O	LCD-D18	LVDS1-D1P	SPI1-MOSI/DBI-SDO	PWM1-2		UART8-RTS	PD-EINT12
PD13	I/O	LCD-D19	LVDS1-D1N	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PWM1-3		UART8-CTS	PD-EINT13
PD14	I/O	LCD-D20	LVDS1-D2P	SPI1-HOLD/DBI-DCX/DBI-WRX	PWM1-4	UART3-TX	UART8-DCD	PD-EINT14
PD15	I/O	LCD-D21	LVDS1-D2N	SPI1-WP/DBI-TE	PWM1-5	UART3-RX	UART8-DSR	PD-EINT15
PD16	I/O	LCD-D22	LVDS1-CKP	CAN2-TX0	PWM1-6	UART3-RTS	UART8-DTR	PD-EINT16
PD17	I/O	LCD-D23	LVDS1-CKN	CAN2-RX0	PWM1-7	UART3-CTS	UART8-RI	PD-EINT17
PD18	I/O	LCD-CLK	LVDS1-D3P	TWI6-SCK	PWM1-8		CAN0-TX0	PD-EINT18
PD19	I/O	LCD-DE	LVDS1-D3N	TWI6-SDA	PWM1-9		CAN0-RX0	PD-EINT19
PD20	I/O	LCD-HSYNC	PWM0-2	UART2-TX	TWI5-SCK			PD-EINT20
PD21	I/O	LCD-VSYNC	PWM0-3	UART2-RX	TWI5-SDA			PD-EINT21
PD22	I/O		PWM0-1	UART2-RTS	TWI4-SCK	TWI0-SCK		PD-EINT22
PD23	I/O		PWM0-0	UART2-CTS	TWI4-SDA	TWI0-SDA		PD-EINT23

4.2.5 Port E

Table 4-30 Port E Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PE0	I/O	MCSI0-MCLK(1)				SPI3-CS0	LBUS-CS0	PE-EINT0
PE1	I/O	TWI2-SCK	UART4-TX			SPI3-CLK	LBUS-CS1	PE-EINT1
PE2	I/O	TWI2-SDA	UART4-RX			SPI3-MOSI	LBUS-CS2	PE-EINT2
PE3	I/O	TWI3-SCK	UART4-RTS	CSI0-XHS		SPI3-MISO	LBUS-CS3	PE-EINT3
PE4	I/O	TWI3-SDA	UART4-CTS	CSI1-XHS		SPI3-WP	LBUS-DP0	PE-EINT4
PE5	I/O	MCSI1-MCLK			LEDC	SPI3-HOLD	LBUS-DP1	PE-EINT5
PE6	I/O		UART12-TX	TWI2-SCK	TCON-FSYNC0		LBUS-DP2	PE-EINT6
PE7	I/O		UART12-RX	TWI2-SDA	CLK-FANOUT0		LBUS-DP3	PE-EINT7
PE8	I/O		UART12-RTS	NCSI-D0	CLK-FANOUT1		LBUS-WR	PE-EINT8
PE9	I/O		UART12-CTS	NCSI-D1		SPI2-CS0	LBUS-READY	PE-EINT9
PE10	I/O	MCSI3-MCLK	PWM0-3	NCSI-D2		SPI2-CLK	LBUS-ALE	PE-EINT10
PE11	I/O	TWI1-SCK	UART5-RTS	NCSI-D3	UART6-TX	SPI2-MOSI	LBUS-BURST0	PE-EINT11
PE12	I/O	TWI1-SDA	UART5-CTS	NCSI-D4	UART6-RX	SPI2-MISO	LBUS-BURST1	PE-EINT12
PE13	I/O	TWI4-SCK	UART5-TX	NCSI-D5	UART6-RTS	SPI2-WP	LBUS-BURST2	PE-EINT13
PE14	I/O	TWI4-SDA	UART5-RX	NCSI-D6	UART6-CTS	SPI2-HOLD	LBUS-LCLK	PE-EINT14
PE15	I/O	MCSI2-MCLK	PWM0-2	NCSI-D7		CAN2-TX0	LBUS-INTR	PE-EINT15
PE16	I/O	TWI6-SCK	PWM0-4	CSI0-XVS-FSYNC	TWI0-SCK	CAN2-RX0	LBUS-DRQ	PE-EINT16
PE17	I/O	TWI6-SDA	PWM0-5	CSI1-XVS-FSYNC	TWI0-SDA		LBUS-LBE	PE-EINT17

4.2.6 Port F

Table 4-31 Port F Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PF0	I/O	SDC0-D1	JTAG-MS		I2S3-DIN0	I2S3-DOUT1	RJTAG-MS	PF-EINT0
PF1	I/O	SDC0-D0	JTAG-DI		I2S3-DOUT0	I2S3-DIN1	RJTAG-DI	PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX		I2S3-DIN2	SPI4-CLK	I2S3-DOUT2	PF-EINT2
PF3	I/O	SDC0-CMD	JTAG-DO		I2S3-LRCK	SPI4-CS0	RJTAG-DO	PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX		I2S3-DIN3	SPI4-MOSI	I2S3-DOUT3	PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK		I2S3-BCLK	SPI4-MISO	RJTAG-CK	PF-EINT5
PF6	I/O				I2S3-MCLK			PF-EINT6

4.2.7 Port G

Table 4-32 Port G Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PG0	I/O	SDC1-CLK		UART13-TX				PG-EINT0
PG1	I/O	SDC1-CMD		UART13-RX				PG-EINT1
PG2	I/O	SDC1-D0	PCIE-PERSTN	UART13-RTS				PG-EINT2
PG3	I/O	SDC1-D1	PCIE-WAKEN	UART13-CTS				PG-EINT3
PG4	I/O	SDC1-D2	PCIE-CLKREQN					PG-EINT4
PG5	I/O	SDC1-D3						PG-EINT5
PG6	I/O	UART1-TX	TWI6-SCK					PG-EINT6
PG7	I/O	UART1-RX	TWI6-SDA					PG-EINT7
PG8	I/O	UART1-RTS	TWI5-SCK					PG-EINT8
PG9	I/O	UART1-CTS	TWI5-SDA					PG-EINT9

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PG10	I/O	UART14-TX	I2S1-MCLK	TWI2-SCK				PG-EINT10
PG11	I/O	UART14-RX	I2S1-BCLK	TWI2-SDA				PG-EINT11
PG12	I/O	UART14-RTS	I2S1-LRCK		CAN3-TX0			PG-EINT12
PG13	I/O	UART14-CTS	I2S1-DOUT0	I2S1-DIN1	CAN3-RX0			PG-EINT13
PG14	I/O		I2S1-DIN0	I2S1-DOUT1				PG-EINT14

4.2.8 Port H

Table 4-33 Port H Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PH0	I/O	TWI0-SCK	PWM2-4	UART1-TX	CAN1-TX0		LBUS-LD24	PH-EINT0
PH1	I/O	TWI0-SDA	PWM2-5	UART1-RX	CAN1-RX0		LBUS-LD25	PH-EINT1
PH2	I/O	TWI1-SCK		UART1-RTS	CLK-FANOUT0		LBUS-LD26	PH-EINT2
PH3	I/O	TWI1-SDA	IR-TX	UART1-CTS	CLK-FANOUT1		LBUS-LD27	PH-EINT3
PH4	I/O	UART3-TX	SPI3-CS0		PWM1-4	DMIC-CLK	LBUS-LD28	PH-EINT4
PH5	I/O	UART3-RX	SPI3-CLK	LEDC	PCIE-PERSTN	DMIC-DATA0	LBUS-LD29	PH-EINT5
PH6	I/O	UART3-RTS	SPI3-MOSI	TWI6-SCK	PCIE-WAKEN	DMIC-DATA1	LBUS-LD30	PH-EINT6
PH7	I/O	UART3-CTS	SPI3-MISO	TWI6-SDA	PCIE-CLKREQN	DMIC-DATA2	LBUS-LD31	PH-EINT7
PH8	I/O	PWM2-6	SPI3-WP	OWA-IN	LCD-D0	DMIC-DATA3	TWI3-SCK	PH-EINT8
PH9	I/O	PWM2-7	SPI3-HOLD	I2S3-MCLK	LCD-D1		TWI3-SDA	PH-EINT9
PH10	I/O	PWM2-8		I2S3-BCLK	LCD-D8	CAN3-TX0		PH-EINT10
PH11	I/O	IR-RX3	PWM2-9	I2S3-LRCK	LCD-D9	CAN3-RX0		PH-EINT11
PH12	I/O	IR-RX1	I2S3-DOUT0	I2S3-DIN1	LCD-D16	CAN2-TX0	UART11-TX	PH-EINT12
PH13	I/O	IR-RX2	I2S3-DOUT1	I2S3-DIN0	LCD-D17	CAN2-RX0	UART11-RX	PH-EINT13
PH14	I/O	IR-TX	I2S3-DOUT2	I2S3-DIN2	PWM1-5		UART11-RTS	PH-EINT14
PH15	I/O	IR-RX0	I2S3-DOUT3	I2S3-DIN3	LEDC		UART11-CTS	PH-EINT15

4.2.9 Port I

Table 4-34 Port I Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PI0	I/O	I2S0-BCLK		CAN0-TX0				PI-EINT0
PI1	I/O	I2S0-LRCK		CAN0-RX0				PI-EINT1
PI2	I/O	I2S0-DIN0	UART9-TX	CAN3-TX0				PI-EINT2
PI3	I/O	I2S0-MCLK	UART9-RX	CAN3-RX0				PI-EINT3
PI4	I/O	TWI5-SCK	UART9-CTS					PI-EINT4
PI5	I/O	TWI5-SDA	UART9-RTS					PI-EINT5
PI6	I/O	UART6-TX	SPI2-CS0	PWM2-0	I2S0-MCLK	LEDC	CLK-FANOUT0	PI-EINT6
PI7	I/O	UART6-RX	SPI2-CLK	PWM2-1	I2S0-DIN2	I2S0-DOUT2	CLK-FANOUT1	PI-EINT7
PI8	I/O	UART6-CTS	SPI2-MOSI	PWM2-2	I2S0-BCLK	CAN2-TX0		PI-EINT8
PI9	I/O	UART6-RTS	SPI2-MISO	PWM2-3	I2S0-LRCK	CAN2-RX0	IR-TX	PI-EINT9
PI10	I/O	OWA-OUT	SPI2-WP	PWM2-7	I2S0-DOUT0	I2S0-DIN1	PCIE-PERSTN	PI-EINT10
PI11	I/O	TWI3-SCK	SPI2-HOLD	PWM2-8	I2S0-DIN0	I2S0-DOUT1	PCIE-WAKEN	PI-EINT11
PI12	I/O	TWI3-SDA	PWM2-4	DMIC-CLK	I2S0-DIN3	I2S0-DOUT3	PCIE-CLKREQN	PI-EINT12
PI13	I/O	UART4-TX	PWM2-5	DMIC-DATA0		IR-RX0	I2S3-BCLK	PI-EINT13
PI14	I/O	UART4-RX	PWM2-6	DMIC-DATA1		IR-RX1	I2S3-LRCK	PI-EINT14
PI15	I/O	UART4-RTS	TWI2-SCK	DMIC-DATA2	CAN0-TX0	IR-RX2	I2S3-DIN0	PI-EINT15
PI16	I/O	UART4-CTS	TWI2-SDA	DMIC-DATA3	CAN0-RX0	IR-RX3	I2S3-MCLK	PI-EINT16

4.2.10 Port J

Table 4-35 Port J Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PJ0	I/O	PWM0-0	I2S2-MCLK		RGMII0-RXD1/RMII0-RXD1			PJ-EINT0
PJ1	I/O	PWM0-1	I2S2-BCLK		RGMII0-RXD0/RMII0-RXD0			PJ-EINT1
PJ2	I/O	PWM0-2	I2S2-LRCK		RGMII0-RXCTL/RMII0-CRS-DV			PJ-EINT2
PJ3	I/O	PWM0-3	I2S2-DOUT0	I2S2-DIN1	RGMII0-CLKIN/RMII0-RXER			PJ-EINT3
PJ4	I/O	PWM0-4	I2S2-DIN0	I2S2-DOUT1	RGMII0-TXD1/RMII0-TXD1			PJ-EINT4
PJ5	I/O	PWM0-5	I2S2-DIN2	I2S2-DOUT2	RGMII0-TXD0/RMII0-TXD0			PJ-EINT5
PJ6	I/O	PWM0-6	I2S2-DIN3	I2S2-DOUT3	RGMII0-TXCK/RMII0-TXCK			PJ-EINT6
PJ7	I/O	PWM0-7	I2S1-MCLK		RGMII0-TXCTL/RMII0-TXEN			PJ-EINT7
PJ8	I/O	PWM0-8	I2S1-BCLK		RGMII0-MDC			PJ-EINT8
PJ9	I/O	PWM0-9	I2S1-LRCK		RGMII0-MDIO			PJ-EINT9
PJ10	I/O	PWM2-0	I2S1-DOUT0	I2S1-DIN1	RGMII0-EPHY-25/50M			PJ-EINT10
PJ11	I/O	PWM2-1	I2S1-DIN0	I2S1-DOUT1	RGMII0-RXD3/RMII0-NULL			PJ-EINT11
PJ12	I/O	PWM2-2	UART10-TX		RGMII0-RXD2/RMII0-NULL			PJ-EINT12
PJ13	I/O	PWM2-3	UART10-RX		RGMII0-RXCK/RMII0-NULL			PJ-EINT13
PJ14	I/O	PWM2-4	UART10-RTS	TWI6-SCK	RGMII0-TXD3/RMII0-NULL			PJ-EINT14
PJ15	I/O	PWM2-5	UART10-CTS	TWI6-SDA	RGMII0-TXD2/RMII0-NULL			PJ-EINT15
PJ16	I/O	PWM2-6		IR-RX0	RGMII1-RXD1/RMII1-RXD1			PJ-EINT16
PJ17	I/O	PWM2-7		IR-RX1	RGMII1-RXD0/RMII1-RXD0			PJ-EINT17
PJ18	I/O	PWM2-8		IR-RX2	RGMII1-RXCTL/RMII1-CRS-DV			PJ-EINT18
PJ19	I/O	PWM2-9		IR-RX3	RGMII1-CLKIN/RMII1-RXER			PJ-EINT19
PJ20	I/O	TWI0-SCK	UART14-TX		RGMII1-TXD1/RMII1-TXD1			PJ-EINT20
PJ21	I/O	TWI0-SDA	UART14-RX		RGMII1-TXD0/RMII1-TXD0			PJ-EINT21
PJ22	I/O		UART14-RTS	IR-TX	RGMII1-TXCK/RMII1-TXCK			PJ-EINT22
PJ23	I/O		UART14-CTS		RGMII1-TXCTL/RMII1-TXEN			PJ-EINT23
PJ24	I/O	PWM2-0	TWI4-SCK	UART13-RTS	RGMII1-MDC			PJ-EINT24
PJ25	I/O	PWM2-1	TWI4-SDA	UART13-CTS	RGMII1-MDIO			PJ-EINT25
PJ26	I/O	PWM2-2	TWI5-SCK	UART13-TX	RGMII1-EPHY-25/50M			PJ-EINT26
PJ27	I/O	PWM2-3	TWI5-SDA	UART13-RX	RGMII1-RXD3/RMII1-NULL			PJ-EINT27
PJ28	I/O		TWI1-SCK		RGMII1-RXD2/RMII1-NULL			PJ-EINT28
PJ29	I/O		TWI1-SDA		RGMII1-RXCK/RMII1-NULL			PJ-EINT29
PJ30	I/O				RGMII1-TXD3/RMII1-NULL			PJ-EINT30
PJ31	I/O				RGMII1-TXD2/RMII1-NULL			PJ-EINT31

4.2.11 Port K

Table 4-36 Port K Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PK0	I/O	MCSIA-D0N		UART11-TX		SPI2-CS0	LBUS-LD0	PK-EINT0
PK1	I/O	MCSIA-D0P		UART11-RX		SPI2-CLK	LBUS-LD1	PK-EINT1
PK2	I/O	MCSIA-D1N	TWI2-SCK	UART11-RTS		SPI2-MOSI	LBUS-LD2	PK-EINT2
PK3	I/O	MCSIA-D1P	TWI2-SDA	UART11-CTS		SPI2-MISO	LBUS-LD3	PK-EINT3
PK4	I/O	MCSIA-CKN		UART12-TX	NCSI-D0	SPI2-WP	LBUS-LD4	PK-EINT4
PK5	I/O	MCSIA-CKP		UART12-RX	NCSI-D1	SPI2-HOLD	LBUS-LD5	PK-EINT5
PK6	I/O	MCSIB-D0N		UART12-RTS	NCSI-D2		LBUS-LD6	PK-EINT6

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PK7	I/O	MCSIB-D0P		UART12-CTS	NCSI-D3		LBUS-LD7	PK-EINT7
PK8	I/O	MCSIB-D1N		CAN1-TX0	NCSI-D4		LBUS-LD8	PK-EINT8
PK9	I/O	MCSIB-D1P	MCSI3-MCLK	CAN1-RX0	NCSI-D5		LBUS-LD9	PK-EINT9
PK10	I/O	MCSIB-CKN	TWI1-SCK	CAN0-TX0	NCSI-D6		LBUS-LD10	PK-EINT10
PK11	I/O	MCSIB-CKP	TWI1-SDA	CAN0-RX0	NCSI-D7		LBUS-LD11	PK-EINT11
PK12	I/O	MCSIC-D0N	UART7-TX	TWI1-SCK	NCSI-D8		LBUS-LD12	PK-EINT12
PK13	I/O	MCSIC-D0P	UART7-RX	TWI1-SDA	NCSI-D9		LBUS-LD13	PK-EINT13
PK14	I/O	MCSIC-D1N	UART7-RTS	UART5-RTS	NCSI-D10	SPI3-CS0	LBUS-LD14	PK-EINT14
PK15	I/O	MCSIC-D1P	UART7-CTS	UART5-CTS	NCSI-D11	SPI3-CLK	LBUS-LD15	PK-EINT15
PK16	I/O	MCSIC-CKN	TWI4-SCK	UART5-TX	NCSI-D12	SPI3-MOSI	LBUS-LD16	PK-EINT16
PK17	I/O	MCSIC-CKP	TWI4-SDA	UART5-RX	NCSI-D13	SPI3-MISO	LBUS-LD17	PK-EINT17
PK18	I/O	MCSID-D0N	MCSI0-MCLK	UART6-TX	NCSI-D14	SPI3-WP	LBUS-LD18	PK-EINT18
PK19	I/O	MCSID-D0P	TWI2-SCK	UART6-RX	NCSI-D15	SPI3-HOLD	LBUS-LD19	PK-EINT19
PK20	I/O	MCSID-D1N	TWI2-SDA	UART6-RTS	NCSI-PCLK		LBUS-LD20	PK-EINT20
PK21	I/O	MCSID-D1P	MCSI1-MCLK	UART6-CTS	NCSI-MCLK		LBUS-LD21	PK-EINT21
PK22	I/O	MCSID-CKN	TWI3-SCK	PWM0-6	NCSI-HSYNC	CAN3-TX0	LBUS-LD22	PK-EINT22
PK23	I/O	MCSID-CKP	TWI3-SDA	PWM0-7	NCSI-VSYNC	CAN3-RX0	LBUS-LD23	PK-EINT23

4.2.12 Port L

Table 4-37 Port L Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PL0	I/O	S-TWI0-SCK						PL-EINT0
PL1	I/O	S-TWI0-SDA						PL-EINT1
PL2	I/O	S-UART0-TX	S-IR-RX	S-PWM0-2				PL-EINT2
PL3	I/O	S-UART0-RX		S-PWM0-3				PL-EINT3
PL4	I/O	S-JTAG-MS	S-UART1-TX	S-IR-RX				PL-EINT4
PL5	I/O	S-JTAG-CK	S-UART1-RX					PL-EINT5
PL6	I/O	S-JTAG-DO	S-UART1-RTS					PL-EINT6
PL7	I/O	S-JTAG-DI	S-UART1-CTS					PL-EINT7
PL8	I/O	S-TWI1-SCK		S-RJTAG-MS				PL-EINT8
PL9	I/O	S-TWI1-SDA		S-RJTAG-CK	S-PWM0-1			PL-EINT9
PL10	I/O	S-PWM0-0	S-UART0-TX			S-SPI0-CS0		PL-EINT10
PL11	I/O	S-IR-RX	S-UART0-RX			S-SPI0-CLK		PL-EINT11
PL12	I/O	S-PWM0-1	S-UART0-RTS			S-SPI0-MOSI		PL-EINT12
PL13	I/O	S-PWM0-3	S-UART0-CTS			S-SPI0-MISO		PL-EINT13

4.2.13 Port M

Table 4-38 Port M Multiplex Function

Pin Name	IO Type	Function2	Function3	Function4	Function5	Function6	Function7	Function14
PM0	I/O	S-TWI0-SCK	S-UART1-TX	S-PWM0-0				PM-EINT0
PM1	I/O	S-TWI0-SDA	S-UART1-RX	S-PWM0-1				PM-EINT1
PM2	I/O	S-TWI1-SCK	S-UART1-RTS	S-UART0-TX				PM-EINT2
PM3	I/O	S-TWI1-SDA	S-UART1-CTS	S-UART0-RX				PM-EINT3
PM4	I/O		S-PWM0-2	S-UART0-RTS				PM-EINT4
PM5	I/O	S-IR-RX	S-PWM0-3	S-UART0-CTS				PM-EINT5

4.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name**: The name of every signal.

[2] **Description**: The detailed function description of every signal.

[3] **Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

4.3.1 SDRAM

Table 4-39 SDRAM Signal Description

Signal Name[1]	Description[2]	Type[3]
SRST	DRAM Reset Signal	O
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
SA0	DRAM Address Signal 0	O
SA1	DRAM Address Signal 1	O
SA2	DRAM Address Signal 2	O
SA3	DRAM Address Signal 3	O
SA4	DRAM Address Signal 4	O
SA5	DRAM Address Signal 5	O
SA6	DRAM Address Signal 6	O
SA7	DRAM Address Signal 7	O
SA8	DRAM Address Signal 8	O

Signal Name[1]	Description[2]	Type[3]
SA9	DRAM Address Signal 9	O
SA10	DRAM Address Signal 10	O
SA11	DRAM Address Signal 11	O
SA12	DRAM Address Signal 12	O
SA13	DRAM Address Signal 13	O
SA14	DRAM Address Signal 14	O
SA15	DRAM Address Signal 15	O
SA16	DRAM Address Signal 16	O
SA17	DRAM Address Signal 17	O
SACT	DRAM Activation Command Output	O
SBA0	DRAM Bank Address Signal 0	O
SBA1	DRAM Bank Address Signal 1	O
SBG0	DRAM Bank Group Address Signal 0	O
SBG1	DRAM Bank Group Address Signal 1	O
SCKE0	DRAM Clock Enable Signal 0	O
SCKN	DRAM Differential Clock (Negative)	O
SCKP	DRAM Differential Clock (Positive)	O
SCS0	DRAM Chip Select Signal 0	O
SCS1	DRAM Chip Select Signal 1	O
SDQM0	DRAM Data Mask Signal	I/O
SDQM1	DRAM Data Mask Signal	I/O
SDQM2	DRAM Data Mask Signal	I/O
SDQM3	DRAM Data Mask Signal	I/O
SDQ0	DRAM Bidirectional Data Line 0	I/O
SDQ1	DRAM Bidirectional Data Line 1	I/O
SDQ2	DRAM Bidirectional Data Line 2	I/O
SDQ3	DRAM Bidirectional Data Line 3	I/O
SDQ4	DRAM Bidirectional Data Line 4	I/O
SDQ5	DRAM Bidirectional Data Line 5	I/O
SDQ6	DRAM Bidirectional Data Line 6	I/O

Signal Name[1]	Description[2]	Type[3]
SDQ7	DRAM Bidirectional Data Line 7	I/O
SDQ8	DRAM Bidirectional Data Line 8	I/O
SDQ9	DRAM Bidirectional Data Line 9	I/O
SDQ10	DRAM Bidirectional Data Line 10	I/O
SDQ11	DRAM Bidirectional Data Line 11	I/O
SDQ12	DRAM Bidirectional Data Line 12	I/O
SDQ13	DRAM Bidirectional Data Line 13	I/O
SDQ14	DRAM Bidirectional Data Line 14	I/O
SDQ15	DRAM Bidirectional Data Line 15	I/O
SDQ16	DRAM Bidirectional Data Line 16	I/O
SDQ17	DRAM Bidirectional Data Line 17	I/O
SDQ18	DRAM Bidirectional Data Line 18	I/O
SDQ19	DRAM Bidirectional Data Line 19	I/O
SDQ20	DRAM Bidirectional Data Line 20	I/O
SDQ21	DRAM Bidirectional Data Line 21	I/O
SDQ22	DRAM Bidirectional Data Line 22	I/O
SDQ23	DRAM Bidirectional Data Line 23	I/O
SDQ24	DRAM Bidirectional Data Line 24	I/O
SDQ25	DRAM Bidirectional Data Line 25	I/O
SDQ26	DRAM Bidirectional Data Line 26	I/O
SDQ27	DRAM Bidirectional Data Line 27	I/O
SDQ28	DRAM Bidirectional Data Line 28	I/O
SDQ29	DRAM Bidirectional Data Line 29	I/O
SDQ30	DRAM Bidirectional Data Line 30	I/O
SDQ31	DRAM Bidirectional Data Line 31	I/O
SDQS0N	DRAM Bidirectional Data Strobe 0 (Active Low)	I/O
SDQS0P	DRAM Bidirectional Data Strobe 0 (Active-High)	I/O
SDQS1N	DRAM Bidirectional Data Strobe 1 (Active Low)	I/O
SDQS1P	DRAM Bidirectional Data Strobe 1 (Active-High)	I/O
SDQS2N	DRAM Bidirectional Data Strobe 2 (Active Low)	I/O

Signal Name[1]	Description[2]	Type[3]
SDQS2P	DRAM Bidirectional Data Strobe 2 (Active-High)	I/O
SDQS3N	DRAM Bidirectional Data Strobe 3 (Active Low)	I/O
SDQS3P	DRAM Bidirectional Data Strobe 3 (Active-High)	I/O
SODT0	DRAM On-Die Termination Output Signal 0	O
SODT1	DRAM On-Die Termination Output Signal 1	O
VCC-DRAM	DRAM IO Power Supply	P
VCC-DRAML	LPDDR4x Power Supply	P
VDD18-DRAM	SDRAM Controller Power Supply	P

4.3.2 Raw NAND Flash

Table 4-40 Raw NAND Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
NAND-WE	NAND Flash Write Enable	O
NAND-ALE	NAND Flash Address Latch Enable	O
NAND-CLE	NAND Flash Command latch Enable	O
NAND-CE0	NAND Flash Chip Select 0	O
NAND-CE1	NAND Flash Chip Select 1	O
NAND-RE	NAND Flash Read Enable	O
NAND-RB0	NAND Flash Ready/Busy Status Indicator Signal 0	I
NAND-RB1	NAND Flash Ready/Busy Status Indicator Signal 1	I
NAND-DQ0	NAND Flash Data Bit 0	I/O
NAND-DQ1	NAND Flash Data Bit 1	I/O
NAND-DQ2	NAND Flash Data Bit 2	I/O
NAND-DQ3	NAND Flash Data Bit 3	I/O
NAND-DQ4	NAND Flash Data Bit 4	I/O
NAND-DQ5	NAND Flash Data Bit 5	I/O
NAND-DQ6	NAND Flash Data Bit 6	I/O
NAND-DQ7	NAND Flash Data Bit 7	I/O
NAND-DQS	NAND Flash Data Strobe	I/O

4.3.3 System Control

Table 4-41 System Control Signal Description

Signal Name[1]	Description[2]	Type[3]
FEL	The signal is used to force this chip into download mode (Active Low).	I
JTAG-SEL	JTAG mode select The signal is used to select the port from which JTAG function outputs.	I
NMI	Non-Maskable Interrupt	I/O, OD
RESET	SoC Reset Signal (Active Low)	I/O, OD

4.3.4 RTC&PLL

Table 4-42 RTC&PLL Signal Description

Signal Name[1]	Description[2]	Type[3]
X32KFOUT	32.768 kHz Clock Fanout Provides low frequency clock for external devices	AO,OD
X32KIN	32.768 kHz Crystal Clock Input	AI
X32KOUT	32.768 kHz Crystal Clock Output	AO
PLLTEST	PLL Test Signal	AO, OD
CPU-PLLTEST	CPU PLL Test Signal	AO, OD
VCC-CPU-PLL	CPU PLL Power Supply	P
VCC-RTC	RTC Power Supply	P
VCC-PLL	System PLL Supply	P

4.3.5 DCXO

Table 4-43 DCXO Signal Description

Signal Name[1]	Description[2]	Type[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO

4.3.6 Clock Fanout

Table 4-44 Clock Fanout Signal Description

Signal Name[1]	Description[2]	Type[3]
CLK-FANOUT0	Internal Clock Fanout Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, 50 MHz	O
CLK-FANOUT1	Internal Clock Fanout Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, 50 MHz	O

4.3.7 SD Card/SDIO/eMMC

Table 4-45 SD Card/SDIO/eMMC Signal Description

Signal Name[1]	Description[2]	Type[3]
SDC0-CMD	SD Card Command Output/Response Input	I/O, OD
SDC0-CLK	SD Card Clock Output	O
SDC0-D0	SD Card Data Input/ Output 0	I/O
SDC0-D1	SD Card Data Input/ Output 1	I/O
SDC0-D2	SD Card Data Input/ Output 2	I/O
SDC0-D3	SD Card Data Input/ Output 3	I/O
SDC1-CMD	SDIO WIFI Command Output/Response Input	I/O, OD
SDC1-CLK	SDIO WIFI Clock Output	O
SDC1-D0	SDIO WIFI Data Input/ Output 0	I/O
SDC1-D1	SDIO WIFI Data Input/ Output 1	I/O
SDC1-D2	SDIO WIFI Data Input/ Output 2	I/O
SDC1-D3	SDIO WIFI Data Input/ Output 3	I/O
SDC2-CMD	eMMC Command Output/Response Input	I/O, OD
SDC2-CLK	eMMC Clock Output	O
SDC2-D0	eMMC Data Input/ Output 0	I/O
SDC2-D1	eMMC Data Input/ Output 1	I/O
SDC2-D2	eMMC Data Input/ Output 2	I/O
SDC2-D3	eMMC Data Input/ Output 3	I/O
SDC2-D4	eMMC Data Input/ Output 4	I/O

Signal Name[1]	Description[2]	Type[3]
SDC2-D5	eMMC Data Input/ Output 5	I/O
SDC2-D6	eMMC Data Input/ Output 6	I/O
SDC2-D7	eMMC Data Input/ Output 7	I/O
SDC2-RST	eMMC Reset	O
SDC2-DS	eMMC Data Strobe	I

4.3.8 SerDes

Table 4-46 SerDes Signal Description

Signal Name[1]	Description[2]	Type[3]
USB0-DM	USB0/USB2_U2 Differential Data (Negative)	A I/O
USB0-DP	USB0/USB2_U2 Differential Data (Positive)	A I/O
USB1-DM	USB1/USB2_U2 Differential Data (Negative)	A I/O
USB1-DP	USB1/USB2_U2 Differential Data (Positive)	A I/O
PCIE-REF-CLKN	SerDes Reference Clock Input/Output (Negative)	A I/O
PCIE-REF-CLKP	SerDes Reference Clock Input/Output (Positive)	A I/O
PCIE-RX0-DN/USB2-U3-RXN	SerDes Differential Receive Signal (Negative)	AI
PCIE-RX0-DP/USB2-U3-RXP	SerDes Differential Receive Signal (Positive)	AI
PCIE-TX0-DN/USB2-U3-TXN	SerDes Differential Transmit Signal (Negative)	AO
PCIE-TX0-DP/USB2-U3-TXP	SerDes Differential Transmit Signal (Positive)	AO
PCIE-REXT	Pin to Connect to External Calibration Resistor	A I/O
PCIE-PERSTN	PCIe2.1 Fundamental Reset	I/O
PCIE-WAKEN	PCIe2.1 Wake Up	I/O
PCIE-CLKREQN	PCIe2.1 Clock Request	I/O
VCC18-COMB	PCIe2.1 & USB3.1 Combo PHY 1.8V Power Supply	P
VCC33-USB0-USB1	USB2.0 DRD and USB 2.0 Host 3.3V Power Supply	P
VDD09-COMB	PCIe2.1 & USB3.1 Combo PHY 0.9V Power Supply	P
VDD09-USB0-USB1	USB2.0 DRD and USB 2.0 Host 0.9V Power Supply	P

4.3.9 I2S/PCM

Table 4-47 I2S/PCM Signal Description

Signal Name[1]	Description[2]	Type[3]
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S0-DIN0	I2S0/PCM0 Serial Data Input 0	I
I2S0-DIN1	I2S0/PCM0 Serial Data Input 1	I
I2S0-DIN2	I2S0/PCM0 Serial Data Input 2	I
I2S0-DIN3	I2S0/PCM0 Serial Data Input 3	I
I2S0-DOUT0	I2S0/PCM0 Serial Data Output 0	O
I2S0-DOUT1	I2S0/PCM0 Serial Data Output 1	O
I2S0-DOUT2	I2S0/PCM0 Serial Data Output 2	O
I2S0-DOUT3	I2S0/PCM0 Serial Data Output 3	O
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S1-DIN0	I2S1/PCM1 Serial Data Input 0	I
I2S1-DIN1	I2S1/PCM1 Serial Data Input 1	I
I2S1-DOUT0	I2S1/PCM1 Serial Data Output 0	O
I2S1-DOUT1	I2S1/PCM1 Serial Data Output 1	O
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S2-DIN0	I2S2/PCM2 Serial Data Input 0	I
I2S2-DIN1	I2S2/PCM2 Serial Data Input 1	I
I2S2-DIN2	I2S2/PCM2 Serial Data Input 2	I
I2S2-DIN3	I2S2/PCM2 Serial Data Input 3	I
I2S2-DOUT0	I2S2/PCM2 Serial Data Output 0	O
I2S2-DOUT1	I2S2/PCM2 Serial Data Output 1	O
I2S2-DOUT2	I2S2/PCM2 Serial Data Output 2	O

Signal Name[1]	Description[2]	Type[3]
I2S2-DOUT3	I2S2/PCM2 Serial Data Output 3	O
I2S3-MCLK	I2S3 Master Clock	O
I2S3-LRCK	I2S3/PCM3 Sample Rate Clock/Sync	I/O
I2S3-BCLK	I2S3/PCM3 Bit Rate Clock	I/O
I2S3-DIN0	I2S3/PCM3 Serial Data Input 0	I
I2S3-DIN1	I2S3/PCM3 Serial Data Input 1	I
I2S3-DIN2	I2S3/PCM3 Serial Data Input 2	I
I2S3-DIN3	I2S3/PCM3 Serial Data Input 3	I
I2S3-DOUT0	I2S3/PCM3 Serial Data Output 0	O
I2S3-DOUT1	I2S3/PCM3 Serial Data Output 1	O
I2S3-DOUT2	I2S3/PCM3 Serial Data Output 2	O
I2S3-DOUT3	I2S3/PCM3 Serial Data Output 3	O

4.3.10 Audio Codec

Table 4-48 Audio Codec Signal Description

Signal Name[1]	Description[2]	Type[3]
LINEOUTN	Lineout Differential Output (Negative)	AO
LINEOUTP	Lineout Differential Output (Positive)	AO
AVCC	Power Supply for Analog Part	P
VRA1	Internal Reference Voltage	AO
AGND	Analog Ground	G

4.3.11 DMIC

Table 4-49 DMIC Signal Description

Signal Name[1]	Description[2]	Type[3]
DMIC-CLK	Digital Microphone Clock Output	O
DMIC-DATA0	Digital Microphone Data Input 0	I
DMIC-DATA1	Digital Microphone Data Input 1	I
DMIC-DATA2	Digital Microphone Data Input 2	I
DMIC-DATA3	Digital Microphone Data Input 3	I

4.3.12 OWA

Table 4-50 OWA Signal Description

Signal Name[1]	Description[2]	Type[3]
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O

4.3.13 GPADC

Table 4-51 GPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
VCC18-VCM-ADC	Pin to Connect to External Capacitor	A I/O
GPADC0-0	General Purpose ADC0 Input 0	AI
GPADC0-1	General Purpose ADC0 Input 1	AI
GPADC0-2	General Purpose ADC0 Input 2	AI
GPADC0-3	General Purpose ADC0 Input 3	AI
GPADC0-4	General Purpose ADC0 Input 4	AI
GPADC0-5	General Purpose ADC0 Input 5	AI
GPADC0-6	General Purpose ADC0 Input 6	AI
GPADC0-7	General Purpose ADC0 Input 7	AI
GPADC0-8	General Purpose ADC0 Input 8	AI
GPADC0-9	General Purpose ADC0 Input 9	AI
GPADC1-0	General Purpose ADC1 Input 0	AI
GPADC1-1	General Purpose ADC1 Input 1	AI
GPADC1-2	General Purpose ADC1 Input 2	AI
GPADC1-3	General Purpose ADC1 Input 3	AI
BOOT-SEL-GPADC1-4	General Purpose ADC1 Input 4/Boot Media Select	AI
DDR-PARA-SEL-GPADC1-5	General Purpose ADC1 Input 5/DDR Parameter Select	AI
GPADC1-6	General Purpose ADC1 Input 6	AI
GPADC1-7	General Purpose ADC1 Input 7	AI
GPADC1-8	General Purpose ADC1 Input 8	AI
GPADC1-9	General Purpose ADC1 Input 9	AI
GPADC3-0	General Purpose ADC3 Input 0	AI

Signal Name[1]	Description[2]	Type[3]
VCC18-ADC	GPADC and LRADC Power Supply	P
AGND-ADC	Analog Ground	G

4.3.14 LRADC

Table 4-52 LRADC Signal Description

Signal Name[1]	Description[2]	Type[3]
LRADC	Low Rate ADC Input	AI

4.3.15 TPADC

Table 4-53 TPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
TP-X1	Touch Panel X1 Input	AI
TP-X2	Touch Panel X2 Input	AI
TP-Y1	Touch Panel Y1 Input	AI
TP-Y2	Touch Panel Y2 Input	AI

4.3.16 MIPI CSI

Table 4-54 MIPI CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
MCSI0-MCLK	MIPI CSI A Master Clock	O
MCSIA-CKN	MIPI CSI A Differential Receive Clock Signal (Negative)	AI
MCSIA-CKP	MIPI CSI A Differential Receive Clock Signal (Positive)	AI
MCSIA-D0N	MIPI CSI A Data Line 0 Input (Negative)	AI
MCSIA-D0P	MIPI CSI A Data Line 0 Input (Positive)	AI
MCSIA-D1N	MIPI CSI A Data Line 1 Input (Negative)	AI
MCSIA-D1P	MIPI CSI A Data Line 1 Input (Positive)	AI
MCSI1-MCLK	MIPI CSI B Master Clock	O
MCSIB-CKN	MIPI CSI B Differential Receive Clock Signal (Negative)	AI
MCSIB-CKP	MIPI CSI B Differential Receive Clock Signal (Positive)	AI
MCSIB-D0N	MIPI CSI B Data Line 0 Input (Negative)	AI
MCSIB-D0P	MIPI CSI B Data Line 0 Input (Positive)	AI

Signal Name[1]	Description[2]	Type[3]
MCSIB-D1N	MIPI CSI B Data Line 1 Input (Negative)	AI
MCSIB-D1P	MIPI CSI B Data Line 1 Input (Positive)	AI
MCSI2-MCLK	MIPI CSI C Master Clock	O
MCSIC-CKN	MIPI CSI C Differential Receive Clock Signal (Negative)	AI
MCSIC-CKP	MIPI CSI C Differential Receive Clock Signal (Positive)	AI
MCSIC-D0N	MIPI CSI C Data Line 0 Input (Negative)	AI
MCSIC-D0P	MIPI CSI C Data Line 0 Input (Positive)	AI
MCSIC-D1N	MIPI CSI C Data Line 1 Input (Negative)	AI
MCSIC-D1P	MIPI CSI C Data Line 1 Input (Positive)	AI
MCSI3-MCLK	MIPI CSI D Master Clock	O
MCSID-CKN	MIPI CSI D Differential Receive Clock Signal (Negative)	AI
MCSID-CKP	MIPI CSI D Differential Receive Clock Signal (Positive)	AI
MCSID-D0N	MIPI CSI D Data Line 0 Input (Negative)	AI
MCSID-D0P	MIPI CSI D Data Line 0 Input (Positive)	AI
MCSID-D1N	MIPI CSI D Data Line 1 Input (Negative)	AI
MCSID-D1P	MIPI CSI D Data Line 1 Input (Positive)	AI
CSI0-XHS	CSI Horizontal SYNC 0	O
CSI1-XHS	CSI Horizontal SYNC 1	O
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC 0	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC 1	I/O
VCC18-MCSI	MIPI CSI Power Supply	P

4.3.17 Parallel CSI

Table 4-55 Parallel CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
NCSI-PCLK	Parallel CSI Pixel Clock Input	I
NCSI-MCLK	Parallel CSI Master Clock Output	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous Input	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous Input	I
NCSI-D0	Parallel CSI Pixel Data 0	I
NCSI-D1	Parallel CSI Pixel Data 1	I

Signal Name[1]	Description[2]	Type[3]
NCSI-D2	Parallel CSI Pixel Data 2	I
NCSI-D3	Parallel CSI Pixel Data 3	I
NCSI-D4	Parallel CSI Pixel Data 4	I
NCSI-D5	Parallel CSI Pixel Data 5	I
NCSI-D6	Parallel CSI Pixel Data 6	I
NCSI-D7	Parallel CSI Pixel Data 7	I
NCSI-D8	Parallel CSI Pixel Data 8	I
NCSI-D9	Parallel CSI Pixel Data 9	I
NCSI-D10	Parallel CSI Pixel Data 10	I
NCSI-D11	Parallel CSI Pixel Data 11	I
NCSI-D12	Parallel CSI Pixel Data 12	I
NCSI-D13	Parallel CSI Pixel Data 13	I
NCSI-D14	Parallel CSI Pixel Data 14	I
NCSI-D15	Parallel CSI Pixel Data 15	I

4.3.18 LCD

Table 4-56 LCD Signal Description

Signal Name[1]	Description[2]	Type[3]
LCD-CLK	LCD Clock	O
LCD-VSYNC	LCD Vertical Synchronization	O
LCD-HSYNC	LCD Horizontal Synchronization	O
LCD-DE	LCD Data Enable	O
TCON-FSYNC0	Frame Synchronization Signal for TCON and Sensor	O
LCD-D0	LCD Data Input/Output 0	I/O
LCD-D1	LCD Data Input/Output 1	I/O
LCD-D2	LCD Data Input/Output 2	I/O
LCD-D3	LCD Data Input/Output 3	I/O
LCD-D4	LCD Data Input/Output 4	I/O
LCD-D5	LCD Data Input/Output 5	I/O
LCD-D6	LCD Data Input/Output 6	I/O
LCD-D7	LCD Data Input/Output 7	I/O

Signal Name[1]	Description[2]	Type[3]
LCD-D8	LCD Data Input/Output 8	I/O
LCD-D9	LCD Data Input/Output 9	I/O
LCD-D10	LCD Data Input/Output 10	I/O
LCD-D11	LCD Data Input/Output 11	I/O
LCD-D12	LCD Data Input/Output 12	I/O
LCD-D13	LCD Data Input/Output 13	I/O
LCD-D14	LCD Data Input/Output 14	I/O
LCD-D15	LCD Data Input/Output 15	I/O
LCD-D16	LCD Data Input/Output 16	I/O
LCD-D17	LCD Data Input/Output 17	I/O
LCD-D18	LCD Data Input/Output 18	I/O
LCD-D19	LCD Data Input/Output 19	I/O
LCD-D20	LCD Data Input/Output 20	I/O
LCD-D21	LCD Data Input/Output 21	I/O
LCD-D22	LCD Data Input/Output 22	I/O
LCD-D23	LCD Data Input/Output 23	I/O

4.3.19 LVDS

Table 4-57 LVDS Signal Description

Signal Name[1]	Description[2]	Type[3]
LVDS0-CKP	LVDS0 Differential Clock (Positive)	AO
LVDS0-CKN	LVDS0 Differential Clock (Negative)	AO
LVDS0-D0P	LVDS0 Differential Data 0 (Positive)	AO
LVDS0-D0N	LVDS0 Differential Data 0 (Negative)	AO
LVDS0-D1P	LVDS0 Differential Data 1 (Positive)	AO
LVDS0-D1N	LVDS0 Differential Data 1 (Negative)	AO
LVDS0-D2P	LVDS0 Differential Data 2 (Positive)	AO
LVDS0-D2N	LVDS0 Differential Data 2 (Negative)	AO
LVDS0-D3P	LVDS0 Differential Data 3 (Positive)	AO
LVDS0-D3N	LVDS0 Differential Data 3 (Negative)	AO
LVDS1-CKP	LVDS1 Differential Clock (Positive)	AO

Signal Name[1]	Description[2]	Type[3]
LVDS1-CKN	LVDS1 Differential Clock (Negative)	AO
LVDS1-D0P	LVDS1 Differential Data 0 (Positive)	AO
LVDS1-D0N	LVDS1 Differential Data 0 (Negative)	AO
LVDS1-D1P	LVDS1 Differential Data 1 (Positive)	AO
LVDS1-D1N	LVDS1 Differential Data 1 (Negative)	AO
LVDS1-D2P	LVDS1 Differential Data 2 (Positive)	AO
LVDS1-D2N	LVDS1 Differential Data 2 (Negative)	AO
LVDS1-D3P	LVDS1 Differential Data 3 (Positive)	AO
LVDS1-D3N	LVDS1 Differential Data 3 (Negative)	AO
VCC18-LVDS	LVDS0/1 Power Supply	P

4.3.20 MIPI DSI

Table 4-58 MIPI DSI Signal Description

Signal Name[1]	Description[2]	Type[3]
DSI-CKP	DSI Differential Clock (Positive)	AO
DSI-CKN	DSI Differential Clock (Negative)	AO
DSI-D0P	DSI Differential Data Line 0 (Positive)	A I/O
DSI-D0N	DSI Differential Data Line 0 (Negative)	A I/O
DSI-D1P	DSI Differential Data Line 1 (Positive)	AO
DSI-D1N	DSI Differential Data Line 1 (Negative)	AO
DSI-D2P	DSI Differential Data Line 2 (Positive)	AO
DSI-D2N	DSI Differential Data Line 2 (Negative)	AO
DSI-D3P	DSI Differential Data Line 3 (Positive)	AO
DSI-D3N	DSI Differential Data Line 3 (Negative)	AO

4.3.21 CAN-FD

Table 4-59 CAN-FD Signal Description

Signal Name[1]	Description[2]	Type[3]
CAN0-RX0	CAN0 Receive Data 0	I
CAN0-TX0	CAN0 Transmit Data 0	O
CAN1-RX0	CAN1 Receive Data 0	I

Signal Name[1]	Description[2]	Type[3]
CAN1-TX0	CAN1 Transmit Data 0	O
CAN2-RX0	CAN2 Receive Data 0	I
CAN2-TX0	CAN2 Transmit Data 0	O
CAN3-RX0	CAN3 Receive Data 0	I
CAN3-TX0	CAN3 Transmit Data 0	O

4.3.22 GMAC

Table 4-60 GMAC Signal Description

Signal Name[1]	Description[2]	Type[3]
RGMII0-RXCK/ RMII0-NULL	RGMII0 Receive Clock	I
RGMII0-TXCK/RMII0-TXCK	RGMII0/RMII0 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input.	I/O
RGMII0-CLKIN/RMII0-RXER	RGMII0 Transmit Clock from External/RMII0 Receive Error	I
RGMII0-RXCTL/RMII0-CRS-DV	RGMII0 Receive Control/RMII0 Carrier Sense Receive Data Valid	I
RGMII0-TXCTL/RMII0-TXEN	RGMII0 Transmit Control/RMII0 Transmit Enable	O
RGMII0-MDC	RGMII0 Management Data Clock	O
RGMII0-MDIO	RGMII0 Management Data Input/ Output	I/O
RGMII0-EPHY-25/50M	GMAC PHY 25 MHz or 50 MHz Clock Output	O
RGMII0-RXD0/RMII0-RXD0	RGMII0/RMII0 Receive Data 0	I
RGMII0-RXD1/RMII0-RXD1	RGMII0/RMII0 Receive Data 1	I
RGMII0-RXD2/RMII0-NULL	RGMII0 Receive Data 2	I
RGMII0-RXD3/RMII0-NULL	RGMII0 Receive Data 3	I
RGMII0-TXD0/RMII0-TXD0	RGMII0/RMII0 Transmit Data 0	O
RGMII0-TXD1/RMII0-TXD1	RGMII0/RMII0 Transmit Data 1	O
RGMII0-TXD2/RMII0-NULL	RGMII0 Transmit Data 2	O
RGMII0-TXD3/RMII0-NULL	RGMII0 Transmit Data 3	O
RGMII1-RXCK/ RMII1-NULL	RGMII1 Receive Clock	I
RGMII1-TXCK/RMII1-TXCK	RGMII1/RMII1 Transmit Clock For RGMII, IO type is output;	I/O

Signal Name[1]	Description[2]	Type[3]
	For RMII, IO type is input.	
RGMII1-CLKIN/RMII1-RXER	RGMII1 Transmit Clock from External/RMII1 Receive Error	I
RGMII1-RXCTL/RMII1-CRS-DV	RGMII1 Receive Control/RMII1 Carrier Sense Receive Data Valid	I
RGMII1-TXCTL/RMII1-TXEN	RGMII1 Transmit Control/RMII1 Transmit Enable	O
RGMII1-MDC	RGMII1 Management Data Clock	O
RGMII1-MDIO	RGMII1 Management Data Input/ Output	I/O
RGMII1-EPHY-25/50M	GMAC PHY 25 MHz or 50 MHz Clock Output	O
RGMII1-RXD0/RMII1-RXD0	RGMII1/RMII1 Receive Data 0	I
RGMII1-RXD1/RMII1-RXD1	RGMII1/RMII1 Receive Data 1	I
RGMII1-RXD2/RMII1-NULL	RGMII1 Receive Data 2	I
RGMII1-RXD3/RMII1-NULL	RGMII1 Receive Data 3	I
RGMII1-TXD0/RMII1-TXD0	RGMII1/RMII1 Transmit Data 0	O
RGMII1-TXD1/RMII1-TXD1	RGMII1/RMII1 Transmit Data 1	O
RGMII1-TXD2/RMII1-NULL	RGMII1 Transmit Data 2	O
RGMII1-TXD3/RMII1-NULL	RGMII1 Transmit Data 3	O

4.3.23 Local Bus Controller

Table 4-61 Local Bus Controller Signal Description

Signal Name[1]	Description[2]	Type[3]
LBUS-CS0	Local Bus Chip Select Signal 0	O
LBUS-CS1	Local Bus Chip Select Signal 1	O
LBUS-CS2	Local Bus Chip Select Signal 2	O
LBUS-CS3	Local Bus Chip Select Signal 3	O
LBUS-DP0	Local Bus Data Parity Signal 0	I/O
LBUS-DP1	Local Bus Data Parity Signal 1	I/O
LBUS-DP2	Local Bus Data Parity Signal 2	I/O
LBUS-DP3	Local Bus Data Parity Signal 3	I/O
LBUS-WR	Local Bus Write Ready	O
LBUS-READY	Local Bus Input Ready	I

Signal Name[1]	Description[2]	Type[3]
LBUS-ALE	Local Bus Address Lock Enable	O
LBUS-BURST0	Local Bus Burst Command 0	O
LBUS-BURST1	Local Bus Burst Command 1	O
LBUS-BURST2	Local Bus Burst Command 2	O
LBUS-LCLK	Local Bus Clock Output	O
LBUS-INTR	Local Bus Interrupt	I
LBUS-DRQ	Local Bus Asynchronous Data Request	I
LBUS-LBE	Local Bus Byte Enable	O
LBUS-LD0	Local Bus Data 0	I/O
LBUS-LD1	Local Bus Data 1	I/O
LBUS-LD2	Local Bus Data 2	I/O
LBUS-LD3	Local Bus Data 3	I/O
LBUS-LD4	Local Bus Data 4	I/O
LBUS-LD5	Local Bus Data 5	I/O
LBUS-LD6	Local Bus Data 6	I/O
LBUS-LD7	Local Bus Data 7	I/O
LBUS-LD8	Local Bus Data 8	I/O
LBUS-LD9	Local Bus Data 9	I/O
LBUS-LD10	Local Bus Data 10	I/O
LBUS-LD11	Local Bus Data 11	I/O
LBUS-LD12	Local Bus Data 12	I/O
LBUS-LD13	Local Bus Data 13	I/O
LBUS-LD14	Local Bus Data 14	I/O
LBUS-LD15	Local Bus Data 15	I/O
LBUS-LD16	Local Bus Data 16	I/O
LBUS-LD17	Local Bus Data 17	I/O
LBUS-LD18	Local Bus Data 18	I/O
LBUS-LD19	Local Bus Data 19	I/O
LBUS-LD20	Local Bus Data 20	I/O
LBUS-LD21	Local Bus Data 21	I/O

Signal Name[1]	Description[2]	Type[3]
LBUS-LD22	Local Bus Data 22	I/O
LBUS-LD23	Local Bus Data 23	I/O
LBUS-LD24	Local Bus Data 24	I/O
LBUS-LD25	Local Bus Data 25	I/O
LBUS-LD26	Local Bus Data 26	I/O
LBUS-LD27	Local Bus Data 27	I/O
LBUS-LD28	Local Bus Data 28	I/O
LBUS-LD29	Local Bus Data 29	I/O
LBUS-LD30	Local Bus Data 30	I/O
LBUS-LD31	Local Bus Data 31	I/O

4.3.24 SPI&SPI DBI

Table 4-62 SPI&SPI DBI Signal Description

Signal Name[1]	Description[2]	Type[3]
SPI0-CS0	SPI0 Chip Select 0 (Active Low)	I/O
SPI0-CS1	SPI0 Chip Select 1 (Active Low)	I/O
SPI0-CLK	SPI0 Clock	I/O
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0-HOLD	SPI0 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-CS0	SPI1 Chip Select 0 (Active Low)	I/O
SPI1-CLK	SPI1 Clock	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-HOLD	SPI1 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI2-CS0	SPI2 Chip Select 0 (Active Low)	I/O

Signal Name[1]	Description[2]	Type[3]
SPI2-CLK	SPI2 Clock	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI2-WP	SPI2 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI2-HOLD	SPI2 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI3-CS0	SPI3 Chip Select 0 (Active Low)	I/O
SPI3-CLK	SPI3 Clock	I/O
SPI3-MOSI	SPI3 Master Data Out, Slave Data In	I/O
SPI3-MISO	SPI3 Master Data In, Slave Data Out	I/O
SPI3-WP	SPI3 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI3-HOLD	SPI3 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI4-CS0	SPI4 Chip Select 0 (Active Low)	I/O
SPI4-CLK	SPI4 Clock	I/O
SPI4-MOSI	SPI4 Master Data Out, Slave Data In	I/O
SPI4-MISO	SPI4 Master Data In, Slave Data Out	I/O
S-SPI0-CS0	S-SPI0 Chip Select 0 (Active Low)	I/O
S-SPI0-CLK	S-SPI0 Clock	I/O
S-SPI0-MOSI	S-SPI0 Master Data Out, Slave Data In	I/O
S-SPI0-MISO	S-SPI0 Master Data In, Slave Data Out	I/O
DBI-CSX	Chip Select Signal (Active Low)	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge.	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command.	I/O

Signal Name[1]	Description[2]	Type[3]
	DCX = 0: register command; DCX = 1: data or parameter.	
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

4.3.25 SPIF

Table 4-63 SPIF Signal Description

Signal Name[1]	Description[2]	Type[3]
SPIF-CS0	SPI Peripheral Chip Select Signal, Low Active	O
SPIF-CLK	SPI Master Mode Clock Output	O
SPIF-MOSI	SPI Master Data Out, Slave Data In	I/O
SPIF-MISO	SPI Master Data In, Slave Data Out	I/O
SPIF-DQS	SPI Data Strobe Signal	I
SPIF-WP	SPI Write Protection (Active Low)	I/O
SPIF-HOLD	SPI Hold Signal	I/O
SPIF-D4	SPI Master Mode Data 4 in Octal Mode.	I/O
SPIF-D5	SPI Master Mode Data 5 in Octal Mode.	I/O
SPIF-D6	SPI Master Mode Data 6 in Octal Mode.	I/O
SPIF-D7	SPI Master Mode Data 7 in Octal Mode.	I/O

4.3.26 UART

Table 4-64 UART Signal Description

Signal Name[1]	Description[2]	Type[3]
UART0-RX	UART0 Data Receiver	I
UART0-TX	UART0 Data Transmitter	O
UART1-CTS	UART1 Clear to Send	I
UART1-RTS	UART1 Request to Send	O
UART1-RX	UART1 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART2-CTS	UART2 Clear to Send	I
UART2-RTS	UART2 Request to Send	O

Signal Name[1]	Description[2]	Type[3]
UART2-RX	UART2 Data Receiver	I
UART2-TX	UART2 Data Transmitter	O
UART3-CTS	UART3 Clear to Send	I
UART3-RTS	UART3 Request to Send	O
UART3-RX	UART3 Data Receiver	I
UART3-TX	UART3 Data Transmitter	O
UART4-CTS	UART4 Clear to Send	I
UART4-RTS	UART4 Request to Send	O
UART4-RX	UART4 Data Receiver	I
UART4-TX	UART4 Data Transmitter	O
UART5-CTS	UART5 Clear to Send	I
UART5-RTS	UART5 Request to Send	O
UART5-RX	UART5 Data Receiver	I
UART5-TX	UART5 Data Transmitter	O
UART6-CTS	UART6 Clear to Send	I
UART6-RTS	UART6 Request to Send	O
UART6-RX	UART6 Data Receiver	I
UART6-TX	UART6 Data Transmitter	O
UART7-CTS	UART7 Clear to Send	I
UART7-RTS	UART7 Request to Send	O
UART7-RX	UART7 Data Receiver	I
UART7-TX	UART7 Data Transmitter	O
UART8-CTS	UART8 Clear to Send	I
UART8-RTS	UART8 Request to Send	O
UART8-DCD	UART8 Data Carrier Detect	I
UART8-DSR	UART8 Data Set Ready	I
UART8-DTR	UART8 Data Terminal Ready	O
UART8-RI	UART8 Ring Information	I
UART8-RX	UART8 Data Receiver	I
UART8-TX	UART8 Data Transmitter	O

Signal Name[1]	Description[2]	Type[3]
UART9-CTS	UART9 Clear to Send	I
UART9-RTS	UART9 Request to Send	O
UART9-RX	UART9 Data Receiver	I
UART9-TX	UART9 Data Transmitter	O
UART10-CTS	UART10 Clear to Send	I
UART10-RTS	UART10 Request to Send	O
UART10-RX	UART10 Data Receiver	I
UART10-TX	UART10 Data Transmitter	O
UART11-CTS	UART11 Clear to Send	I
UART11-RTS	UART11 Request to Send	O
UART11-RX	UART11 Data Receiver	I
UART11-TX	UART11 Data Transmitter	O
UART12-CTS	UART12 Clear to Send	I
UART12-RTS	UART12 Request to Send	O
UART12-RX	UART12 Data Receiver	I
UART12-TX	UART12 Data Transmitter	O
UART13-CTS	UART13 Clear to Send	I
UART13-RTS	UART13 Request to Send	O
UART13-RX	UART13 Data Receiver	I
UART13-TX	UART13 Data Transmitter	O
UART14-CTS	UART14 Clear to Send	I
UART14-RTS	UART14 Request to Send	O
UART14-RX	UART14 Data Receiver	I
UART14-TX	UART14 Data Transmitter	O
S-UART0-CTS	S_UART0 Clear to Send	I
S-UART0-RTS	S_UART0 Request to Send	O
S-UART0-RX	S_UART0 Data Receiver	I
S-UART0-TX	S_UART0 Data Transmitter	O
S-UART1-CTS	S_UART1 Clear to Send	I
S-UART1-RTS	S_UART1 Request to Send	O

Signal Name[1]	Description[2]	Type[3]
S-UART1-RX	S_UART1 Data Receiver	I
S-UART1-TX	S_UART1 Data Transmitter	O

4.3.27 PWM

Table 4-65 PWM Signal Description

Signal Name[1]	Description[2]	Type[3]
PWM0-0	PWM0 Wave Output /Capture Wave Input 0	I/O
PWM0-1	PWM0 Wave Output /Capture Wave Input 1	I/O
PWM0-2	PWM0 Wave Output /Capture Wave Input 2	I/O
PWM0-3	PWM0 Wave Output /Capture Wave Input 3	I/O
PWM0-4	PWM0 Wave Output /Capture Wave Input 4	I/O
PWM0-5	PWM0 Wave Output /Capture Wave Input 5	I/O
PWM0-6	PWM0 Wave Output /Capture Wave Input 6	I/O
PWM0-7	PWM0 Wave Output /Capture Wave Input 7	I/O
PWM0-8	PWM0 Wave Output /Capture Wave Input 8	I/O
PWM0-9	PWM0 Wave Output /Capture Wave Input 9	I/O
PWM1-0	PWM1 Wave Output /Capture Wave Input 0	I/O
PWM1-1	PWM1 Wave Output /Capture Wave Input 1	I/O
PWM1-2	PWM1 Wave Output /Capture Wave Input 2	I/O
PWM1-3	PWM1 Wave Output /Capture Wave Input 3	I/O
PWM1-4	PWM1 Wave Output /Capture Wave Input 4	I/O
PWM1-5	PWM1 Wave Output /Capture Wave Input 5	I/O
PWM1-6	PWM1 Wave Output /Capture Wave Input 6	I/O
PWM1-7	PWM1 Wave Output /Capture Wave Input 7	I/O
PWM1-8	PWM1 Wave Output /Capture Wave Input 8	I/O
PWM1-9	PWM1 Wave Output /Capture Wave Input 9	I/O
PWM2-0	PWM2 Wave Output /Capture Wave Input 0	I/O
PWM2-1	PWM2 Wave Output /Capture Wave Input 1	I/O
PWM2-2	PWM2 Wave Output /Capture Wave Input 2	I/O
PWM2-3	PWM2 Wave Output /Capture Wave Input 3	I/O
PWM2-4	PWM2 Wave Output /Capture Wave Input 4	I/O

Signal Name[1]	Description[2]	Type[3]
PWM2-5	PWM2 Wave Output /Capture Wave Input 5	I/O
PWM2-6	PWM2 Wave Output /Capture Wave Input 6	I/O
PWM2-7	PWM2 Wave Output /Capture Wave Input 7	I/O
PWM2-8	PWM2 Wave Output /Capture Wave Input 8	I/O
PWM2-9	PWM2 Wave Output /Capture Wave Input 9	I/O
S-PWM0-0	S_PWM0 Wave Output /Capture Wave Input 0	I/O
S-PWM0-1	S_PWM0 Wave Output /Capture Wave Input 1	I/O
S-PWM0-2	S_PWM0 Wave Output /Capture Wave Input 2	I/O
S-PWM0-3	S_PWM0 Wave Output /Capture Wave Input 3	I/O

4.3.28 TWI

Table 4-66 TWI Signal Description

Signal Name[1]	Description[2]	Type[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O
TWI4-SCK	TWI4 Serial Clock Signal	I/O
TWI4-SDA	TWI4 Serial Data Signal	I/O
TWI5-SCK	TWI5 Serial Clock Signal	I/O
TWI5-SDA	TWI5 Serial Data Signal	I/O
TWI6-SCK	TWI6 Serial Clock Signal	I/O
TWI6-SDA	TWI6 Serial Data Signal	I/O
S-TWI0-SCK	S_TWI0 Serial Clock Signal	I/O
S-TWI0-SDA	S_TWI0 Serial Data Signal	I/O
S-TWI1-SCK	S_TWI1 Serial Clock Signal	I/O
S-TWI1-SDA	S_TWI1 Serial Data Signal	I/O

4.3.29 IR RX

Table 4-67 IR RX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-RX0	Consumer Infrared Receiver	I
IR-RX1	Consumer Infrared Receiver	I
IR-RX2	Consumer Infrared Receiver	I
IR-RX3	Consumer Infrared Receiver	I
S-IR-RX	Consumer infrared Receiver	I

4.3.30 IR TX

Table 4-68 IR TX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-TX	Consumer Infrared Transmitter	O

4.3.31 LEDC

Table 4-69 LEDC Signal Description

Signal Name[1]	Description[2]	Type[3]
LEDC	Intelligent Control LED Signal Output	O

4.3.32 JTAG

Table 4-70 JTAG Signal Description

Signal Name[1]	Description[2]	Type[3]
JTAG-MS	A55 JTAG Mode Selection	I
JTAG-CK	A55JTAG Clock Signal	I
JTAG-DI	A55 JTAG Data Input	I
JTAG-DO	A55 JTAG Data Output	O
RJTAG-MS	E907 JTAG Mode Selection	I
RJTAG-CK	E907JTAG Clock Signal	I
RJTAG-DI	E907 JTAG Data Input	I
RJTAG-DO	E907 JTAG Data Output	O
S-RJTAG-MS	E902 JTAG Mode Select	I
S-RJTAG-CK	E902 JTAG Clock Signal	I

Signal Name[1]	Description[2]	Type[3]
S-JTAG-MS	AR100 JTAG Mode Selection	I
S-JTAG-CK	AR100 JTAG Clock Signal	I
S-JTAG-DI	AR100 JTAG Data Input	I
S-JTAG-DO	AR100 JTAG Data Output	O

4.3.33 Interrupt

Table 4-71 Interrupt Signal Description

Signal Name[1]	Description[2]	Type[3]
PA-EINT0	Port A Interrupt	I
PA-EINT1	Port A Interrupt	I
PA-EINT2	Port A Interrupt	I
PA-EINT3	Port A Interrupt	I
PA-EINT4	Port A Interrupt	I
PA-EINT5	Port A Interrupt	I
PA-EINT6	Port A Interrupt	I
PA-EINT7	Port A Interrupt	I
PA-EINT8	Port A Interrupt	I
PA-EINT9	Port A Interrupt	I
PB-EINT0	Port B Interrupt	I
PB-EINT1	Port B Interrupt	I
PB-EINT2	Port B Interrupt	I
PB-EINT3	Port B Interrupt	I
PB-EINT4	Port B Interrupt	I
PB-EINT5	Port B Interrupt	I
PB-EINT6	Port B Interrupt	I
PB-EINT7	Port B Interrupt	I
PB-EINT8	Port B Interrupt	I
PB-EINT9	Port B Interrupt	I
PB-EINT10	Port B Interrupt	I
PB-EINT11	Port B Interrupt	I
PB-EINT12	Port B Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PB-EINT13	Port B Interrupt	I
PB-EINT14	Port B Interrupt	I
PC-EINT0	Port C Interrupt	I
PC-EINT1	Port C Interrupt	I
PC-EINT2	Port C Interrupt	I
PC-EINT3	Port C Interrupt	I
PC-EINT4	Port C Interrupt	I
PC-EINT5	Port C Interrupt	I
PC-EINT6	Port C Interrupt	I
PC-EINT7	Port C Interrupt	I
PC-EINT8	Port C Interrupt	I
PC-EINT9	Port C Interrupt	I
PC-EINT10	Port C Interrupt	I
PC-EINT11	Port C Interrupt	I
PC-EINT12	Port C Interrupt	I
PC-EINT13	Port C Interrupt	I
PC-EINT14	Port C Interrupt	I
PC-EINT15	Port C Interrupt	I
PC-EINT16	Port C Interrupt	I
PD-EINT0	Port D Interrupt	I
PD-EINT1	Port D Interrupt	I
PD-EINT2	Port D Interrupt	I
PD-EINT3	Port D Interrupt	I
PD-EINT4	Port D Interrupt	I
PD-EINT5	Port D Interrupt	I
PD-EINT6	Port D Interrupt	I
PD-EINT7	Port D Interrupt	I
PD-EINT8	Port D Interrupt	I
PD-EINT9	Port D Interrupt	I
PD-EINT10	Port D Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PD-EINT11	Port D Interrupt	I
PD-EINT12	Port D Interrupt	I
PD-EINT13	Port D Interrupt	I
PD-EINT14	Port D Interrupt	I
PD-EINT15	Port D Interrupt	I
PD-EINT16	Port D Interrupt	I
PD-EINT17	Port D Interrupt	I
PD-EINT18	Port D Interrupt	I
PD-EINT19	Port D Interrupt	I
PD-EINT20	Port D Interrupt	I
PD-EINT21	Port D Interrupt	I
PD-EINT22	Port D Interrupt	I
PD-EINT23	Port D Interrupt	I
PE-EINT0	Port E Interrupt	I
PE-EINT1	Port E Interrupt	I
PE-EINT2	Port E Interrupt	I
PE-EINT3	Port E Interrupt	I
PE-EINT4	Port E Interrupt	I
PE-EINT5	Port E Interrupt	I
PE-EINT6	Port E Interrupt	I
PE-EINT7	Port E Interrupt	I
PE-EINT8	Port E Interrupt	I
PE-EINT9	Port E Interrupt	I
PE-EINT10	Port E Interrupt	I
PE-EINT11	Port E Interrupt	I
PE-EINT12	Port E Interrupt	I
PE-EINT13	Port E Interrupt	I
PE-EINT14	Port E Interrupt	I
PE-EINT15	Port E Interrupt	I
PE-EINT16	Port E Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PE-EINT17	Port E Interrupt	I
PF-EINT0	Port F Interrupt	I
PF-EINT1	Port F Interrupt	I
PF-EINT2	Port F Interrupt	I
PF-EINT3	Port F Interrupt	I
PF-EINT4	Port F Interrupt	I
PF-EINT5	Port F Interrupt	I
PF-EINT6	Port F Interrupt	I
PG-EINT0	Port G Interrupt	I
PG-EINT1	Port G Interrupt	I
PG-EINT2	Port G Interrupt	I
PG-EINT3	Port G Interrupt	I
PG-EINT4	Port G Interrupt	I
PG-EINT5	Port G Interrupt	I
PG-EINT6	Port G Interrupt	I
PG-EINT7	Port G Interrupt	I
PG-EINT8	Port G Interrupt	I
PG-EINT9	Port G Interrupt	I
PG-EINT10	Port G Interrupt	I
PG-EINT11	Port G Interrupt	I
PG-EINT12	Port G Interrupt	I
PG-EINT13	Port G Interrupt	I
PG-EINT14	Port G Interrupt	I
PH-EINT0	Port H Interrupt	I
PH-EINT1	Port H Interrupt	I
PH-EINT2	Port H Interrupt	I
PH-EINT3	Port H Interrupt	I
PH-EINT4	Port H Interrupt	I
PH-EINT5	Port H Interrupt	I
PH-EINT6	Port H Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PH-EINT7	Port H Interrupt	I
PH-EINT8	Port H Interrupt	I
PH-EINT9	Port H Interrupt	I
PH-EINT10	Port H Interrupt	I
PH-EINT11	Port H Interrupt	I
PH-EINT12	Port H Interrupt	I
PH-EINT13	Port H Interrupt	I
PH-EINT14	Port H Interrupt	I
PH-EINT15	Port H Interrupt	I
PI-EINT0	Port I Interrupt	I
PI-EINT1	Port I Interrupt	I
PI-EINT2	Port I Interrupt	I
PI-EINT3	Port I Interrupt	I
PI-EINT4	Port I Interrupt	I
PI-EINT5	Port I Interrupt	I
PI-EINT6	Port I Interrupt	I
PI-EINT7	Port I Interrupt	I
PI-EINT8	Port I Interrupt	I
PI-EINT9	Port I Interrupt	I
PI-EINT10	Port I Interrupt	I
PI-EINT11	Port I Interrupt	I
PI-EINT12	Port I Interrupt	I
PI-EINT13	Port I Interrupt	I
PI-EINT14	Port I Interrupt	I
PI-EINT15	Port I Interrupt	I
PI-EINT16	Port I Interrupt	I
PJ-EINT0	Port J Interrupt	I
PJ-EINT1	Port J Interrupt	I
PJ-EINT2	Port J Interrupt	I
PJ-EINT3	Port J Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PJ-EINT4	Port J Interrupt	I
PJ-EINT5	Port J Interrupt	I
PJ-EINT6	Port J Interrupt	I
PJ-EINT7	Port J Interrupt	I
PJ-EINT8	Port J Interrupt	I
PJ-EINT9	Port J Interrupt	I
PJ-EINT10	Port J Interrupt	I
PJ-EINT11	Port J Interrupt	I
PJ-EINT12	Port J Interrupt	I
PJ-EINT13	Port J Interrupt	I
PJ-EINT14	Port J Interrupt	I
PJ-EINT15	Port J Interrupt	I
PJ-EINT16	Port J Interrupt	I
PJ-EINT17	Port J Interrupt	I
PJ-EINT18	Port J Interrupt	I
PJ-EINT19	Port J Interrupt	I
PJ-EINT20	Port J Interrupt	I
PJ-EINT21	Port J Interrupt	I
PJ-EINT22	Port J Interrupt	I
PJ-EINT23	Port J Interrupt	I
PJ-EINT24	Port J Interrupt	I
PJ-EINT25	Port J Interrupt	I
PJ-EINT26	Port J Interrupt	I
PJ-EINT27	Port J Interrupt	I
PJ-EINT28	Port J Interrupt	I
PJ-EINT29	Port J Interrupt	I
PJ-EINT30	Port J Interrupt	I
PJ-EINT31	Port J Interrupt	I
PK-EINT0	Port K Interrupt	I
PK-EINT1	Port K Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PK-EINT2	Port K Interrupt	I
PK-EINT3	Port K Interrupt	I
PK-EINT4	Port K Interrupt	I
PK-EINT5	Port K Interrupt	I
PK-EINT6	Port K Interrupt	I
PK-EINT7	Port K Interrupt	I
PK-EINT8	Port K Interrupt	I
PK-EINT9	Port K Interrupt	I
PK-EINT10	Port K Interrupt	I
PK-EINT11	Port K Interrupt	I
PK-EINT12	Port K Interrupt	I
PK-EINT13	Port K Interrupt	I
PK-EINT14	Port K Interrupt	I
PK-EINT15	Port K Interrupt	I
PK-EINT16	Port K Interrupt	I
PK-EINT17	Port K Interrupt	I
PK-EINT18	Port K Interrupt	I
PK-EINT19	Port K Interrupt	I
PK-EINT20	Port K Interrupt	I
PK-EINT21	Port K Interrupt	I
PK-EINT22	Port K Interrupt	I
PK-EINT23	Port K Interrupt	I
PL-EINT0	Port L Interrupt	I
PL-EINT1	Port L Interrupt	I
PL-EINT2	Port L Interrupt	I
PL-EINT3	Port L Interrupt	I
PL-EINT4	Port L Interrupt	I
PL-EINT5	Port L Interrupt	I
PL-EINT6	Port L Interrupt	I
PL-EINT7	Port L Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PL-EINT8	Port L Interrupt	I
PL-EINT9	Port L Interrupt	I
PL-EINT10	Port L Interrupt	I
PL-EINT11	Port L Interrupt	I
PL-EINT12	Port L Interrupt	I
PL-EINT13	Port L Interrupt	I
PM-EINT0	Port M Interrupt	I
PM-EINT1	Port M Interrupt	I
PM-EINT2	Port M Interrupt	I
PM-EINT3	Port M Interrupt	I
PM-EINT4	Port M Interrupt	I
PM-EINT5	Port M Interrupt	I

5 Electrical characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 5.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Supply Name	Description	Min(1)	Max(1)	Unit
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-CPU-PLL	CPU PLL Power Supply	-0.3	2.16	V
VCC-PLL	System PLL Supply	-0.3	2.16	V
VCC-RTC	RTC Power Supply	-0.3	2.16	V
VCC-DRAM	DRAM IO Power Supply	-0.3	VDDQ+0.3	V
VCC-DRAML	LPDDR4x Power Supply	-0.3	VDDQ+0.3	V
VCC18-ADC	GPADC and LRADC Power Supply	-0.3	2.16	V
VCC18-EFUSE	eFuse Power Supply	-0.3	2.16	V
VCC18-LVDS	LVDS and MIPI DSI Power Supply	-0.3	2.16	V
VCC18-MCSI	MIPI CSI Power Supply	-0.3	2.16	V
VCC-IO	GPIO/FEL/BOOT_SEL/JTAG_SEL Power Supply	-0.3	3.96	V
VCC-PA	Digital Port A Power	-0.3	3.96	V
VCC-PC	Digital Port C Power	-0.3	3.96	V
VCC-PD	Digital Port D Power	-0.3	3.96	V
VCC-PE	Digital Port E Power	-0.3	3.96	V
VCC18-PF	Digital Port F Power	-0.3	2.16	V
VCC-PG	Digital Port G Power	-0.3	3.96	V
VCC-PH	Digital Port H Power	-0.3	3.96	V
VCC-PI	Digital Port I Power	-0.3	3.96	V
VCC-PJ	Digital Port J Power	-0.3	3.96	V
VCC-PK	Digital Port K Power	-0.3	3.96	V
VCC-PL	Digital Port L Power	-0.3	3.96	V
VCC-PM	Digital Port M Power	-0.3	3.96	V
VCC18-COMB	PCIe2.1 & USB3.1 Combo PHY 1.8V Power Supply	-0.3	2.16	V
VCC33-USB0-USB1	USB2.0 DRD and USB 2.0 Host 3.3V Power Supply	-0.3	3.63	V
VDD18-DRAM	SDRAM Controller Power Supply	-0.3	2.16	V

Supply Name	Description	Min(1)	Max(1)	Unit
VDD09-USB0-USB1	USB2.0 DRD and USB 2.0 Host 0.9V Power Supply	-0.3	1.08	V
VDD09-COMB	PCIe2.1 & USB3.1 Combo PHY 0.9V Power Supply	-0.3	1.05	V
VDD-VE	VE Power Supply	-0.3	1.05	V
VDD-CPUS	CPUS Power Supply	-0.3	1.05	V
VDD-CPU	ARM Cortex™-A55 Power Supply	-0.3	1.2	V
VDD-NPU	NPU Power Supply	-0.3	1.2	V
VDD-SYS	System Power Supply	-0.3	1.05	V
V_{ESD}	Human Body Model (HBM)(3)	±2000		V
	Charged Device Model (CDM)(4)	±500		V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)	PASS		
	Latch-up over-voltage performance voltage injection on each IO pin(6)	PASS		

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2023.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2022.

(5) Based on JESD78F; each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78F; each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3 Recommended Operating Conditions

The following table describes operating conditions of the device.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Supply Name	Description	Min	Typ	Max	Unit
AVCC	Power Supply for Analog Part	1.782	1.8	1.818	V
VCC-CPU-PLL	CPU PLL Power Supply	1.71	1.8	1.89	V
VCC-PLL	System PLL Supply	1.71	1.8	1.89	V
VCC-RTC	RTC Power Supply	1.62	1.8	1.98	V
VCC-DRAM	DDR3 Power Supply	1.425	1.5	1.575	V
	DDR3L Power Supply	1.283	1.35	1.45	
	LPDDR3 Power Supply	1.14	1.2	1.30	
	DDR4 Power Supply	1.14	1.2	1.26	
	LPDDR4 and LPDDR4x Power Supply	1.06	1.1	1.17	
VCC-DRAML	LPDDR4x Power Supply	0.57	0.6(1)	0.65	V
VCC18-ADC	GPADC and LRADC Power Supply	1.782	1.8	1.818	V
VCC18-EFUSE	eFuse Power Supply	1.71	1.8	1.98	V
VCC18-LVDS	LVDS and MIPI DSI Power Supply	1.71	1.8	1.89	V
VCC18-MCSI	MIPI CSI Power Supply	1.71	1.8	1.89	V
VCC-IO	GPIO/FEL/BOOT_SEL/JTAG_SEL Power Supply	2.97	3.3	3.63	V
VCC-PA	Digital Port A Power 1.8 V Voltage 3.3 V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC-PC	Digital Port C Power 1.8 V Voltage 3.3 V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC-PD	Digital Port D Power 1.8 V Voltage 3.3 V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC-PE	Digital Port E Power 1.8 V Voltage 3.3 V Voltage	 1.62 2.97	 1.8 3.3	 1.98 3.63	V
VCC18-PF	Digital Port F Power 1.8 V Voltage	1.62	1.8	1.98	V

Supply Name	Description	Min	Typ	Max	Unit
VCC-PG	Digital Port G Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PH	Digital Port H Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PI	Digital Port I Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PJ	Digital Port J Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PK	Digital Port K Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PL	Digital Port L Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PM	Digital Port M Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC18-COMB	PCIe & USB3.1 Combo PHY 1.8V Power Supply	1.71	1.8	1.89	V
VCC33-USB0-USB1	USB2.0 DRD and USB 2.0 Host 3.3V Power Supply	2.97	3.3	3.63	V
VDD18-DRAM	SDRAM Controller Power Supply	1.71	1.8	1.89	V
VDD09-USB0-USB1	USB2.0 DRD and USB 2.0 Host 0.9V Power Supply	0.837	0.9	1.00	V
VDD09-COMB	PCIe & USB3.1 Combo PHY 0.9V Power Supply	0.9	-	1.00	V
VDD-VE	VE Power Supply	0.9	-	1.00	V
VDD-CPUS	CPUS Power Supply	0.88	-	0.99	V
VDD-CPU	ARM Cortex™-A55 Power Supply	0.9	-	1.15	V
VDD-NPU	NPU Power Supply	0.9	-	1.15	V

Supply Name	Description	Min	Typ	Max	Unit
VDD-SYS	System Power Supply	0.9	-	1.00	V

(1) When only LPDDR4x is selected, VCC-DRAML is 0.6 V. Otherwise, VCC-DRAM and VCC-DRAML are the same.

5.4 GPIO DC Electrical Characteristics

Table 5-3 summarizes the GPIO DC electrical characteristics of the device.

Table 5-3 GPIO DC Electrical Characteristics(1)

(VCC: VCC-IO/VCC-PA/VCC-PC/ VCC-PD/VCC18-PF/VCC-PH/VCC-PG/ VCC-PI/VCC-PJ/VCC-PK/ VCC-PL)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-Level Input Voltage		0.7 * VCC	-	1.1*VCC	V
V_{IL}	Low-Level Input Voltage		-0.3	-	0.3 * VCC	V
R_{PU}	Output Pull-up Resistance	PI4, PI5, PL0, PL1	2.82	4.7	6.58	kΩ
		PC0, PC1, PC3, PC6, PC7, PF3, PF6	9	15	21	kΩ
		PG1, PG2, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
R_{PD}	Output Pull-down Resistance	PI4, PI5, PL0, PL1	2.82	4.7	6.58	kΩ
		PC0, PC1, PC3, PC6, PC7, PF3, PF6	9	15	21	kΩ
		PG1, PG2, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
I_{IH}	High-Level Input Current		-	-	10	uA
I_{IL}	Low-Level Input Current		-	-	10	uA
V_{OH}	High-Level Output Voltage		VCC – 0.3	-	VCC	V
V_{OL}	Low-Level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

(1) Guaranteed by design.

5.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 5-1 SMHC Voltage Waveform

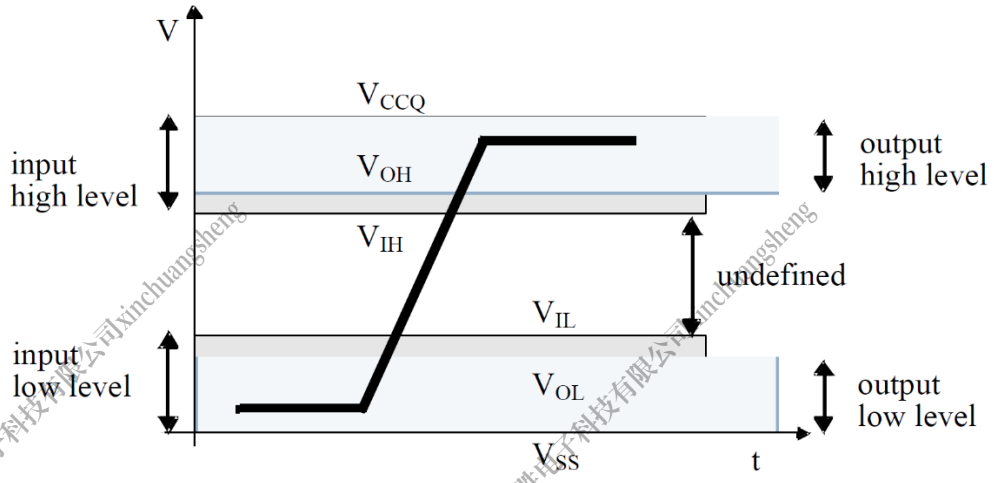


Table 5-4 shows 3.3 V SMHC electrical parameters.

Table 5-4 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8 V SMHC electrical parameters.

Table 5-5 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.65 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V

Symbol	Parameter	Min	Typ	Max	Unit
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6 GPADC Electrical Characteristics

Table 5-6 lists the GPADC electrical characteristics.

Table 5-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	VCC18-ADC	V
Sampling Rate	-	-	2	MHz
Conversion Time	0.5	-	-	us

5.7 LRADC Electrical Characteristics

The following table lists the LRADC electrical characteristics.

Table 5-7 LRADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	6	-	bits
Full-scale Input Range			LEVELB(1)	V
Effective Precision	-	5	-	bits
Sampling Rate	-	-	2	kHz
Conversion Time	-	6	-	ADC Clock Cycles

(1) The maximum value of LEVELB is 1.286 V. For details, see the register description of LRADC in *T536_User_Manual*.

5.8 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz.

Table 5-8 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTP/N(R=100K)					

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
	Full-scale	0dBFS 1kHz	-	1.08	-	Vrms
	SNR(A-weighted)	0data	-	100	-	dB
	THD+N	0dBFS 1kHz	-	-89	-	dB

5.9 External Clock Source Electrical Characteristics

5.9.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-9 High-speed 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of the device. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 5-10 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/ (C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

5.9.2 Low-speed Crystal/Ceramic Resonator Characteristics

This device contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.

This device also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-11 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X32K_IN}	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C (1)	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	1.1	-	pF

This device has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.

The 1.1 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

5.10 Interface Timing Characteristics

5.10.1 Raw NAND Flash Interface Timing

Figure 5-2 Conventional Serial Access Cycle Timing (SAM0)

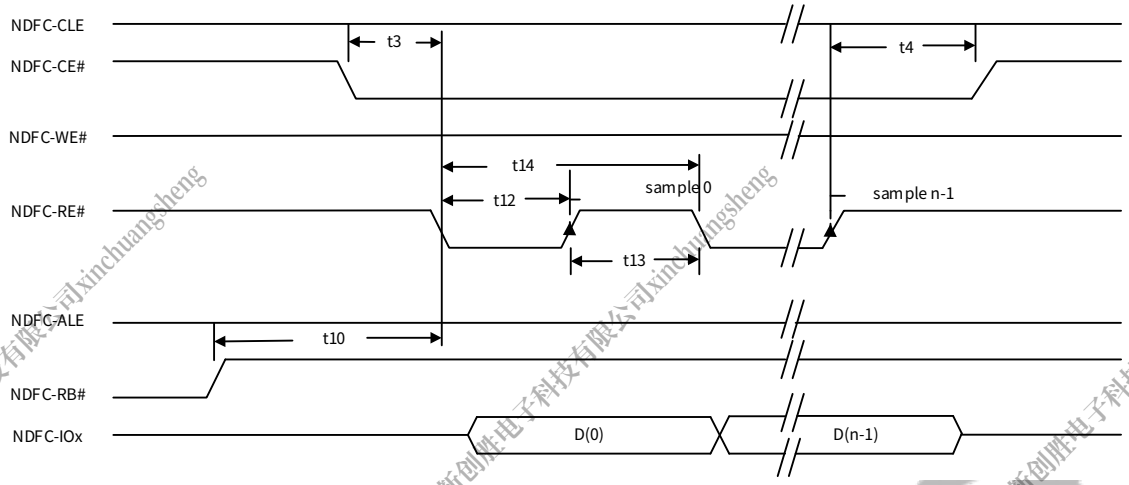


Figure 5-3 EDO Type Serial Access after Read Cycle Timing (SAM1)

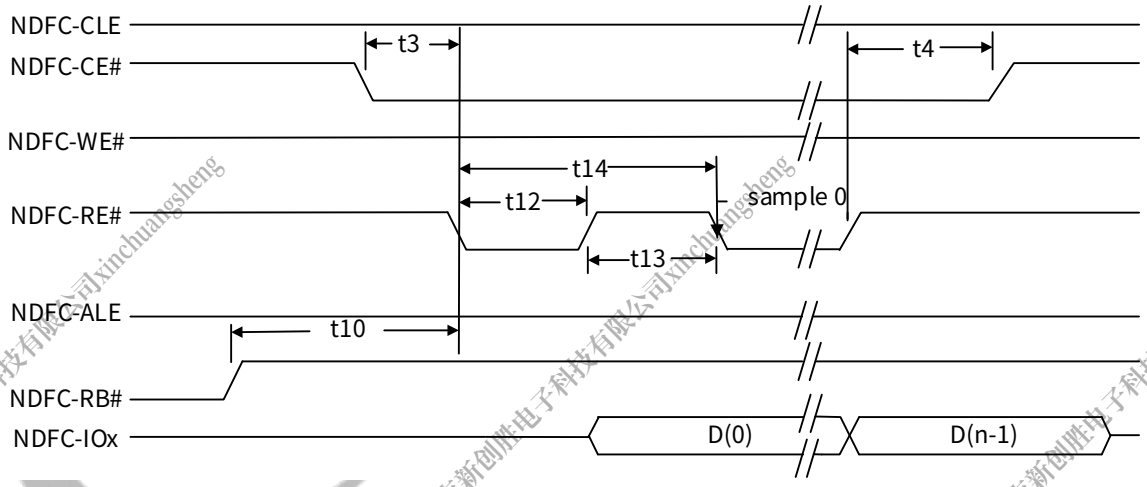


Figure 5-4 Extending EDO Type Serial Access Mode Timing (SAM2)

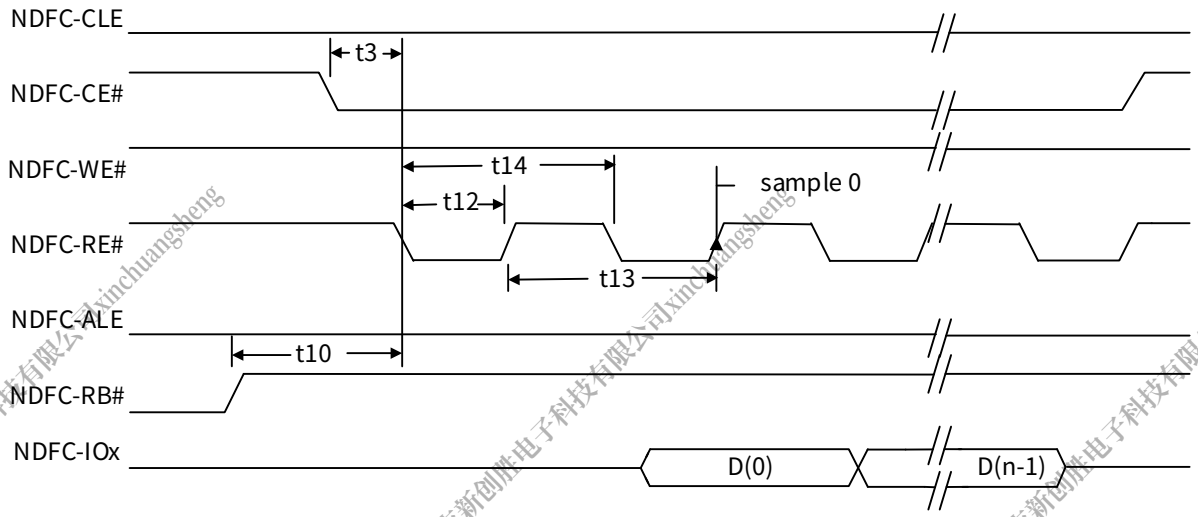


Figure 5-5 Command Latch Cycle Timing

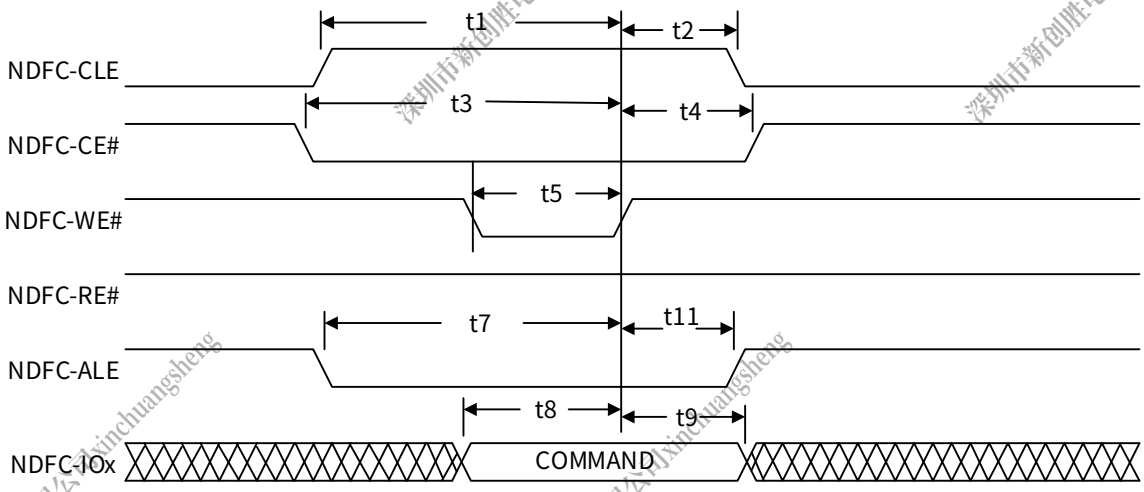


Figure 5-6 Address Latch Cycle Timing

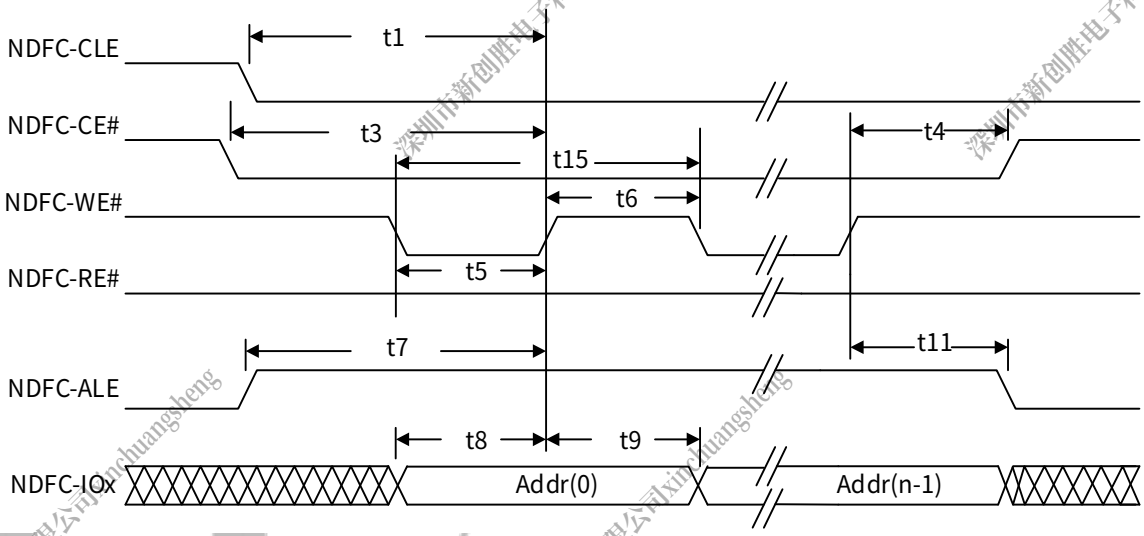


Figure 5-7 Write Data to Flash Cycle Timing

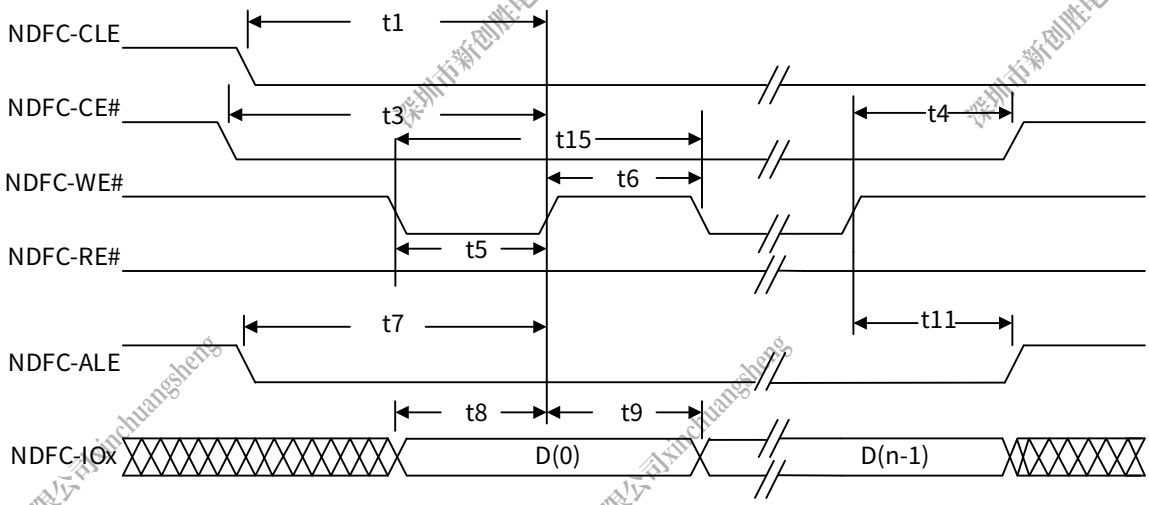


Figure 5-8 Waiting R/B# Ready Timing

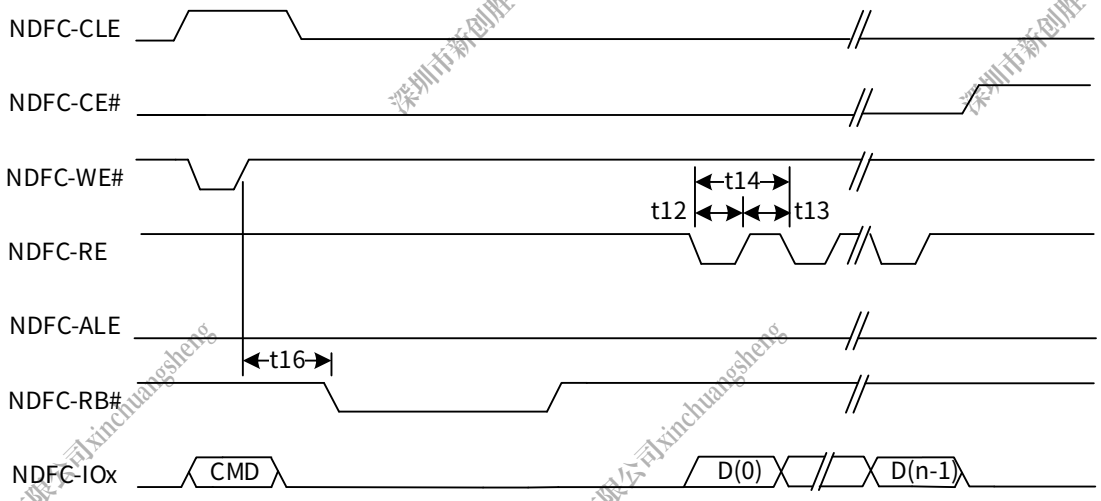


Figure 5-9 WE# High to RE# Low Timing

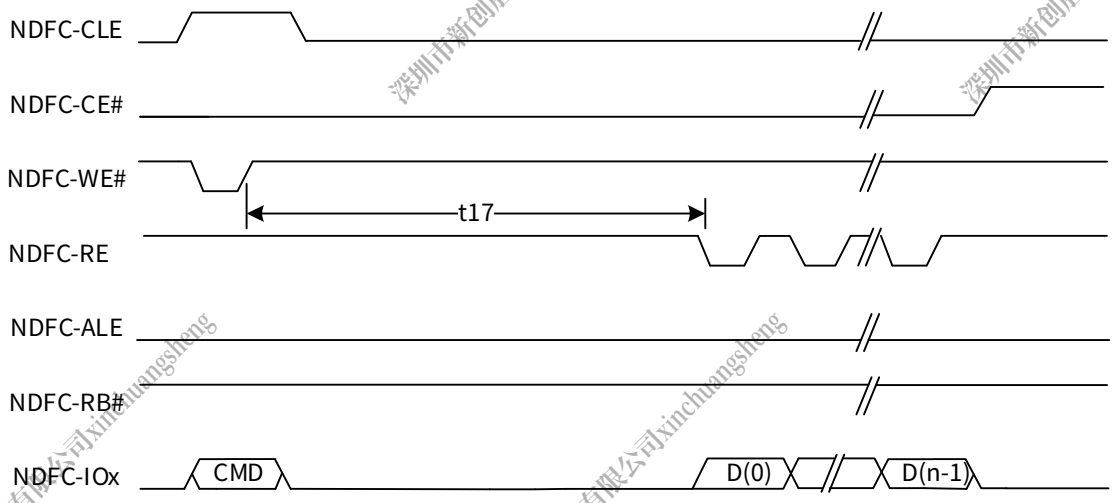


Figure 5-10 RE# High to WE# Low Timing

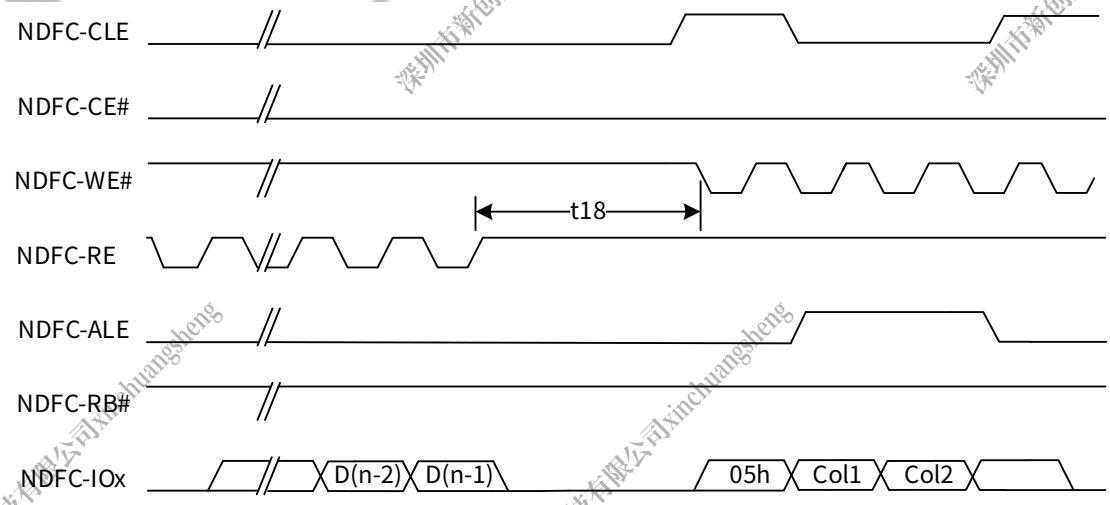


Figure 5-11 Address to Data Loading Timing

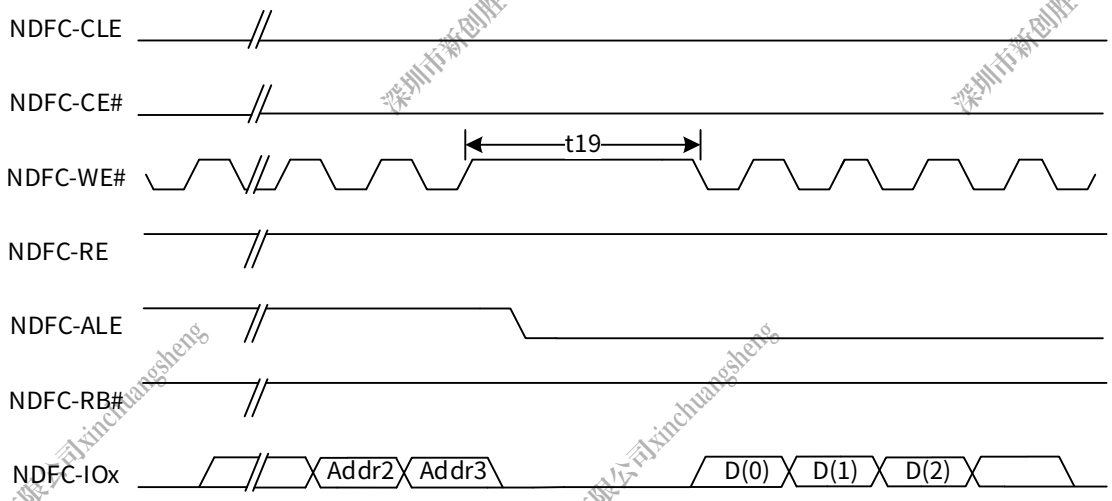


Table 5-12 Raw NAND Flash Timing Constants

Parameter	Symbol	Timing	Unit
NDFC-CLE setup time	t1	2T	ns
NDFC-CLE hold time	t2	2T	ns
NDFC-CE setup time	t3	2T	ns
NDFC-CE hold time	t4	2T	ns
NDFC-WE# pulse width	t5	T(1)	ns
NDFC-WE# hold time	t6	T	ns
NDFC-ALE setup time	t7	2T	ns
Data setup time	t8	T	ns
Data hold time	t9	T	ns
Ready to NDFC-RE# low	t10	3T	ns
NDFC-ALE hold time	t11	2T	ns
NDFC-RE# pulse width	t12	T	ns
NDFC-RE# hold time	t13	T	ns
Read cycle time	t14	2T	ns
Write cycle time	t15	2T	ns
NDFC-WE# high to R/B# busy	t16	T_WB(2)	ns
NDFC-WE# high to NDFC-RE# low	t17	T_WHR(3)	ns
NDFC-RE# high to NDFC-WE# low	t18	T_RHW(4)	ns

Parameter	Symbol	Timing	Unit
Address to Data Loading time	t19	T_ADL(5)	ns
(1) T is the cycle of internal clock. (2), (3), (4), (5) This values are configurable in NAND Flash controller. The value of T_WB could be 14*2T/22*2T/30*2T/38*2T, the value of T_WHR could be 8*2T/16*2T/24*2T/32*2T, the value of T_RHW could be 4*2T/8*2T/12*2T/20*2T, the value of T_ADL could be 0*2T/8*2T/16*2T/24*2T.			

5.10.2 SMHC Interface Timing

5.10.2.1 HS-SDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

Figure 5-12 SMHC HS-SDR Mode Output Timing Diagram

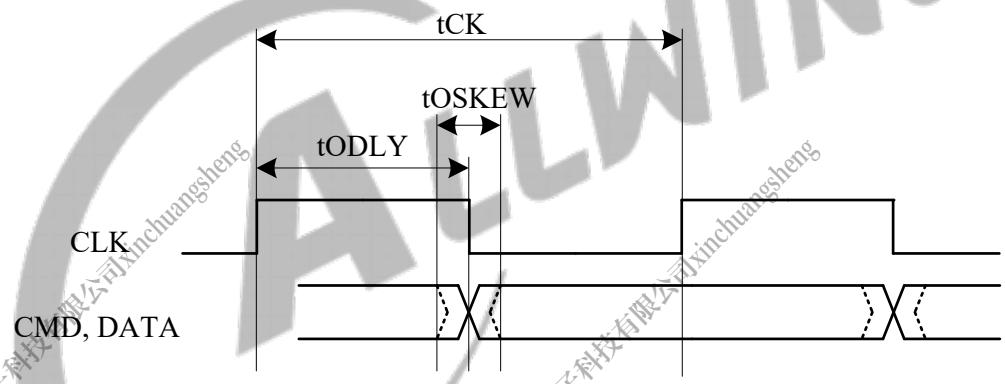


Table 5-13 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-13 SMHC HS-SDR Mode Input Timing Diagram

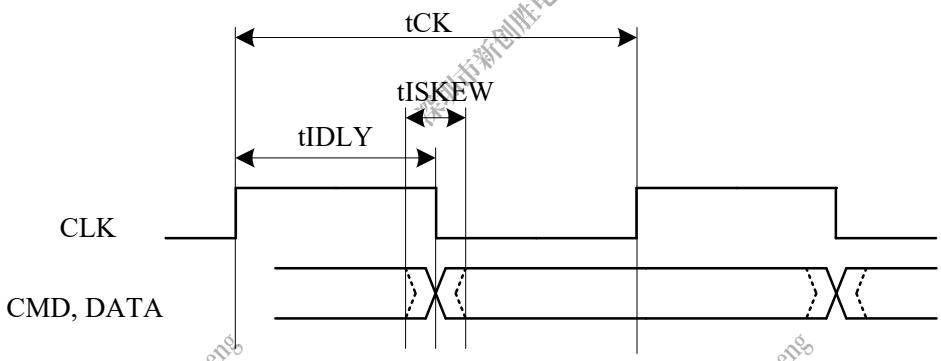


Table 5-14 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
Data input skew time in SDR mode	tISKEW	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

5.10.2.2 HS-DDR Mode

Figure 5-14 SMHC HS-DDR Mode Output Timing Diagram

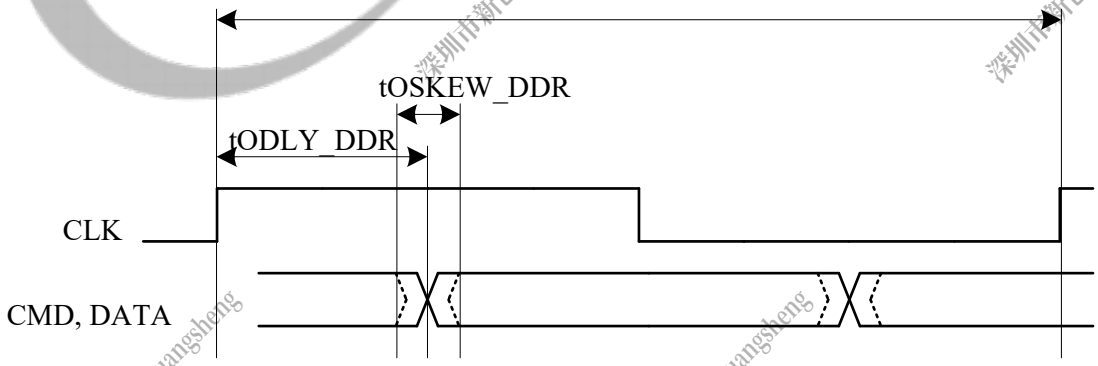


Table 5-15 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time in DDR mode	tODLY-DDR		0.25	0.25	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-15 SMHC HS-DDR Mode Input Timing Diagram

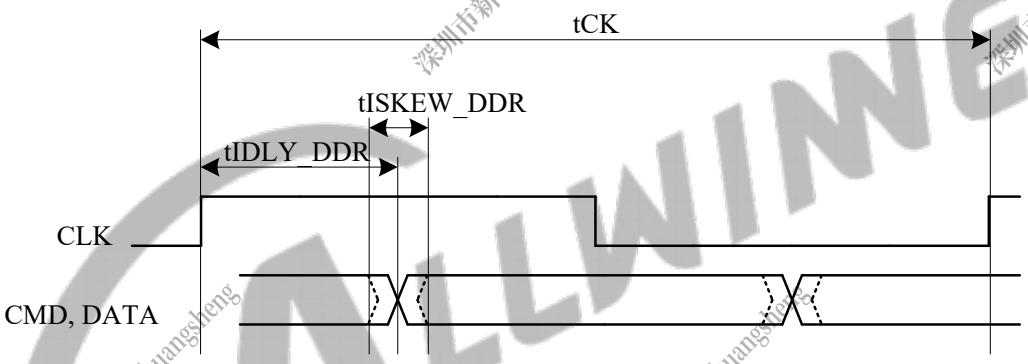


Table 5-16 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
Data input skew time in DDR mode	tISKEW-DDR	-	-	0.858	ns
The driver strength level of GPIO is 2 for test.					

5.10.2.3 HS200/SDR104 Mode

Figure 5-16 SMHC HS200/SDR104 Mode Output Timing Diagram

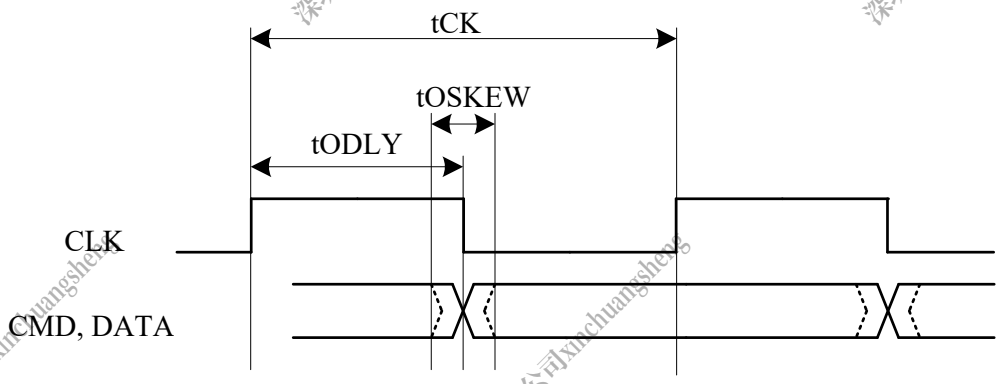


Table 5-17 SMHC HS200/SDR104 Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	-	-	200	MHz
Duty Cycle	DC	45	50	55	%
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI
Output CMD, DATA (referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
Data output delay skew time	tOSKEW	-	-	0.884	ns
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.					

Figure 5-17 SMHC HS200/SDR104 Mode Host Input Timing and Device Output Timing Diagram

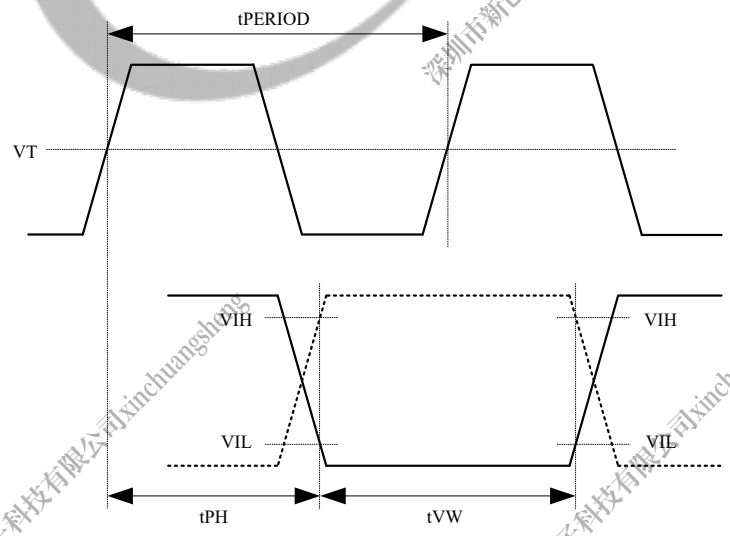


Table 5-18 SMHC HS200/SDR104 Mode Host Input Timing and Device Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	5	-	-	ns	Max: 200 MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Input CMD, DATA (referenced to CLK)						
Output delay	tPH	0	-	2	UI	
Output delay variation due to temperature change after tuning	dPH	-350(3)	-	1550(4)	ps	
CMD, Data valid window	tVW	0.575	-	-	UI	

(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.
(2) The driver strength level of GPIO is 3 for test.
(3) Temperature variation: -20 °C.
(4) Temperature variation: 90 °C.

5.10.2.4 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 5-18 SMHC HS400 Mode Host Output Timing and Device Input Timing Diagram

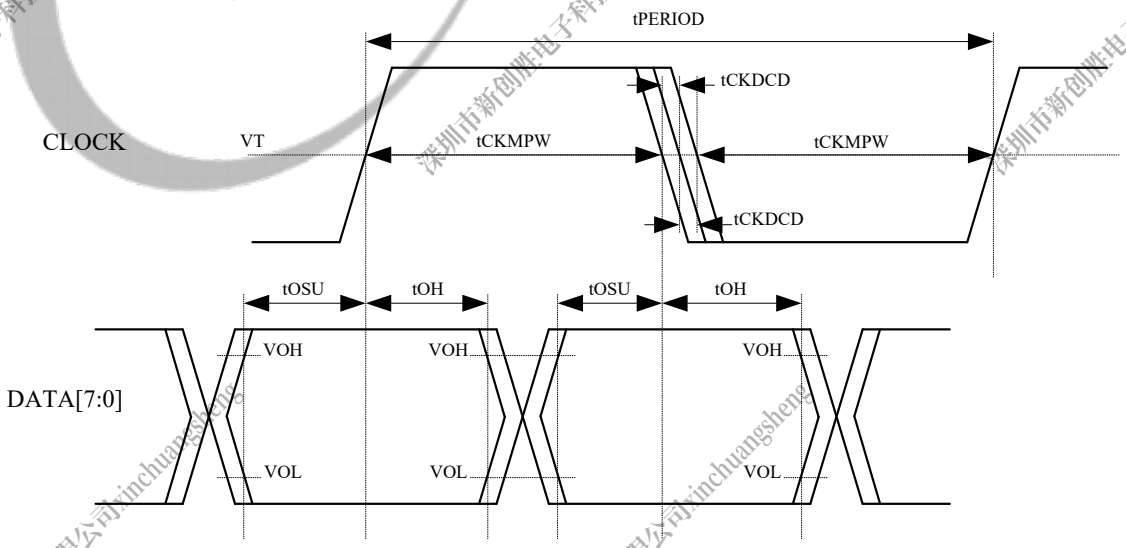


Table 5-19 SMHC HS400 Mode Host Output Timing and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.66	-	-	ns	Max: 150MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA (referenced to CLK)						
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

Figure 5-19 SMHC HS400 Mode Host Input Timing and Device Output Timing Diagram

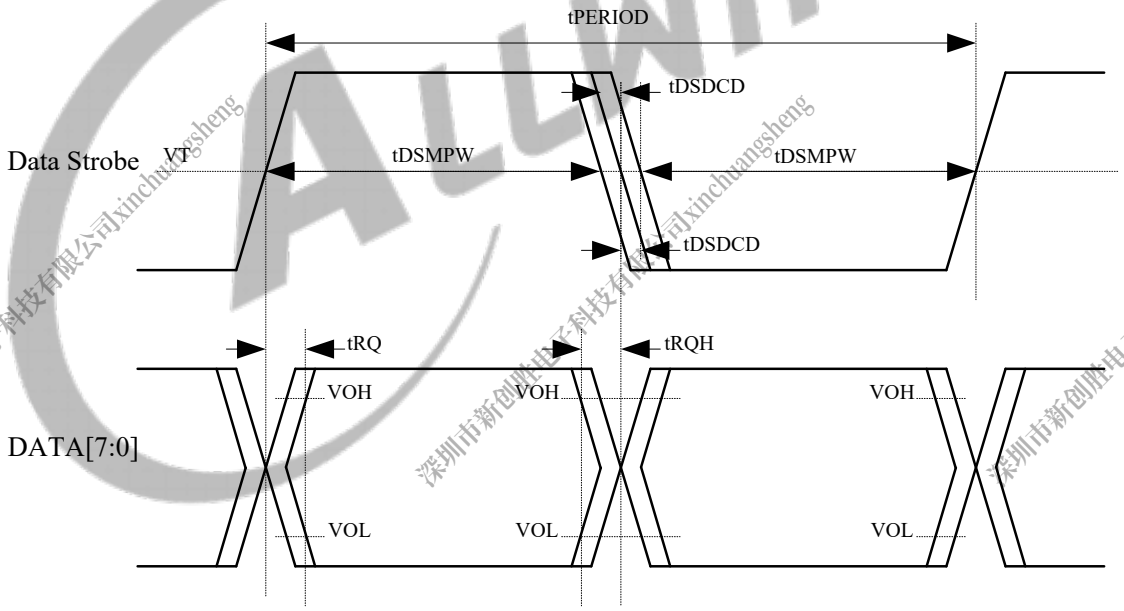


Table 5-20 SMHC HS400 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS (Data Strobe)						
DS period	tPERIOD	6.66	-	-	ns	Max: 150MHz
DS slew rate	SR	1.125	-	-	V/ns	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Output DATA (referenced to CLK)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

5.10.3 LCD Interface Timing

Figure 5-20 HV_IF Vertical Timing

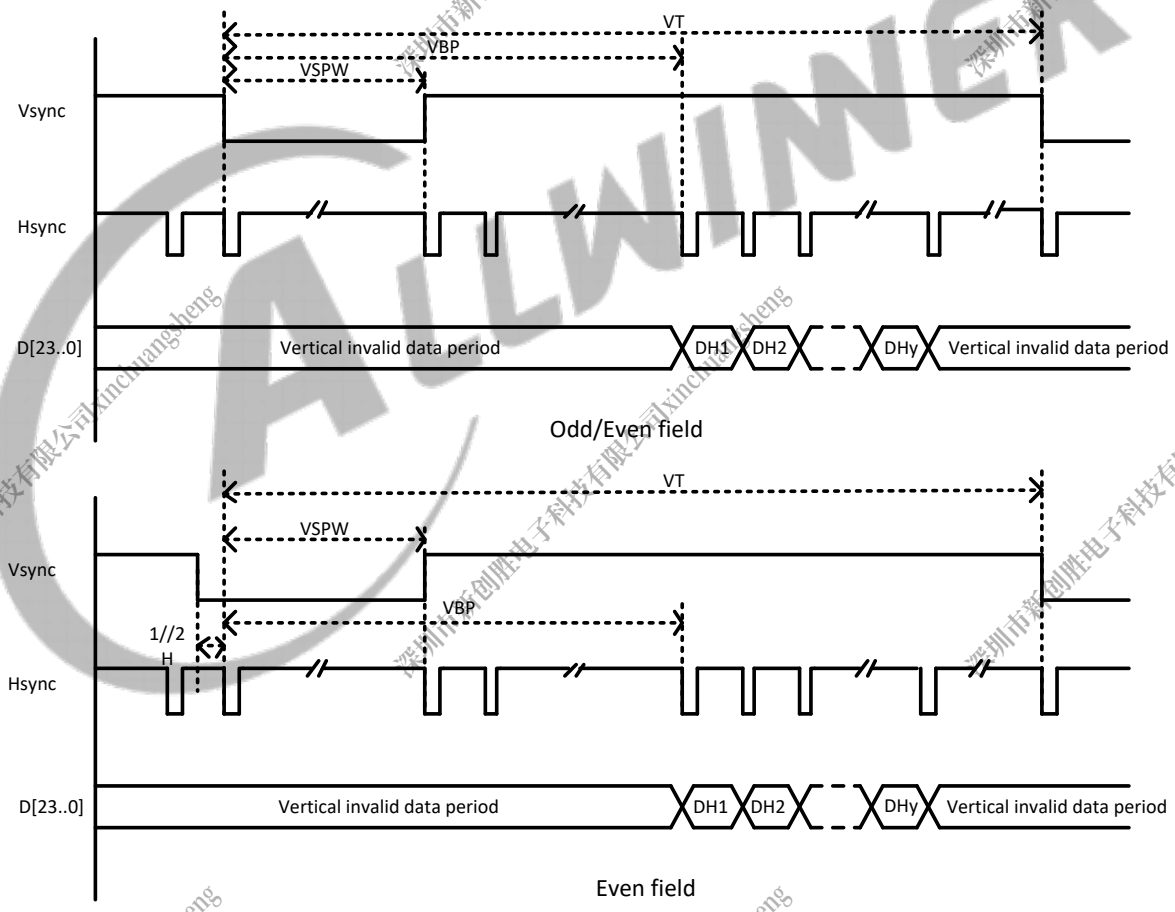
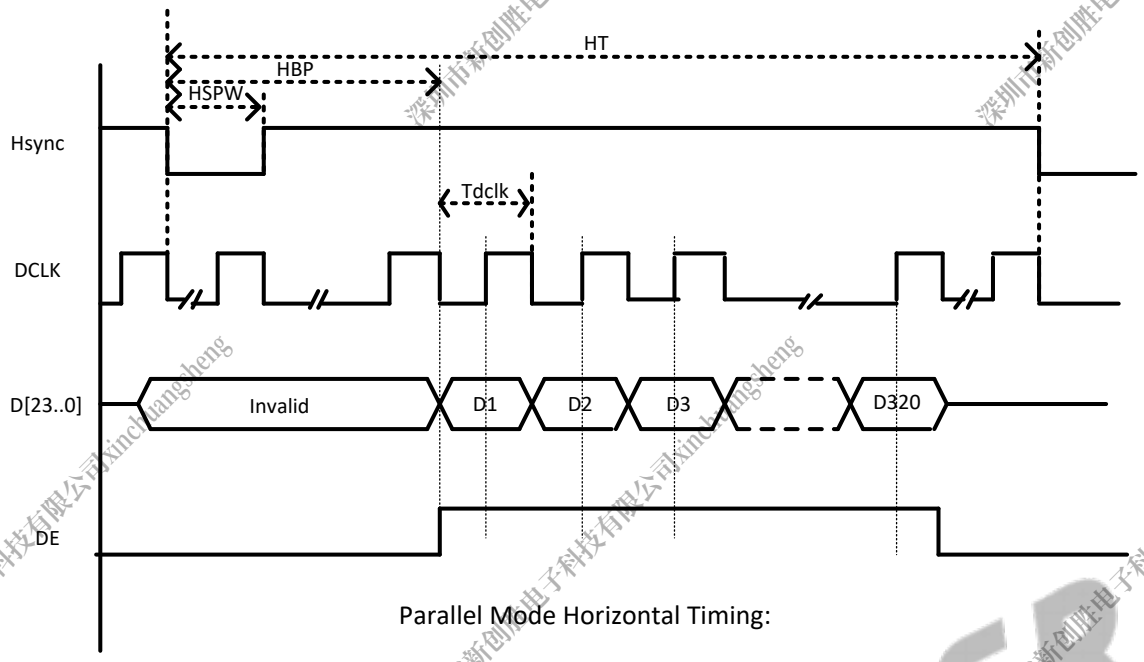
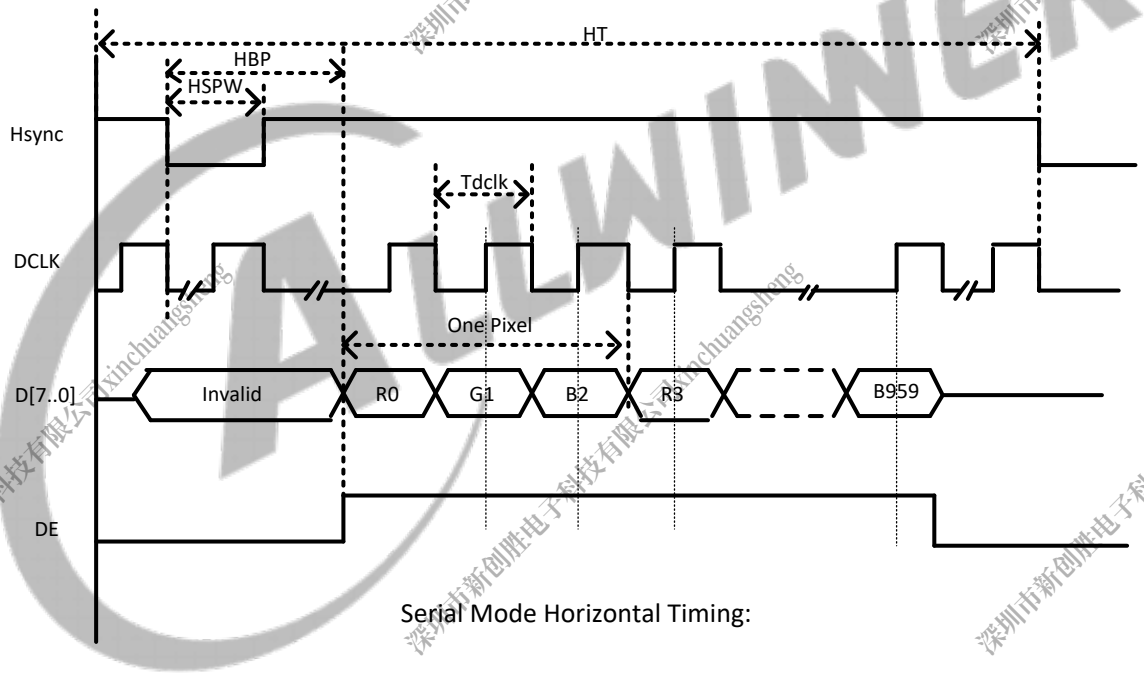


Figure 5-21 HV_IF Horizontal Timing



Parallel Mode Horizontal Timing:



Serial Mode Horizontal Timing:

Table 5-21 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5.9	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
Vsync Back Porch	tVBP	-	VBP+1	-	tHT

(1) Vsync: Vertical sync, indicates one new frame.
(2) Hsync: Horizontal sync, indicate one new scan line.
(3) DCLK: Dot clock, pixel data are sync by this clock.
(4) LDE: LCD data enable.
(5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

5.10.4 Parallel CSI Interface Timing

Figure 5-22 Parallel CSI Data Sample Timing

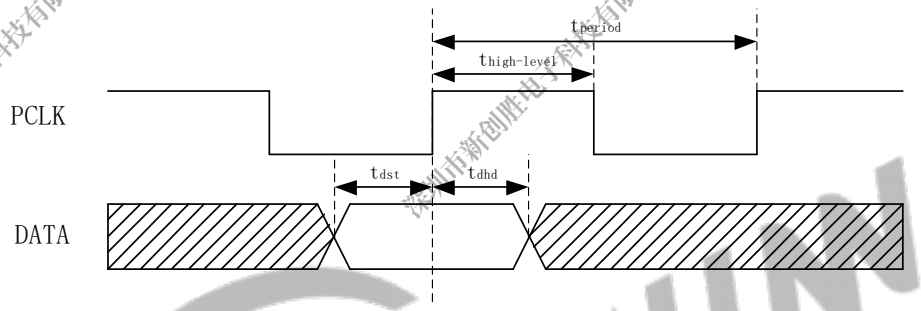


Table 5-22 Parallel CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.73	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.10.5 MIPI CSI Interface Timing

Figure 5-23 MIPI CSI Interface Timing

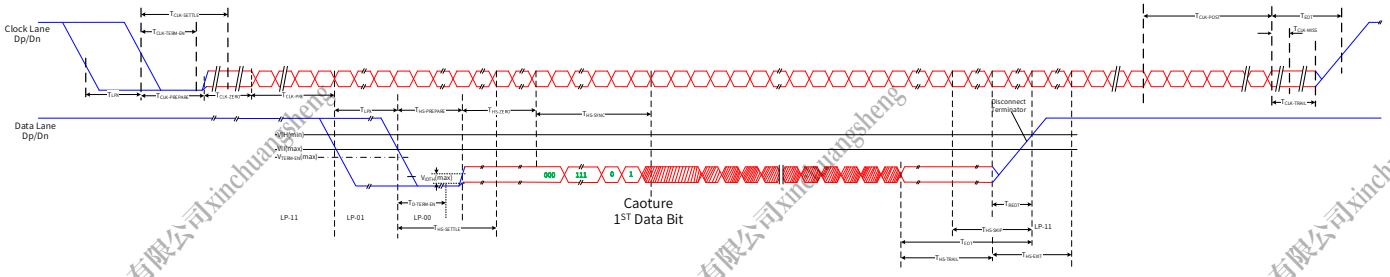


Table 5-23 MIPI CSI Interface Timing Constants

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	(1), (6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns	(5)
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	(5)
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	(5)
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns	(6), (7)
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	(6)
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	(5)
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	(5)
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns + 4*UI		(6)
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start			105ns + n*12*UI		(3), (5)

Parameter	Description	Min	Typ	Max	Unit	Notes
	of the LP-11 state following a HS burst.					
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	(5)
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85ns + 6*UI	ns	(5)
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns	(5)
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6*UI		145ns + 10*UI	ns	(6)
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40			ns	(6)
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60ns + n*4*UI)			ns	(2), (3), (5)
T_{INIT}		100			ns	(5)
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	(4), (5)
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2	ns	
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	5*T_{LPX}			ns	(5)

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns	(5)
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2*T_{LPX}$	ns	(5)
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	(5)

NOTE

(1) The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

(2) If a > b then max (a, b) = a otherwise max (a, b) = b.

(3) Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

(4) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

(5) Transmitter-specific parameter.

(6) Receiver-specific parameter.

(7) The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

5.10.6 MIPI DPHY Interface Timing

Figure 5-24 MIPI DPHY Timing

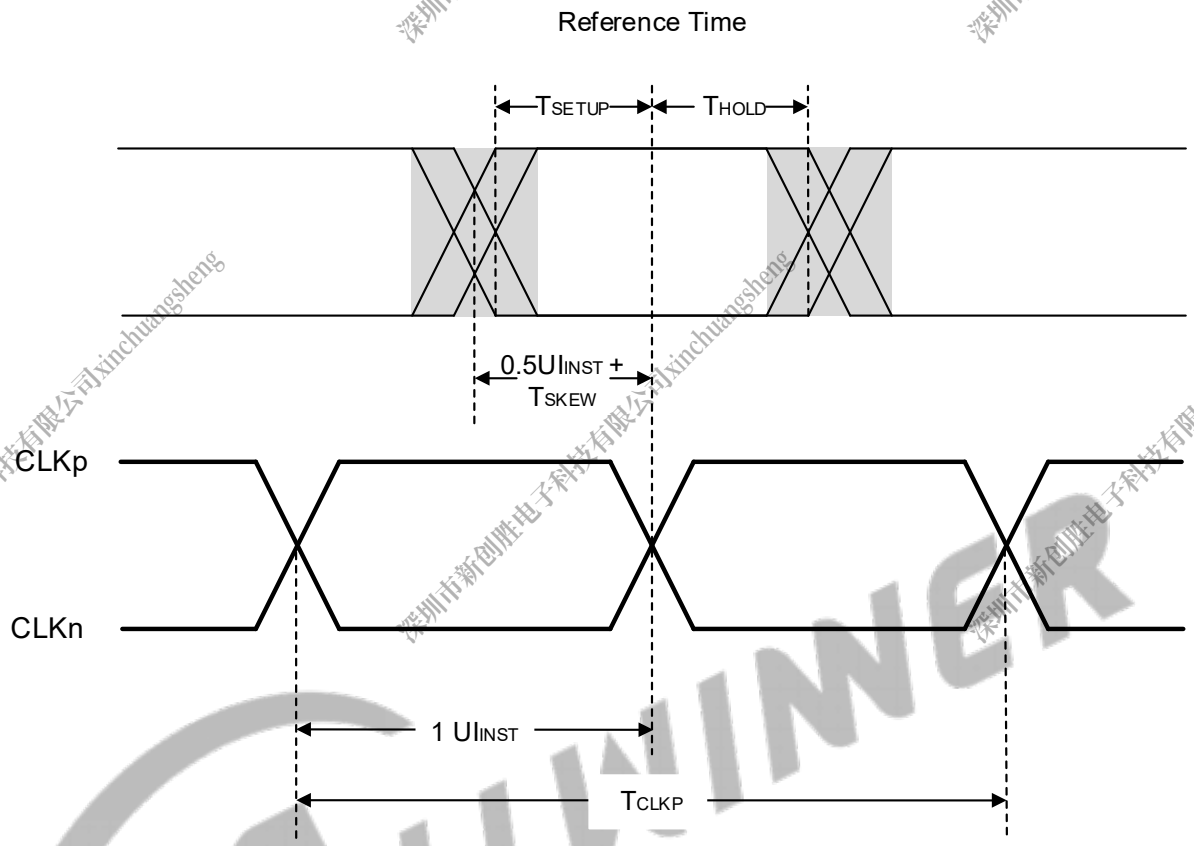


Table 5-24 MIPI DPHY Timing Constants

Parameter	Symbol	Units in Ulinst			Oprational Frequency in Gbps	
		Min	Max	Total	Min	Max
Data to Clock Skew	$T_{skew[tx]}$	-0.15	0.15	0.3	0.08	1.0
		-0.20	0.20	0.4	>1.0	1.5
Data to Clock Setup Time	$T_{setup[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5
Clock to Data Hold Time	$T_{hold[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5

5.10.7 GMAC Interface Timing

5.10.7.1 RGMII

Figure 5-25 RGMII Receive Timing

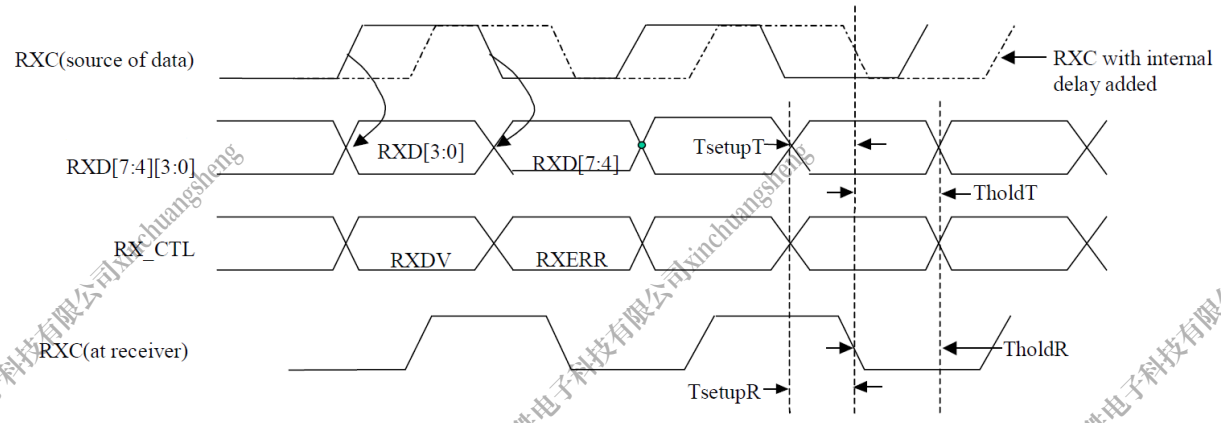


Figure 5-26 RGMII Transmit Timing

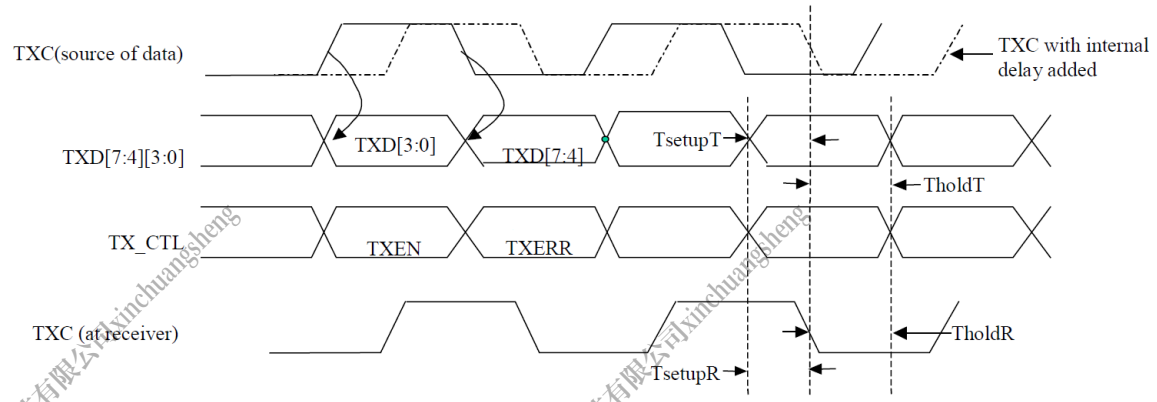


Table 5-25 RGMII Timing Parameters

Parameter	Description	Min	Typical	Max	Unit
Tcyc	Clock Cycle Duration *note1	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to clock output setup(at Transmitter integrated delay)	1.2	2.0		ns
TholdT	Data to clock output hold(at Transmitter integrated delay)	1.2	2.0		ns
TsetupR	Data to clock input setup(at Receiver integrated delay)	1.0	2.0		ns

Parameter	Description	Min	Typical	Max	Unit
TholdR	Data to clock input hold(at Receiver integrated delay)	1.0	2.0		ns
For 10Mbps and 100Mbps, Tcyc will scale 400ns±40ns and 40ns±4ns.					

5.10.7.2 RMII

Figure 5-27 RMII Receive Timing

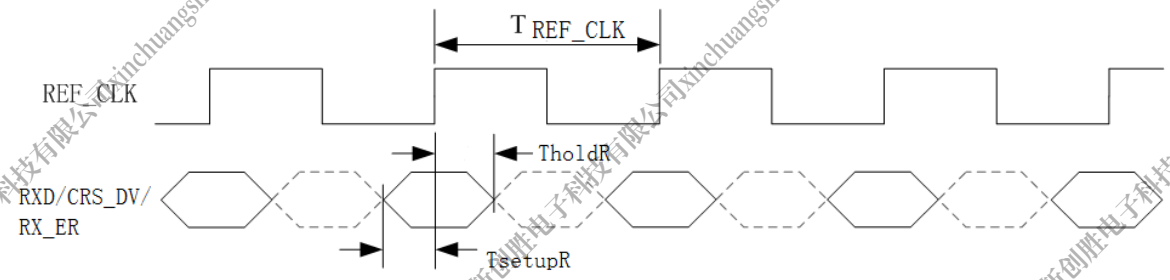


Figure 5-28 RMII Transmit Timing

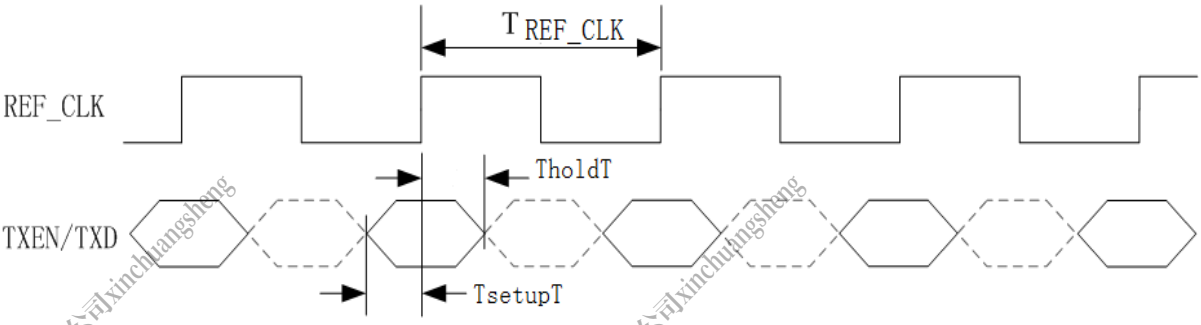


Table 5-26 RMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

5.10.8 SPI Interface Timing

Figure 5-29 SPI Writing Timing

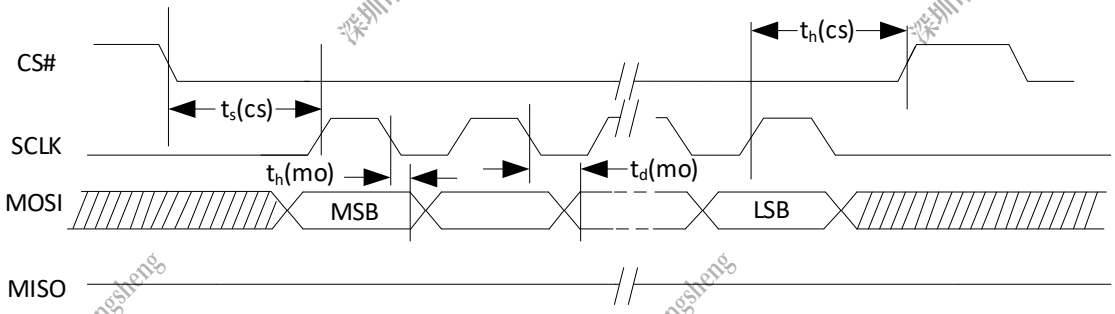


Figure 5-30 SPI Reading Timing

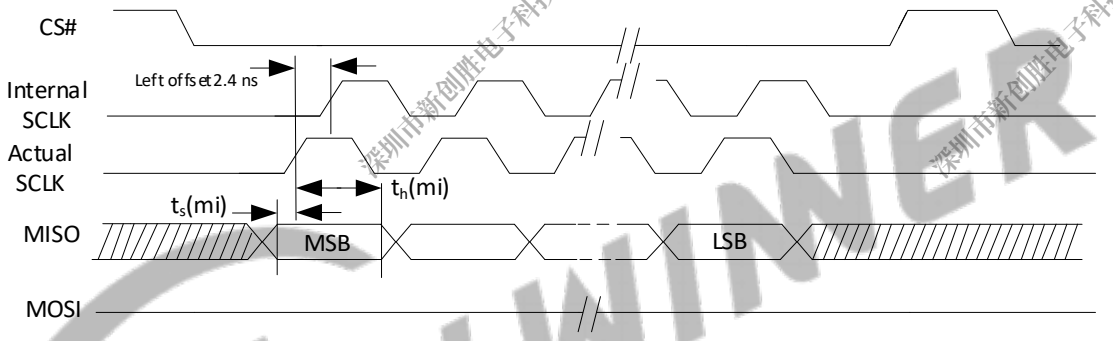


Table 5-27 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	t_s(cs)	-	2T(1)	-	ns
CS# Active Hold Time	t_h(cs)	-	2T(1)	-	ns
Data output Delay Time	t_v(mo)	-	T(1)/2-3	-	ns
Data output Hold Time	t_h(mo)	-	T(1)/2-3	-	ns
Data In Setup Time	t_s(mi)	0.2	-	-	ns
Data In Hold Time	t_h(mi)	0.2	-	-	ns
(1) T is the cycle of clock.					

5.10.9 SPI-DBI Interface Timing

Figure 5-31 DBI 3-line Serial Interface Timing

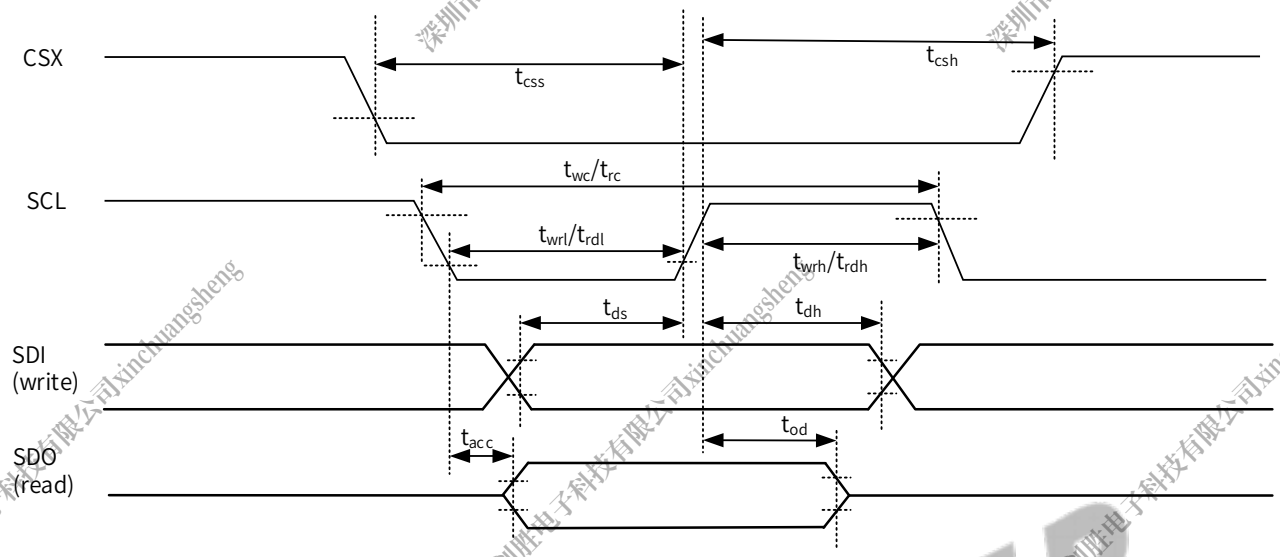


Table 5-28 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-29 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10(1)	50	ns
	Output disable time	t_{od}	15(1)	50	ns

Signal	Parameter	Symbol	Min	Max	Unit
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 5-32 DBI 4-line Serial Interface Timing

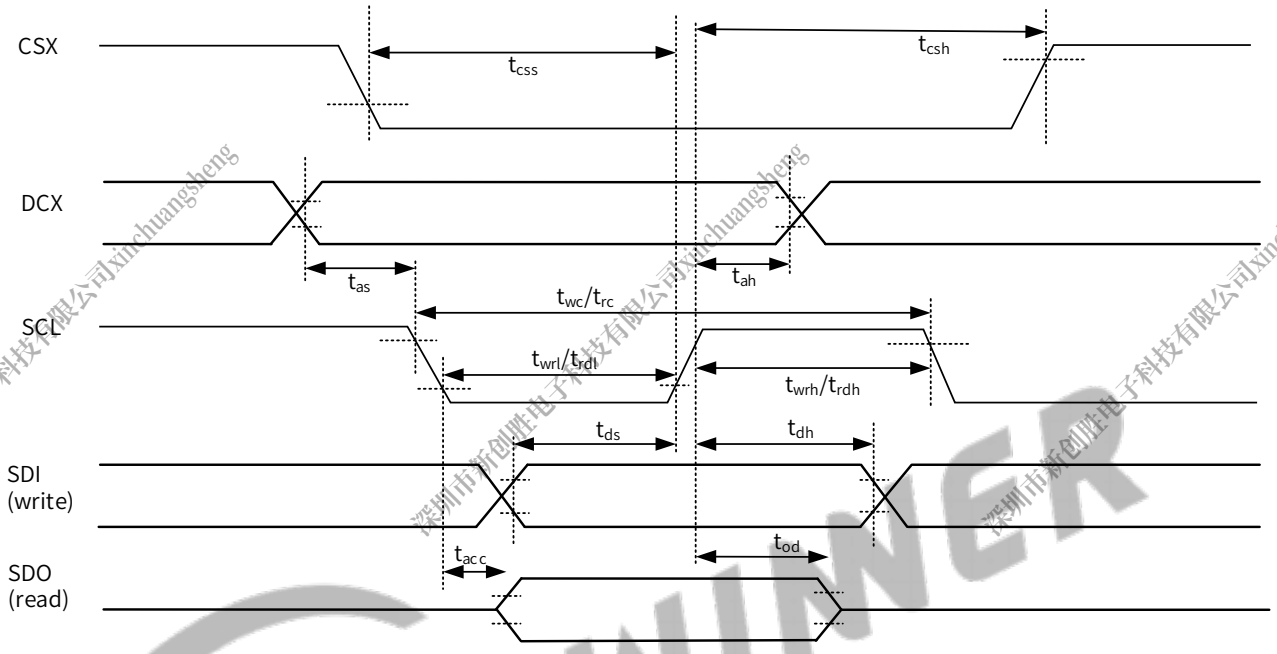


Table 5-30 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-31 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns

Signal	Parameter	Symbol	Min	Max	Unit
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

5.10.10 SPI Flash Interface Timing

5.10.10.1 Controller Output to Target Input Timing

Figure 5-33 xSPI Target Data Input Timing

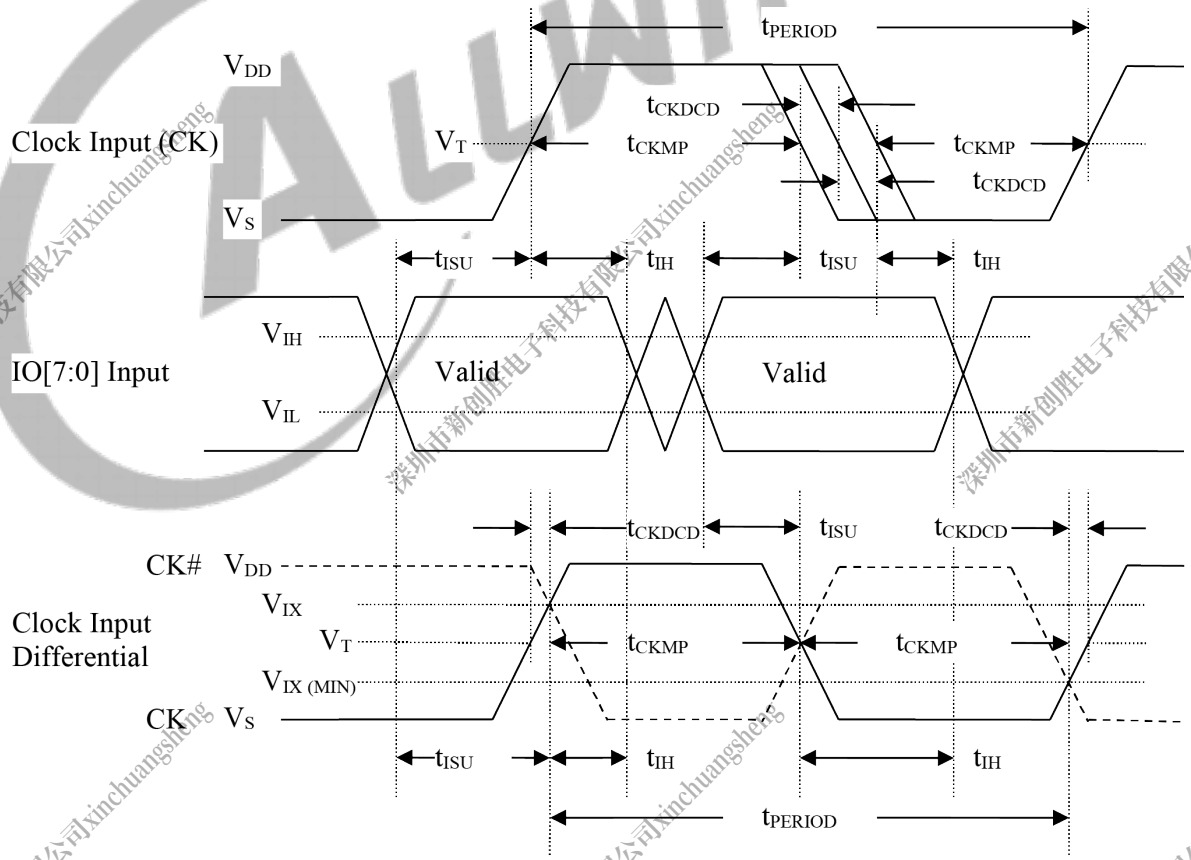


Table 5-32 Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	$V_{T\ (AC)}$	0.50 * V_{DD}	0.50 * V_{DD}	V
Input differential crossing (AC)	$V_{IX\ (AC)}$	0.4 * V_{DD}	0.60 * V_{DD}	V

Table 5-33 xSPI Device Input Timing

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Input CK									
Cycle Time Data Transfer Mode	t_{PERIOD}	6	-	7.5	-	10	-	ns	150 MHz (max) between the rising edges with respect to V_T.
Slew Rate	SR	0.94	-	0.75	-	0.56	-	V/ns	With respect to VIH/VIL.
Duty Cycle Distortion	t_{CKDCD}	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{CKMPW}	2.7	-	3.375	-	4.5	-	ns	With respect to V_T.
Input Signals (Referenced to CK)									
Input Setup Time (DTR)	t_{ISUddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (DTR)	t_{IHddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Setup Time (STR)	t_{ISU}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (STR)	t_{IH}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Slew Rate @ 1.8 V	SR	0.94	--	0.75	-	0.56	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 3.0 V	SR	1.72	-	1.37	-	1.03	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		

Note:

(1) xSPI-333: Up to 166 MHz; up to 333 MT/s.

(2) xSPI-266: Up to 133 MHz; up to 266 MT/s.

(3) xSPI-200: Up to 100 MHz; up to 200 MT/s.

5.10.10.2 Target Output to Controller Input Timing

Figure 5-34 xSPI Target Data Output Timing

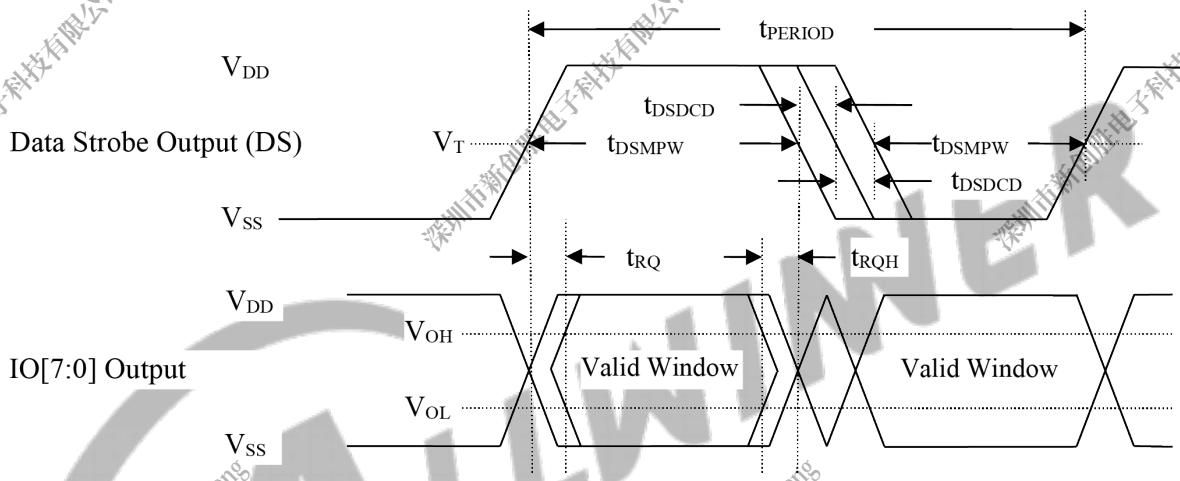


Table 5-34 xSPI Device Output Timing

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Data Strobe(2)					
Cycle Time Data Transfer Mode	t_{PERIOD}	10	-	ns	100 MHz (max) between the rising edges with respect to V_T.
Duty Cycle Distortion	t_{DSDCD}	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (tCKDCD) with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{DSMPW}	4.1	-	ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With respect to V_T.

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Output DATA (Referenced to DS)					
Output skew	t_{RQ}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Output hold skew	t_{RQH}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Note: (1) xSPI-200: Up to 100 MHz; up to 200 MT/s. (2) Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their relat ed (triggering) CK edges.					

5.10.11 UART Interface Timing

Figure 5-35 UART RX Timing

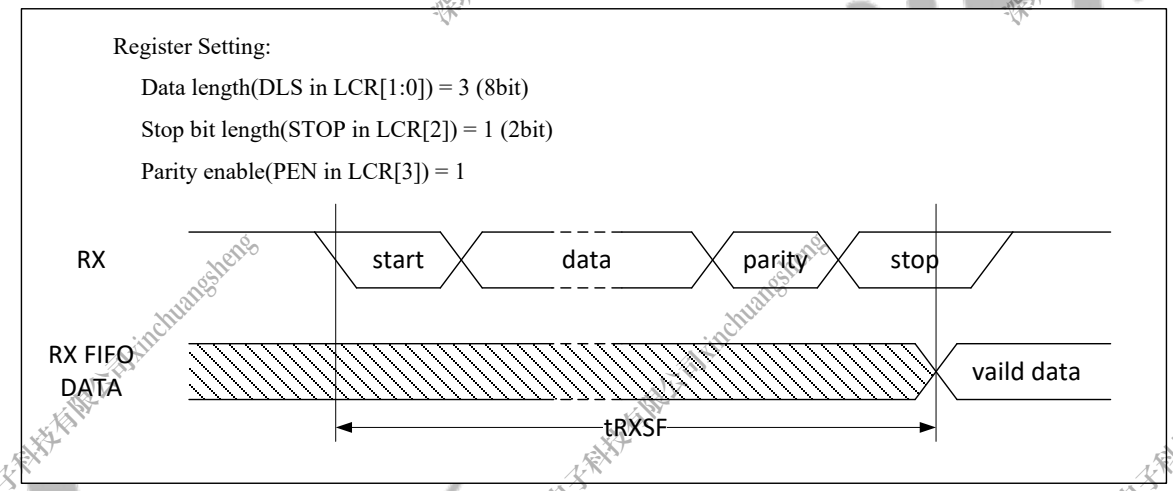


Figure 5-36 UART nCTS Timing

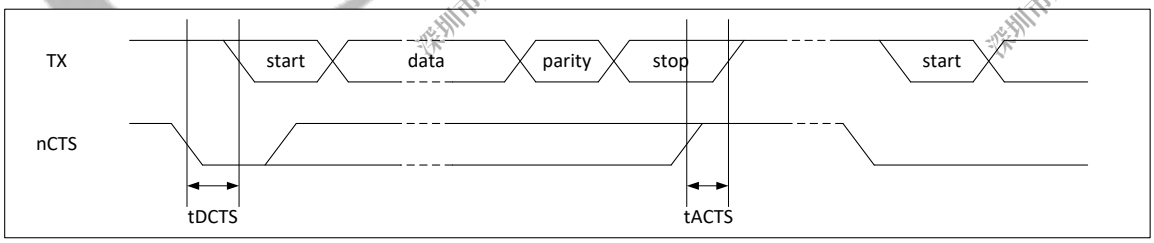


Figure 5-37 UART nRTS Timing

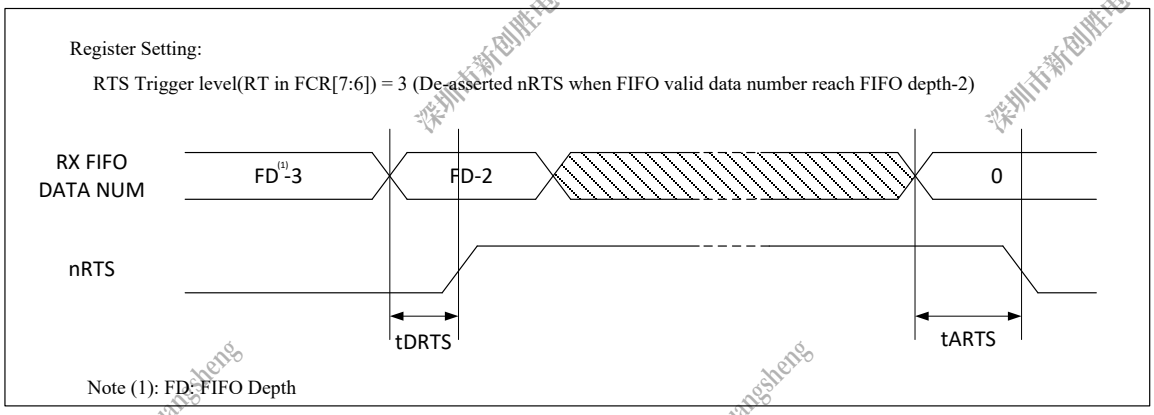


Table 5-35 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5*BRP(1)	-	11*BRP(1)	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1) /4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1) BRP: Baud-Rate Period.					

5.10.12 TWI Interface Timing

Figure 5-38 TWI Timing

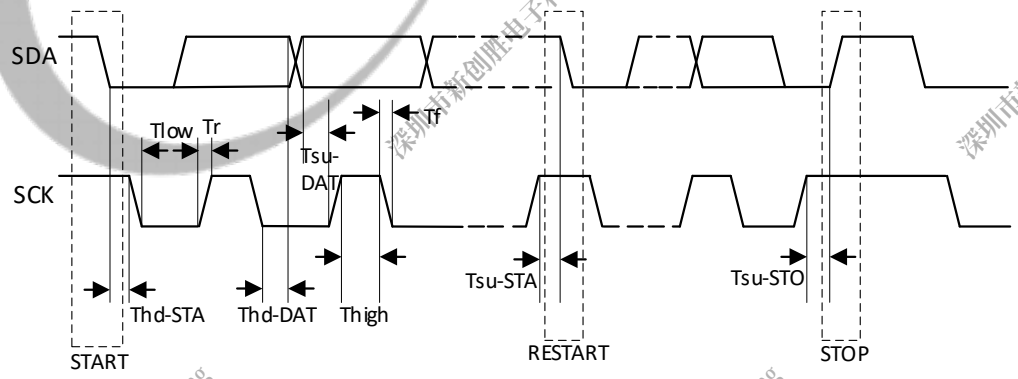


Table 5-36 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	5.0	-	-	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.10.13 I2S/PCM Interface Timing

Figure 5-39 I2S/PCM Timing in Master Mode

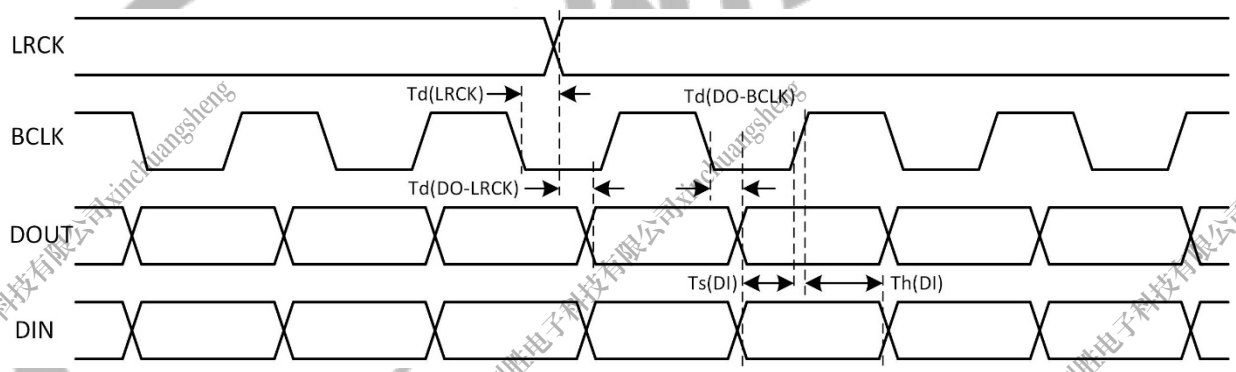


Table 5-37 I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

Figure 5-40 I2S/PCM Timing in Slave Mode

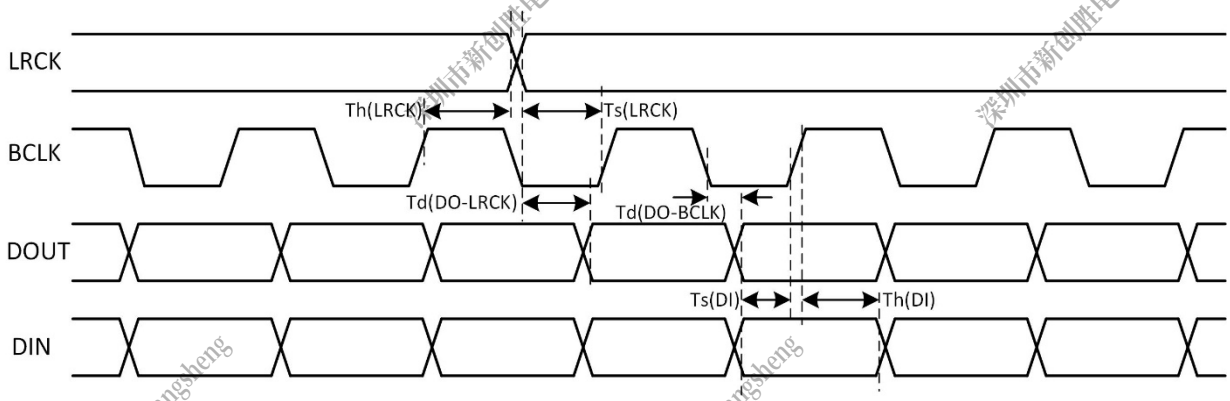


Table 5-38 Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.10.14 DMIC Interface Timing

Figure 5-41 DMIC Timing

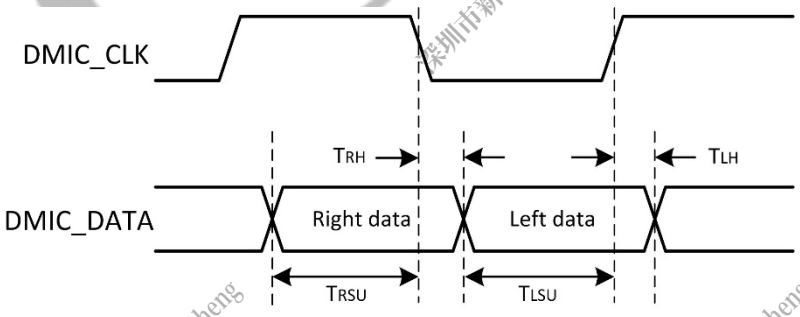


Table 5-39 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) Setup Time to Falling Edge of DMIC_CLK	T_{RSU}	15	-	-	ns

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) Hold Time from Falling Edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) Setup Time to Rising Edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) Hold Time From Rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

5.10.15 OWA Interface Timing

Figure 5-42 OWA Timing

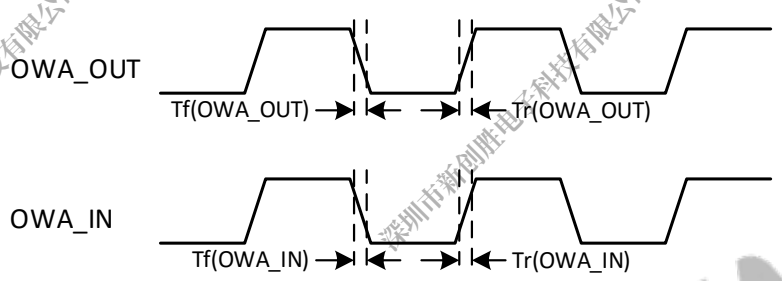


Table 5-40 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT Fall Time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN Rise Time	Tr(OWA_IN)	-	-	4	ns
OWA_IN Fall Time	Tf(OWA_IN)	-	-	4	ns

5.11 Power-Up and Power-Down Sequence

NOTE

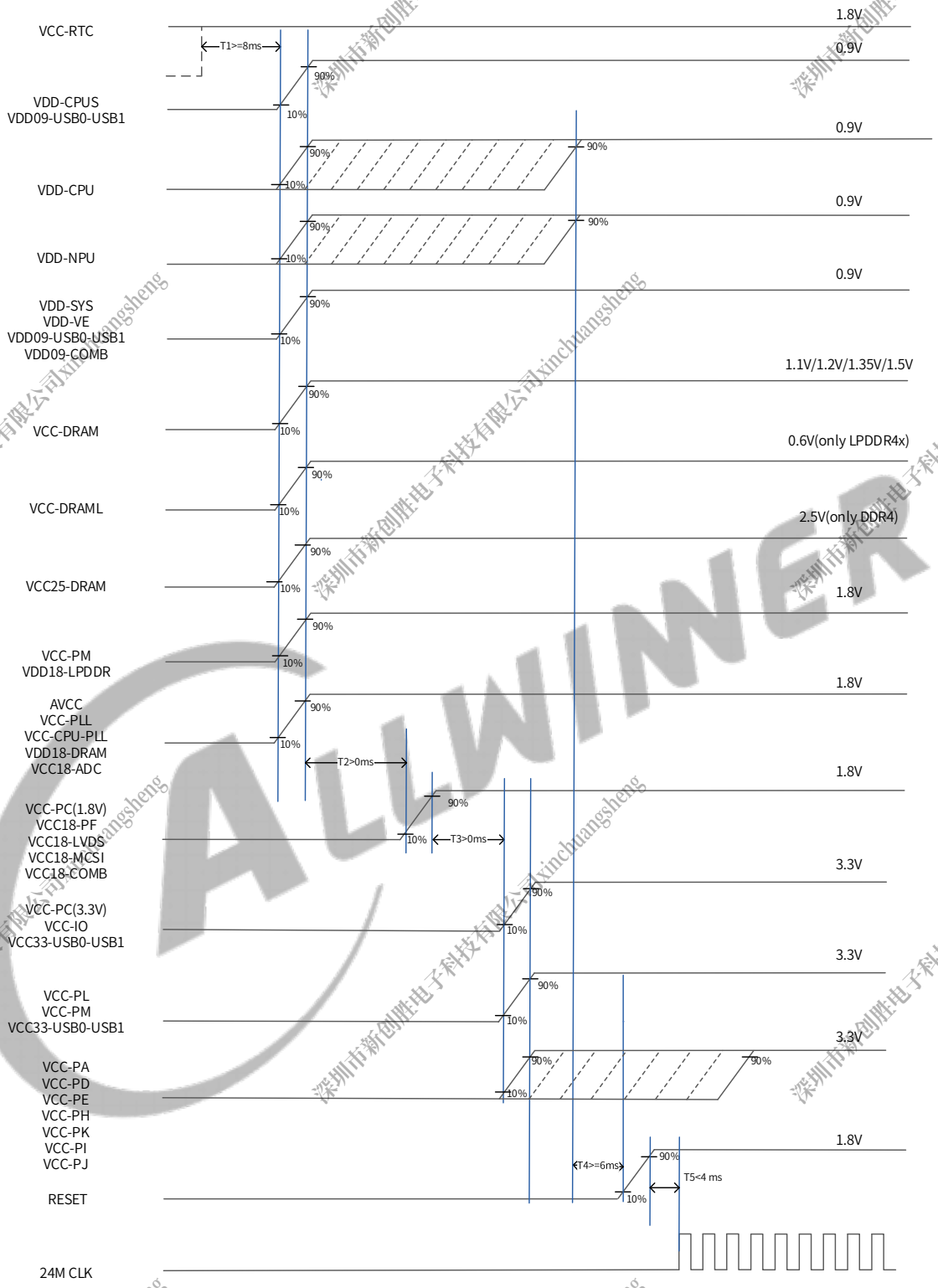
- All “Tn” markers represent different steps during power-on and power-off process and show the minimum time interval between current step and previous step.
- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90%-110% of their nominal voltage, unless stated otherwise.
- Different power rails at the same Tn step should become stable within 1ms.
- VCC25-DRAM and VDD18-LPDDR mentioned in Figure 5-43 and Figure 5-44 are external DRAM power supplies

5.11.1 Power-Up Sequence

Figure 5-43 shows an example of the power-up sequence. The description of the power-up sequence is as follows.

- VCC18-LVDS must be ramped before VCC-PD.
- VCC18-MCSI must be ramped before 3.3 V VCC-PK.
- VCC18-ADC must be ramped before VCC-PA.
- During the entire power on sequence, the reset signal must be held on low until all other power rails (except 24 MHz CLK) are stable for at least 6 ms.
- The 24MHz clock starts oscillating and be stable within 4 ms after the reset signal is stable.

Figure 5-43 Power-Up Sequence

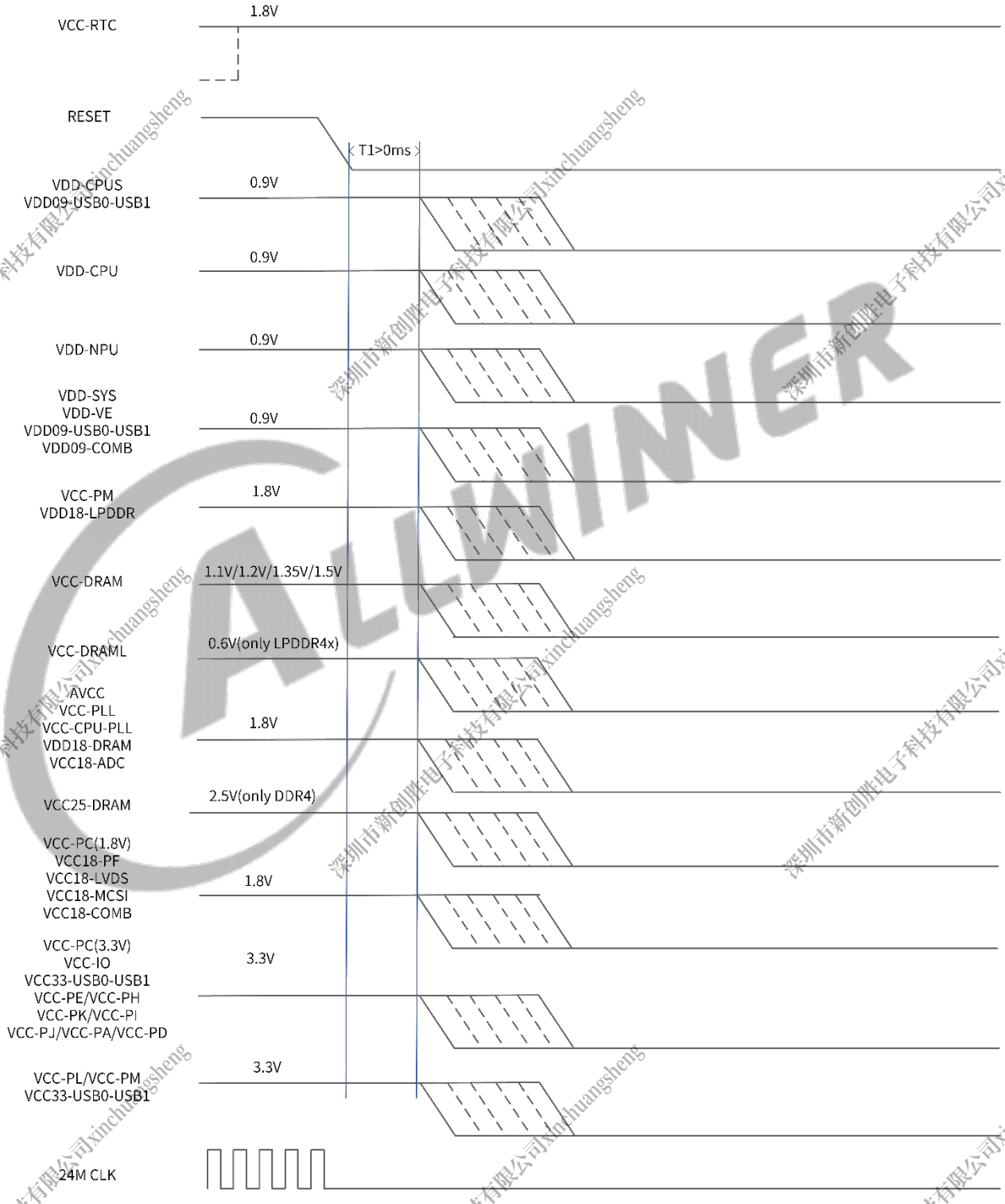


5.11.2 Power-Down Sequence

Figure 5-44 shows an example of the power-down sequence. The description of the power-down sequence is as follows.

- Reset this device. After PMIC receives the power-down command, pull-down RESET.
- VCC-RTC holds high.
- After RESET ramps down, other powers start to ramp down, and the ramp rate of each power rail is generally determined by the load on that power.

Figure 5-44 Power-Down Sequence



6 Temperature and Thermal Characteristics

6.1.1 Temperature

The following tables describe the temperature of the device

Table 6-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
T_a	Ambient Operating Temperature	-40	85	°C
T_{STG}	Storage Temperature	-40	150	°C

Table 6-2 Junction Temperature

Chip	Recommended Operating Temperature (T_j)		Absolute Maximum Junction Temperature	Unit
	Min	Max		
T536	-40	110	125	°C

6.1.2 Package Thermal Characteristics

The maximum chip junction temperature ($T_{J\ max}$) must never exceed the values given in Table 6-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-3 Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	23.04	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	8.64	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	-	-	°C/W

(1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

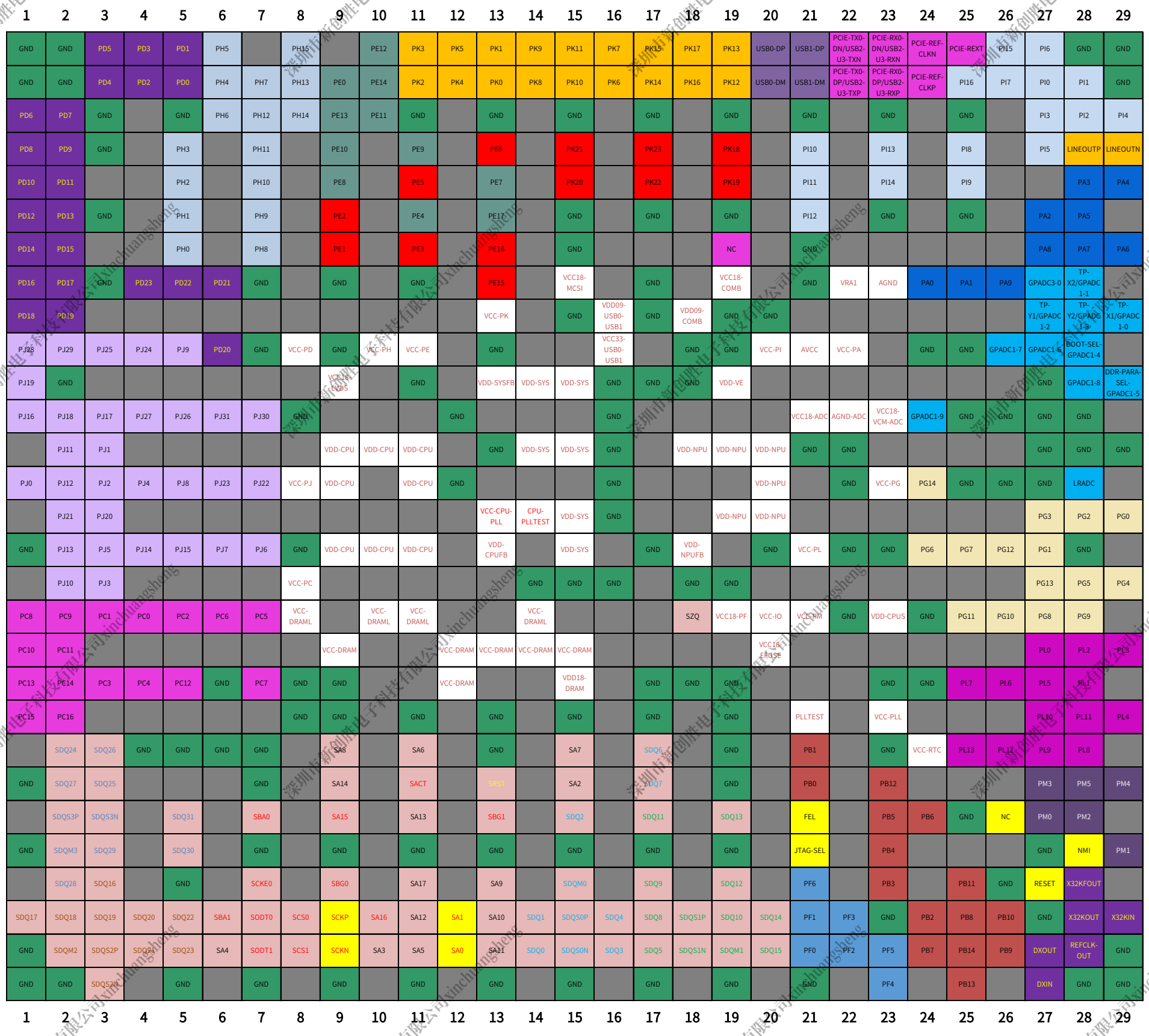
(2) The testing PCB is 4 layers, 114.5 mm x 76.2 mm body, and 1.6 mm thickness. Ambient temperature is 25 °C.

7 Pin Assignment

7.1.1 Pin Map

The following shows the ED-FCCSP 533 balls, 15 mm x 15 mm, 0.5 mm ball pitch, 0.3 mm ball size pin map.

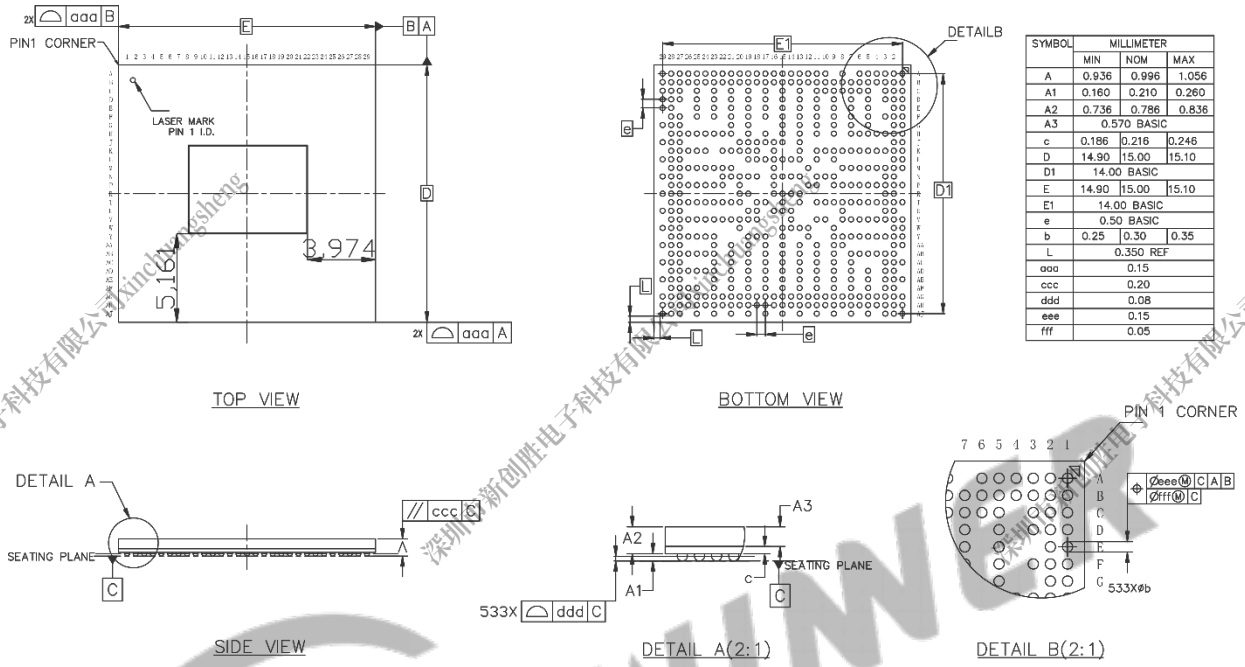
Figure 7-1 Pin Map



7.1.2 Package Dimension

The following figure shows the top, bottom, and side views of the package.

Figure 7-2 Package Dimension



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.936	0.996	1.056
A1	0.160	0.210	0.260
A2	0.736	0.786	0.836
A3		0.570 BASIC	
c	0.186	0.216	0.246
D	14.90	15.00	15.10
D1		14.00 BASIC	
E	14.90	15.00	15.10
E1		14.00 BASIC	
e		0.50 BASIC	
b	0.25	0.30	0.35
L		0.350 REF	
aaa		0.15	
ccc		0.20	
ddd		0.08	
eee		0.15	
fff		0.05	

8 Carrier, Storage and Backing Information

8.1 Carrier

NOTE

- The entire chip with ED-PCCSP package can withstand a maximum plane pressure of 1500 N (approximately 966.67 PSI pressure).
- Chips with ED-FCCSP package are susceptible to stress. Please be careful not to subject the chip to excessive stress during transportation or usage.

The following table shows matrix tray carrier information.

Table 8-1 Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	126 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

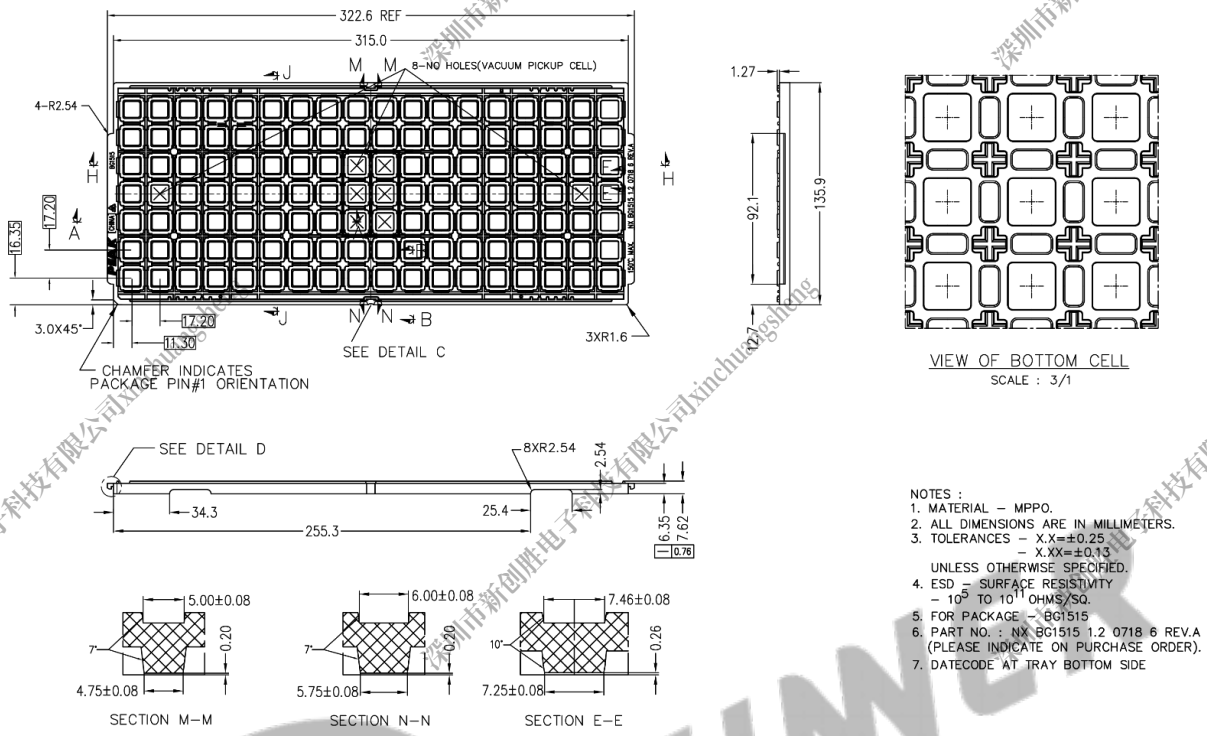
The following table shows packing quantity.

Table 8-2 Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
T536	15 mm x 15 mm	126	10	1260	6	7560

The following figure shows tray dimension drawing.

Figure 8-1 Tray Dimension Drawing



8.2 Storage

Reliability is affected if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-3 defines all MSL.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	⩽30°C / 85%RH
2	1 year	⩽30°C / 60%RH
2a	4 weeks	⩽30°C / 60%RH
3	168 hours	⩽30°C / 60%RH
4	72 hours	⩽30°C / 60%RH
5	48 hours	⩽30°C / 60%RH
5a	24 hours	⩽30°C / 60%RH
6	Time on Label (TOL)	⩽30°C / 60%RH

NOTE

The T536 device samples are classified as MSL3.

8.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 8-4 Bagged Storage Conditions

Packing Mode	Vacuum packing
Storage Temperature	20 26°C
Storage Humidity	40% 60%RH
Shelf Life	12 months

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 8-5 Out-of-bag Duration

Storage Temperature	20 26°C
Storage Humidity	40% 60%RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake chips if the conditions specified in section 8.2.2 and section 8.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

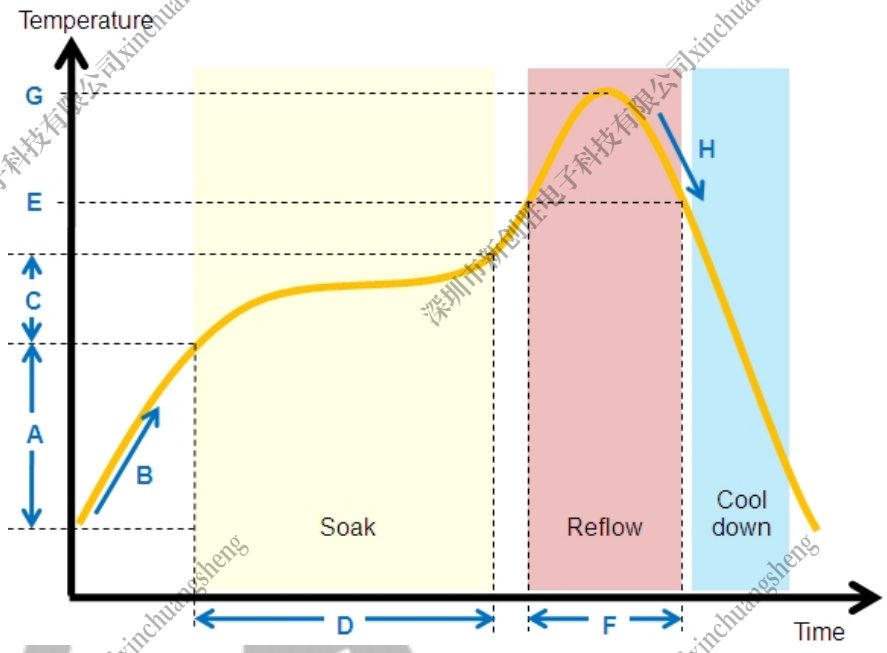


Table 9-1 Lead-free Reflow Profile Conditions

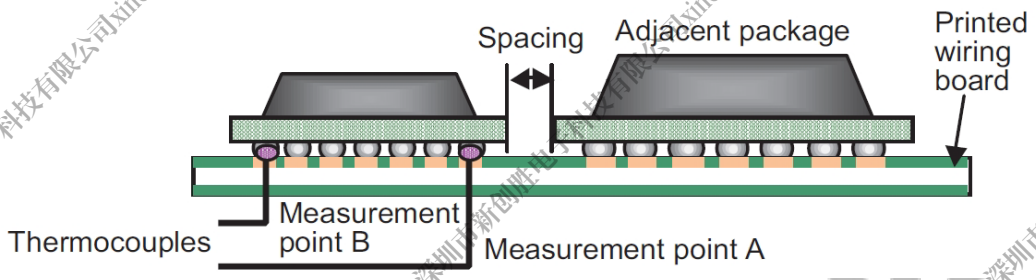
	QTI typical SMT reflow profile conditions (for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5–2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s
G	Peak temperature	240–250 °C

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
H	Cool down temperature rate	⩽4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe.

Figure 9-2 Measuring the Reflow Soldering Process



NOTE

To measure the temperature of the QFP-packaged chip, place the temperature probe directly at the pin.

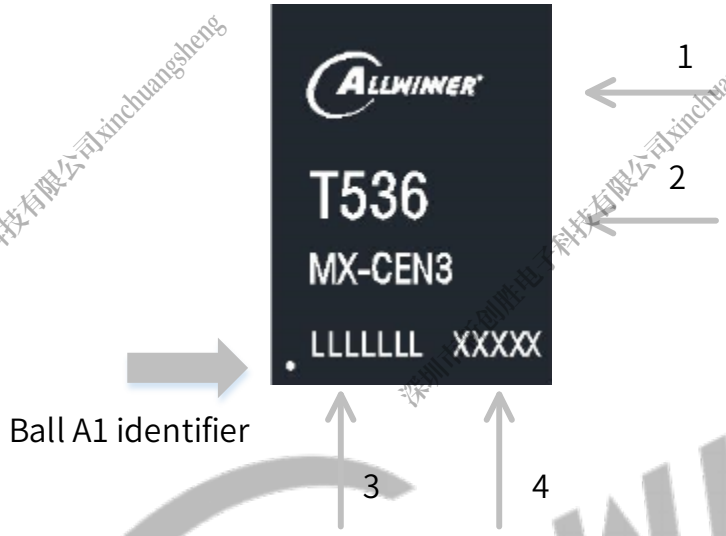
If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 Part Marking

10.1 T536MX-CEN3

The following figure shows the T536MX-CEN3 marking.

Figure 10-1 T536MX-CEN3 Marking



The following table describes the T536MX-CEN3 marking definitions.

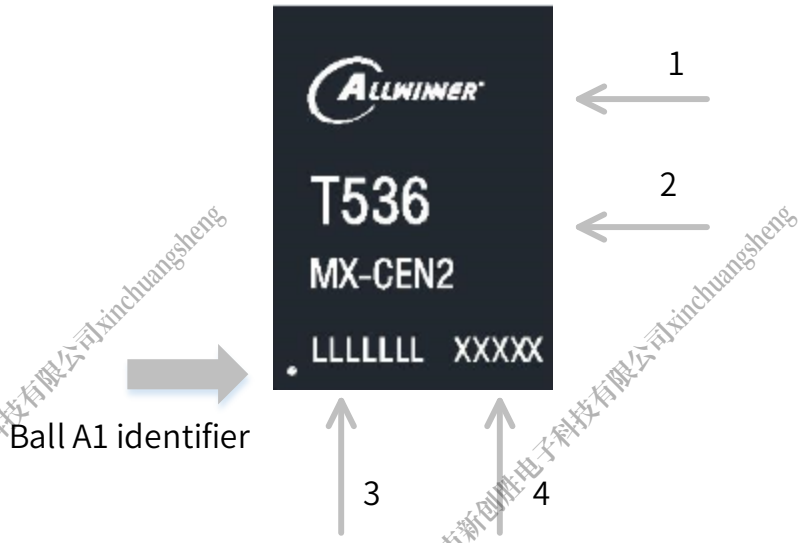
Table 10-1 T536MX-CEN3 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T536MX-CEN3	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.2 T536MX-CEN2

The following figure shows the T536MX-CEN2 marking.

Figure 10-2 T536MX-CEN2 Marking



The following table describes the T536MX-CEN2 marking definitions.

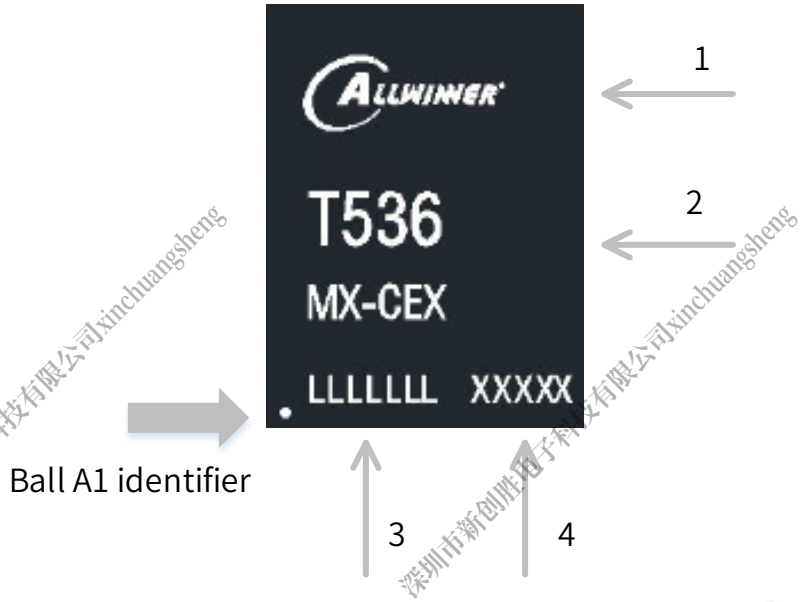
Table 10-2 T536MX-CEN2 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T536MX-CEN2	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.3 T536MX-CEX

The following figure shows the T536MX-CEX marking.

Figure 10-3 T536MX-CEX Marking



The following table describes the T536MX-CEX marking definitions.

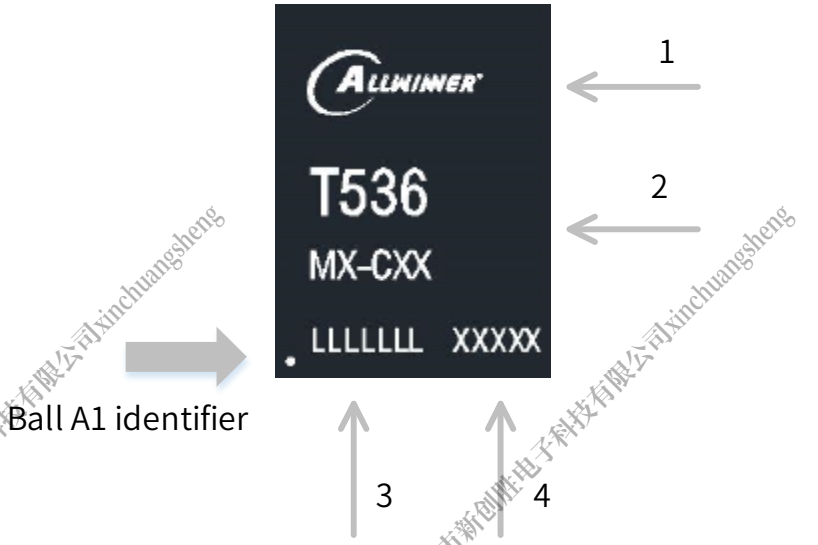
Table 10-3 T536MX-CEX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T536MX-CEX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.4 T536MX-CXX

The following figure shows the T536MX-CXX marking.

Figure 10-4 T536MX-CXX Marking



The following table describes the T536MX-CXX marking definitions.

Table 10-4 T536MX-CXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T536MX-CXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

Allwinner Technology Co., Ltd.
No.9 Technology Road 2, High-Tech Zone,
Zhuhai, Guangdong Province, China

Contact US:
Service@allwinnertech.com
www.allwinnertech.com