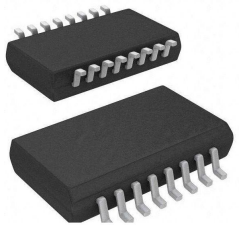
16 bit Σ-Δ Analog to Digital Converter

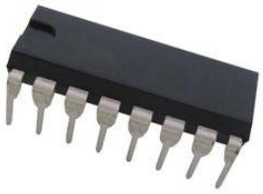
PRODUCT DESCRIPTION

The MS7705/MS7706 is an analog-to-digital converter for low-frequency measurement. It uses Σ-Δ conversion technology to realize 16 bit lossless code feature. The operating voltage range is 2.7V-3.3V or 4.75V-5.25V.

The MS7705/MS7706 is ideal for intelligent, micro-controller, or DSP-based systems. It can set gain, signal polarity and output rate through serial interface. Self calibration and system calibration can be applied to eliminate gain and offset errors of the system. The typical power dissipation is 20 μW in standby mode.



SOP16



DIP16

FEATURES

- MS7705：Two Fully Differential Input Channels
- MS7706：Three Pseudo Differential Input Channels
- 16 bit Lossless Code
- 0.003% Non-linearity
- PGA: Gain from 1 to 128
- Serial Port: SPI, QSPI, MICROWIRE, DSP Compatible
- Operating Voltage : 2.7V to 3.3V or 4.75V to 5.25V
- Maximum Power Dissipation : 1mW under 3V supply voltage
- Maximum Standby Current : 8μA
- SOP16 andDIP16 Package

APPLICATIONS

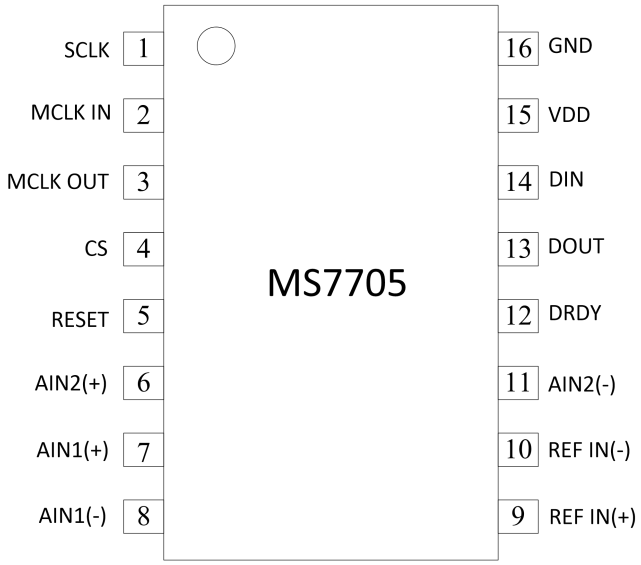
- Pressure Measurement
- Temperature Measurement
- Battery Monitoring
- Intelligent Transmitter

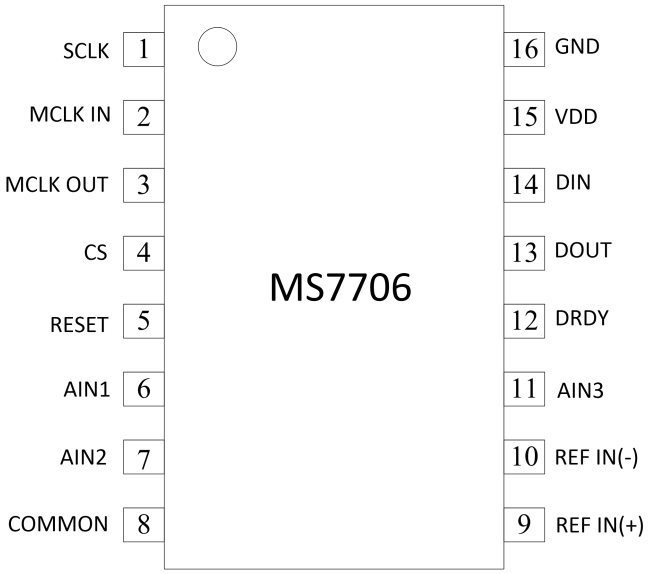
PRODUCT SPECIFICATION

Part Number	Package	Marking
MS7705	SOP16	MS7705
MS7705D	DIP16	MS7705D
MS7706D	DIP16	MS7706D
*MS7706	SOP16	MS7706

*Don't provide the package temporarily.
If necessary, please contact Ruimeng Sales Department.

PIN CONFIGURATION



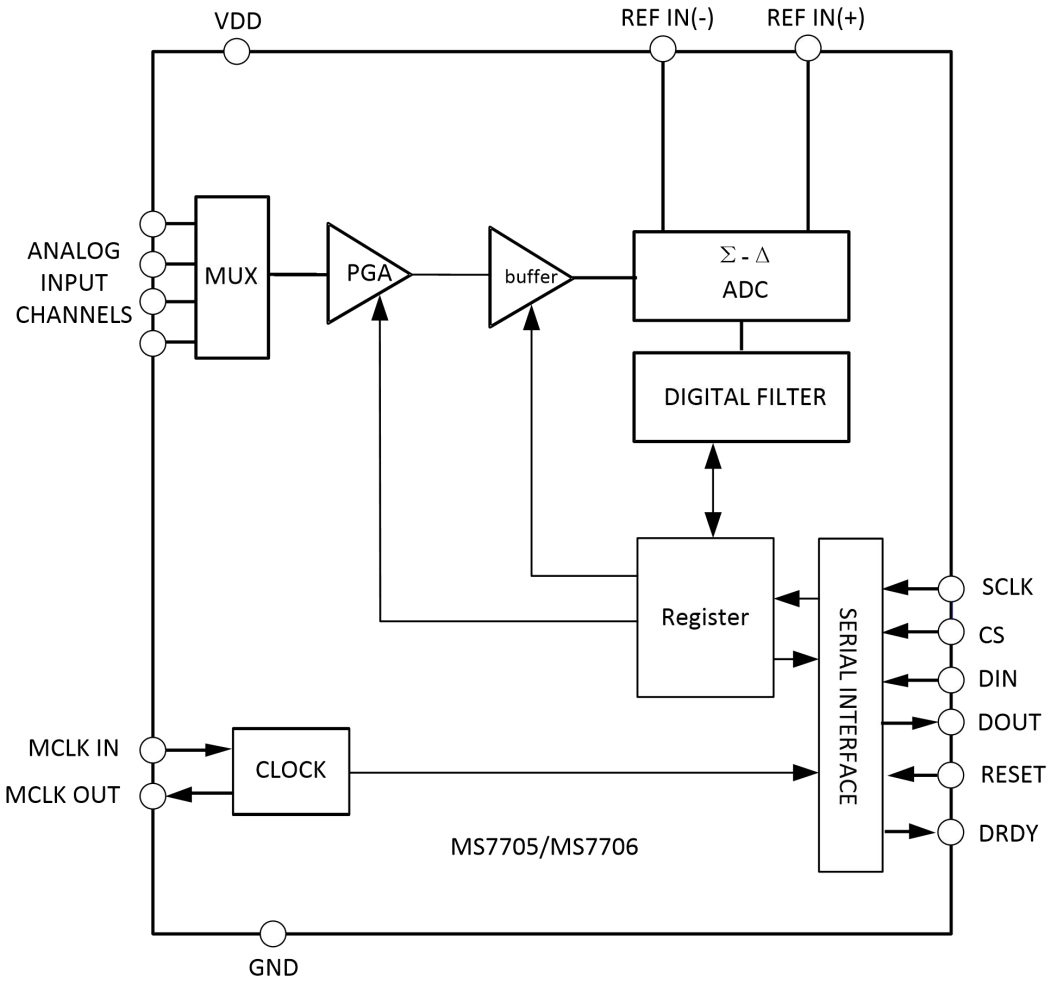


PIN DESCRIPTION

Pin	Name		Type	Description
	MS7705	MS7706		
1	SCLK	SCLK	I	Serial Clock Input
2	MCLK IN	MCLK IN	I	Master Clock Signal. It can be provided in the form of crystal / resonator or external clock. The crystal / resonator can be connected between MCLK IN and MCLK OUT pins. MCLK IN can also be driven by CMOS compatible clock, but MCLK OUT is not connected. The clock frequency ranges from 500kHz to 5MHz.
3	MCLK OUT	MCLK OUT	O	When master clock is crystal / resonator, it is connected between MCLK IN and MCLK OUT pins. If the external clock is received at MCLK IN, the MCLK OUT will provide an inverted clock signal. This clock can be used to provide clock source for external circuit and drive a CMOS load. MCLK OUT can be turned off by CLKDIS bit in clock register.
4	CS	CS	I	Chip Selection, Low Level Active Logic Input.
5	RESET	RESET	I	Reset Input. Low Level Active Input.
6	AIN2(+)	AIN1	I	For MS7705, Positive Input of Differential Analog Input Channel 2; For MS7706, Input of Analog Input Channel 1.
7	AIN1(+)	AIN2	I	For MS7705, Positive Input of Differential Analog Input Channel 1; For MS7706, Input of Analog Input Channel 2.
8	AIN1(-)	COMMON	I	For MS7705, Negative Input of Differential Analog Input Channel 1; For MS7706, COMMON Input, Analog Channel 1, 2, 3 Input with reference to the Input Terminal.
9	REF IN(+)	REF IN(+)	I	Reference Input Terminal. The reference input is differential and requires that REFIN (+) must be greater than REFIN (-). REFIN (+) can be any value between VDD and GND.
10	REF IN(-)	REF IN(-)	I	Reference Input Terminal. REFIN (-) can be any value between VDD and GND , and REFIN (+) must be greater than REFIN (-).
11	AIN2(-)	AIN3	I	For MS7705, Negative Input of Differential Analog Input Channel 2. For Ms7706, Input of Analog Input Channel 3 .

Pin	Name		Type	Description
	MS7705	MS7706		
12	DRDY	DRDY	O	Logic Output. The low logic level on this output terminal indicates that the newest results can be obtained from the MS7705/7706 data register. After completing read operation of a complete output word, DRDY immediately returns to high level. If there is no data readout between the two output updates, DRDY will return to high level for 500× tCLKIN before the next update occures . When DRDY is high level, it can not read data, for fear that data in the data register is being read when it is updating. After data is updated, DRDY returns to low level. DRDY is also used to indicate when MS7705/7706 has completed the calibration sequence of chip.
13	DOUT	DOUT	O	Serial Data Output Terminal.
14	DIN	DIN	I	Serial Data Input Terminal.
15	VDD	VDD	P	Power Supply Voltage, + 2.7V - + 5.25V.
16	GND	GND	P	Ground Reference Point of Internal Circuit.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability.The absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power Supply	VDD	-0.3 ~ +7.0	V
Analog Input Voltage	V_{IN}	-0.3 ~ VDD+0.3	V
Reference Input Voltage	V_{REF}	-0.3 ~ VDD+0.3	V
Digital Input Voltage	V_{DIN}	-0.3 ~ VDD+0.3	V
Digital Output Voltage	V_{OUT}	-0.3 ~ VDD+0.3	V
Operating Temperature	T_A	-40 ~ 85	°C
Storage Temperature	T_{stg}	-60 ~ 150	°C
Welding Temperature(10s)		260	°C
Electrostatic Protection	ESD	>4000	V

ELECTRICAL CHARACTERISTICS

If not specified, VDD=3V,5V or 2.5V, REF(+)=1.225V, REF(-)=GND, MCLK IN=2.4576MHz.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Static Performance						
No Missing Code				16		Bits Min
Output Noise			See Table 1 and Table 3			
Integral Nonlinearity				±0.003		%of FSR MAX
Unipolar Offset Error						
Unipolar Offset Drift				0.5		μV/°C
Bipolar Offset Error						
Bipolar Offset Drift		GAIN=1~4		0.5		μV/°C
		GAIN=8~128		0.1		
Positive Full-Scale Error						
Full-Scale Drift				0.5		μV/°C
GAIN Error						
GAIN Drift				0.5		ppm of FSR/°C
Bipolar Negative Full-Scale Error				±0.001	±0.003	%of FSR
Bipolar Negative Full-Scale Drift		GAIN=1~4		1		μV/°C
		GAIN=8~128		0.6		μV/°C
Analog Input / Reference Input (if not specified, Only for AIN and REF IN)						
Common-Mode Rejection	CMR	VDD=5V, GAIN=1		96		dB
		VDD=5V, GAIN=2		105		
		VDD=5V, GAIN=4		110		
		VDD=5V, GAIN=8~128		130		
		VDD=3V, GAIN=1		105		
		VDD=3V, GAIN=2		110		
		VDD=3V, GAIN=4		120		
		VDD=3V, GAIN=8~128		130		
Normal-Mode 50 Hz Rejection		Filter Notches 25Hz,50Hz, $\pm 0.02 \times f_{NOTCH}$		98		dB
		Filter Notches 20Hz,60Hz, $\pm 0.02 \times f_{NOTCH}$		98		dB
		Filter Notches 25Hz,50Hz, $\pm 0.02 \times f_{NOTCH}$		150		dB
		Filter Notches 20Hz,60Hz, $\pm 0.02 \times f_{NOTCH}$		150		dB

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Absolute/Common REF IN Voltage			GND		VDD	V
Absolute/Common AIN Voltage		Register Bit BUF=0	GND-0.1		VDD+0.03	V
Absolute/Common AIN Voltage		Register Bit BUF =1	GND+0.05		VDD-1.5	V
AIN DC Input Current					1	nA
AIN Sampling Capacitance					10	pF
AIN Differential Voltage Range		Register Bit BUF =1		0 to $+V_{REF}$/GAIN		V
		Register Bit BUF =0		$\pm V_{REF}$/GAIN		
AIN Input Sampling Rate	f_s			GAIN×f_{CLKIN}/64		MHz
				f_{CLKIN}/8		
Reference Input Range		VDD=2.7~3.3V V_{REF}=1.225±1%	1		1.75	V
		VDD=4.75~5.25V V_{REF}=2.5±1%	1		3.5	
REF IN Input Sampling Rate				f_{CLKIN}/64		MHz
Logic Input						
Input Current		All Inputs Except MCLK IN		±1nA	±1μA	μA
		MCLK IN		±2	±10	
Input Low Voltage, Except SCLK and MCLK IN	V_{INL}	VDD=5V			0.8	V
		VDD=3V			0.4	
Input High Voltage, Except SCLK and MCLK IN	V_{INH}	VDD=3 or 5V	2.0			V
SCLK Input Voltage	V_{T+}	VDD=5V	1.4		3	V
	V_{T-}		0.8		1.4	
	V_{T+}- V_{T-}		0.4		0.8	
	V_{T+}	VDD=3V	1		2	
	V_{T-}		0.4		1.1	
	V_{T+}- V_{T-}		0.375		0.8	
MCLK IN Low Voltage		VDD=5V			0.8	V
		VDD=3V			0.4	

Logic Output (including MCLK OUT)						
Output Low Voltage		VDD=5V, I_{SINK}=800μA (Except for MCLK OUT)			0.4	V
		VDD=3V, I_{SINK}=100μA (Except for MCLK OUT)			0.4	
Output High Voltage		VDD=5V, I_{SOURCE}=200μA (Except for MCLK OUT)	4			V
		VDD=3V, I_{SOURCE}=100μA (Except for MCLK OUT)	VDD-0.6			
Floating State Leakage Current					±10	μA
Floating State Capacitance				9		pF
Data Output Code		Unipolar Mode	Binary			
		Bipolar Mode	Offset Binary			
System Calibration						
Positive Full-Scale Limit		GAIN=1~128			$(1.05\times V_{REF})$/GAIN	V
Negative Full-Scale Limit		GAIN=1~128			$-(1.05\times V_{REF})$/GAIN	V
Offset Limit		GAIN=1~128			$-(1.05\times V_{REF})$/GAIN	V
Input Range		GAIN=1~128	$(0.8\times V_{REF})$/GAIN		$(2.1\times V_{REF})$/GAIN	V
Power Dissipation (Apply External Clock , CLKDIS =1, Digital I/Ps = 0V or VDD)						
Power Supply Current	VDD=2.7~3.3V					
	I_{DD}	BUF=0, f_{CLKIN}=1MHz, GAIN＝1~128			0.32	mA
		BUF=1, f_{CLKIN}=1MHz, GAIN＝1~128			0.6	
		BUF=0, f_{CLKIN}=2.4576MHz, GAIN＝1~4			0.4	
		BUF=0, f_{CLKIN}=2.4576MHz, GAIN＝8~128			0.6	
		BUF=1, f_{CLKIN}=2.4576MHz, GAIN＝1~4			0.7	
		BUF=1, f_{CLKIN}=2.4576MHz, GAIN＝8~128			1.1	
Power Supply Current	VDD=4.75~5.25V					
	I_{DD}	BUF=0, f_{CLKIN}=1MHz, GAIN＝1~128			0.45	mA
		BUF=1, f_{CLKIN}=1MHz, GAIN＝1~128			0.7	
		BUF=0, f_{CLKIN}=2.4576MHz, GAIN＝1~4			0.6	
		BUF=0, f_{CLKIN}=2.4576MHz, GAIN＝8~128			0.85	
		BUF=1, f_{CLKIN}=2.4576MHz, GAIN＝1~4			0.9	
		BUF=1, f_{CLKIN}=2.4576MHz, GAIN＝8~128			1.3	
Power Supply Rejection	PSRR	VDD=5V, GAIN＝8~128		90		dB

TIMING CHARACTERISTICS

If there is no special description, VDD=2.7 to 5.25V, GND=0V; fCLKIN=2.4576MHz, input logic low is 0V, input logic high is VDD.Test at 25°C. All input signals meet tR=tF =5ns (10% to 90% of VDD) and start timing from 1.6V. See Figure 1 and Figure 2.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Master Clock Frequency	f_{CLKIN}		0.4		2.5	MHz
Master Clock Cycle	t_{CLKIN}		2500		400	ns
Master Clock Low Level Time	$t_{CLK\ LO}$		$0.4\times t_{CLKIN}$			ns
Master Clock High Level Time	$t_{CLK\ HI}$		$0.4\times t_{CLKIN}$			ns
CS High Level Time	t_1			$500\times t_{CLKIN}$		ns
RESET Pulse Width	t_2		100			ns
Read Operation						
DRDY to CS Setup Time	t_3		0			
CS Falling Edge to SCLK Rising Edge Setup Time	t_4		120			ns
SCLK Falling Edge to Data Valid Delay	t_5	VDD=5V	0		80	ns
		VDD=3V	0		100	
SCLK High Pulse Width	t_6		100			ns
SCLK Low Pulse Width	t_7		100			ns
CS Rising Edge to SCLK Rising Edge Holding Time	t_8		0			ns
Bus Release Time after SCLK Rising Edge	t_9	VDD=5V	10		60	ns
		VDD=3V	10		100	
SCLK Falling Edge to DRDY High Level[5]	t_{10}				100	ns
Write Operation						
CS Falling Edge to SCLK Rising Edge Setup Time	t_{11}		120			ns
Data Valid to SCLK Rising Edge Setup Time	t_{12}		30			ns
Data Valid to SCLK Falling Edge Setup Time	t_{13}		20			ns
SCLK High Pulse Width	t_{14}		100			ns
SCLK Low Pulse Width	t_{15}		100			ns
CS Rising Edge to SCLK Rising Edge Holding Time	t_{16}		0			ns

OUTPUT NOISE

Table 1 and 3 show the output noise (RMS) of MS7705/7706 at the selectable notch and -3dB frequencies, selected by the clock registers FS0 and FS1. Data is at bipolar input, VREF=+2.5V/1.225, VDD=5V/3V.

These values are typical values when the device operates in buffered or unbuffered mode and the analog input voltage is 0V. Table 2 and Table 4 show the peak to peak output noise. Note that the resolution represented by these numbers is not code blinking. These values apply to the bipolar input range in buffered and unbuffered modes (VREF = + 2.5V / + 1.225). These values are typical and close to the nearest LSB. It's required that CLKDIV bit of clock register is set 0.

Table 1. Output Noise VS. Gain and Output Rate @ 5V

Filter Notch and Data Rate	-3dB Freq								
		Gain=1	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
60Hz	15.72Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
250Hz	65.5Hz	110	49	31	17	8	3.6	2.3	1.7
500Hz	131Hz	550	285	145	70	41	22	9.1	4.7
MCLK IN = 1MHz									
20Hz	5.24Hz	4.1	2.1	1.2	0.75	0.7	0.66	0.63	0.6
25Hz	6.55Hz	5.1	2.5	1.4	0.8	0.75	0.7	0.67	0.62
100Hz	26.2Hz	110	49	31	17	8	3.6	2.3	1.7
200Hz	52.4Hz	550	285	145	70	41	22	9.1	4.7

Table 2. Effective Bits VS. Gain and Output Rate @5V

Filter Trap and Data Rate	-3dB Freq								
		Gain=1	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	16	16	16	16	16	16	15	14
60Hz	15.72Hz	16	16	16	16	15	14	14	13
250Hz	65.5Hz	13	13	13	13	13	13	12	12
500Hz	131Hz	10	10	10	10	10	10	10	10

MCLK IN = 1MHz									
20Hz	5.24Hz	16	16	16	16	16	16	15	14
25Hz	6.55Hz	16	16	16	16	15	14	14	13
100Hz	26.2Hz	13	13	13	13	13	13	12	12
200Hz	52.4Hz	10	10	10	10	10	10	10	10

Table 3. Output Noise VS. Gain and Output Rate @ 3V

Filter Notch and Data Rate	-3dB Freq	Gain=1	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
60Hz	15.72Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
250Hz	65.5Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
500Hz	131Hz	270	135	65	41	22	9.7	5.1	3.3
MCLK IN = 1MHz									
20Hz	5.24Hz	3.8	2.4	1.5	1.3	1.1	1.0	0.9	0.9
25Hz	6.55Hz	5.1	2.9	1.7	1.5	1.2	1.0	0.9	0.9
100Hz	26.2Hz	50	25	14	9.9	5.1	2.6	2.3	2.0
200Hz	52.4Hz	270	135	65	41	22	9.7	5.1	3.3

Table 4. Effective Bits VS. Gain and Output Rate @3V

Filter Trap and Data Rate	-3dB Freq	Gain=1	Gain=2	Gain=4	Gain=8	Gain=16	Gain=32	Gain=64	Gain=128
MCLK IN = 2.4576MHz									
50Hz	13.1Hz	16	16	15	15	14	13	13	12
60Hz	15.72Hz	16	16	15	14	14	13	13	12
250Hz	65.5Hz	13	13	13	13	12	12	11	11
500Hz	131Hz	10	10	10	10	10	10	10	10
MCLK IN = 1MHz									
20Hz	5.24Hz	16	16	15	15	14	13	13	12
25Hz	6.55Hz	16	16	15	14	14	13	13	12
100Hz	26.2Hz	13	13	13	13	12	12	11	11
200Hz	52.4Hz	10	10	10	10	10	10	10	10

FUNCTIONAL DESCRIPTION

On-chip Register

MS7705/7706 contains registers (communication register,setting register,clock register,data register, test register, zero-scale calibration register, full-scale calibration register), which are accessed through serial ports of the device.

Communication Register (RS2, RS1, RS0=0, 0, 0)

Communication register is an 8-bit register, which can read and write data. The data written determines which register the next read or write occurs on. Once the next read or write operation is completed on the selected register, the interface returns to the communication register to receive a write operation. This is interface default state. After power on or reset, MS7705/7706 is in this default state, waiting for a write operation to the communication register. Under the condition of lost interface sequence, if write operation at DIN level persists for a long time (at least 32 serial clock cycles), MS7705/7706 will go back to default state.

Table 5. Communication Register

Bit	7	6	5	4	3	2	1	0
Name	0/DRDY(0)	RS2(0)	RS1(0)	RS0(0)	R/W(0)	STBY(0)	CH1(0)	CH0(0)

Note: The content in bracket is the default value of power on reset.

Table 6. Function Description of Each Bit of Communication Register

Register	Description
0/DRDY	To write to the communication register, a "0" must be written to this one. If "1" is written to this, subsequent bits will not be able to write to the register. It will stay in this bit until a "0" is written to it, and the next seven bits will be loaded into the communication register. For read operation, this bit provides DRDY flag of the device. The state of the bit is the same as the state of DRDY output pin.
RS2-RS0	Register Select Bit. These three bits choose which register to read / write next.
R/W	Read / Write Selection. "0" indicates that the next operation is write, and "1" indicates that the next operation is read.
STBY	Standby Mode. If "1" is written to this bit, it is in wait or power down mode. In this mode, the power supply current consumed by the device is only 10 μA. In standby mode, the device will maintain its calibration coefficient and control word information. Write "0" and the device is in normal operation mode.
CH1, CH0	Channel Selection. These two bits select a channel for data conversion or access calibration coefficient, as shown in Table 8. Three pairs of calibration registers in the device are used to store the calibration coefficients. Table 8 and Table 9 indicate which channel combinations have independent calibration coefficients. When CH1 is logic 1 and CH0 is logic 0, AIN (-) /COMMON input pin of MS7705/7706 is shorted to itself respectively. This can be used as a test method to evaluate the noise performance (without external noise source). In this mode, the AIN1 (-) /COMMON input terminal must be connected to an external voltage and within the allowable common mode voltage range.

Table 7. Register Selection

RS2	RS1	RS0	Register	Register bits
0	0	0	Communication Register	8 bits
0	0	1	Setting Register	8 bits
0	1	0	Clock Register	8 bits
0	1	1	Data Register	16 bits
1	0	0	Test Register	8 bits
1	0	1	None	
1	1	0	Offset Register	24 bits
1	1	1	Gain Register	24 bits

Table 8. MS7705 Input Channel Selection

CH1	CH0	AIN(+)	AIN(-)	Calibration Register Pair
0	0	AIN1(+)	AIN1(-)	Register Pair0
0	1	AIN2(+)	AIN2(-)	Register Pair1
1	0	AIN1(-)	AIN1(-)	Register Pair0
1	1	AIN1(-)	AIN2(-)	Register Pair2

Table 9. MS7706 Input Channel Selection

CH1	CH0	AIN	Reference	Calibration Register Pair
0	0	AIN1	COMMON	Register Pair0
0	1	AIN2	COMMON	Register Pair1
1	0	COMMON	COMMON	Register Pair0
1	1	AIN3	COMMON	Register Pair2

Setting Register (RS2, RS1, RS0 = 0, 0, 1), Power On / Reset Status: 01Hex

The setting register is an 8-bit register, which can read and write data.

Table 10. Setting Register

Bit	7	6	5	4	3	2	1	0
NAME	MD1(0)	MD0(0)	G2(0)	G1(0)	G0(0)	B/U(0)	BUF(0)	FSYNC(1)

Table 11. Function Description of Each Bit of Setting Register

Register	Description
MD1, MD0	MSC Mode Control. These two bits control the working mode of MSC, as shown in Table 12.
G2-G0	Gain Select Bit. These three bits control the gain of PGA on chip, as shown in Table 13.
B/U	Bipolar / Unipolar Control. "0" indicates bipolar operation and "1" indicates unipolar operation.
BUF	Buffer Control. This bit is "0", the on-chip buffer is short, and the VDD consumption current is reduced. When this bit is "1", the on-chip buffer is connected with analog input, and it can connect to a higher impedance input source.
FSYNC	Filter Synchronization. At high level, the node of digital filter, control logic and calibration control logic are in reset state, and the analog modulator is also controlled in reset state. At low level, the modulator and filter begin to process data and produce a valid word within 3 × (1 / output rate) time (i.e. filter setup time). Fsync doesn't affect digital interface and reset the DRDY output(if it is low).

Table 12. Working Mode Selection

MD1	MD0	Working Mode
0	0	Normal Mode. In this mode, the converter performs normal analog-to-digital conversion.
0	1	Self Calibration. Self calibration is activated on the channels selected by CH1 and CH2 of the communication register. This is a step calibration. After completing this task, it returns to normal mode, that is, MD1 and MD0 are 0. At the beginning of calibration, the DRDY output pin or DRDY bit is high level and returns to low level after calibration. At this time, a new valid word is generated in the data register. The zero-scale calibration is performed at the input internal short circuit (zero input), and the full-scale calibration is performed at the selected gain and internally generated VREF / selected gain conditions.
1	0	Zero-scale System Calibration. Activate zero-scale system calibration on the channel selected by CH1 and CH2 of the communication register. When this calibration sequence is used, the input voltage on the analog input is calibrated at the selected gain. During calibration, the input voltage should be stable. At the beginning of calibration, DRDY outputs or the DRDY bit is high, and the zero-scale system returns to low level after the calibration is completed. At this time, a new valid word is generated on the data register. At the end of calibration, the device returns to normal mode, that is, MD1 and MD0 are 0.
1	1	Full-scale System Calibration: activates full-scale system calibration on the selected input channel. In this calibration sequence, the input voltage on the analog input terminal completes the calibration at the selected gain. The input voltage should be stable during calibration. At the beginning of calibration, DRDY outputs or DRDY bit is high level, and after the full-scale system calibration is completed, it returns to low level. At this time, a new valid word is generated in the data register. At the end of calibration, the device returns to normal mode, that is, MD1 and MD0 are 0.

Table 13. Gain Selection

G2	G1	G0	Gain
0	0	0	1
0	0	1	2
0	1	0	4
0	1	1	8
1	0	0	16
1	0	1	32
1	1	0	64
1	1	1	128

Clock Register (RS2, RS1, RS0 = 0,1,0), Power On / Reset Status: 05Hex

The clock register is an 8-bit register that can read / write data.

Table 14. Clock Register

Bit	7	6	5	4	3	2	1	0
Name	ZERO(0)	ZERO(0)	ZERO(0)	CLKDIS(0)	CLKDIV(0)	CLK(1)	FS1(0)	FS0(0)

Table 15. Function Description of Each Bit of Clock Register

Register	Description
ZERO	Must write 0.
CLKDIS	Master Clock Inhibit Bit. Logic "1" prevents the master clock from outputting on the MCLK out pin. When prohibited, MCLK OUT output pin is at low level. This feature enables users to flexibly use MCLK OUT pin. For example, MCLK OUT can be used as the clock source of other devices in the system, or MCLK OUT can be turned off, so that the device has the power saving performance. When an external master clock is connected to MCLK IN, MS7705/7706 keeps the internal clock and performs normal conversion when CLKDIS bit is valid. When a crystal oscillator or a ceramic resonator is connected between MCLK IN and MCLK OUT, so when the CLKDIS bits are valid, the MS7705/7706 clock will stop and no analog-to-digital conversion will be performed.
CLKDIV	Clock Divider Bit. When set to logic 1, the clock frequency at the MCLK IN pin is divided by 2. When set to logic 0, the frequency at the MCLK IN pin is actually the internal frequency of the device.
CLK	Clock Bit. CLK bit should be set according to working frequency of MS7705/7706. If the main clock frequency of converter is 2.4576MHz (CLKDIV=0) or 4.9152MHz (CLKDIV=1), CLK should be set "1". If the main clock frequency of the device is 1MHz (CLKDIV== 0) or 2MHz (CLKDIV= 1), this bit should be set to "0". This bit sets appropriate scale current for a given operating frequency and also selects the output update rate of the device (along with FS1 and FS0). If CLK isn’t set correctly according to the main clock frequency, MS7705/7706 will not be able to achieve the target.
FS1,FS0	Filter Selects Bit, which together with CLK determine the output update rate of the device. Table 16 shows the first notch and - 3dB frequency of the filter.

Table 16. Output Rate Selection

CLK[1]	FS1	FS0	Output Rate	-3dB Cut-off Frequency of Filter
0	0	0	20 Hz	5.24 Hz
0	0	1	25 Hz	6.55 Hz
0	1	0	100 Hz	26.2 Hz
0	1	1	200 Hz	52.4 Hz
1	0	0	50 Hz	13.1 Hz
1	0	1	60 Hz	15.7 Hz
1	1	0	250 Hz	65.5 Hz
1	1	1	500 Hz	131 Hz

Note: 1. Assuming that the clock frequency of MCLK IN is correct, the setting of CLKDIV bit is also appropriate.

Data Register (RS2, RS1, RS0 = 0,1,1)

Data register is a 16-bit read-only register, which contains the latest conversion results from MS7705/7706.

Test Register (RS2, RS1, RS0 = 1,0,0); Power On / Reset Status: 00Hex

Test register is used to test device. It is suggested that user should not change the default value of any bit of the test register.

Zero-Scale Calibration Register (RS2, RS1, RS0 = 1,1,0); Power On / Reset Status: 1f4000Hex

MS7705/7706 contains several independent zero-scale registers, each of which is responsible for one input channel. They are all 24-bit read / write registers. 24-bit data must be written before it can be transferred to the zero-scale calibration register.

Full-Scale Calibration Register (RS2, RS1, RS0 = 1,1,1); Power on / Reset Status: 5761ABHex

MS7705/7706 contains several independent full-scale registers, and each full-scale register is responsible for one input channel. They are all 24-bit read / write registers. 24-bit data must be written before it can be transferred to the full-scale calibration register.

Calibration Process

Table 17 summarizes these calibration types, operation contents and operation time. There are two ways to judge whether the calibration is over. The first method is to monitor DRDY. If DRDY returns to low level, it indicates that the calibration process is over and that there is a new valid data in the data register. The second method is to monitor MD1 and MD0 bits of the setting register. If MD1 and MD0 return to "0" (after calibration, MD1 and MD0 return to "0"), it indicates that the calibration process has ended. This method can not prompt whether there is a new conversion result in the data register, but it's earlier than the first judgment method in time, that is, it can quickly know whether the calibration has completed . The duration when Mode bits (i.e. MD1, MD0) return to "0" is shown in Table 17. The process of DRDY returning to low level includes a normal conversion time and a delay time tp with correct scale for the first conversion result. tp shall not exceed 2000 × tCLKIN. The time required for these two methods is shown in the table below.

Table 17. Calibration Process

Calibration Type	MD1,MD0	Calibration Sequence	Setting Time	DRDY Setting Time
Self Calibration	0,1	Zero-scale Calibration @ Selected Gain + Full-scale Calibration @ Selected Gain	6 ×1/Output Rate	9 ×1/Output rate+tP
Zero-scale Calibration	1,0	Zero-scale Calibration @ Selected Gain	3 ×1/Output Rate	4 ×1/Output rate+tP
Full-Scale Calibration	1,1,	Full-scale Calibration @ Selected Gain	3 ×1/Output Rate	1×1/Output rate+tP

Analog Input Range

In non-buffered mode, the common-mode input range is from GND to VDD. The absolute value of analog input voltage is between GND-30mV and VDD+30mV. In non-buffer mode, the analog input connects directly to a 7pF sampling capacitor, C_{SAMP}. As a result, the analog input connects a dynamic load that is converted at the input sampling rate. The typical value of the effective on-off resistance (R_{SW}) of the switch is 7K. Table 18 lists the allowable external resistance/capacitance values in non-buffer mode.

Table 18. External Resistance and Capacitance Values without 16-Bit Gain Error (Non-buffer Mode)

Gain	External Capacitance(pF)					
	10	50	100	500	1000	5000
1	152kΩ	53.9kΩ	31.4kΩ	8.4kΩ	4.76kΩ	1.36kΩ
2	75.1kΩ	26.6kΩ	15.4kΩ	4.14kΩ	2.36kΩ	670Ω
4	34.2kΩ	12.77kΩ	7.3kΩ	1.95kΩ	1.15kΩ	320Ω
8~128	16.7kΩ	5.95kΩ	3.46kΩ	924Ω	526Ω	150Ω

Sampling Rate

The sampling frequency of the MS7705/7706 modulator maintains at fCLKIN/128 (fCLKIN=2.4576MHz at 19.2kHz), regardless of the selected gain. However, gain greater than 1 is a combination of multiple input sampling in each modulator cycle and the ratio of the reference capacitance to the input capacitance. So the input sampling rate varies with the selected gain (see Table 19).

Table 19. Relationship Between Input Sampling Frequency and Gain

Gain	Input Sampling Frequency(fs)
1	$f_{CLKIN}/64$(38.4kHz@f_{CLKIN}=2.4576MHz)
2	$2\times f_{CLKIN}/64$(76.8kHz@f_{CLKIN}=2.4576MHz)
4	$4\times f_{CLKIN}/64$(153.6kHz@f_{CLKIN}=2.4576MHz)
8~128	$8\times f_{CLKIN}/64$(307.2kHz@f_{CLKIN}=2.4576MHz)

Digital Interface

The serial interface of MS7705/7706 includes five signals: CS, SCLK, DIN, DOUT and DRDY.DIN lines are used to transfer data to in-chip registers, while DOUT lines are used to access data in registers. SCLK is a serial clock input. All data transfers are related to SCLK signal. The DRDY acts as a status signal to indicate when the data is ready to read from registers. DRDY becomes low when there are new data words in the output register. If DRDY becomes high before the output register data is updated, it is prompted not to read the data at this time to avoid reading the data during the register update process. CS is used to select devices.

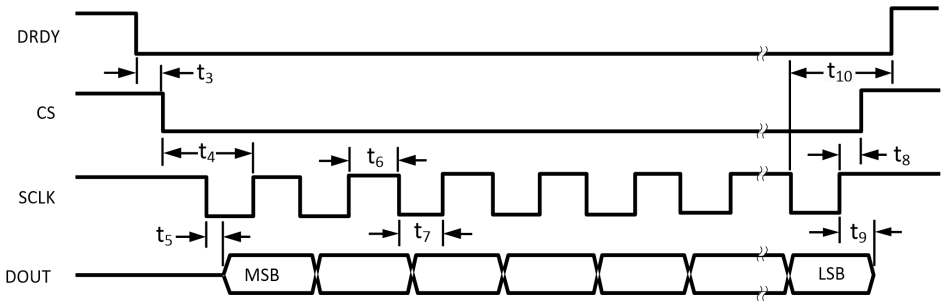


Figure 1. Read Cycle Timing Diagram

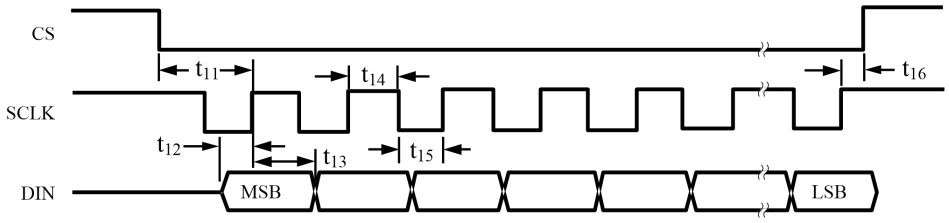
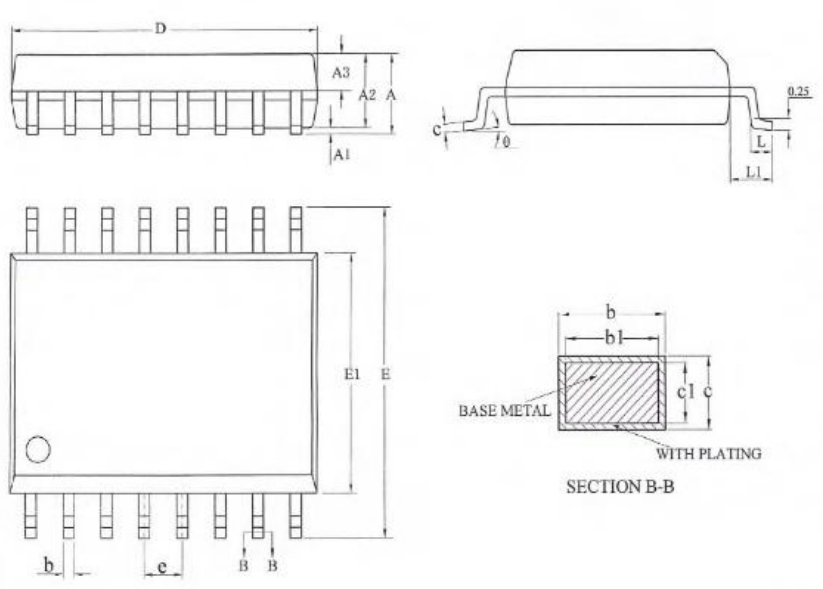


Figure 2. Writing Cycle Sequence Diagram

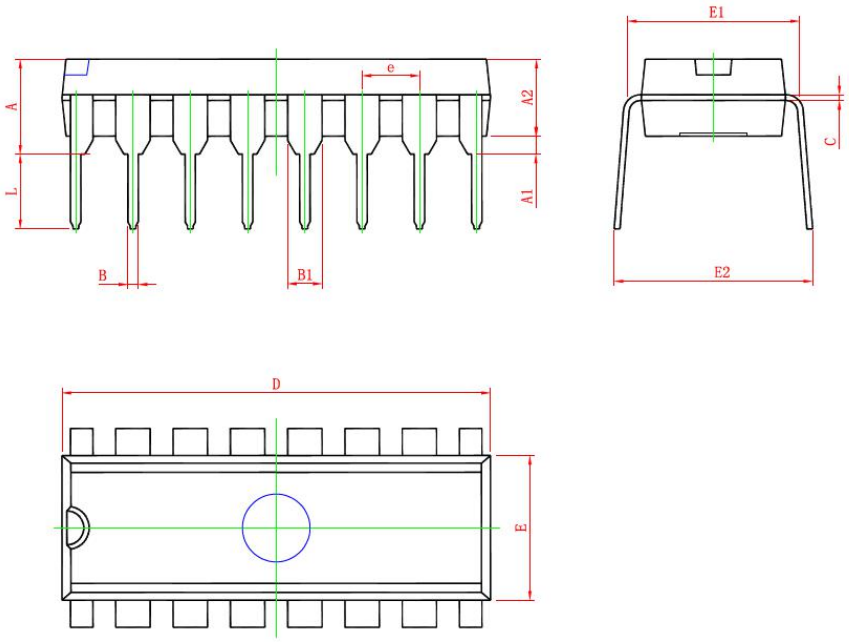
PACKAGE OUTLINE DIMENSIONS

SOP16



Symbol	Millimeter		
	Min	Typ	Max
A	-	-	2.65
A1	0.10	-	0.30
A2	2.25	2.30	2.35
A3	0.97	1.02	1.07
b	0.35	-	0.44
b1	0.34	0.37	0.39
c	0.25	-	0.31
c1	0.24	0.25	0.26
D	10.10	10.30	10.50
E	10.26	10.41	10.60
E1	7.30	7.50	7.70
e	1.27BSC		
L	0.55	-	0.85
L1	1.40BSC		
θ	0	-	8°

DIP16



Symbol	Millimeter	
	Min	Max
A	3.710	4.310
A1	0.510	-
B	0.380	0.570
B1	1.524(BSC)	
C	0.204	0.360
D	18.800	19.200
E	6.200	6.600
E1	7.320	7.974
e	2.540(BSC)	
L	3.000	3.600
E2	8.400	9.000

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS7705, MS7706, MS7705D, MS7706D

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS7705	SOP16	1000	1	1000	8	8000
MS7706	SOP16	1000	1	1000	8	8000

Device	Package	Piece/Tube	Tube/Box	Piece/Box	Box/Carton	Piece/Carton
MS7705D	DIP16	25	40	1000	10	10000
MS7706D	DIP16	25	40	1000	10	10000

STATEMENT

- All Revision Rights of Datasheets Reserved for Ruimeng. Don't release additional notice.

  Customer should get latest version information and verify the integrity before placing order.
- When using Ruimeng products to design and produce, purchaser has the responsibility to observe safety standard and adopt corresponding precautions, in order to avoid personal injury and property loss caused by potential failure risk.
- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com