T536

Quad-core 64-bit Industrial Device Processor

Overview

T536 family features high-performance quad-core Cortex™-A55 platform SoCs for the Industrial and intelligent hardware fields. T536 family can be applied in interactive terminals, smart manufacturing, and other intelligent hardware and Industrial devices.

High-Performance Compute Engine

The T536 integrates an quad-core Cortex™-A55 CPU with independent L2 cache per core and a single-core E907 RISC-V with computing power scalability. T536 also has a neural processing unit (NPU) delivering up to 3 TOPS. With multiple heterogeneous expansion modes and multiple OS architectures, This processor family can meet the requirements of different application scenarios.

Rich Interfaces

T536 family supports the combination of RGB/MIPI DSI/LVDS interfaces. The T536 also supplies high-speed interfaces for connectivity with 2 x GMAC and 1 x USB3.1 Gen1&PCIe2.1 Combo. In addition, the T536 processors contain 4 x CAN-FD and 1 x Local Bus for industrial application and expansion.

Industrial Grade Quality

Industrial temperature range: -40°C to 85 °C T_a

Differentiated Features

Features	T536MX-CEN3	T536MX-CEN2	T536MX-CEX	T536MX-CXX
NPU	Up to 3 TOPS	Up to 2 TOPS	/	/
ECC Protection	Support	Support	Support	/

Features

Processors	• Quad-core ARM Cortex™-A55
	  - 32 KB I/D-cache+64 KB L2 cache+512 KB L3 cache
	  - ECC protection on L1 cache, L2 cache, and L3 cache
	• Single-core E907 RISC-V MCU
	  - 16 KB I-cache+16 KB D-cache
	  - ECC protection on I/D cache
	• Embedded E902 RISC-V for low-power management
	• Up to 3 TOPS NPU

Features

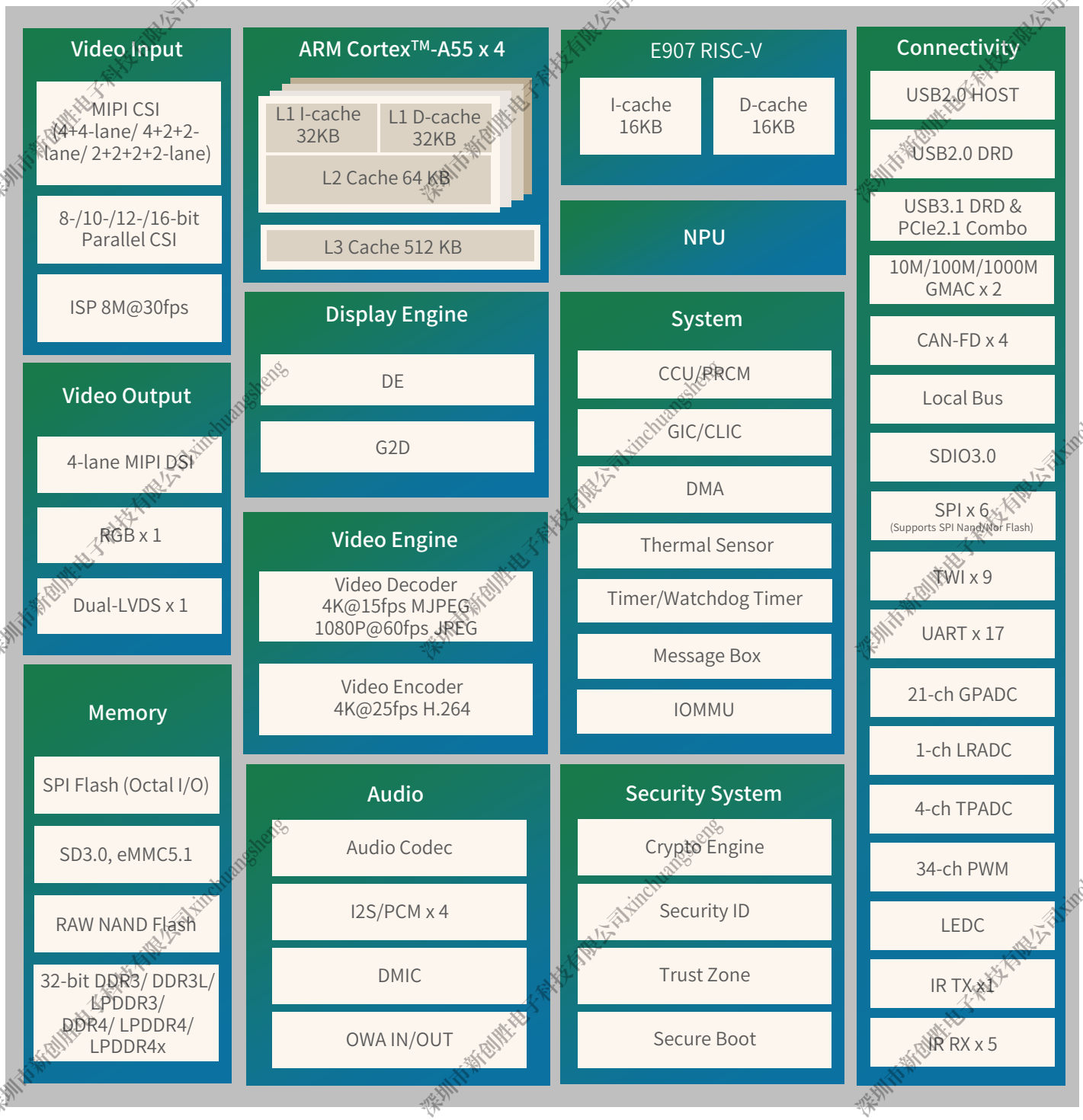
Memory	• 32-bit DDR3/DDR3L/LPDDR3/DDR4/LPDDR4/LPDDR4X interfaces with inline ECC, supporting maximum capacity of 8 GB
	  - Not supports 6GB (4 GB +2 GB) LPDDR3 address space when inline ECC is enabled
	  - Not supports inline ECC when the DQ width of BL8 DDR(DDR3, DDR4, LPDDR3 and BL8 mode LPDDR4) is 16 bits
	• SD3.0, eMMC5.1, SPI NOR/NAND Flash, and RAW NAND Flash for boot
	• ECC protection for SD3.0 and eMMC5.1
	• 8-bit parallel NAND flash interface with maximum 80-bit/1KB BCH
	• One octal SPI interface for Flash devices

Video Engine	• Video decoder and video encoder are time-multiplexed **Video Decoder** • MJPEG decoder, up to 4K@15fps • JPEG Baseline decoder, up to 1080P@60fps **Video Encoder** • H.264 encoder, up to 4K@25fps • MJPEG encoder, up to 4K@15fps • JPEG encoder. up to 8K x 8K resolution • Supports encoder pre-processing (ENCPP) - Supports Geometric Distortion Correction (GDC), including Lens Distortion Correction (LDC) and Fish Eye Correction (FEC)
Display Engine	• Allwinner SmartColor2.0 post processing for an excellent display experience • G2D hardware accelerator including rotate, mixer, and scaler functions
Video Input	**ISP** • Maximum resolution: 4800 x 4224 (offline), 2688 x 4224(online) • Maximum frame rate: 8M@30fps (offline), 5M@30fps (online) • Time Division Multiplexing (TDM) mode and maximum 4-lane multiplexing **Parallel CSI Interface** • 8/10/12/16-bit width • BT.656, BT.601, BT.1120, and Digital Camera (DC) protocol • BT.656 up to 4*720P@30fps and BT.1120 up to 4*1080P@30fps **MIPI CSI Interface** • 4 + 4-lane/4 + 2 + 2-lane/2 + 2 + 2 + 2-lane MIPI CSI, up to 2.0 Gbit/s per lane in HS transmission, compliant with MIPI-CSI2 V1.1 and MIPI DPHY V1.1 • Maximum video capture resolution of 8M@30fps (4-lane performance)
Video Output	• 4-lane MIPI-DSI output interface up to 1920 x 1200@60fps (reduced blanking) • LVDS interface with dual link, up to 1920 x 1080@60fps • One RGB interface with DE/SYNC mode, up to 1920 x 1200@60fps (reduced blanking)
Audio	• 1 DAC • 1 x audio output: LINEOUTP/N • Embedded 4 I2S/PCM interfaces, supporting maximum 16 channels, 8 kHz-384 kHz sample rate, and 8-bit-32-bit width • Maximum 8 digital PDM microphones (DMIC) • One OWA input and one OWA output
Security Engine	• AES, DES, 3DES, and SM4 encryption and decryption algorithms • MD5, SHA, and SM3 tamper proofing • RSA, ECC, SM2 signature and verification algorithms • Supports 160-bit hardware pseudo random number generator(PRNG) with 175-bit seed • Supports 256-bit hardware true random number generator(TRNG) • Integrated 2048-bit eFuse for chip ID and security application
Industrial Connectivity	• 1 x USB3.1 DRD & PCIe2.1 Combo, and PCIe supports RAS DP (Data Protection) for RAMs using ECC • 1 x USB2.0 DRD, 1 x USB2.0 Host • 2 x GMAC (10/100/1000 Mbit/s port with RGMII and RMII interfaces) • 4 x CAN-FD, 1 x Local Bus

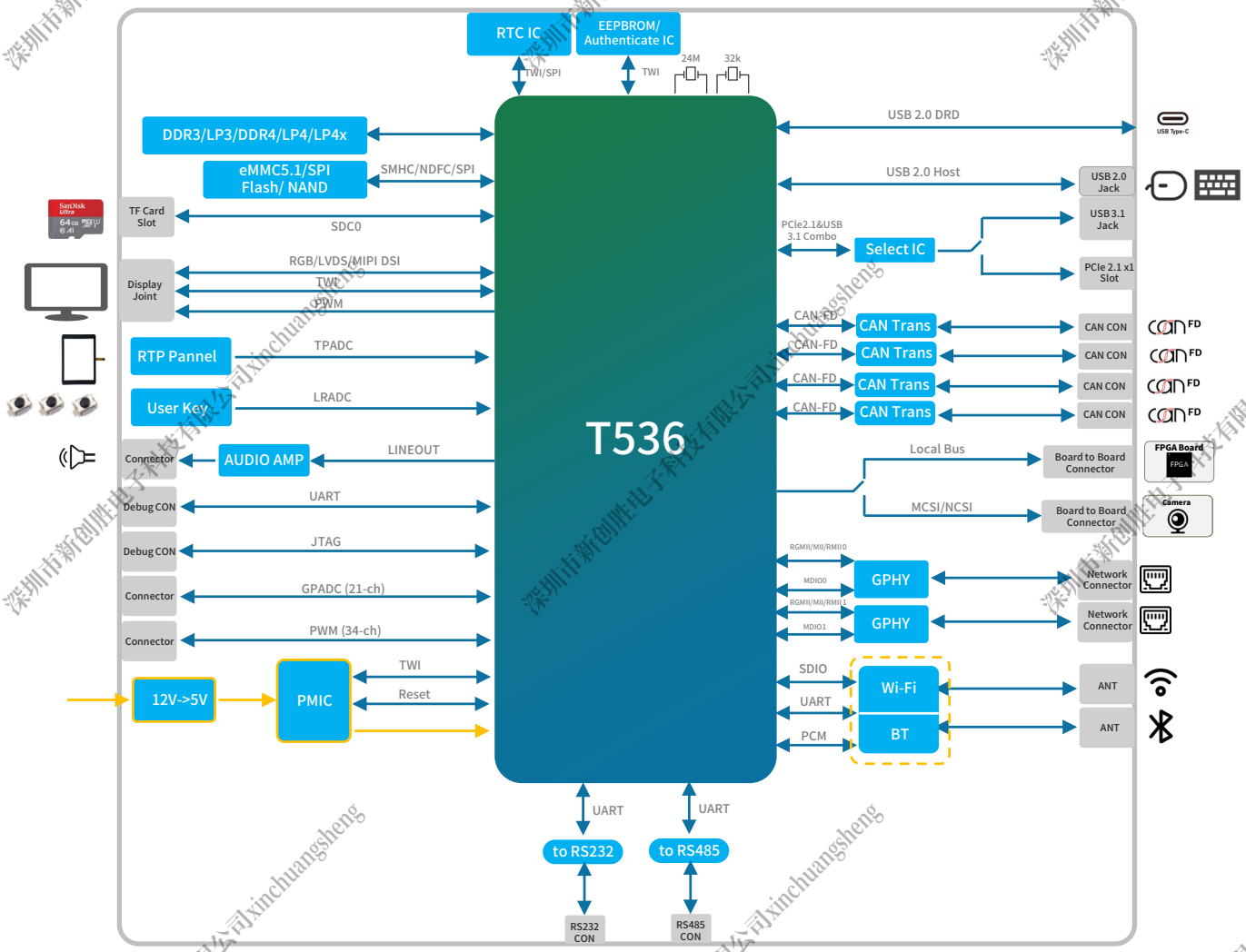
Features

General Connectivity	• 6 x SPI, 5 x IR RX, 1 x IR TX, 9 x TWI, 17 x UART • 4-ch TPADC (TPADC pad can be used by GPADC), 34-ch PWM, 21-ch GPADC, 1-ch LRADC • SDIO 3.0, LEDC
PMIC	• Companion Allwinner Power Management IC
Package	• ED-FCCSP 533 balls • 15 mm x 15 mm size, 0.5 mm ball pitch, 0.3 mm ball size
Process	• 22nm ULP

Block Diagram



Application Diagram



ABOUT ALLWINNER

Allwinner Technology, founded in 2007, is a outstanding designer dedicated to intelligent application SoC, high performance analog component and wireless connectivity IC. It is headquartered in Zhuhai China, with other R&D centers and offices in Shenzhen, HongKong, Xi'an, Beijing and Shanghai. Listed on the GEM of the Shenzhen Stock Exchange in 2015, with the stock code 300458.

Motivated by customer-oriented strategy, Allwinner aligns remarkable R&D teams with long-term core-technology investment in UHD video processing, high-performance multi-core CPU/GPU integration with AI and advanced manufacturing process in terms of high integration , ultra-low power consumption and full-stack integration platform, providing competitive turnkey solutions with considerate services. The products powered by Allwinner spread across from smart hardware, smart home, consumer electronics, HD media, smart video, connected car, industry control, wireless communication to analog products.

CONTACT US

Email: service@allwinnertech.com