24bit High Precision/Low Power ADC

PRODUCT DESCRIPTION

The MS1242 and MS1243 are precision, wide dynamic range, delta-sigma, analog-to-digital (A/D) converters with 24-bit resolution operating from 2.7V to 5.25V supplies.

These delta-sigma, A/D converters provide up to 24 bits of no missing code performance and effective resolution of 21 bits.

TSSOP16

TSSOP20

FEATURES

- 24 Bits no Missing Codes
- 21 Bits Effective Resolution(PGA = 1), 19 Bits (PGA = 128)
- Simultaneous 50Hz and 60Hz Rejection(-90dB Minimum)
- 0.0015% INL
- PGA Gains from 1 to 128
- Single-cycle Setting
- Programmable Data Output Rates
- External Differential Reference of 0.1V to 5V
- SPI™ Compatible
- 600μW Power Consumption
- UP to Four Input Channels (MS1242)
- UP to Eight Input Channels(MS1243)

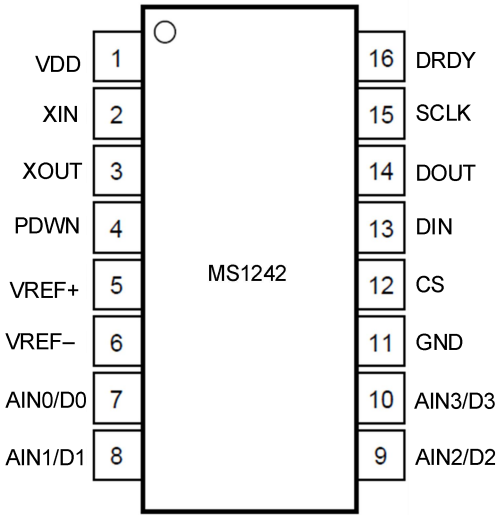
APPLICATIONS

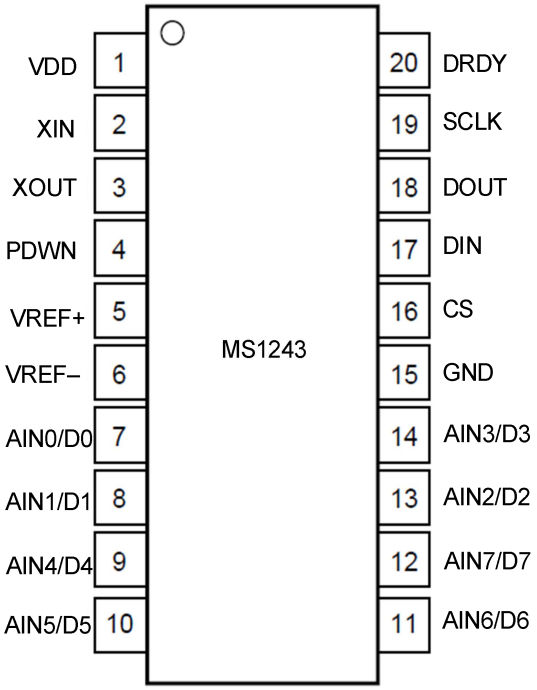
- Industrial Process Control
- Liquid/Gas Chromatograph
- Blood Analysis
- Smart Transmitters
- Portable Instrumentation
- Weight Scale

PRODUCT SPECIFICATION

Part Number	Package	Marking
MS1242	TSSOP16	MS1242
MS1243	TSSOP20	MS1243

PIN CONFIGURATION





PIN DESCRIPTION

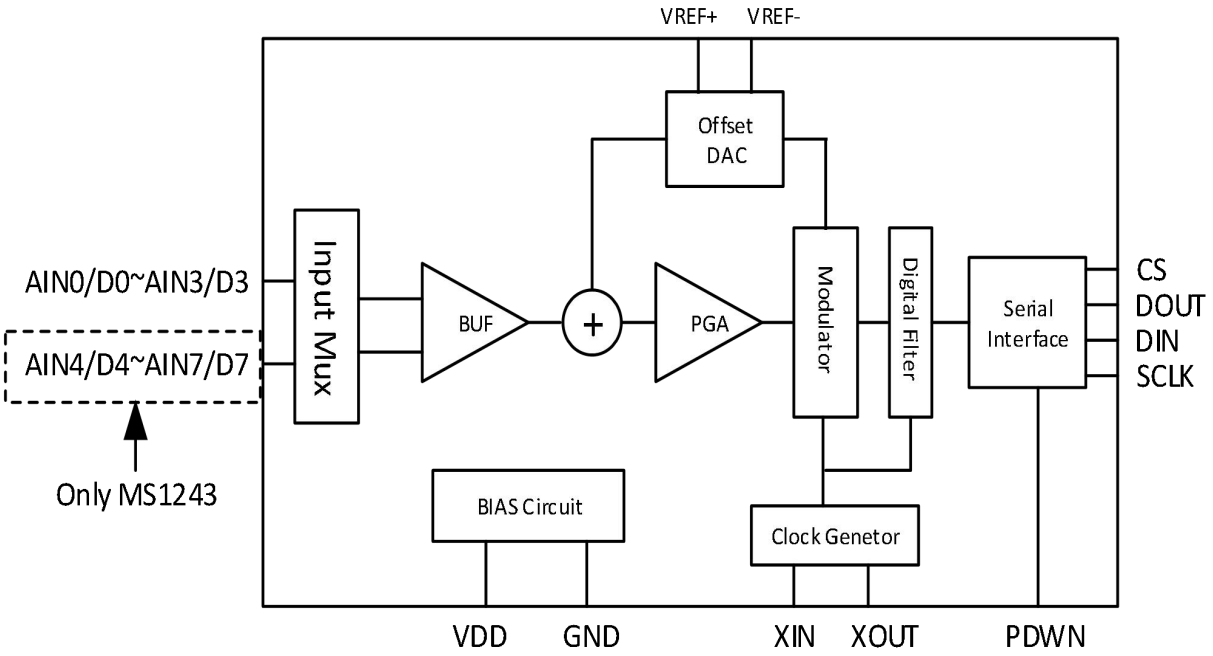
MS1242

Pin	Name	Type	Description
1	VDD	--	Power Supply
2	XIN	I	Clock Input
3	XOUT	O	Clock Output
4	PDWN	I	Active Low Power Down. The power down function shuts down the analog and digital circuits.
5	VREF+	I	Positive Differential Reference Input
6	VREF–	I	Negative Differential Reference Input
7	AIN0/D0	I	Analog Input 0/Data I/O 0
8	AIN1/D1	I	Analog Input 1/Data I/O 1
9	AIN2/D2	I	Analog Input 2/Data I/O 2
10	AIN3/D3	I	Analog Input 3/Data I/O 3
11	GND	--	Ground
12	CS	I	Active Low, Chip Select
13	DIN	I	Serial Data Input, Schmitt Trigger
14	DOUT	O	Serial Data Output
15	SCLK	I	Serial Clock, Schmitt Trigger
16	DRDY	O	Active Low, Data Ready

MS1243

Pin	Name	Type	Description
1	VDD	--	Power Supply
2	XIN	I	Clock Input
3	XOUT	O	Clock Output
4	PDWN	I	Active Low Power Down. The power down function shuts down the analog and digital circuits.
5	VREF+	I	Positive Differential Reference Input
6	VREF–	I	Negative Differential Reference Input
7	AIN0/D0	I	Analog Input 0/Data I/O 0
8	AIN1/D1	I	Analog Input 1/Data I/O 1
9	AIN4/D4	I	Analog Input 4/Data I/O 4
10	AIN5/D5	I	Analog Input 5/Data I/O 5
11	AIN6/D6	I	Analog Input 6/Data I/O 6
12	AIN7/D7	I	Analog Input 7/Data I/O 7
13	AIN2/D2	I	Analog Input 2/Data I/O 2
14	AIN3/D3	I	Analog Input 3/Data I/O 3
15	GND	--	Ground
16	CS	I	Active Low, Chip Select
17	DIN	I	Serial Data Input, Schmitt Trigger
18	DOUT	O	Serial Data Output
19	SCLK	I	Serial Clock, Schmitt Trigger
20	DRDY	O	Active Low, Data Ready

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Parameter	Symbol	Range	Unit
Power	VDD	-0.3 ~ 6	V
Input Current	Iin	100 (Momentary)	mA
Input Current	Iin	10 (Continuous)	mA
Analog Input Voltage	Ain	-0.5 ~ VDD+0.5	V
Digital Input Voltage	Din	-0.3 ~ VDD+0.3	V
Digital Output Voltage	Dout	-0.3 ~ VDD+0.3	V
Maximum Junction Temperature	Jt	150	°C
Operating Temperature	TA	-40 ~ 85	°C
Storage Temperature	Tstg	-60 ~ 150	°C
Soldering Temperature(10s)		260	°C

ELECTRICAL CHARACTERISTICS

Digital Characteristics： TMIN to TMAX, VDD: 2.7V to 5.25V.

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Digital Input High	VIH		0.8×VDD		VDD	V
Digital Input Low	VIL		GND		0.2 • VDD	V
Digital Output High	VIH	IOH = 1mA	VDD – 0.4			V
Digital Output Low	VIL	IOL = 1mA	GND		GND + 0.4	V
Input High Leakage	IIH				10	uA
Input Low Leakage	IIL		-10			uA
Master Clock Frequency	fosc		1		5	MHz
Master Clock Period	Tosc	1/fOSC	200		1000	ns

Electrical Characteristics： TMIN to TMAX, VDD=+5V, fMOD=19.2kHz, PGA=1, Buffer ON, fDATA=15Hz, VREF≡(REFIN+)–(REFIN–)= +2.5V.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Buffer Off	GND-0.1		VDD+0.1	V
	Buffer On	GND+0.05		VDD-1.5	V
Full-Scale Input Range (AIN+) - (AIN-)	RANGE = 0			±VREF /PGA	V
	RANGE = 1			±VREF /(2×PGA)	V
Differential Input Impedance	Buffer Off		5/PGA		MΩ
	Buffer On		5		GΩ
Bandwidth (-3dB)	fDATA = 3.75Hz		1.66		Hz
	fDATA = 7.50Hz		3.44		Hz
	fDATA = 15.0Hz		14.6		Hz
PGA	User-Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator Off , T = 25°C		5		pA
Burnout Current Sources			2		uA
System Performance					
Resolution	No Missing Codes		24		Bits
Integral Nonlinearity				±0.0015	% of FS
Offset Error			8ppm		of FS
Offset Drift			0.02ppm		of FS/°C
Gain Error			0.005		%
Gain Error Drift			1.0		ppm/°C

Parameter	Condition	Min	Typ	Max	Unit
Common-Mode Rejection	at DC	100			dB
	fCM = 60Hz, fDATA =15Hz		130		dB
	fCM = 50Hz, fDATA = 15Hz		120		dB
Normal-Mode Rejection	fCM = 60Hz, fDATA = 15Hz		100		dB
	fCM = 50Hz, fDATA = 15Hz		100		dB
Power-Supply Rejection	at DC	80	95		dB
Voltage Reference Input					
REF≡REFP-REFN	RANGE = 0	0.1	2.5	2.6	V
	RANGE = 1	0.1		VDD	V
REFP,REFN Input Range	RANGE = 0	0		VDD	V
	RANGE = 1	0		VDD	V
Common-Mode Rejection	at DC		120		dB
	fVREFCM = 60Hz		120		dB
Bias Current	VREF = 2.5V		1.3		uA

Parameter	Condition	Min	Typ	Max	Unit
Offset DAC					
Offset DAC Range	RANGE = 0		±VREF/ (2×PGA)		V
	RANGE = 1		±VREF/ (4×PGA)		V
Monotonicity		8			Bits
Gain Error			±10		%
Gain Error Drift			1		ppm/°C
Power					
Power-Supply Voltage	VDD	4.75		5.25	V
Current	PGA = 1, Buffer Off		240	375	uA
	PGA = 128, Buffer Off		450	800	uA
	PGA = 1, Buffer On		290	425	uA
	PGA = 128, Buffer On		960	1400	uA
	SLEEP Mode		60		uA
	Read Data Continuous Mode		230		uA
	PDWN = 0		0.5		nA
Power Dissipation	PGA = 1, Buffer Off		1.2	1.9	mW
Temperature Range					
Operating		-40		+85	°C

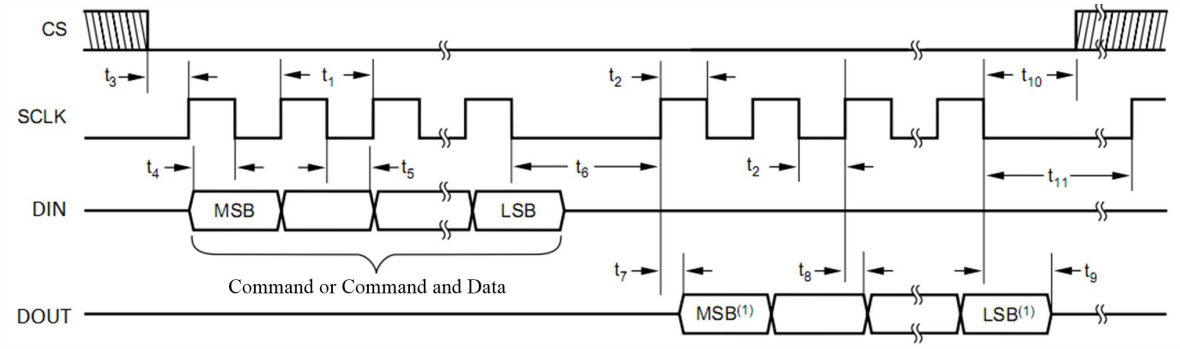
Electrical Characteristics : TMIN to TMAX, VDD = +3V, fMOD = 19.2kHz, PGA = 1, Buffer ON, fDATA = 15Hz, VREF≡(REFIN+)–(REFIN–) = +1.25V.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Buffer Off	GND-0.1		VDD+0.1	V
	Buffer On	GND+0.05		VDD-1.5	V
Full-Scale Input Range (AIN+) - (AIN-)	RANGE = 0			±VREF /PGA	V
	RANGE = 1			±VREF /(2×PGA)	V
Differential Input Impedance	Buffer Off		5/PGA		MΩ
	Buffer On		5		GΩ
Bandwidth (-3dB)	fDATA = 3.75Hz		1.66		Hz
	fDATA = 7.50Hz		3.44		Hz
	fDATA = 15.0Hz		14.6		Hz
PGA	User-Selectable Gain Ranges	1		128	
Input Capacitance			9		pF
Input Leakage Current	Modulator Off, T = 25°C		5		pA
Burnout Current Sources			2		uA
System Performance					
Resolution	No Missing Codes		24		Bits
Integral Nonlinearity				±0.0015	% of FS
Offset Error			15ppm		of FS
Offset Drift			0.04ppm		of FS/°C
Gain Error			0.01		%
Gain Error Drift			1.0		ppm/°C
Common-Mode Rejection	at DC	100			dB
	fCM = 60Hz, fDATA =15Hz		130		dB
	fCM = 50Hz, fDATA = 15Hz		120		dB
Normal-Mode Rejection	fCM = 60Hz, fDATA = 15Hz		100		dB
	fCM = 50Hz, fDATA = 15Hz		100		dB
Power-Supply Rejection	at DC	75	90		dB
Voltage Reference Input					
REF≡REFP-REFN	RANGE = 0	0.1	1.25	1.26	V
	RANGE = 1	0.1	2.5	2.6	V
REFP,REFN Input Range	RANGE = 0	0		VDD	V
	RANGE = 1	0		VDD	V
Common-Mode Rejection	at DC		120		dB
	fVREFCM = 60Hz		120		dB
Bias Current	VREF = 1.25		0.65		uA

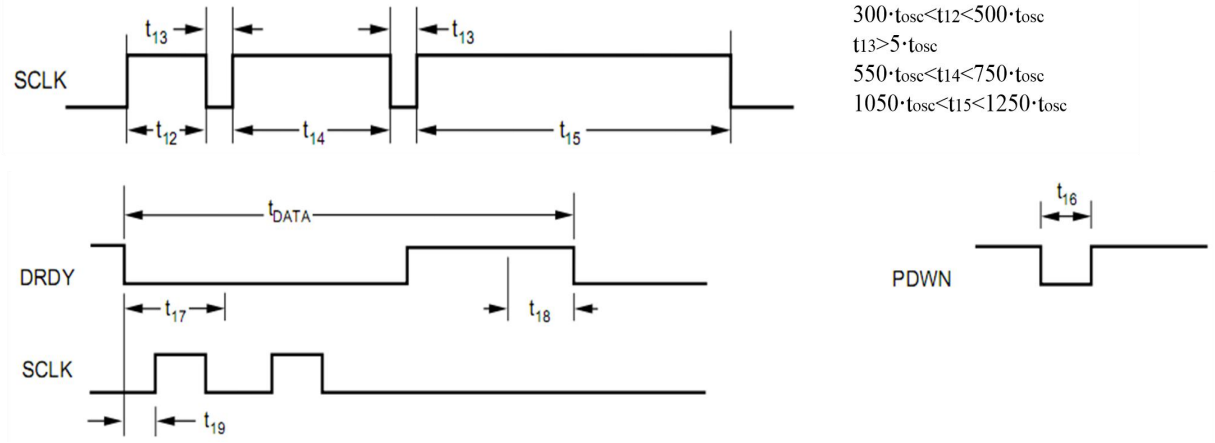
Parameter	Condition	Min	Typ	Max	Unit
Offset DAC					
Offset DAC Range	RANGE = 0		±VREF/ (2×PGA)		V
	RANGE = 1		±VREF/ (4×PGA)		V
Monotonicity		8			Bits
Gain Error			±10		%
Gain Error Drift			1		ppm/°C
Power					
Power-Supply Voltage	VDD	2.7		3.3	V
Current	PGA = 1, Buffer Off		190	375	uA
	PGA = 128, Buffer Off		460	700	uA
	PGA = 1, Buffer On		240	375	uA
	PGA = 128, Buffer On		870	1325	uA
	SLEEP Mode		75		uA
	Read Data Continuous Mode		1130		uA
	PDWN = 0		0.5		nA
Power Dissipation	PGA = 1, Buffer Off		0.6	1.2	mW
Temperature Range					
Operating		-40		+85	°C

FUNCTIONAL DESCRIPTION

1. Timing Diagrams



MS1242/MS1243 Reset
On the Falling Edge



$300 \cdot t_{osc} < t_{12} < 500 \cdot t_{osc}$
$t_{13} > 5 \cdot t_{osc}$
$550 \cdot t_{osc} < t_{14} < 750 \cdot t_{osc}$
$1050 \cdot t_{osc} < t_{15} < 1250 \cdot t_{osc}$

MS1242/MS1243 Timing Diagram

MS1242/MS1243 Timing Table

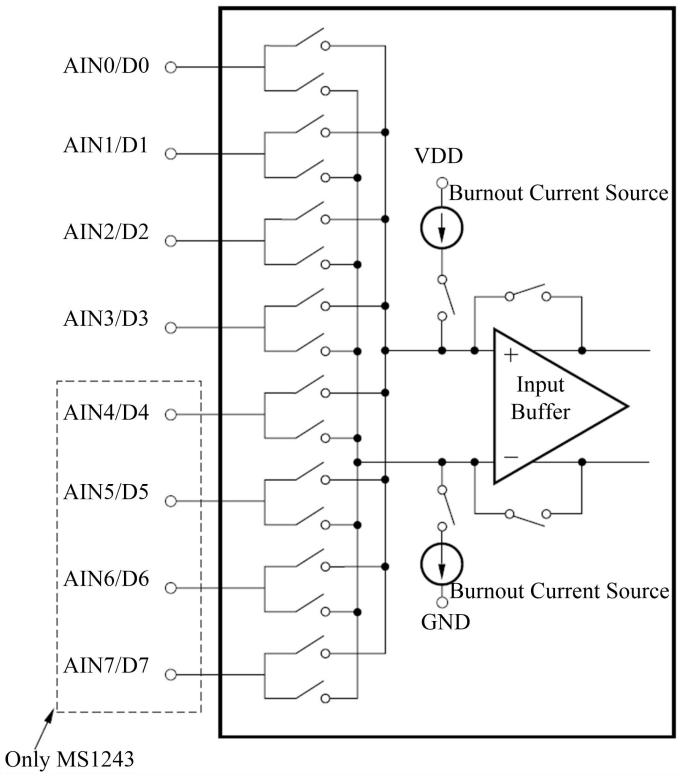
Parameter	Description	Min	Max	Unit
t_1	SCLK Period	4		tosc Period
			3	DRDY Period
t_2	SCLK Pulse Width, High and Low	200		ns
t_3	CS Low to First SCLK Edge; Setup Time	0		ns
t_4	DIN Valid to SCLK Edge; Setup Time	50		ns
t_5	DIN Valid to SCLK Edge; Hold Time	50		ns
t_6	Delay Between Last SCLK Edge for DIN and First SCLK Edge for DOUT: RDATA, RDATAC, RREG, WREG	50		tosc Period
t_7	SCLK Edge to Valid New DOUT		50	ns
t_8	SCLK Edge to DOUT, Hold Time	0		ns
t_9	Last SCLK Edge to DOUT Tri-State	6	10	tosc Period
t_{10}	CS Low Time after Final SCLK Edge.	0		ns

Parameter	Description		Min	Max	Unit
t_{11}	Final SCLK Edge of One Command until First Edge SCLK of Next Command	RREG, WREG, DSYNC, SLEEP, RDATA, RDATAC, STOPC	4		tosc Period
		OCALSYS, GCALSYS	8		DRDY Period
		RESET	16		tosc Period
t_{16}	Pulse Width		4		tosc Period
t_{17}	Allowed Analog Input Change for Next Valid Conversion			5000	tosc Period
t_{18}	DOR Update, DOR Data not Valid.		4		tosc Period
t_{19}	First SCLK after DRDY Goes Low	RDATAC Mode	10		tosc Period
t_{16}		Any Other Mode	0		tosc Period

2. Module Description

2.1 Input Multiplexer

The input multiplexer provides for any combination of differential inputs to be selected on any of the input channels, as shown blow.



MS1242 has two independent differential input channels or three single-ended input channels at most. For example, if AIN1 is selected as the positive (negative) differential input channel, any other channel can be selected as the negative (positive) terminal for the differential input channel.

MS1242 can switch input signal select and realize stable output of digital filter within single clock period. In order to decrease switch error, configure MUX register immediately after DRDY signal goes low.

2.2 Burnout Current Sources

The Burnout Current Sources can be used to detect sensor short-circuit or open-circuit conditions. Setting the Burnout Current Sources (BOCS) bit in the SETUP register activates two 2uA current sources called burnout current sources. When sensor is short-circuit, burnout current source makes MS1242 output zero. When sensor is open-circuit, burnout current source makes MS1242 output full-scale (7FFFFFHex).

2.3 Input Buffer

The input impedance of the MS1242 without the buffer enabled is approximately 5MΩ/PGA. For systems requiring very high input impedance, the activated buffer raises input impedance to approximately 5GΩ.

The buffer can be enabled using the BUF pin or the BUF bit in the ACR register.。 The buffer is on when the BUF pin is high and the BUF bit is set to one. The buffer draws additional current when activated. The current required by the buffer depends on the PGA setting. When the PGA is set to 1, the buffer uses approximately 50uA; when the PGA is set to 128, the buffer uses approximately 500uA. When buffer is on, the required buffer's input range is approximately AGND+0.3V ~ AVDD-1.5V.

2.4 PGA

The Programmable Gain Amplifier (PGA) can be set to gains of 1, 2, 4, 8, 16, 32, 64, or 128. Using the PGA can improve the effective resolution of the A/D converter. For instance, with a PGA of 1 on a 5V full-scale signal, the A/D converter can resolve down to 1μV. With a PGA of 128 and a full-scale signal of 39mV, the A/D converter can resolve down to 75nV.

2.5 Offset DAC

In order to extend input range, MS1242 integrates an offset 8bit DAC (ODAC). In concept, offset DAC is a programmable voltage source. The input signal is magnified by PGA, then added up to ODAC output, and last input into Δ-Σ modulator.

2.6 Modulator

The modulator is a single-loop and delta-sigma second-order system. The frequency division is determined by the SPEED bit (ACR bit5), as shown blow.

fosc (MHz)	Speed	fMOD (kHz)	DR Bits			1st Notch (Hz)
			00	01	10	
2.4576	0	19.200	15	7.5	3.75	50/60
	1	9.600	7.5	3.75	1.875	25/30
4.9152	0	38.400	30	15	7.5	100/120
	1	19.200	15	7.5	3.75	50/60

2.7 Calibration

MS1242 supports both self and system calibration. Calibration includes offset calibration and gain calibration.

Self-calibration is handled by three commands: SELFCAL, SELFGAL, and SELFOCAL and each calibration takes two tDATA periods to complete. During self-calibration, the ADC inputs are disconnected internally from the input pins. The PGA must be set to 1 prior to issuing a SELFCAL or SELFGCAL command. For operation with a reference voltage greater than (VDD–1.5) volts, the buffer must also be turned off.

System calibration corrects both internal and external offset and gain errors. While performing system calibration, the appropriate signal must be applied to the inputs. The system offset calibration command (SYSOCAL) requires a zero input differential signal. It then computes the offset that nullifies the offset in the OCR register. The system gain calibration command (SYSGCAL) requires a positive full-scale input signal. It then computes a value to nullify the gain error in the FSR register. Each of these calibrations takes two tDATA periods to complete.

Calibration should be performed after power on, a change in temperature, or a change of the PGA. The RANGE bit (ACR bit2) must be zero and the ODAC is disable during calibration. At the completion of calibration, the DRDY signal goes low, indicating the calibration is finished. The first data after calibration should be discarded since it may be incorrect due to delay of external circuit.

2.8 External Voltage Reference

The MS1242 requires an external voltage reference. The selection for the voltage reference value is made through the ACR register. Voltage reference is connected between the pins: +VREF and –VREF, and the voltage range from GND to VDD. However, the following limitations apply.

For VDD = 5.0V and RANGE = 0, the differential VREF must not exceed 2.5V.

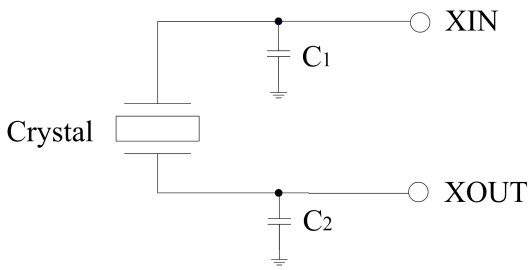
For VDD = 5.0V and RANGE = 1, the differential VREF must not exceed 5V.

For VDD = 3.0V and RANGE = 0, the differential VREF must not exceed 1.25V.

For VDD = 3.0V and RANGE = 1, the differential VREF must not exceed 2.5V.

2.9 Clock Generator

The clock source for the MS1242 can be provided from a crystal, oscillator, or external clock. When the clock source is external clock, it is connected with XIN pin and XOUT pin is NC. When the clock source is a crystal, external capacitors (10~20pF) must be provided on XIN and XOUT pin, as shown follow.



2.10 Digital Filter

The MS1242 has a programmable Finite Impulse Response (FIR) digital filter that a user can configure for various output data rates. When a 2.4576MHz crystal is used, the device can be programmed for an output data rate of 15Hz, 7.5Hz, or 3.75Hz. Under these conditions, the digital filter rejects both 50Hz and 60Hz interference.

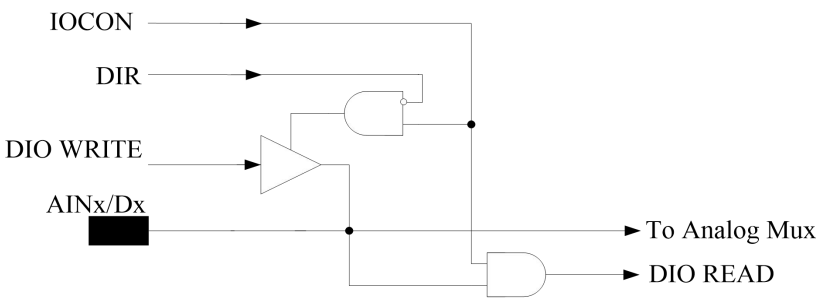
If a different data output rate is desired, a different crystal frequency can be used. However, the rejection frequencies shift accordingly. For example, a 3.6864MHz master clock with the default register condition has:

Output Data Rate: (3.6864MHz/2.4576MHz) ×15Hz = 22.5Hz

The First and Second Notch: (3.6864MHz/2.4576MHz) × (50Hz and 60Hz) = (75Hz and 90Hz)

2.11 Data I/O Interface

The data interface serves a dual purpose as both analog input and data I/O. The interface is configured through the IOCON, DIR, and DIO register. The default configuration of power on is analog input. When the interface is configured as data I/O, it is used as self-test mode. The equivalent schematic see blow.



2.12 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) allows a controller to communicate synchronously with the MS1242. The MS1242 operates in slave-only mode. The serial interface is a standard four-wire SPI (CS, SCLK, DIN and DOUT) interface.

2.12.1 Chip Select

The chip select (CS) input must be externally asserted before communicating with the MS1242. CS must stay low for the duration of the communication. Whenever CS goes high, the serial interface is reset. CS may be hard-wired low.

When CS signal stay constant low, the serial interface can operate in three-wire mode. The condition is appropriate for communication between MS1242 and external microcontroller.

2.12.2 SCLK

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock DIN and DOUT data. Make sure to have a clean SCLK to prevent false sample data. If SCLK is not toggled within three DRDY pulses, the serial interface resets on the next SCLK pulse and starts a new communication cycle. A special pattern on SCLK resets the entire chip.

2.12.3 Data Input and Data Output

The data input (DIN) and data output (DOUT) receive and send data from the MS1242. DOUT is high impedance when not in use to allow DIN and DOUT to be connected together and driven by a bidirectional bus. Note: the Read Data Continuous Mode (RDATAC) command should not be issued when DIN and DOUT are connected. While in RDATAC mode, DIN looks for the STOPC or RESET command. If either of these 8-bit bytes appear on DOUT (which is connected to DIN), the RDATAC mode ends.

2.13 Data Ready

The Data Ready (DRDY) line is used as a status signal to indicate when data is ready to be read from the internal data register. DRDY goes low when a new data is available in the DOR register. It is reset high when a read operation from the data register is complete. It also goes high prior to the updating of the output register to indicate when not to read from the device to ensure that a data read is not attempted while the register is being updated. The status of DRDY can also be obtained by bit 7 of the ACR register.

2.14 DSYNC Operation

Synchronization can be achieved through the DSYNC command. When the DSYNC command is sent, the digital filter is reset on the edge of the last SCLK of the DSYNC command. The modulator is held in RESET until the next edge of SCLK is detected. Synchronization occurs on the next rising edge of the system clock after the first SCLK following the DSYNC command.

2.15 SUPPLY VOLTAGE RAMP RATE

The power-on reset circuitry is designed to accommodate digital supply ramp rates as slow as 1V/10ms. To ensure proper operation, the power supply should ramp monotonically.

3. Registers Description

The operation of MS1242 is set up through individual registers. Collectively, the registers contain all the information needed to configure the part, such as data format, multiplexer settings, data rate, calibration settings, etc.

3.1 Registers table

MS1242/MS1243 registers are shown in blow table

Add	Reg	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
00H	SETUP	ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0
01H	MUX	PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0
02H	ACR	DRDY	U/B	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0
03H	ODAC	SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
04H	DIO	DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
05H	DIR	DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
06H	IOCON	IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
07H	OCR0	OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00
08H	OCR1	OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08
09H	OCR2	OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16
0AH	FSR0	FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00
0BH	FSR1	FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08
0CH	FSR2	FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16
0DH	DOR2	DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16
0EH	DOR1	DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08
0FH	DOR0	DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

3.2 Detailed Register Definition

SETUP (Address=00H, Reset Value=xxxx0000) PGA Control (Setup Register)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID	ID	ID	ID	BOCS	PGA2	PGA1	PGA0

bit 7-4：Factory Programmed Bits
bit 3 ： BOCS: Burnout Current Source
0 = Disabled (default)； 1 = Enabled
bit 2-0： PGA2: PGA1: PGA0: Programmable Gain Amplifier
000 = 1 (default)
001 = 2
010 = 4
011 = 8
100 = 16
101 = 32
110 = 64
111 = 128

MUX (Address=01H， Reset Value=01H) Multiplexer Control Register

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

MUX. 7-4 : PS3 ~ 0, Positive Channel Selection

0000 = AIN0 (default)
0001 = AIN1
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
Other = Reserved

MUX. 3-0 : NS3 ~ 0, Negative Channel Selection

0000 = AIN0
0001 = AIN1 (default)
0010 = AIN2
0011 = AIN3
0100 = AIN4
0101 = AIN5
0110 = AIN6
0111 = AIN7
Other = Reserved

ACR (Address=02H, Reset Value=00H) Analog Control Register

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DRDY	U/B	SPEED	BUFEN	BIT ORDER	RANGE	DR1	DR0

ACR.7 : DRDY, Data Ready (Read Only) This bit duplicates the state of the DRDY pin.

ACR.6 : U/B , Data Format

0 = Bipolar (default)
1 = Unipolar

ACR.5 : SPEED, Modulator Clock Speed

0 = fosc/128 (default)
1 = fosc/256

ACR.4 : BUFEN, Buffer Enable

0 = Buffer Disabled (default)
1 = Buffer Enabled

ACR.3 : BITOR, Data Output Bit Order

0 = Most Significant Bit Transmitted First (default)
1 = Least Significant Bit Transmitted First

ACR.2 : RANGE, Range Select 0 = Full-Scale Input Range equal to +/-VREF (default) 1 = Full-Scale Input Range equal to +/- VREF/2 ACR.1-0 : DR1/DR0, Data Rate 00 = 15Hz (default) 01 = 7.5Hz 10 = 3.75Hz 11 = Reserved

ODAC (Address=03H, Reset Value=00H) Offset DAC

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
SIGN	OSET6	OSET5	OSET4	OSET3	OSET2	OSET1	OSET0
ODAC.7 : SIGN, Sign Bit, 0 = Positive, 1 = Negative ODAC.6-0 : Offset Value							

DIO (Address=04H, Reset Value=00H) Data I/O

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIO_7	DIO_6	DIO_5	DIO_4	DIO_3	DIO_2	DIO_1	DIO_0
If the IOCON register is configured for data, a value written to this register appears on the data I/O pins if the pin is configured as an output in the DIR register. Reading this register returns the value of the data I/O pins.							

DIR (Address= 05H, Reset Value=FFH) Direction Control for Data I/O

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIR_7	DIR_6	DIR_5	DIR_4	DIR_3	DIR_2	DIR_1	DIR_0
Each bit controls whether the corresponding data I/O pin is an output (= 0) or input (= 1). The default power-up state is as inputs.							

IOCON (Address=06H, Reset Value=00H） I/O Configuration Register

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
IO7	IO6	IO5	IO4	IO3	IO2	IO1	IO0
bit 7-0: Data I/O Configuration 0 = Analog (default) 1 = Data Bits 4 to 7 are not used in MS1242.							

OCR0 (Address=07H, Reset Value=00H) Offset Calibration Coefficient (Least Significant Byte)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCR07	OCR06	OCR05	OCR04	OCR03	OCR02	OCR01	OCR00

OCR1 (Address=08H, Reset Value=00H) Offset Calibration Coefficient (Middle Byte)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCR15	OCR14	OCR13	OCR12	OCR11	OCR10	OCR09	OCR08

OCR2 (Address=09H, Reset Value=00H) Offset Calibration Coefficient (Most Significant Byte)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OCR23	OCR22	OCR21	OCR20	OCR19	OCR18	OCR17	OCR16

FSR0 (Address=0AH, Reset Value=59H) Gain Calibration Coefficient (Least Significant Byte)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR07	FSR06	FSR05	FSR04	FSR03	FSR02	FSR01	FSR00

FSR1 (Address=0BH, Reset Value=55H) Gain Calibration Coefficient (Middle Byte)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR15	FSR14	FSR13	FSR12	FSR11	FSR10	FSR09	FSR08

FSR2 (Address=0CH, Reset Value=55H) Gain Calibration Coefficient (Most Significant Byte)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSR23	FSR22	FSR21	FSR20	FSR19	FSR18	FSR17	FSR16

DOR2 (Address=0DH, Reset Value=00H) Data Output Register (Most Significant Byte) (Read Only)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOR23	DOR22	DOR21	DOR20	DOR19	DOR18	DOR17	DOR16

DOR1 (Address=0EH, Reset Value=00H) Data Output Register (Middle Byte) (Read Only)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOR15	DOR14	DOR13	DOR12	DOR11	DOR10	DOR09	DOR08

DOR0 (Address=0FH, Reset Value=00H) Data Output Register (Least Significant Byte) (Read Only)

MSB							LSB
Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DOR07	DOR06	DOR05	DOR04	DOR03	DOR02	DOR01	DOR00

4. MS1242 Command Definitions

MS1242 uses a series of commands, which control the operation mode, speed, calibration and so on. Some of the commands are stand-alone commands (such as RESET), while others require additional bytes (for example, WREG requires the count and data bytes).

Operands:

n = count (0 to 127)

r = register (0 to 15)

x = don't care

Command Summary

Commands	Description	Op Code	2nd Command Byte
RDATA	Read Data	00000001(01H)	—
RDATAC	Read Data Continuously	00000011(03H)	—
STOPC	Stop Read Data Continuously	00001111(0FH)	—
RREG	Read from REG "rrrr"	0001XXXX(1xH)	xxxx_nnnn(#of regs-1)
WREG	Write to REG "rrrr"	0101XXXX(5xH)	xxxx_nnnn(#of regs-1)
SELFCAL	Offset and Gain Self Cal	11110000(F0H)	—
SELFOCAL	Self Offset Cal	11110001(F1H)	—
SELFGCAL	Self Gain Cal	11110010(F2H)	—
SYSOCAL	Sys Offset Cal	11110011(F3H)	—
SYSGCAL	Sys Gain Cal	11110100(F4H)	—
WAKEUP	Wakup from SLEEP Mode	11111011(FBH)	—
DSYNC	Sync DRDY	11111100(FCH)	—
SLEEP	Put in SLEEP Mode	11111101(FDH)	—
RESET	Reset to Power-Up Values	11111110(FEH)	—
NOTE: The received data format is always MSB first. The data out format is set by the BIT ORDER bit in the ACR register. of regs-1 represents that the count of required registers needs to decrease 1.			

RDATA—Read Data

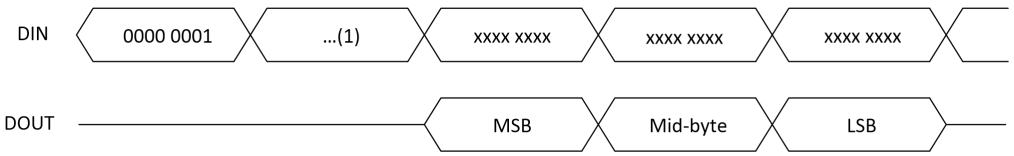
Description: Read the most recent conversion result from Data Output Register (DOR). This is a 24-bit value.

Operands: None

Bytes: 1

Encoding: 0000 0001

Data Transfer Sequence:



NOTE : (1) For wait time, refer to timing specification.

RDATAC—Read Data Continuous

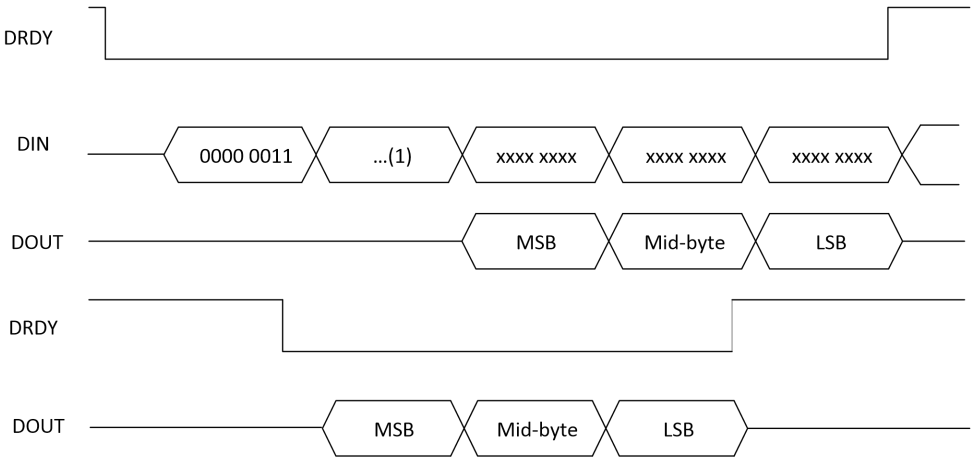
Description: Read Data Continuous mode enables the continuous output of new data on each DRDY. This command eliminates the need to send the Read Data Command on each DRDY. This mode may be terminated by either the STOPC command or the RESET command. Wait at least 10 fOSC after DRDY falls before reading.

Operands: None

Bytes: 1

Encoding: 0000 0011

Data Transfer Sequence:



NOTE : (1) For wait time, refer to timing specification.

STOPC—Stop Continuous

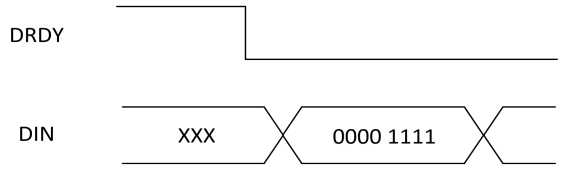
Description: Ends the continuous data output mode. Issue after DRDY goes low.

Operands: None

Bytes: 1

Encoding: 0000 1111

Data Transfer Sequence:



RREG—Read from Registers

Description: Output the data from up to 16 registers starting with the register address specified as part of the instruction. The number of registers read will be one plus the second byte count. If the count exceeds the remaining registers, the addresses wrap back to the beginning.

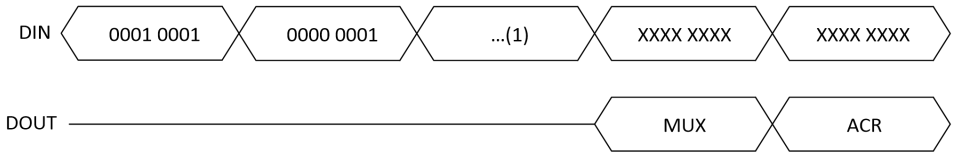
Operands: r, n

Bytes: 2

Encoding: 0001 rrrr xxxx nnnn

Data Transfer Sequence:

Read Two Registers Starting from Register 01H (MUX)



NOTE : (1) For wait time, refer to timing specification.

WREG—Write to Registers

Description: Write to the registers starting with the register address specified as part of the instruction. The number of registers that will be written is one plus the value of the second byte.

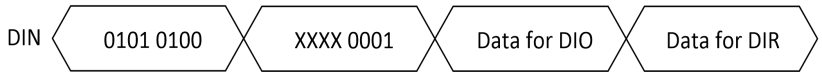
Operands: r, n

Bytes: 2

Encoding: 0101 rrrr xxxx nnnn

Data Transfer Sequence:

Write Two Registers Starting from 04H (DIO)



SELFCAL—Offset and Gain Self Calibration

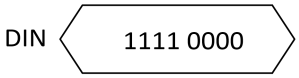
Description: Starts the process of self-calibration. The Offset Calibration Register (OCR) and the Full-Scale Register (FSR) are updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0000

Data Transfer Sequence:



SELFOCAL—Offset Self Calibration

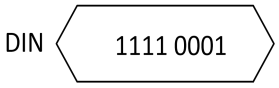
Description: Starts the process of self-calibration for offset. The Offset Calibration Register (OCR) is updated after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0001

Data Transfer Sequence:



SELFGCAL—Gain Self Calibration

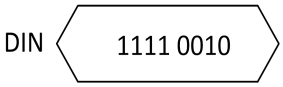
Description: Starts the process of self-calibration for gain. The Full-Scale Register (FSR) is updated with new values after this operation.

Operands: None

Bytes: 1

Encoding: 1111 0010

Data Transfer Sequence:



SYSOCAL—System Offset Calibration

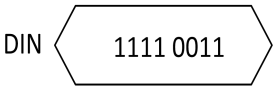
Description: Initiates a system offset calibration. The input should be set to 0V, and the MS1242 computes the OCR value that compensates for offset errors. The Offset Calibration Register (OCR) is updated after this operation. The user must apply a zero input signal to the appropriate analog inputs. The OCR register is automatically updated afterwards.

Operands: None

Bytes: 1

Encoding: 1111 0011

Data Transfer Sequence:



SYSGCAL—System Gain Calibration

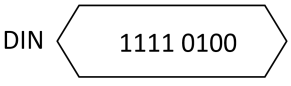
Description: Starts the system gain calibration process. For a system gain calibration, the input should be set to the reference voltage and the MS1242 computes the FSR value that will compensate for gain errors. The FSR is updated after this operation. To initiate a system gain calibration, the user must apply a full-scale input signal to the appropriate analog inputs. FSR register is updated automatically.

Operands: None

Bytes: 1

Encoding: 1111 0100

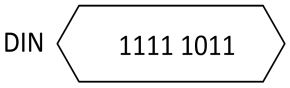
Data Transfer Sequence:



WAKEUP

Description: Wakes the MS1242 from SLEEP mode.
Operands: None
Bytes: 1
Encoding: 1111 1011

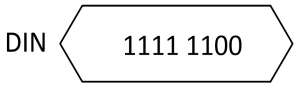
Data Transfer Sequence:



DSYNC—Sync DRDY

Description: Synchronizes the MS1242 to an external event.
Operands: None
Bytes: 1
Encoding: 1111 1100

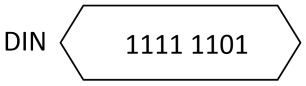
Data Transfer Sequence:



SLEEP—Sleep Mode

Description: Puts the MS1242 into a low power sleep mode. To exit sleep mode, issue the WAKEUP command.
Operands: None
Bytes: 1
Encoding: 1111 1101

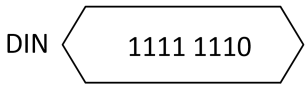
Data Transfer Sequence:



RESET—Reset to Default Values

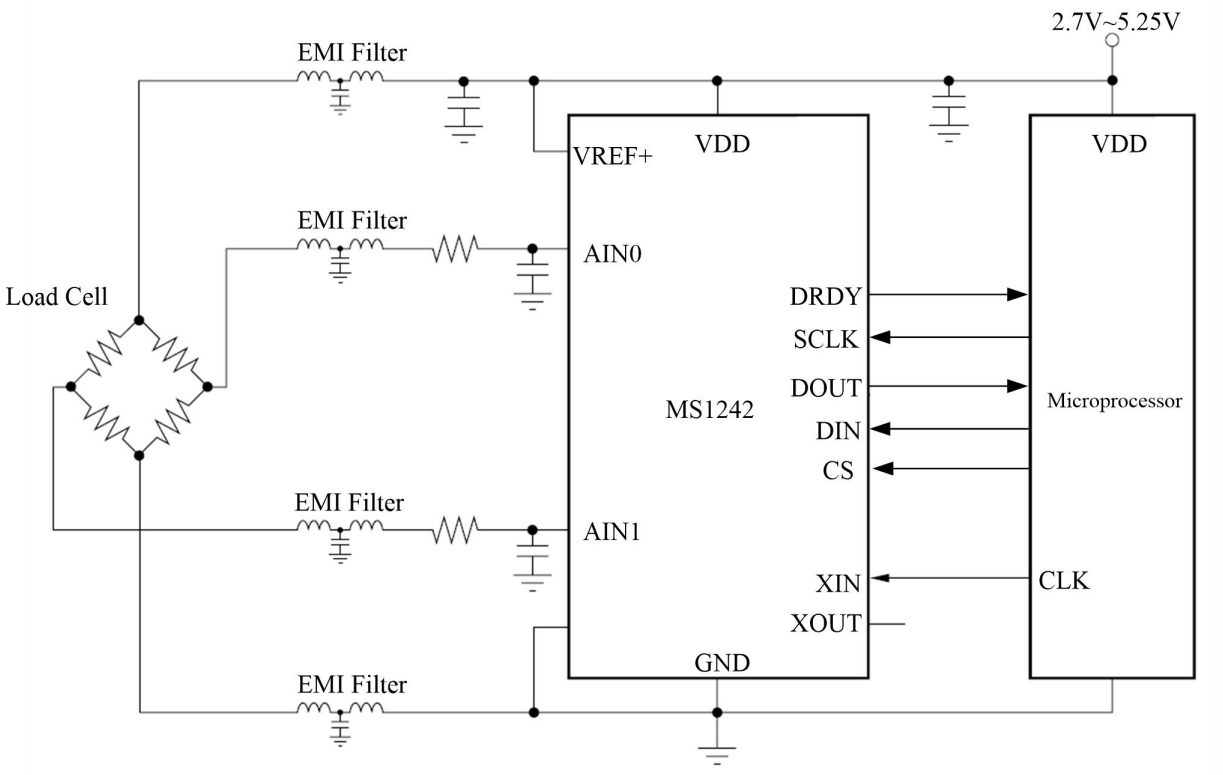
Description: Restore the registers to their power-up values. This command stops the Read Continuous mode.
Operands: None
Bytes: 1
Encoding: 1111 1110

Data Transfer Sequence:

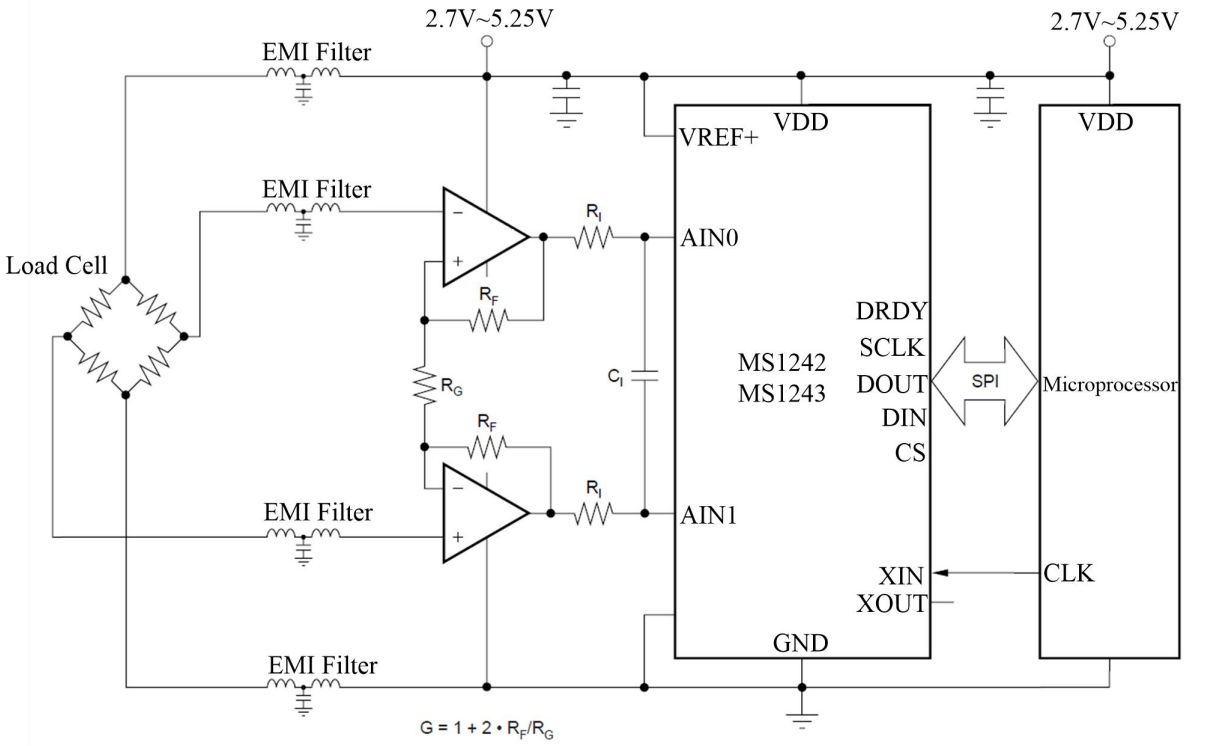


TYPICAL APPLICATION DIAGRAM

The diagram below shows a typical schematic of a general-purpose weight scale application using the MS1242.

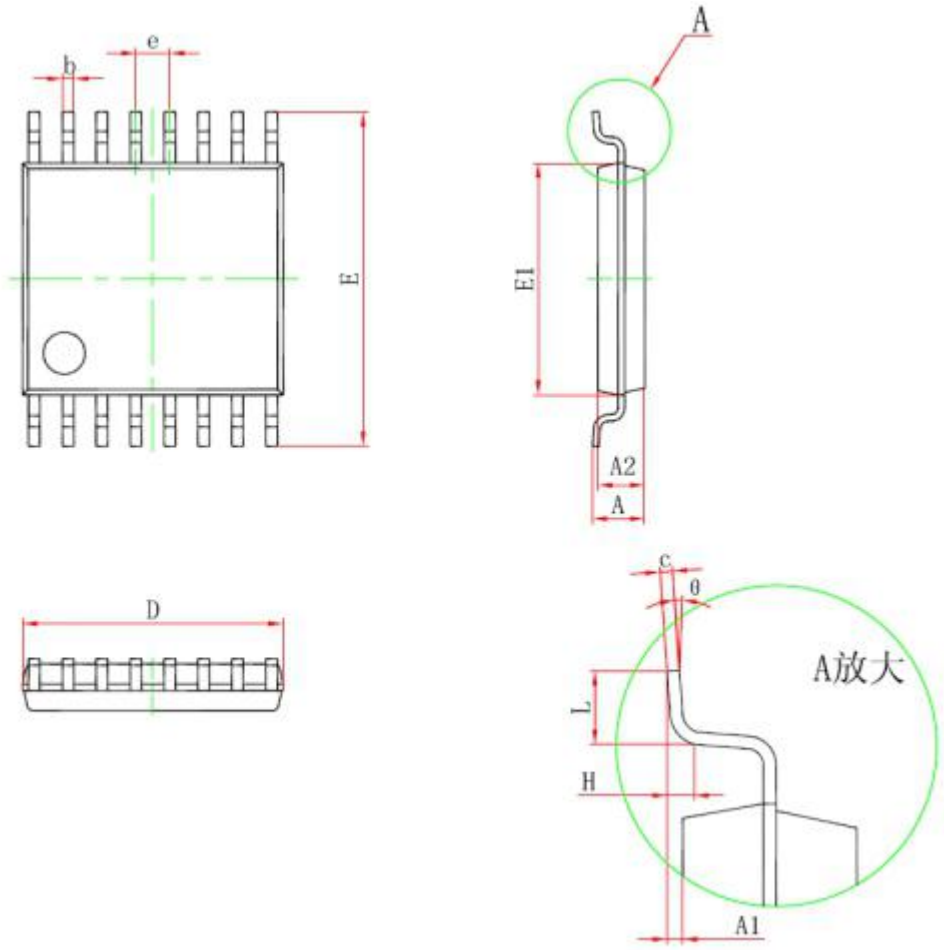


The diagram below shows a typical schematic of a high-precision weight scale application using the MS1242 and MS1243.



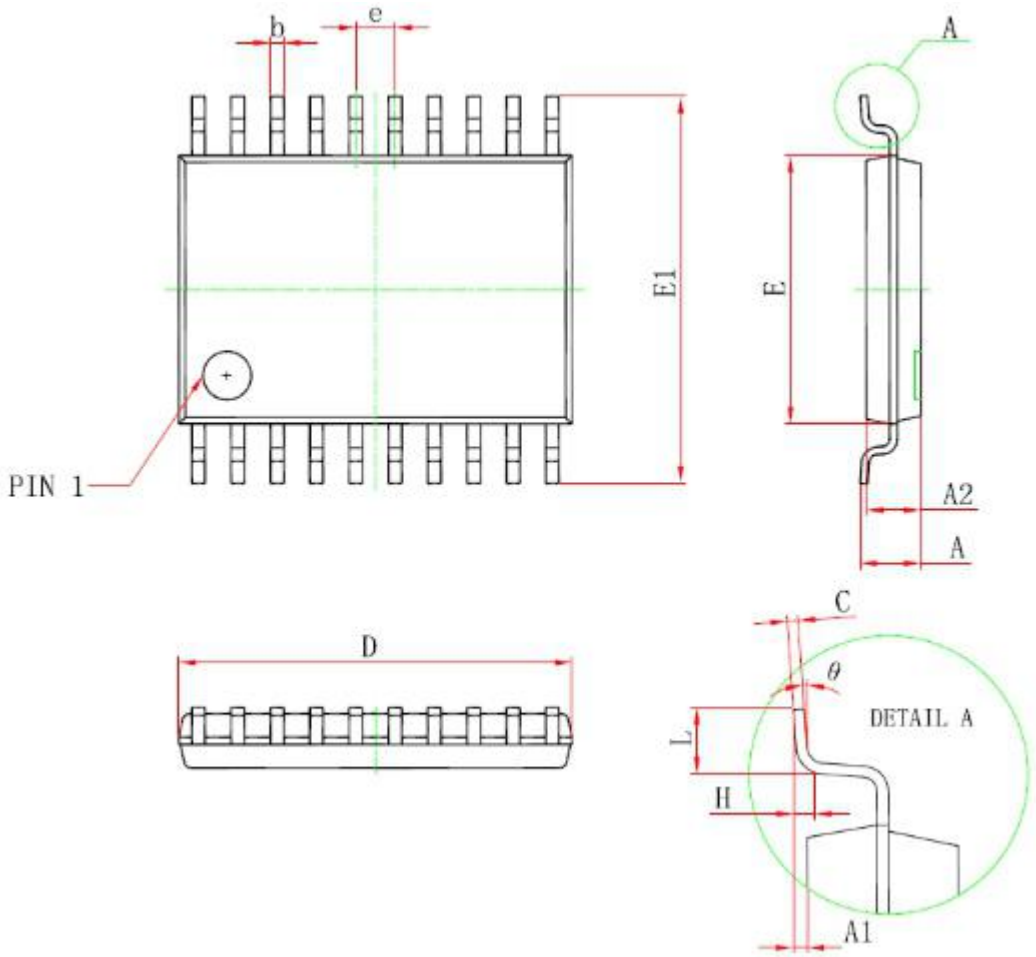
PACKAGE OUTLINE DIMENSIONS

TSSOP16



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.246	0.258
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	4.300	4.500	0.169	0.177
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

TSSOP20



Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
D	6.400	6.600	0.252	0.259
E	4.300	4.500	0.169	0.177
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
E1	6.250	6.550	0.246	0.258
A		1.200		0.047
A2	0.800	1.000	0.031	0.039
A1	0.050	0.150	0.002	0.006
e	0.65(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
H	0.25(TYP)		0.01(TYP)	
θ	1°	7°	1°	7°

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : MS1242, MS1243

Product Code : XXXXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece/Box	Box/Carton	Piece/Carton
MS1242	TSSOP16	3000	1	3000	8	24000
MS1243	TSSOP20	3000	1	3000	8	24000

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- The process of improving product is endless. And our company would sincerely provide more excellent product for customer.

MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

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