AXP717D PMIC For Multi-Core High-Performance System

1 Features

- 3.9V–5.5V Input Operating Range
- Support TWSI(Two Wire Serial Interface)
- 4 DCDCS

  DCDC1: 0.5~1.54V, IMAX=4A

  DCDC2: 0.5~3.4V, IMAX=3A

  DCDC3: 0.5~1.84V, IMAX=1.5A

  DCDC4: 1.0~3.4V, IMAX=3A
- 14 LDOS

  RTCLDO: 1.8V/ 2.5V/ 3V/ 3.3V, 30mA; Support supplied by backup battery (button battery)

  A/B/CLDO: 0.5~3.5V, 0.1V/step

  ALDO2, BLDO1/3, CLDO1/3/4: IMAX=500mA

  ALDO1/4, BLDO4, CLDO2: IMAX=400mA

  ALDO3, BLDO2: IMAX=200mA

  CPUSLDO: for CPUs, 0.5~1.4V, IMAX=30mA, Supplied by DCDC3
- Startup sequence and default voltage of DCDC/LDO setting
- Protection

  Input Over-Voltage Protection

  Thermal Shutdown

  DCDC Over-Voltage/Under-Voltage Protection

  LDO Current Limit Protection

2 Applications

- Sweeper, Commercial display
- Automotive Electronics

3 Description

AXP717D is a highly integrated power management IC (PMIC) targeting at applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

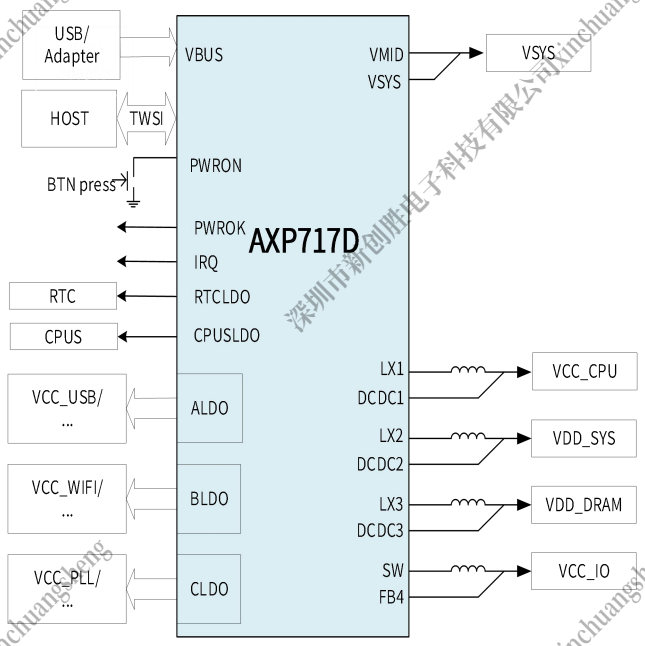
AXP717D supports 18 channel power outputs which include 4 channels DCDC and 14 channels LDO. To ensure the security and stability of the system, AXP717D provides multiple channels 14-bit ADC for voltage/temperature monitor and integrates protection circuits such as over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP).

AXP717D supports TWSI for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

Device Information

Part Number	Package	Body Size
AXP717D	QFN-52	6mm * 6mm

Simplified Application Diagram



Revision History

Revision	Date	Author	Description
1.0	Apr. 26, 2024	AWA 1017	Initial version
1.1	May 07, 2024	AWA 1017	1. Update Table 6-1

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Tables

4 Pin Configuration and Functions

Figure 4-1 Pin Map

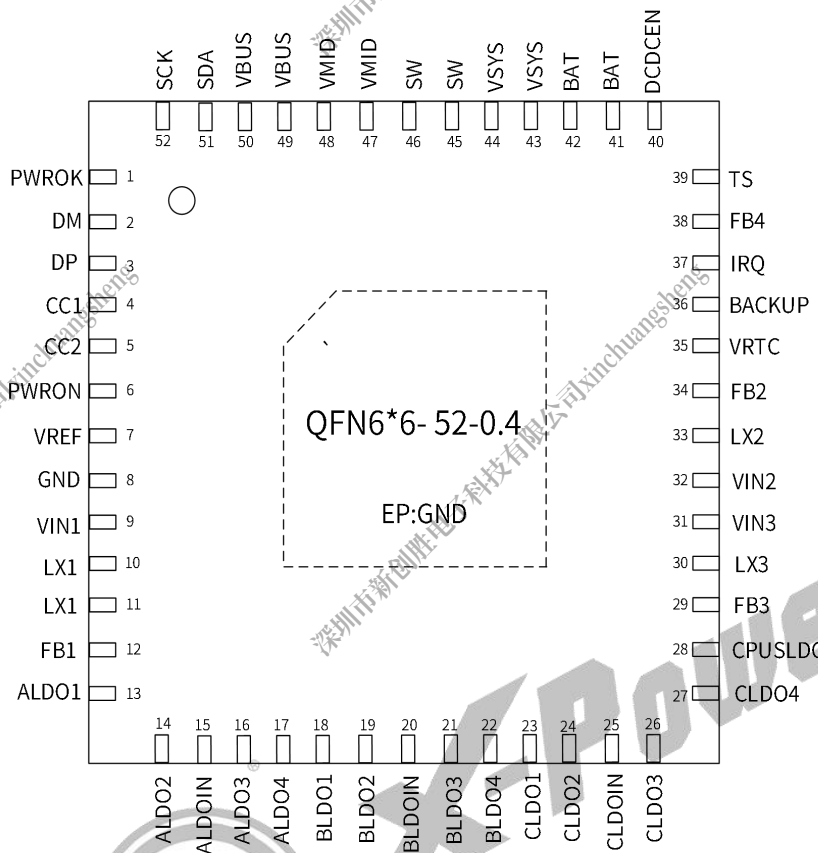


Table 4-1 Pin Description

NO.	Pin Name	I/O(1)	Description
1	PWROK	DIO	Power good indication output
2	DM	DIO	BC1.2 detection, connect to DM of USB connector
3	DP	DIO	BC1.2 detection, connect to DP of USB connector
4	CC1	DIO	Type-C cc logic, connect to CC1 of USB connector
5	CC2	DIO	Type-C cc logic, connect to CC2 of USB connector
6	PWRON	DIO	Power On-Off key input, Internal pulled up.
7	VREF	P	Internal reference voltage
8	GND	G	GND for internal analog circuit
9	VIN1	PI	DCDC1 input source
10/11	LX1	PIO	Inductor pin for DCDC1
12	FB1	AI	DCDC1 feedback pin
13	ALDO1	PO	Output pin of ALDO1
14	ALDO2	PO	Output pin of ALDO2
15	ALDOIN	PI	ALDO input source, connected to VSYS
16	ALDO3	PO	Output pin of ALDO3
17	ALDO4	PO	Output pin of ALDO4
18	BLDO1	PO	Output pin of BLDO1

19	BLDO2	PO	Output pin of BLDO2
20	BLDOIN	PI	BLDO input source, connected to VSYS or DCDC output
21	BLDO3	PO	Output pin of BLDO3
22	BLDO4	PO	Output pin of BLDO4
23	CLDO1	PO	Output pin of CLDO1
24	CLDO2	PO	Output pin of CLDO2
25	CLDOIN	PI	CLDO input source, connected to VSYS or DCDC output
26	CLDO3	PO	Output pin of CLDO3
27	CLDO4	PO	Output pin of CLDO4
28	CPUSLDO	PO	Output pin of CPUSLDO
29	FB3	AI	DCDC3 feedback pin
30	LX3	PIO	Inductor pin for DCDC3
31	VIN3	PI	DCDC3 input source
32	VIN2	PI	DCDC2 input source
33	LX2	PIO	Inductor pin for DCDC2
34	FB2	AI	DCDC2 feedback pin
35	VRTC	PO	RTC power output
36	BACKUP	P	Input pin of backup battery.
37	IRQ	DIO	IRQ output. Connect the IRQ to a logic rail via a resistor. The IRQ pin sends a low level signal to host to report device status and fault.
38	FB4	AI	DCDC4 feedback pin
39	TS	AI	Battery Temperature Sensor Input
40	DCDCEN	DO	Be connected to external DCDC enable pin. The start-up sequence of DCDCEN is the same as that of CLDO2. High level available, internal pulled up to RTCLDO.
41/42	BAT	P	Battery connection point
43/44	VSYS	P	System connection point
45/46	SW	P	Switching node connecting to output inductor
47/48	VMID	P	VMID Power output
49/50	VBUS	P	VBUS input
51	SDA	DIO	Data pin for serial interface.
52	SCK	DI	Clock pin for serial interface.

(1)**O** for output, **I** for input, **IO** for input/output, **D** for digital, **A** for analog, **P** for power, and **G** for ground.

5 Specifications

5.1 Absolute Maximum Ratings (1)

Over operating free-air temperature range (unless otherwise noted)

Table 5-1 Absolute Maximum Ratings

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VBUS	Voltage range(with respect to GND)	-0.3	12	V
Others pin (exp VBUS,EP, GND)		-0.3	7	V
		-0.3	7	V
EP to GND		-0.3	0.3	V
T_a	Operating Temperature Range	-40	85	°C
T_J	Junction Temperature Range	-40	125	°C
T_s	Storage Temperature Range	-40	150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads，10sec)		300	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

Table 5-2 ESD Ratings

		VALUE	UNIT
VESD	Human body model(HBM)(1)	±2000	V
	Charged device model(CDM)(2)	±750	V

(1) Reference: ESDA/JEDEC JS-001-2017.

(2) Reference: ESDA/JEDEC JS-002-2018.

5.3 Recommended Operating Conditions

Table 5-3 Recommended Operating Conditions

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
VIN	Input voltage(VBUS)	3.9	5.5	V
VBAT	Battery voltage		4.4	V

5.4 Thermal Information

Table 5-4 Thermal Information

Thermal Metric(1)		VALUE	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	24.43	°C/W
θ_{JB}	Junction-to-board thermal resistance	3.26	
θ_{JC}	Junction-to-case(top) thermal resistance	11.91	

(1)Thermal metrics are calculated refer to JEDEC document JESD51.

5.5 Electrical Characteristics

T_A=25°C

Table 5-5 Electrical Characteristics

Symbol	Parameters	Test Conditions	MIN	TYP	MAX	UNIT
VBUS POWER UP						
V_{VBUS_OP}	VBUS operating range		3.9		5.5	V
V_{VBUS_UVLOZ}	VBUS under voltage threshold		3.5		3.9	V
V_{VBUS_OV}	VBUS over-voltage rising threshold			7		V
V_{OFF}	VSYS power off threshold		2.6		3.3	V
V_{OFF_HYST}	VSYS power off hysteresis			0.3		V
V_{SYS_OVP}	VSYS over-voltage turn-off		5.8		6	V
THERMAL SHUTDOWN						
T_{SHUT}	Thermal Shutdown Rising Temperature	Temperature rising		145		°C
T_{SHUT_HYS}	Thermal Shutdown Hysteresis	Temperature falling		20		°C
DCDC						
DCDC1/2/3						
VIN	Input Voltage		2.6		5.5	V
UVP				85%		
OVP				130%		
FSW	Switching Frequency			3		MHz
Accuracy	Output Accuracy	Accuracy, PWM mode, V_{OUT}<1V	-30		30	mV
		Accuracy, PWM mode, V_{OUT}>1V	-3.00%		3.00%	
DCDC1						
V_{OUT}	Output Voltage	Output Range	0.5		1.54	V
		Step Size, V_{OUT}=0.5V~1.2V		10		mV
		Step Size, V_{OUT}=1.22V~1.54V		20		mV
I_{OUT}	Output Load Current			4		A
DCDC2						
V_{OUT}	Output Voltage	Output Range	0.5		3.4	V
		Step Size, V_{OUT}=0.5V~1.2V		10		mV
		Step Size, V_{OUT}=1.22V~1.54V		20		mV
		Step Size, V_{OUT}=1.6~3.4V		100		mV
I_{OUT}	Output Load Current			3		A
DCDC3						
V_{OUT}	Output Voltage	Output Range	0.5		1.84	V
		Step Size, V_{OUT}=0.5V~1.2V		10		mV
		Step Size, V_{OUT}=1.22V~1.84V		20		mV
I_{OUT}	Output Load Current			1.5		A
DCDC4						
V_{OUT}	Output Voltage	Output Range	1.0		3.4	V
		Step Size		100		mV
I_{OUT}	Output Load Current			3		A

Accuracy	Output Accuracy	V_{OUT}=3.3V	-3.00%		3.00%	
LDO						
RTCLDO						
V_{OUT}	Output Voltage		1.8		3.3	V
	Output voltage accuracy		-10%		+10%	
I_{OUT}	Output Load Current			30		mA
CPUSLDO						
VIN	Input Voltage	Input is DCDC3	0.8		1.84	V
V_{OUT}	Output Voltage	Output Range	0.5		1.4	V
		Step size		50		mV
		Accuracy,VIN=0.8V~1.84V, V_{OUT}<1V, I_{load}=10mA	-30		30	mV
		Accuracy,VIN=0.8V~1.84V, V_{OUT}>1V, I_{load}=10mA	-3%		3%	
I_{OUT}	Output Load Current			30		mA
ILIM	Current Limit			300		mA
ALDO/BLDO/CLDO 1~4						
VIN	Input Voltage		2.6		5.5	V
V_{Drop}	Dropout	V_{OUT}=3.3V		200		mV
V_{OUT}	Output Voltage	Output Range	0.5		3.5	V
		Step size		100		mV
		Accuracy, ALDOIN=2.6V~5.5V, V_{OUT}<1V, I_{load}=10mA only for ALDO3/4	-20		20	mV
		Accuracy, ALDOIN=2.6V~5.5V, V_{OUT}>1V, I_{load}=10mA only for ALDO3/4	-2%		2%	
		Accuracy, ALDOIN=2.6V~5.5V, V_{ALDO4}=1.8V, I_{load}<50mA	-1%		1%	
		Accuracy, xLDOIN=2.6V~5.5V, V_{OUT}<1V, I_{load}=10mA	-30		30	mV
		Accuracy,xLDOIN=2.6V~5.5V, V_{OUT}>1V, I_{load}=10mA	-3%		3%	
I_{OUT}	Output Load Current	ALDO2, BLDO1/3, CLDO1/3/4		500		mA
		ALDO1/4, BLDO4, CLDO2		400		mA
		ALDO3, BLDO2		200		mA
ILIM	Current Limit			500		mA
TWSI & IO						
TWSI (SCL, SDA)						
VIH	Input high threshold level, SCL and SDA		1.3			V
VIL	Input low threshold level				0.8	V
VOL	Output low threshold level	Sink Current = 5mA, sink current			0.4	V
Logic I/O pin Characteristics (IRQ/PWRON/PWROK)						

VIH	Input high threshold level		1.3			V
VIL	Input low threshold level				0.8	V

6 Detail Description

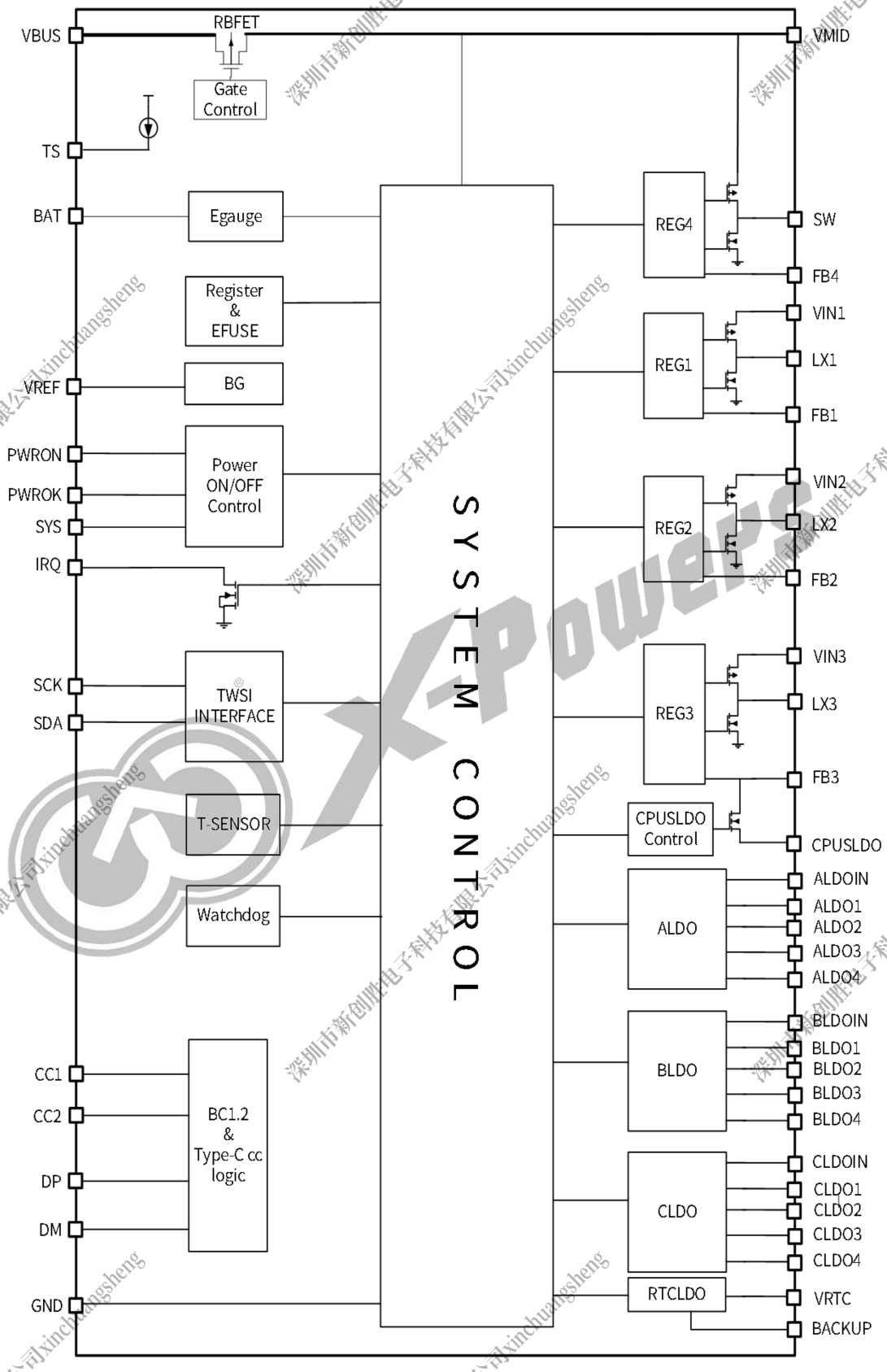
6.1 Overview

AXP717D is a highly integrated power management IC (PMIC) targeting at applications that require multi-channel power conversion outputs. It provides an easy and flexible power management solution for multi-core processors to meet the complex and accurate requirements of power control.

AXP717D supports 18 channel power outputs which include 4 channels DCDC and 14 channels LDO. To ensure the security and stability of the system, AXP717D provides multiple channels 14-bit ADC for voltage/temperature monitor and integrates protection circuits such as over-voltage protection (OVP), over-current protection (OCP) and over-temperature protection (OTP).

AXP717D supports TWSI for system to dynamically adjust output voltages, enable power outputs and configure interrupt condition.

6.2 Function Block Diagram



6.3 Serial Interface Communication

AXP717D supports TWSI protocol and performs as a TWSI slave device with default address 0x68/0x69(8 bits). When AXP717D powers on, SCK/SDA pin of TWSI will be pulled up to IO Power and then Host can adjust and monitor AXP717D with rich feedback information.

Note: "Host" here refers to processor.

6.4 Power On/Off and reset

6.4.1 Power up from VBUS

When VBUS is inserted, PMIC detects the input source whether it is good or not. If VBUS is good, the RBFET is open and PMIC is working.

6.4.1.1 Good source condition

PMIC needs to check the power capability of the input source. Only when the input source meets the following requirements can AXP717D work.

a. VBUS voltage is lower than V_{ACOV}(typical 7V)

b. VBUS voltage is higher than $V_{VBUSUVLO}$ when pulling I_{BADBUS}(typical 15mA)

Once the input source meets the requirements above, the register bit reg00H[5](VBUS_GD) is set to 1 to indicate the input source is good.

6.4.2 System power on/off management

PMIC has power off and power on status. When at off state, all voltage outputs are turned off except RTCLDO.

6.4.2.1 Power on-off Key (POK)

The Power on-off Key (POK) can be connected between PWRON pin and GND of AXP717D. AXP717D can automatically identify the four status (Long-press, Short-press, Negative edge, Positive edge) and then correspond respectively.

6.4.2.2 Power on

Power on sources include:

(1). POK. AXP717D can be powered on by pressing and holding POK for a period of time that longer than "ONLEVEL".

(2). VBUS low to high.

(3). IRQ Low level. IRQ pin is low level for more than 4ms, AXP717D will be powered on.

After power on, DCDCs and LDOs will be soft booted in preset timing sequence.

6.4.2.3 Power off

Power off sources include:

(1). POK. AXP717D can be powered off by pressing and holding POK for a period of time that longer than "OFFLEVEL". The function can be configured by REG22H [1] and REG22H [0] decides whether the PMIC auto turns on or not when it shuts down after OFFLEVEL POK.

(2). Write "1" to REG27H [0].

(3). VSYSGOOD high to low. When VSYS<VOFF or VBUS>7V, AXP717D will be powered off. The default of VOFF is 2.6V which can be configured by REG24H [6:4].

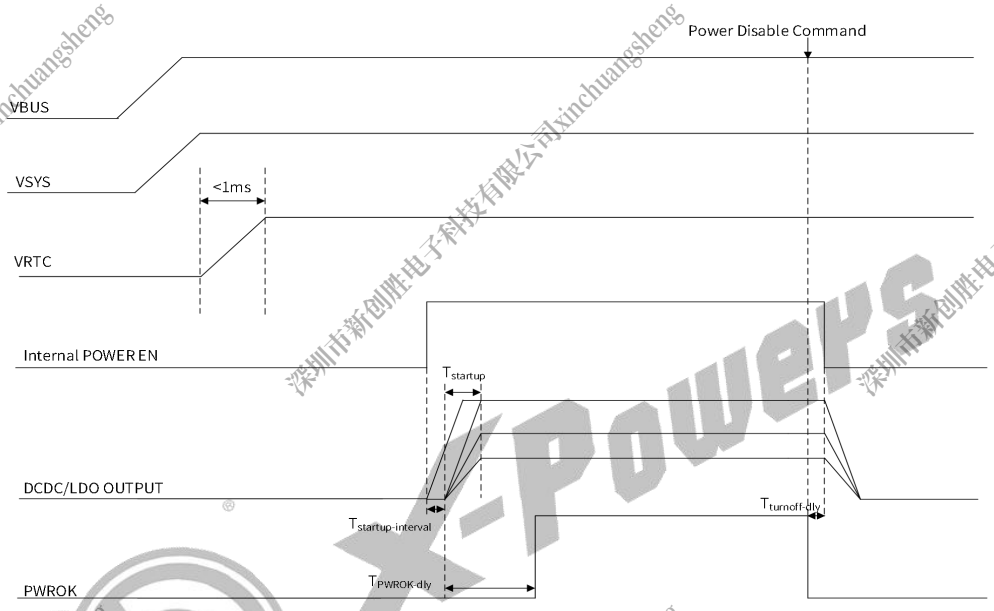
(4). The output voltage of DCDC is 15% lower than the setting value. The function can be configured by REG23H [3:0].

(5). The output voltage of DCDC is much larger than their setting(130%). The function can be configured by REG23H [4].

(6). Die temperature is over the warning level2(145°C). The function can be configured by REG22H [2].

(7). LDO over current(typical 500mA for ALDO/BLDO/CLDO). The function can be configured by REG22H [3].

Figure 6-1 System power up and shut down sequence



6.4.2.4 Sleep and wakeup

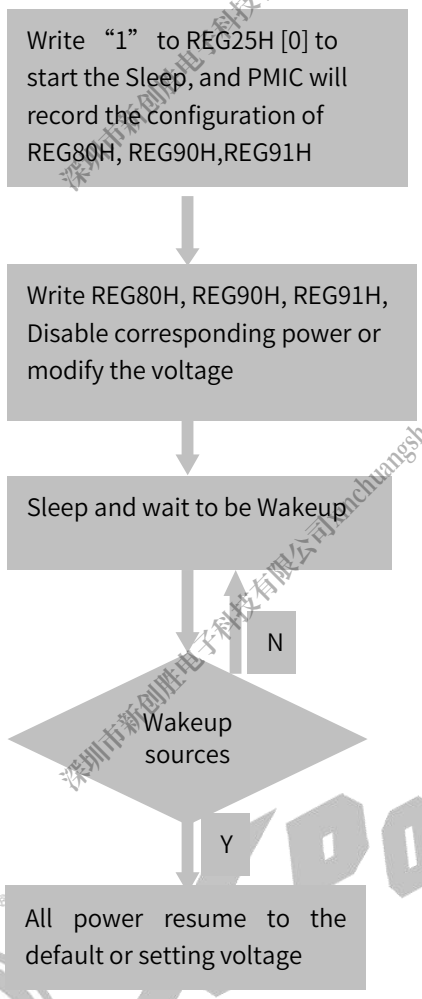
When the running system needs to enter Sleep mode, maybe one or several power outputs should be disabled or changed to other voltage. Wakeup can be initiated by the following sources:

1. Software wakeup (REG25H [1] is set to 1)
2. IRQ pin wakeup (REG25H [5]=1 and IRQ pin is low level for more than 4ms)

These sources will make all the power outputs resume to the default voltage or the setting voltage, which is configured by REG25H [2], and all shutdown powers will resume by the startup sequence.

The control process under sleep and wakeup modes is as below.

Figure 6-2 Sleep and Wakeup



6.4.2.5 System Reset

System reset means the related registers will be reset when PMIC is power off. The system will power off and then power on. VRTC will not be off during restart. Restart can be initiated by the following sources:

(1). PWROK drive low.

The PWROK pin can be used as the reset signal of application system. During AXP717D startup, PWROK outputs low level, which will be pulled up to startup the system after output voltage reaches the regulated value.

When application system works normally, if the PWROK pin is driven low for about 128us, the PMIC will be restarted. The function can be configured by REG27H [3].

(2). Write “1” to REG27H [1] to restart the PMIC.

(3). Watchdog timeout. The function can be configured by REG19H [0] and REG1AH [5:4].

6.4.2.6 POR

Power on reset means all the registers will be reset when PMIC is power down. All voltage outputs are turned off including RTCLDO and VREF. Pressing and holding POK for more than 16s can force POR.

6.5 Multi-Power Outputs

The following table has listed the multi-power outputs and their functions of AXP717D.

Table 6-1 Multi-Power Outputs

Output Path	Type	Default Voltage	Startup Sequence	Application Suggestion	Load Capacity
DCDC1	BUCK	0.9	1	SYS	4000mA
DCDC2	BUCK	0.9	1	NPU	3000mA
DCDC3	BUCK	1.1	1	DRAM	1500mA
DCDC4	BUCK	3.3	OFF	WIFI	3000mA
ALDO1	LDO	1.8	OFF	AVDD-CSI	400mA
ALDO2	LDO	1.8	OFF	VCC-PE	500mA
ALDO3	LDO	3.3	3	VCC-USB/VCC-PL	200mA
ALDO4	LDO	1.8	1	AVCC/PLL/DRAM	400mA
BLDO1	LDO	1.8	OFF	PG	500mA
BLDO2	LDO	1.8	1	LPDDR	200mA
BLDO3	LDO	2.8	OFF	MOTOR	500mA
BLDO4	LDO	1.2	OFF	DVDD-CSI	400mA
CLDO1	LDO	1.8	2	MIPI/LVDS	500mA
CLDO2	LDO	2.5	1	DDR	400mA
CLDO3	LDO	3.3	3	FLASH	500mA
CLDO4	LDO	3.3	OFF	LCD	500mA
VCPUS	LDO	0.9	1	CPUS	30mA
VRTC	LDO	1.8	Always on	RTC	30mA

AXP717D includes 4 synchronous step-down DCDCs and 14 LDOs. The work frequency of DCDC1/2/3 is 3MHz . External small inductors and capacitors can be connected. In addition, DCDC1/2/3 can be set in fixed PWM mode or auto mode (automatically switchable according to the load). See register REG81H.

DCDC1/2/3 has DVM enable option. In DVM mode, when there is a change in the output voltage, DCDC will change to the new targeted value step by step. It supports two kinds of DVM slope: 1 step/15.625us and 1step/31.250us. The slope can be chosen by REG82H [0].

6.6 ADC

AXP717D has a low speed 14 bits ADC for measuring BAT voltage, VBUS voltage, VSYS voltage, TS voltage and die temperature.

Table 6-2 ADC channel

No.	Channel function	000H	001H	002H	…	1FFFH
0	BAT voltage	0mV	1mV	2mV	…	8.191V
1	VBUS voltage	0mV	1mV	2mV	…	8.191V
2	VSYS voltage	0mV	1mV	2mV	…	8.191V
3	TS voltage	0mV	0.5mV	1mV	…	4.0955V
4	die temperature	0mV	0.1mV	2mV	…	0.8191V

Note: ADC data is 14 bits. In order to get the complete data, TWSI must read the high 6 bits firstly and then the low 8 bits.

6.7 E-Gauge

AXP717D features a Fuel Gauge system which can measure the external battery power. The Fuel Gauge system is able to export information about battery capacity percentage (regA4H) and Battery Voltage (regC4H, regC5H). The Fuel Gauge can be enabled or disabled through reg0BH[2]. The Battery low warning level can be set through reg1BH, and IRQ will be sent out to alert the platform when the battery capacity percentage is lower than the warning level set through reg1BH.

Once a default battery is selected for a particular design, it is highly recommended to program the battery module to achieve better Fuel Gauge accuracy. Once the battery module data are available, user can write these information to battery parameter (REGA1H) after brom is enabled on each boot. Additionally, the Fuel Gauge system is capable to learn the battery characteristic automatically.

6.8 IRQ /BACKUP

6.8.1 IRQ

AXP717D has an IRQ pin which is used to indicate whether there interrupt events occur.

PMIC Interrupt Controller monitors the trigger events such as over voltage, over current, PWRON pin signal, over temperature and so on. When the events occur and their IRQ enabled bits are set to 1 (Refer to registers reg40H~44H), corresponding IRQ status will be set to 1 (Refer to registers reg48H~4CH), and IRQ pin will be pulled down. When Host detects triggered IRQ signal, Host will scan through the IRQ Status registers and respond accordingly. Meanwhile, Host will reset the IRQ status by writing "1" to status bit.

6.8.2 BACKUP

AXP717D has a backup pin which is used to connect backup battery. It is the source of RTCLDO when PMIC has only backup battery.

When PMIC is power on, the backup battery also can be charged by configuring reg19H[3]. The charger is working under linear mode with 100uA charge current and the termination voltage can be configured by reg6AH in range from 2.6V to 3.3V (default 2.9V).

6.9 Register

6.9.1 Register List

Address	Description	R/W
0X00	PMIC status1	R
0X01	PMIC status2	R
0X05	BC_detect	R
0X08	PMIC fault	RW1C
0X0B	Module enable control1	RW
0X10	DCDC/LDO Discharge configure	RW
0X14	Tshut configure	RW
0X18	Reset the fuel gauge	RW
0X19	Module enable control2	RW
0X1A	Watchdog control	RW
0X1B	Low Battery warning threshold setting	RW
0X20	PWRON status	R
0X21	PWROFF status	R
0X22	PWROFF_EN	RW
0X23	PWROFF of DCDC OVP/UVP control	RW
0X24	VSYS voltage for PWROFF threshold setting	RW
0X25	Sleep and Wakeup configure	RW
0X26	IRQLEVEL/OFFLEVEL/ONLEVEL setting	RW
0X27	Soft Poweroff configure	RW
0X40-0X42	IRQ Enable	RW
0X48-0X4A	IRQ Status	RW
0X50	TS pin configure	RW
0X6A	Button battery charge termination voltage setting	RW
0X80-0X82	DCDC configure0/1/2	RW
0X83-0X86	DCDC1/2/3/4 voltage setting	RW
0X90-0X91	LDOS ON/OFF control	RW
0X93-0X9F	LDOS voltage setting	RW
0XA1	Battery parameter	RW
0XA2	Fuel gauge control	RW
0XA4	Battery percentage data	R
0XC0	ADC Channel enable control	RW
0XC4-0XC9	VBAT/VBUS/VSYS ADC data	R
0XCD	ADC_data select	RW
0XCE/0XCF	adc_data	R

6.9.2 Register Description

6.9.2.1 REG 00: PMIC status1

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	VBUS good indication 0: not good 1: good	RO	POR	0
4:0	Reserved	RO	/	0

6.9.2.2 REG 01: PMIC status2

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	System status indication 0: System is power off. 1: System is power on.	RO	POR	0
3:0	Reserved	RO	/	0

6.9.2.3 REG 05: BC_detect

Bit	Description	R/W	Reset	Default
7:5	USB BC1.2 Detect result 000:Reserved 001:SDP 010:CDP 011:DCP 1XX:Reserved	RO	POR	000
4:0	Reserved	RO	/	0

6.9.2.4 REG 08: PMIC fault

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	VBUS Over Voltage 0:VBUS<=7V 1:VBUS>7V	RW1C	POR	0
4	DCDC Over Voltage 0: DCDC Voltage <= 130% 1: DCDC Voltage > 130%	RW1C	POR	0
3	VSYS Over Voltage of 5V 0: VSYS < 5V 1: VSYS >= 5V	RW1C	POR	0
2:0	Reserved	RO	/	0

6.9.2.5 REG 0B: Module enable control1

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	BC1.2 detect enable 0:disable 1:enable	RW	POR	1
3	Type-C CC detect enable 0:disable 1:enable	RW	POR	1
2	Gauge enable 0:disable 1:enable	RW	POR	1
1	Reserved	RO	/	0
0	Watchdog enable 0:disable 1:enable	RWAC	POR	0

6.9.2.6 REG 10: DCDC/LDO Discharge configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	00100b
2	Internal off-discharge enable for DCDC & LDO 0:disable 1:enable	RW	POR	1
1:0	Reserved	RW	/	10b

6.9.2.7 REG 14: Tshut configure

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2:1	DIE Over Temperature Protection Level1 Configuration 00: 115deg 01: 125deg 10: 135deg 11: Reserved	RW	POR	01b
0	DIE Temperature Detect Enable 0: disable 1: enable	RW	POR	1

6.9.2.8 REG 18: Reset the fuel gauge

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	Reset the gauge(includes registers) 0: normal 1: reset	RWAC	POR	0
2	Reset the gauge besides registers 0: normal 1: reset	RW	POR	0
1:0	Reserved	RO	/	0

6.9.2.9 REG 19: Module enable control2

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	Button Battery charge enable 0: disable 1: enable	RW	System Reset	0
2:1	Reserved	RO	/	11b
0	Watchdog Module enable 0: disable 1: enable	RW	System Reset	0

6.9.2.10 REG 1A: Watchdog control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:4	Watchdog Reset Configuration 00: IRQ only 01: IRQ and Registers System Reset 10: Registers System Reset and Pull down PWROK 1s 11: RESTART	RW	POR	0
3	Watchdog clear signal 0: normal 1: clear	RWAC	POR	0
2:0	TWSI watchdog timer configuration 000: 1s 001: 2s 010: 4s 011: 8s 100: 16s 101: 32s 110: 64s 111: 128s	RW	POR	110b

6.9.2.11 REG 1B: Gauge low battery warning threshold setting

Bit	Description	R/W	Reset	Default
7:4	low battery warning threshold 5-20%, 1% per step 0000: 5% 0001: 6%	RW	POR	1010b

	…… 1111: 20%			
3:0	low battery shutdown threshold 0-15%, 1% per step 0000: 0% 0001: 1% …… 1111: 15%	RW	POR	0001b

6.9.2.12 REG 20: PWRON status

Bit	Description	R/W	Reset	Default
7:3	Reserved	RO	/	0
2	VBUS insert and good as POWERON Source 0: no 1: yes	RO	System Reset	0
1	IRQ pin pull-down as POWERON Source 0: no 1: yes	RO	System Reset	0
0	PWRON pin low for ONLEVEL as POWERON Source 0: no 1: yes	RO	System Reset	0

6.9.2.13 REG 21: PWROFF status

Bit	Description	R/W	Reset	Default
7	Die over temperature as POWEROFF Source 0: no 1: yes	RO	POR	0
6	DCDC over voltage as POWEROFF Source 0: no 1: yes	RO	POR	0
5	DCDC under voltage as POWEROFF Source 0: no 1: yes	RO	POR	0
4	LDO over current as POWEROFF Source 0: no 1: yes	RO	POR	0
3	VSYS under voltage as POWEROFF Source 0: no 1: yes	RO	POR	0
2	Reserved	RO	/	0
1	Software configuration as POWEROFF Source 0: no 1: yes	RO	POR	0
0	PWRON pin low for OFFLEVEL as POWEROFF Source 0: no 1: yes	RO	POR	0

6.9.2.14 REG 22: PWROFF_EN

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	LDO Over-Current as POWEROFF Source enable 0: disable 1: enable	RW	POR	0
2	Reserved	RO	/	1
1	PWRON > OFFLEVEL as POWEROFF Source enable 0: disable 1: enable	RW	POR	1
0	Function Select when REG22H[1]=1 and button event occur 0: Power-off 1: Restart	RW	POR	0

6.9.2.15 REG 23: PWROFF of DCDC OVP/UVP control

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0

4	DCDC 120%(130%) high voltage turn off PMIC function 0: disable 1: enable	RW	POR	1
3	DCDC4 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	0
2	DCDC3 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1
1	DCDC2 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1
0	DCDC1 85% low voltage turn off PMIC function 0: disable 1: enable	RW	POR	1

6.9.2.16 REG 24: VSYS voltage for PWROFF threshold setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:4	VSYS Voltage for POWEROFF 2.6~3.3V,0.1V/step,8steps 000: 2.6V 001: 2.7V …… 111: 3.3V	RW	POR	000
3	Reserved	RO	/	0
2	Check the PWROK Pin enable after all dcdc/ldo output valid 128ms 0: disable 1: enable	RW	POR	1
1	POWEROFF Delay 4ms after PWROK disable 0: disable 1: enable	RW	POR	1
0	POWEROFF Sequence Control 0: At the same time 1: the reverse of the startup	RW	POR	0

6.9.2.17 REG 25: Sleep and Wakeup configure

Bit	Description	R/W	Reset	Default
7:6	Reserved	R0	/	0
5	IRQ pin low to wakeup 0: disable 1: enable	RW	POR	0
4:3	Reserved	RO	POR	0
2	DCDC/LDO voltage select when wakeup 0: The default 1: The voltage before wakeup	RW	POR	0
1	Wakeup enable 0: disable 1: enable	RWLC	System Reset	0
0	Sleep enable 0: disable 1: enable	RWLC	System Reset	0

6.9.2.18 REG 26: IRQLEVEL/OFFLEVEL/ONLEVEL setting

Bit	Description	R/W	Reset	Default
7:6	Reserved	R0	/	0
5:4	IRQLEVEL configuration 00: 1s 01: 1.5s 10: 2s 11: 2.5s	RW	POR	01b
3:2	OFFLEVEL configuration	RW	POR	01b

	00: 4s 01: 6s 10: 8s 11: 10s			
1:0	ONLEVEL configuration 00: 128ms 01: 512ms 10: 1s 11: 2s	RW	POR	10b

6.9.2.19 REG 27: Soft Poweroff configure

Bit	Description	R/W	Reset	Default
7:4	Reserved	R0	POR	0
3	PWROK pin pull low to restart the system 0: disable 1: enable	RW	POR	0
2	PWRON 16s to shutdown the PMIC enable 0: disable 1: enable	RW	POR	1
1	Restart the system, POWOFF/POWON and reset the related registers 0: normal 1: reset	RWAC	POR	0
0	Soft PWROFF 0: Normal 1: PWROFF Configure	RWAC	POR	0

6.9.2.20 REG 40: IRQ Enable 0

Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level2 IRQ enable 0: disable 1: enable	RW	System Reset	1
6	SOC drop to Warning Level1 IRQ enable 0: disable 1: enable	RW	System Reset	1
5	Reserved	RO	/	1
4	Gauge New SOC IRQ enable 0: disable 1: enable	RW	System Reset	1
3:2	Reserved	RO	/	00
1	VBUS Over Voltage IRQ enable 0: disable 1: enable	RW	System Reset	1
0	VBUS Fault IRQ enable 0: disable 1: enable	RW	System Reset	1

6.9.2.21 REG 41: IRQ Enable 1

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	1111b
3	POWERON Short PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1
2	POWERON Long PRESS IRQ enable 0: disable 1: enable	RW	System Reset	1
1	POWERON Negative Edge IRQ enable 0: disable 1: enable	RW	System Reset	0
0	POWERON Positive Edge IRQ enable 0: disable 1: enable	RW	System Reset	0

6.9.2.22 REG 42: IRQ Enable 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ enable	RW	System	0

	0: disable 1: enable		Reset	
6	LDO Over Current IRQ enable 0: disable 1: enable	RW	System Reset	1
5:3	Reserved	RO	/	011b
2	DIE Over Temperature level1 IRQ enable 0: disable 1: enable	RW	System Reset	1
1:0	Reserved	RO	/	11b

6.9.2.23 REG 48: IRQ Status 0

Bit	Description	R/W	Reset	Default
7	SOC drop to Warning Level IRQ 0: no irq 1: irq when SOC >= Warning Level or SOC < shutdown Level to clear it	RW1C	System Reset	0
6	SOC drop to Shutdown Level IRQ 0: no irq 1: irq when SOC >= Shutdown Level to clear it	RW1C	System Reset	0
5	Reserved	RO	/	0
4	Gauge New SOC IRQ 0: no irq 1: irq	RW1C	System Reset	0
3:2	Reserved	RO	/	0
1	VBUS OverVoltage IRQ 0: no irq 1: irq	RW1C	System Reset	0
0	VBUS Fault IRQ 0: no irq 1: irq	RW1C	System Reset	0

6.9.2.24 REG 49: IRQ Status 1

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	POWERON Short PRESS IRQ 0: no irq 1: irq	RW1C	System Reset	0
2	POWERON Long PRESS IRQ 0: no irq 1: irq	RW1C	System Reset	0
1	POWERON Negative Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0
0	POWERON Positive Edge IRQ 0: no irq 1: irq	RW1C	System Reset	0

6.9.2.25 REG 4A: IRQ Status 2

Bit	Description	R/W	Reset	Default
7	Watchdog Expire IRQ 0: no irq 1: irq	RW1C	System Reset	0
6	LDO Over Current IRQ 0: no irq 1: irq LDO Current to normal to clear it	RW1C	System Reset	0
5:3	Reserved	RO	/	0
2	DIE Over Temperature level1 IRQ 0: no irq 1: irq DIE Temperature to normal to clear it	RW1C	System Reset	0
1:0	Reserved	RO	/	0

6.9.2.26 REG 50: TS pin configure

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3:2	TS current source on/off enable 00: off 01/10: on when TS channel of ADC is enabled 11: always on	RW	POR	00b
1:0	current source to TS pin configuration 00: 20uA 01: 40uA 10: 50uA 11: 60uA	RW	POR	10b

6.9.2.27 REG 6A: Button battery charge termination voltage setting

Bit	Description	R/W	Reset	Default
7:3		RO	/	0
2:0	Button Battery charge termination voltage 2.6~3.3V，100mV/step，8steps 000: 2.6V 001: 2.7V 010: 2.8V 011: 2.9V 100: 3.0V 101: 3.1V 110: 3.2V 111: 3.3V	RW	POR	011b

6.9.2.28 REG 80: DCDC configure0

Bit	Description	R/W	Reset	Default
7:4	Reserved	RO	/	0
3	DCDC4 enable 0: disable 1: enable	RW	System Reset	0
2	DCDC3 enable 0: disable 1: enable	RW	System Reset	1
1	DCDC2 enable 0: disable 1: enable	RW	System Reset	1
0	DCDC1 enable 0: disable 1: enable	RW	System Reset	1

6.9.2.29 REG 81: DCDC configure1

Bit	Description	R/W	Reset	Default
7	DCDC frequency spread enable 0: disable 1: enable	RW	System Reset	0
6	DCDC frequency spread range control 0: 50KHz 1: 100kHz	RW	System Reset	0
5	Reserved	RO	/	0
4	DCDC3 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0
3	DCDC2 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0
2	DCDC1 PWM/PFM Control 0: Auto Switch 1: Always PWM	RW	System Reset	0
1:0	Reserved	RO	/	0

6.9.2.30 REG 82: DCDC configure2

Bit	Description	R/W	Reset	Default
7:1	Reserved	RO	/	0
0	DVM voltage ramp control 0: 15.625 us/step 1: 31.250 us/step	RW	System Reset	0

6.9.2.31 REG 83: DCDC1 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC1 DVM enable control 0: disable 1: enable	RW	System Reset	1
6:0	DCDC1 output voltage config 0.5~1.2V,10mV/step,71steps 1.22~1.54V,20mV/step,17steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1010111: 1.54V 1011000~1111111: Reserved	RW	System Reset	0101000

6.9.2.32 REG 84: DCDC2 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC2 DVM enable control 0: disable 1: enable	RW	System Reset	1
6:0	DCDC2 output voltage config 0.5~1.2V,10mV/step,71steps 1.22~1.54V,20mV/step,17steps 1.6~3.4V,100mV/step,19steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1010111: 1.54V 1011000: 1.60V 1011001: 1.70V …… 1101011: 3.40V 1101100~1111111: Reserved	RW	System Reset	0101000

6.9.2.33 REG 85: DCDC3 voltage setting

Bit	Description	R/W	Reset	Default
7	DCDC3 DVM enable control	RW	System	1

	0: disable 1: enable		Reset	
6:0	DCDC3 output voltage config 0.5~1.2V,10mV/step,71steps 1.22~1.84V,20mV/step,32steps 0000000: 0.50V 0000001: 0.51V …… 1000110: 1.20V 1000111: 1.22V 1001000: 1.24V …… 1100110: 1.84V 1100111~1101000: Reserved	RW	System Reset	0111100

6.9.2.34 REG 86: DCDC4 voltage setting

Bit	Description	R/W	Reset	Default
7	Reserved	RO	/	0
6:0	DCDC4 output voltage config 1.0~3.4V,100mV/step,21steps 00000: 1.0V 00001: 1.1V …… 11000: 3.4V 11001~11111: Reserved	RW	System Reset	0010111

6.9.2.35 REG 90: LDOS ON/OFF control 0

Bit	Description	R/W	Reset	Default
7	bldo4 enable 0: disable 1: enable	RW	System Reset	0
6	bldo3 enable 0: disable 1: enable	RW	System Reset	0
5	bldo2 enable 0: disable 1: enable	RW	System Reset	1
4	bldo1 enable 0: disable 1: enable	RW	System Reset	0
3	aldo4 enable 0: disable 1: enable	RW	System Reset	1
2	aldo3 enable 0: disable 1: enable	RW	System Reset	1
1	aldo2 enable 0: disable 1: enable	RW	System Reset	0
0	aldo1 enable 0: disable 1: enable	RW	System Reset	0

6.9.2.36 REG 91: LDOS ON/OFF control 1

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4	cpusldo enable 0: disable 1: enable	RW	System Reset	1
3	cldo4 enable	RW	System	0

	0: disable 1: enable		Reset	
2	cldo3 enable 0: disable 1: enable	RW	System Reset	1
1	cldo2 enable 0: disable 1: enable	RW	System Reset	1
0	cldo1 enable 0: disable 1: enable	RW	System Reset	1

6.9.2.37 REG 93: ALDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	aldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	01101

6.9.2.38 REG 94: ALDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	aldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	01101

6.9.2.39 REG 95: ALDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	aldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	11100

6.9.2.40 REG 96: ALDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	aldo4 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	01101

6.9.2.41 REG 97: BLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	bldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	01101

6.9.2.42 REG 98: BLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	bldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	01101

6.9.2.43 REG 99: BLDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	bldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	10111

6.9.2.44 REG 9A: BLDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	bldo4 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	00111

6.9.2.45 REG 9B: CLDO1 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	cldo1 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V ……	RW	System Reset	01101

	11110: 3.5V 11111: Reserved			

6.9.2.46 REG 9C: CLDO2 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	cldo2 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	10100

6.9.2.47 REG 9D: CLDO3 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	cldo3 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	11100

6.9.2.48 REG 9E: CLDO4 voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	cldo4 output voltage configuration 0.5~3.5V，100mV/step，31steps 00000: 0.5V 00001: 0.6V …… 11110: 3.5V 11111: Reserved	RW	System Reset	11100

6.9.2.49 REG 9F: CPUSLDO voltage setting

Bit	Description	R/W	Reset	Default
7:5	Reserved	RO	/	0
4:0	cpusldo output voltage configuration 0.5~1.4V，50mV/step，20steps 00000: 0.50V 00001: 0.55V …… 10011: 1.40V 10100~11111: Reserved	RW	System Reset	01000

6.9.2.50 REG A1: Battery parameter

Bit	Description	R/W	Reset	Default
7:0	Battery parameter ROM	RO	POR	xx

6.9.2.51 REG A2: Fuel gauge control

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5	Reserved	RW	POR	0
4	ROM or SRAM select 0: select rom 1: select sram	RW	POR	0
3:1	Reserved	RO	/	0
0	brom writer control 0: disable 1: enable	RW	POR	0

6.9.2.52 REG A4: Battery percentage data

Bit	Description	R/W	Reset	Default
7:0	battery percentage	RO	POR	00h

6.9.2.53 REG C0: ADC Channel enable control

Bit	Description	R/W	Reset	Default
7	button battery(backup battery) voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0
6	VMID voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0
5	Reserved	RO	/	0
4	die temperature measure ADC channel enable 0: disable 1: enable	RW	POR	0
3	system voltage voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0
2	VBUS voltage measure ADC channel enable 0: disable 1: enable	RW	POR	0
1	TS pin measure ADC channel enable 0: disable 1: enable	RW	POR	1
0	battery voltage measure ADC channel enable 0: disable 1: enable	RW	POR	1

6.9.2.54 REG C4: vbat_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:0	vbat[13:8]	RO	POR	0

6.9.2.55 REG C5: vbat_l

Bit	Description	R/W	Reset	Default
7:0	vbat[7:0]	RO	POR	0

6.9.2.56 REG C6: VBUS_h

Bit	Description	R/W	Reset	Default

7:6	Reserved	RO	/	0
5:0	VBUS[13:8]	RO	POR	0

6.9.2.57 REG C7: VBUS_l

Bit	Description	R/W	Reset	Default
7:0	VBUS[7:0]	RO	POR	0

6.9.2.58 REG C8: VSYS_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:0	VSYS[13:8]	RO	POR	0

6.9.2.59 REG C9: VSYS_l

Bit	Description	R/W	Reset	Default
7:0	VSYS[7:0]	RO	POR	0

6.9.2.60 REG CD: ADC_data select

Bit	Description	R/W	Reset	Default
7:2	Reserved	RO	/	0
1:0	adc_data_h/adc_data_l select configure: 00: TS 01:TDIE 10:VMID 11:VBACKUP	RW	POR	0

6.9.2.61 REG CE: adc_data_h

Bit	Description	R/W	Reset	Default
7:6	Reserved	RO	/	0
5:0	adc_data_h[13:8]	RO	POR	0

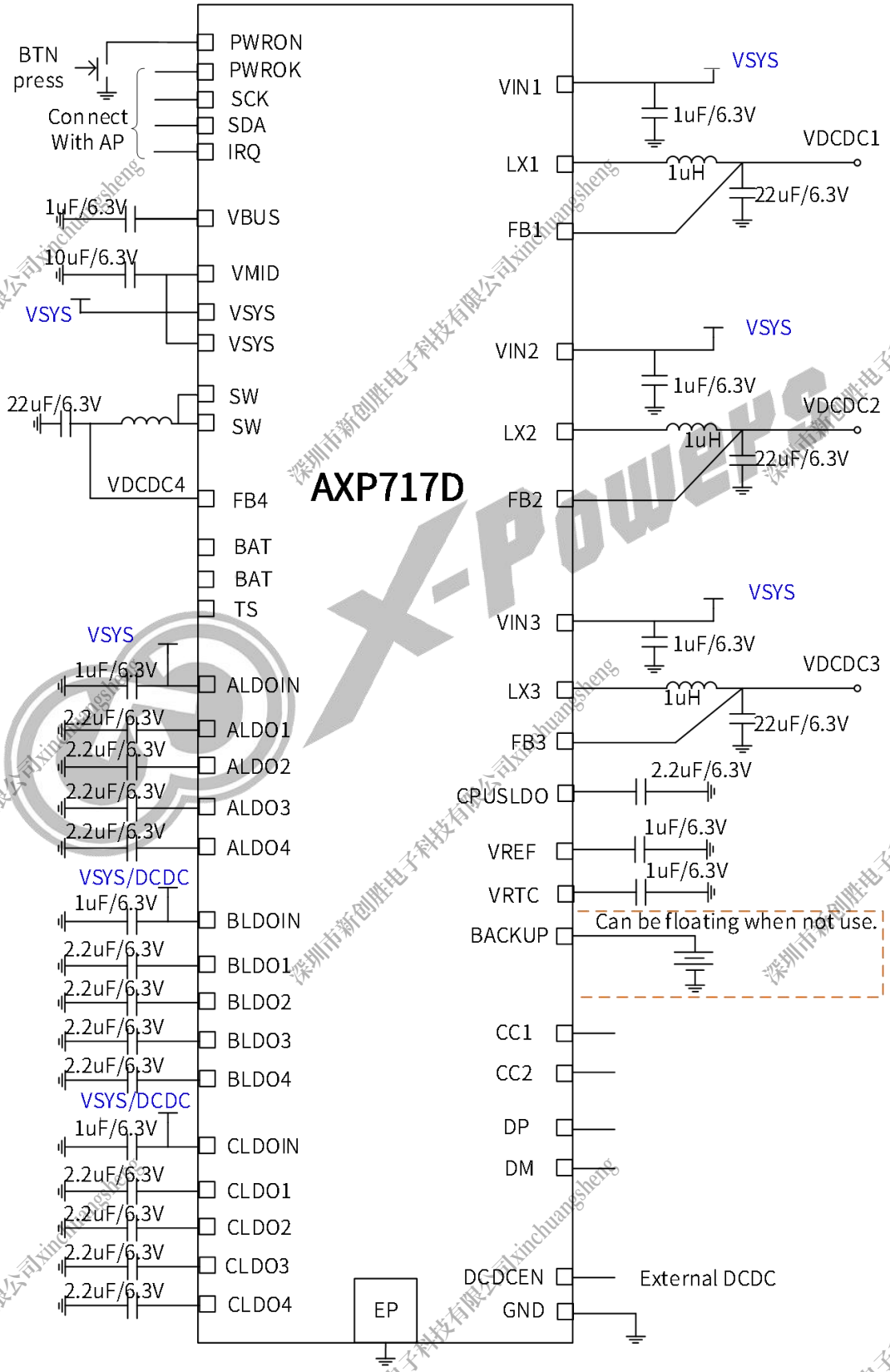
6.9.2.62 REG CF: adc_data_l

Bit	Description	R/W	Reset	Default
7:0	adc_data_l[7:0]	RO	POR	0

7 Application Information

7.1 Typical Application

Figure 7-1 Typical Application

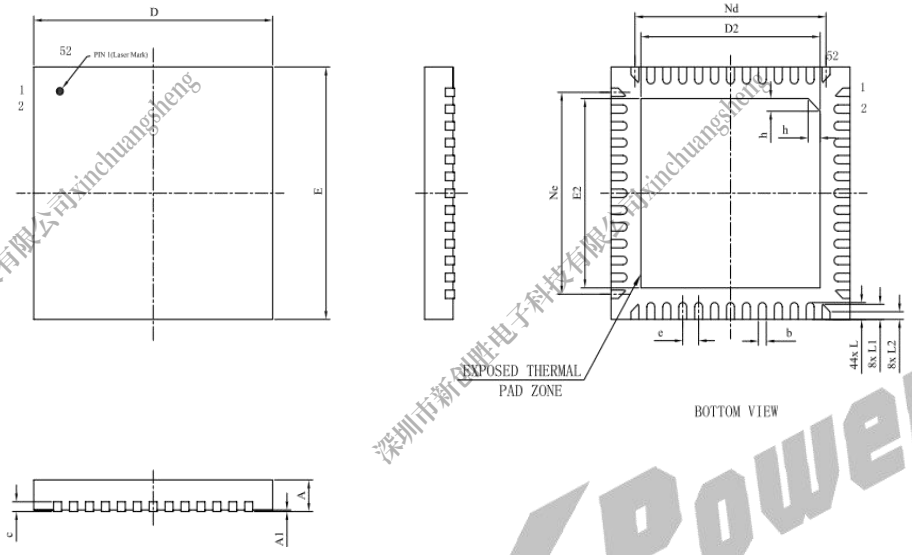


8 Package, Carrier, Storage and Baking Information

8.1 Package

AXP717D package is QFN6*6, 52-pin. Figure 8-1 shows AXP717D package.

Figure 8-1 Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.035	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	5.90	6.00	6.10
D2	4.40	4.50	4.60
e	0.40BSC		
Nd	4.80BSC		
E	5.90	6.00	6.10
E2	4.40	4.50	4.60
Ne	4.80BSC		
L	0.36	0.40	0.45
L1	0.31	0.36	0.41
L2	0.13	0.18	0.23
h	0.25	0.30	0.35
芯片数体尺寸 (mil)	185*185		

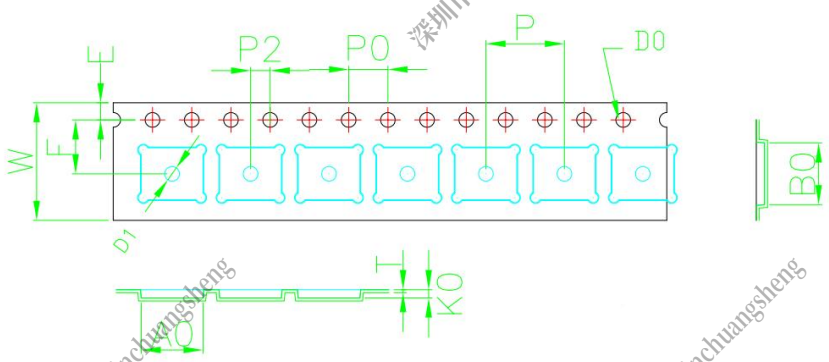
Figure 8-2 AXP717D Marking

Table 8-1 Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	AXP717D	Product name	Fixed
2	LLLLLLL	Lot number	Dynamic
3	XXXX	Date code	Dynamic
4		X-POWERS logo	Fixed
5	White dot	Package pin 1	Fixed

8.2 Carrier

Figure 8-3 AXP717D Tape Dimension Drawing



W	16.00±0.30	P	8.00±0.10	A0	6.30±0.10	B0	6.30±0.10
S	0.00±0.10	P0	4.00±0.10	A1		B1	
E	1.75±0.10	P2	2.00±0.10			B2	
F	7.50±0.10	D0	$\phi 1.50^{+0.10}_{0}$	K0	$0.85^{+0.10}_{-0.05}$	K1	
T	0.30±0.05	D1	$\phi 1.50^{+0.10}_{0.10}$				

Table 8-2 AXP717D Packing Quantity Information

Type	Quantity	Part Number
Tape	3000pcs/Tape	AXP717D

8.3 Storage

8.3.1 Moisture Sensitivity Level(MSL)

A package’ s MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factor floor longer than a high MSL device sample. ALL MSL are defined in the following table.

Table 8-3 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C/85%RH
2	1 year	≤30°C/60%RH
2a	4 weeks	≤30°C/60%RH
3	168 hours	≤30°C/60%RH
4	72 hours	≤30°C/60%RH
5	48 hours	≤30°C/60%RH
5a	24 hours	≤30°C/60%RH
6	Time on Label(TOL)	≤30°C/60%RH

AXP717D device samples are classified as MSL3.

8.3.2 Bagged Storage Conditions

The shelf life of AXP717D are defined in the following table.

Table 8-4 Bagged Storage Conditions

Packing mode	Vacuum packing
Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Shelf life	12 months

8.3.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration of AXP717D is as follows.

Table 8-5 Out-of-bag Duration

Storage temperature	20°C~26°C
Storage humidity	40%~60%RH
Moisture Sensitivity Level(MSL)	3
Floor life	168 hours

For no mention of storage rules in this document, please refer to the latest *IPC/JEDEC J-STD-020C*.

8.4 Baking

It is not necessary to bake AXP717D if the conditions specified in Section 8.3.2 and Section 8.3.3 have not been exceeded. It is necessary to bake AXP717D if any condition specified in Section 8.3.2 and Section 8.3.3 have been exceeded.

Table 8-6 Baking Conditions

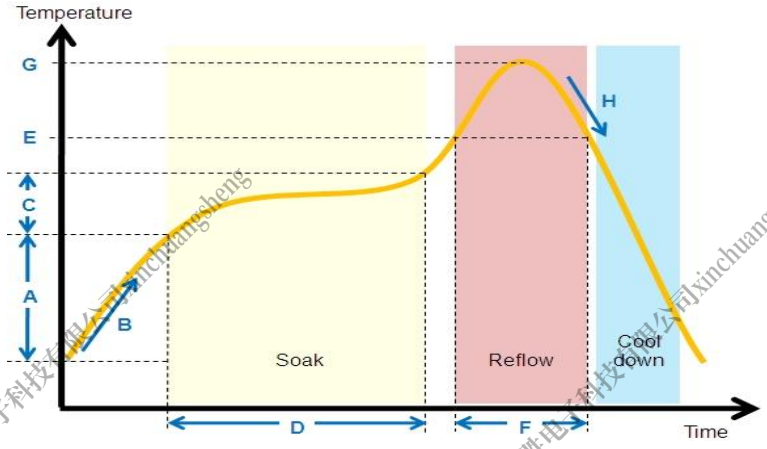
Surrounding	Condition	Note
Nitrogen	Tape: 60°C/72 hours, ≤5% RH	Bake no more than once.

9 Reflow Profile

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste.

The following figure shows the typical reflow profile of AXP717D device sample.

Figure 9-1 AXP717D Typical Reflow Profile



Reflow profile conditions of AXP717D device sample is given in the following table.

Table 9-1 AXP717D Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25°C -> 150°C
B	Preheat ramp up rate	1.5~2.5 °C /sec
C	Soak temperature range	150°C -> 190°C
D	Soak time	80~110 sec
E	Liquidus temperature	217°C
F	Time above liquidus	60-90 sec
G	Peak temperature	240-250°C
H	Cool down temperature rate	≤4°C /sec

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