3V-40V, Low I_Q, LDO with Watchdog and V_{BAT} Sense

1 Features

- Automotive AEC-Q100 Grade 1 Qualified
- Functional Safety Ready
  - Provide Functional Safety documentations to support system level functional safety design.
  - Internal Safety Mechanisms are ready to be used in safety applications.
- LDO Function
  - Wide Input Voltage Range: 3V to 40V
  - Fixed 3.3V/5V Output Voltage, ±2% Accuracy
  - Up to 300mA Output Current
  - Low Operation I_Q: 16µA
  - Low Shutdown I_{SHDN}: 1.5µA
  - High PSRR 60dB @ 100Hz
  - Accurate EN control
- Watchdog Function
  - Window Watchdog
  - Adjustable Watchdog Timer
- V_{BAT} Sense Function
  - V_{BAT} UVLO: Open Drain Output
  - V_{BAT} Sense: Analog Output to ADC
  - Dedicated BEN Pin to Minimize System I_Q
- Protection Function
  - V_{OUT} OV/UV Detection
  - Thermal Shutdown and Auto Restart
  - Over-Current Protection
- Device Operating: –40°C to + 150°C
- DFN12(3X3) Package with Wettable Flanks

2 Applications

- In-Vehicle Infotainment (IVI)
- Body Control Module (Body)
- ADAS
- Powertrain

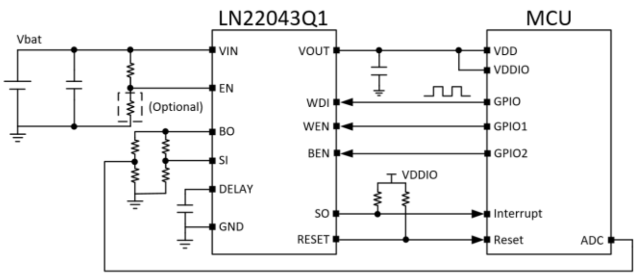
3 Description

LN22043Q1 is a low quiescent current watchdog LDO with a wide input voltage range of 3V to 40V. The series provides 3.3V, 5V fixed outputs and delivers up to 300mA output current. Typical shutdown current of LN22043Q1 is less than 1.5µA, while the quiescent current under no-load condition is 16µA.

Watchdog function can provide an independent monitor for microcontrollers. Window watchdog mode can monitor whether the frequency of watchdog service signal (WDI) is within a preset range. Different fault conditions of missing pulse in open window and receiving pulse in close window can both be reported on RESET pin. The duration of watchdog window can be set by delay capacitor.

LN22043Q1 provides a battery voltage sense function. By integrating an independent switch and a dedicated BEN pin, V_{BAT} sense function can be achieved by a minimum of peripheral circuit, without sacrificing system quiescent consumption.

LN22043Q1 also features power good indicator, over current protection and over temperature shutdown with auto restart. The product family are available in DFN12(3X3) package with wettable flanks.



Typical Application

Table of Contents

4 Version History

Version	Description	Date
1.0	Initial Version	2024/5/20

5 Order Information

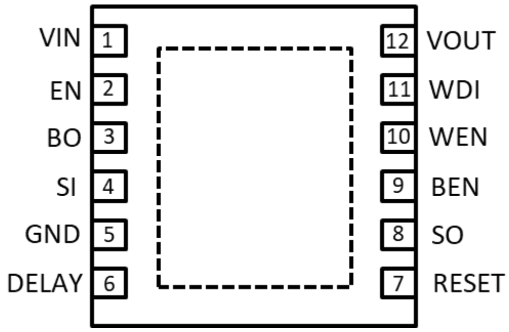
Part Number	V_{OUT}	Max Load	Watchdog	V_{BAT} Sense	PG	IC Package	MSL-Peak-Temp (1)	Material	Package Qty	Top Marking (2)
LN220433AQ1CHR	3.3V	300mA	Window	Yes	Yes	DFN12(3X3)	Level-2- 260C	RoHS	Tape & Reel 3000	20433A
LN220435AQ1CHR	5V	300mA	Window	Yes	Yes	DFN12(3X3)	Level-2- 260C	RoHS	Tape & Reel 3000	20435A

(1) MSL (Moisture Sensitivity Level) is based on JEDEC industrial classification and the tabled temperature is the maximum solder temperature.

(2) There may be additional marking related to the internal trace code on the device.

6 Pin Configuration and Function

6.1 Pin Configuration



6.2 Pin Function

Name	Number	Description
VIN	1	Input pin, place a ceramic capacitor of at least 1µF between VIN and GND.
EN	2	Enable pin, connect to a logic control signal or to VIN directly. This pin is pulled down to GND through internal resistor.
BO	3	Battery voltage analog output (controlled by BEN).
SI	4	Battery voltage sense input. SO is pulled down when V_{SI} falls below the sense-low threshold. If not used, connect to the BO pin.
GND	5	Connect to GND.
DELAY	6	Connected to an external delay capacitor. Set power good delay time and watchdog period.
RESET	7	V_{OUT} power good signal output and watchdog timeout reset signal output. Open drain, connect a pull-up resistor between RESET and an external power supply (1) or to VOUT pin, if not used, left this pin floating is recommended.
SO	8	Battery voltage sense output. Open drain, connect a pull-up resistor between SO and an external power supply (1) or to VOUT pin, if not used, left this pin floating is recommended.
BEN	9	V_{BAT} sense function enable. This pin is pulled down to GND through internal resistor.
WEN	10	Watchdog function enable. This pin is pulled down to GND through internal resistor.
WDI	11	Watchdog signal input.
VOUT	12	Output pin, place a ceramic capacitor of at least 0.47µF between VOUT and GND.

(1) The external power supply voltage should not exceed V_{OUT}.

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

Parameters	Min	Max	Unit
V_{IN}	-0.3	42	V
V_{EN} / V_{SI} / V_{BO}	-0.3	V_{IN}	
V_{RESET} / V_{WEN} / V_{WDI} / V_{BEN} / V_{SO}	-0.3	6.5	
V_{OUT}	-0.3	6.5	
V_{DELAY}	-0.3	6.5	
Operating Junction Temperature	-40	150	˚C
Operating Ambient Temperature	-40	125	
Storage Temperature	-55	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

Parameters			Value	Unit
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011, corner pins	±750	
		Charged-device model (CDM), per AEC Q100-011, other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Condition

Over operating free-air temperature range (unless otherwise noted)

Parameters		Min	Nom	Max	Unit
V_{IN}	Input voltage	3		40	V
V_{OUT}	Output voltage		3.3/5		
V_{EN} / V_{SI} / V_{BO}	EN/SI/BO voltage	0		V_{IN}	
V_{WEN} / V_{WDI} / V_{BEN}	WEN/WDI/BEN voltage	0		5.5	
V_{RESET} / V_{SO}	RESET/SO voltage	0		V_{OUT}	
I_{OUT}	Output current	0		300	mA
C_{IN}	Input capacitor	1			uF
C_{OUT}	Output capacitor(1)	0.47		200	
T_A	Operating Ambient Temperature	-40		125	˚C
T_J	Operating Junction Temperature	-40		150	

(1) Consider the decrease of voltage and temperature, minimum effective capacitance of 0.47µF is required for stability.

7.4 Package Thermal Parameters

Parameter		DFN12(3X3)	Unit
$R_{\Theta ja}$ (1)	Junction-to-ambient thermal resistance	43	°C/W
ψ_{JT} (1)	Junction-to-top characterization parameter	3	°C/W
$R_{\Theta ja\text{-}EVM}$	Junction-to-ambient thermal resistance on LENEVM	26	°C/W

(1) Measurements are based on standard 2s2p PCB defined in JESD 51-7 2s2p, under no wind, 2W loss, and 25˚C ambient temperature.

7.5 Electrical Characteristics

Unless otherwise stated, the minimum and maximum limits apply over the recommended operating junction temperature range of -40˚C to 150˚C. Typical values are measured at 25˚C and represent the most likely norm. The default conditions apply: VIN = 13.5V.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VIN, VOUT (VIN, VOUT, GND PINS)						
V_{IN}	Operating Input Voltage Range		3		40	V
I_{OUT}	Output current	V_{OUT} in regulation	0		300	mA
I_{SHDN}	Input Shutdown Current	V_{EN} = 0V		1.5	4.3	µA
I_Q	Input Quiescent Current (Only LDO)	V_{EN} = 5V, I_{OUT} = 0A, measured on GND pin.		16	32	µA
	Input Quiescent Current with WD Function	V_{EN} = 5V, I_{OUT} = 0A, V_{WEN} = 5V, measured on GND pin.		22	40	µA
	Input Quiescent Current with V_{BAT} Function	V_{EN} = 5V, I_{OUT} = 0A, V_{SI} = 5V, V_{BEN}=5V, measured on GND pin.		18	34	µA
	Input Quiescent Current with WD Function and V_{BAT} Function	V_{EN} = 5V, I_{OUT} = 0A, V_{SI} = 5V, V_{WEN} = 5V, V_{BEN} = 5V, measured on GND pin.		24	42	µA
REGULATION (VOUT PIN)						
V_{OUT}%	Regulated Output Voltage Error for Fixed V_{OUT} Parts	40V > V_{IN} > V_{OUT} + 1V, I_{OUTMAX} > I_{OUT} > 1mA	-2		2	%
	Line Regulation	40V > V_{IN} > V_{OUT} + 1V, I_{OUT} = 10 mA		±0.1		%
	Load Regulation	V_{IN} = 13.5V, I_{OUTMAX} > I_{OUT} > 1mA		±0.5		%
DROP OUT						
V_{DO-5V}	Drop Out Voltage @ 300mA	I_{OUT} = 300mA, V_{IN} = 5.1V, $V_{OUT-NOM}$ = 5V		300	550	mV
$V_{DO-3.3V}$	Drop Out Voltage @ 300mA	I_{OUT} = 300mA, V_{IN} = 3.4V, $V_{OUT-NOM}$ = 3.3V		430	750	mV
OVER CURRENT PROTECTION						
I_{LIMIT}	Current Limit Threshold	V_{IN} = 6V to 40V, V_{OUT} = 90%*$V_{OUT-NOM}$	301	430	650	mA

Electrical Characteristics (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY REJECTION RATIO (PSRR)						
$G_{PSRR-100Hz}$	PSRR@100Hz	I_{OUT} = 50mA, V_{OUT} = 5V or 3.3V		60 (1)		dB
$G_{PSRR-1kHz}$	PSRR@1kHz	I_{OUT} = 50mA, V_{OUT} = 5V or 3.3V		50 (1)		dB
$G_{PSRR-100kHz}$	PSRR@100kHz	I_{OUT} = 50mA, V_{OUT} = 5V or 3.3V		30 (1)		dB
ENABLE (EN PIN)						
V_{EN-H}	EN Enable Threshold Voltage		1.352	1.47	1.588	V
V_{EN-L}	EN Disable Threshold Voltage		1.187	1.237	1.287	V
I_{EN-H}	EN Leakage Current	V_{EN} = 5V		1	2	µA
THERMAL SHUTDOWN						
T_{SD}	Thermal Shutdown Threshold		151	164 (1)		˚C
T_{SD-HYS}	Thermal Shutdown Recovery Hysteresis			16 (1)		˚C
V_{BAT} SENSE						
V_{SI-H}	V_{BAT} Under-Voltage Reference Voltage Rising		1.181	1.237	1.293	V
V_{SI-L}	V_{BAT} Under-Voltage Reference Voltage Falling		1.067	1.1	1.133	V
I_{SI}	SI Leakage Current	V_{SI} = 5V	-150		150	nA
V_{BEN-H}	V_{BAT} Sense Enable High-Level Voltage		2			V
V_{BEN-L}	V_{BAT} Sense Enable Low-Level Voltage				0.7	V
I_{BEN-H}	BEN Leakage Current	V_{BEN} = 5V		1	2	µA
R_{BO}	BO MOSFET On Resistance	V_{BEN} = 5V, V_{EN} = 5V		125	260	Ω
R_{BO-DN}	BO Pull-Down Resistor When Disabled	V_{BEN} = 0V, V_{BO} = 1V, V_{EN} = 5V or 0V		40	64	kΩ
R_{SO-DN}	SO Internal Pull-Down Resistance When Battery Detected	V_{EN} = 5V, V_{SO} = 1V		170	220	Ω
		V_{EN} = 0V, V_{SO} = 1V		203	260	Ω
$t_{SO-RISING}$	V_{BAT} Sense Delay time			5		µs
$t_{SO-FALLING}$	V_{BAT} Sense Deglitch time			2.5		µs

Electrical Characteristics (Continued)

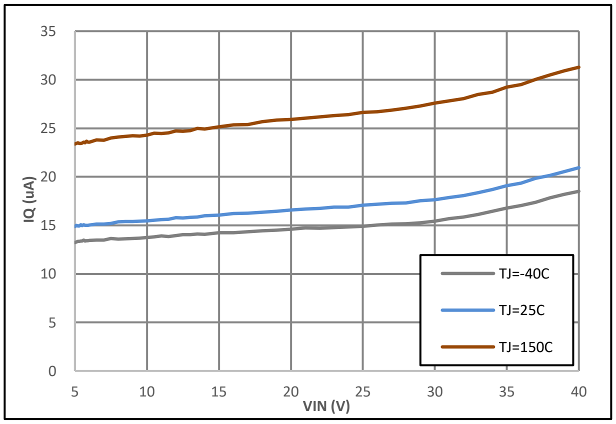
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
WATCHDOG						
$I_{CS\text{-}CHG}$	Delay Capacitor WD Charge Current	Measured on delay pin.	3.1	4.4	6.2	µA
$I_{CS\text{-}DHG}$	Delay Capacitor WD Discharge Current	Measured on delay pin.	30	46	68	µA
V_{DH}	DELAY Pin High Threshold Under WD Monitor	Measured on delay pin.		1.237		V
V_{DL}	DELAY Pin Low Threshold Under WD Monitor	Measured on delay pin.		0.35		V
$V_{D\text{-}HYS}$	DELAY Pin Threshold Hysteresis Under WD Monitor	Measured on delay pin.	0.8	0.887	0.95	V
$V_{WD\text{-}H}$	WDI/WEN High-Level Voltage		2			V
$V_{WD\text{-}L}$	WDI/WEN Low-Level Voltage				0.7	V
I_{WD}	WDI/WEN input current	WDI/WEN = 5V		1	2	µA
t_{WDI}	Minimum WDI Pulse	Both WDI High and Low pulses	5			µs
POWER GOOD						
$\%V_{UV\text{-}RISE}$	UV Rising Threshold	V_{OUT} Ramping Up	80	88	96	%
$\%V_{UV\text{-}FALL}$	UV Falling Threshold	V_{OUT} Ramping Down	77	85	93	%
$\%V_{OV\text{-}RISE}$	OV Rising Threshold		104	107	110	%
$\%V_{OV\text{-}FALL}$	OV Falling Threshold		102	105	108	%
$I_{CS\text{-}ST}$	Delay Capacitor PG Charge Current	Measured on delay pin.	28	42	62	µA
$V_{D\text{-}CLAMP}$	Delay Voltage Clamping Threshold			4.7		V
$R_{RESET\text{-}DN}$	RESET Internal Pull-Down Resistance When Fault Happened	EN = 5V, V_{RESET} = 1V		170	220	Ω
		EN = 0V, V_{RESET} = 1V		203	260	Ω

(1) Not subject to production test, specified by design.

7.6 Typical Characteristics

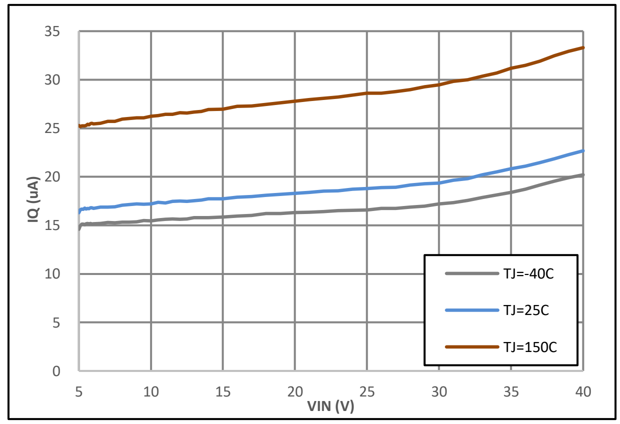
7.6.1 Characteristics Over Temperature

Unless otherwise stated, the test conditions are the same as Chapter 7.5. T_A = 25˚C.



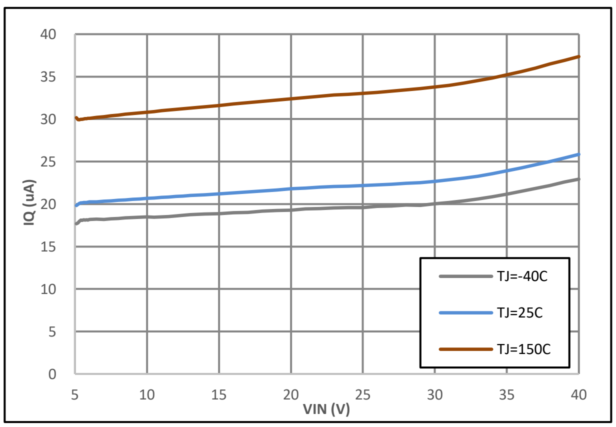
LN220435AQ1, V_{EN}=5V, Fixed V_{OUT} = 5V, No load

Figure 1. I_{GND} (Only LDO)



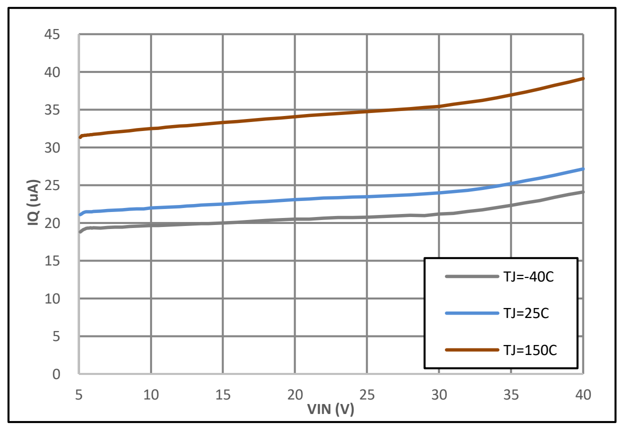
LN220435AQ1, V_{EN}=5V, Fixed V_{OUT} = 5V, No load

Figure 2. I_{GND} (with V_{BAT} Sense Function)



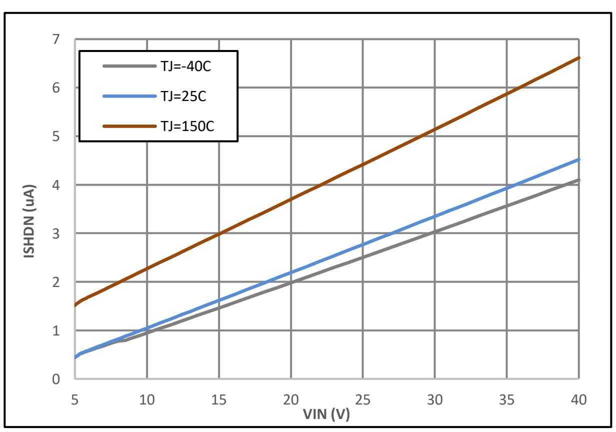
LN220435AQ1, V_{EN}=5V, Fixed V_{OUT} = 5V, No load

Figure 3. I_{GND} (with Watchdog Function)



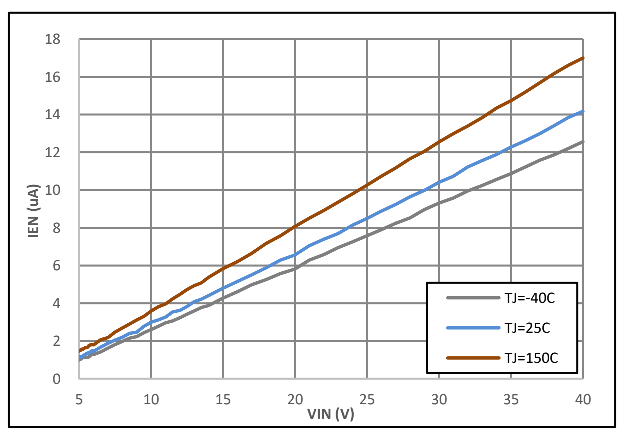
LN220435AQ1, V_{EN}=5V, Fixed V_{OUT} = 5V, No load

Figure 4. I_{GND} (with Full Function)



LN220435AQ1, Fixed V_{OUT} = 5V, No load

Figure 5. I_{SHDN}

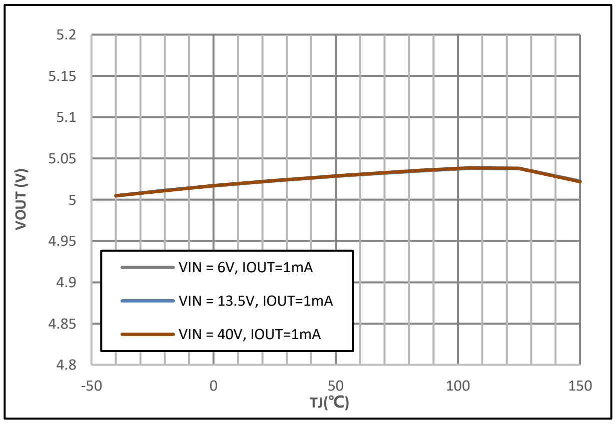


LN220435AQ1, Fixed V_{OUT} = 5V, No load

Figure 6. I_{EN}

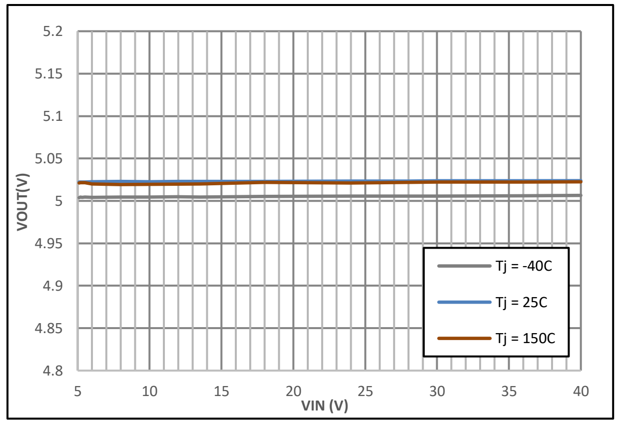
Characteristics Over Temperature (Continued)

Unless otherwise stated, the test conditions are the same as Chapter 7.5. T_A = 25˚C.



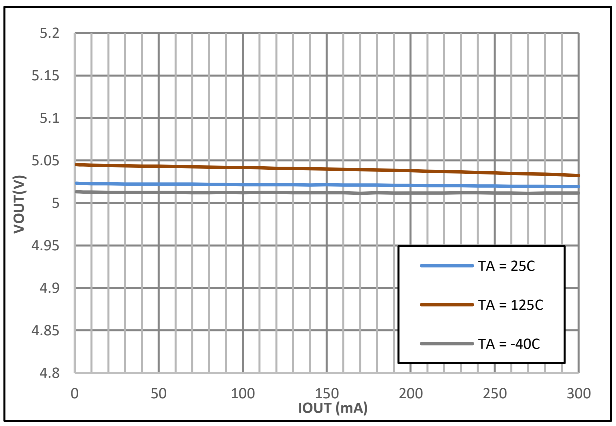
LN220435AQ1, Fixed V_{OUT} = 5V

Figure 7. V_{OUT} vs. Temperature



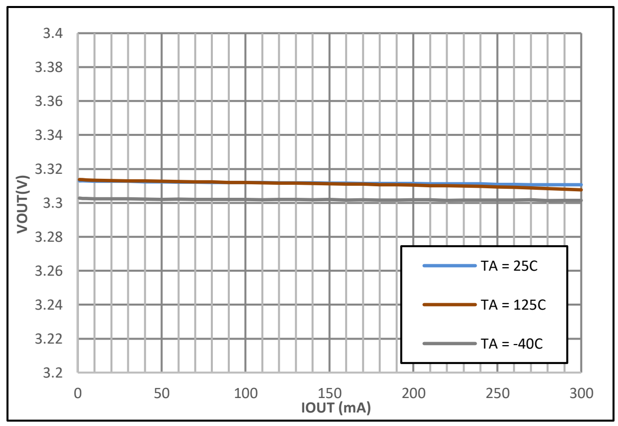
LN220435AQ1, Fixed V_{OUT} = 5V, I_{OUT} = 10mA

Figure 8. Line Regulation



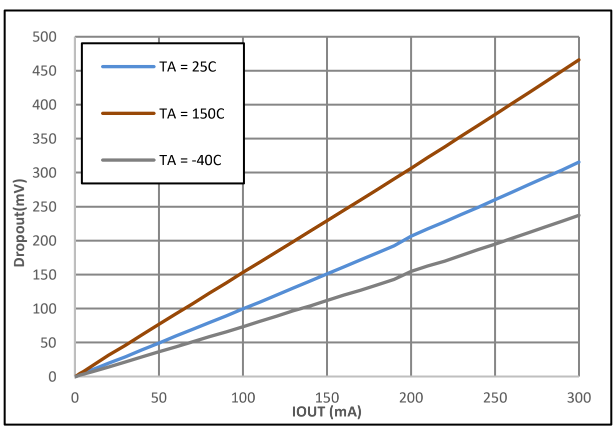
LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 6V

Figure 9. Load Regulation



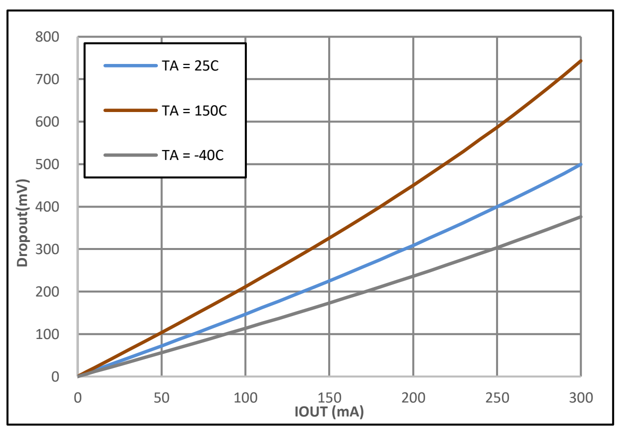
LN220433AQ1, Fixed V_{OUT} = 3.3V, V_{IN} = 4V

Figure 10. Load Regulation



LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 4.75V

Figure 11. Dropout

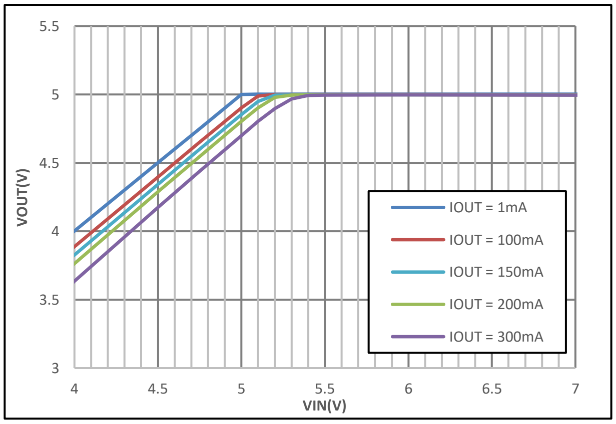


LN220433AQ1, Fixed V_{OUT} = 3.3V, V_{IN} = 3.2V

Figure 12. Dropout

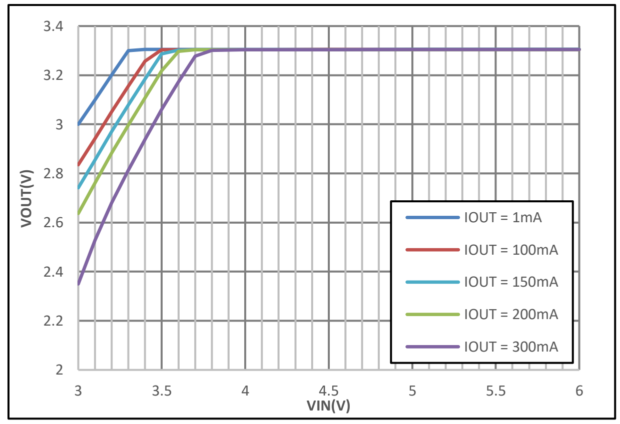
Characteristics Over Temperature (Continued)

Unless otherwise stated, the test conditions are the same as Chapter 7.5. T_A = 25˚C.



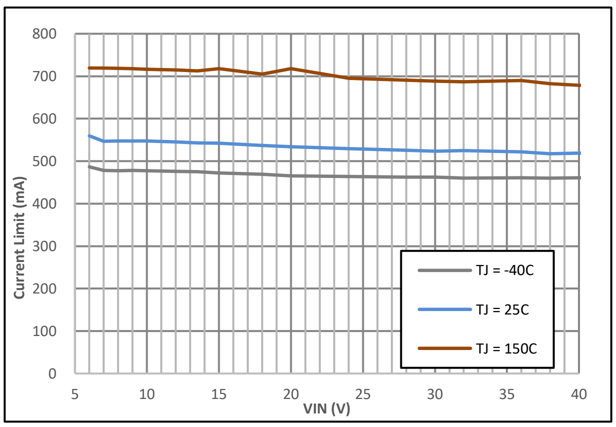
LN220435AQ1, Fixed V_{OUT} = 5V

Figure 13. Dropout



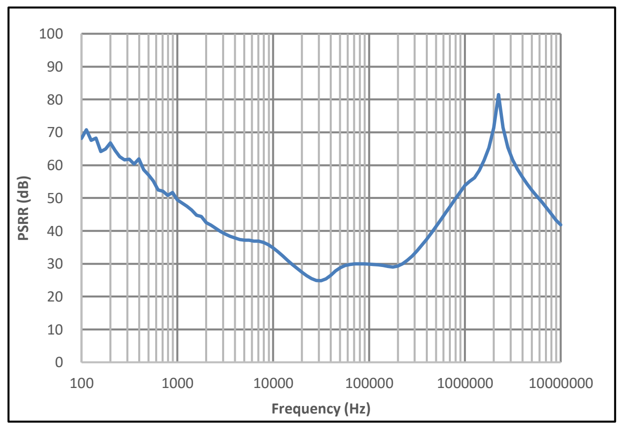
LN220433AQ1, Fixed V_{OUT} = 3.3V

Figure 14. Dropout



LN220435AQ1, Fixed V_{OUT} = 5V, Measured at V_{OUT} short

Figure 15. Current Limit vs. V_{IN}

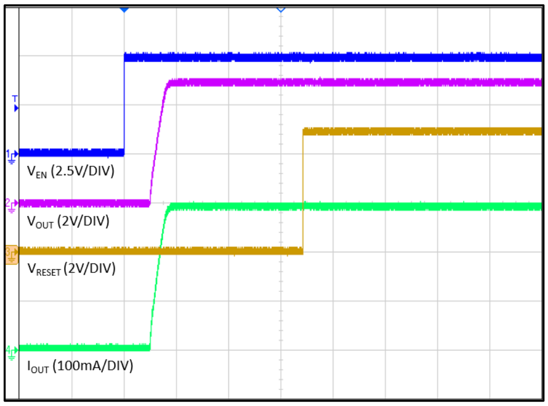


LN220435AQ1, Fixed V_{OUT} = 5V, C_{IN} = 100pF, V_{IN} = 13.5V, I_{OUT} = 50mA

Figure 16. PSRR

7.6.2 Typical Waveforms

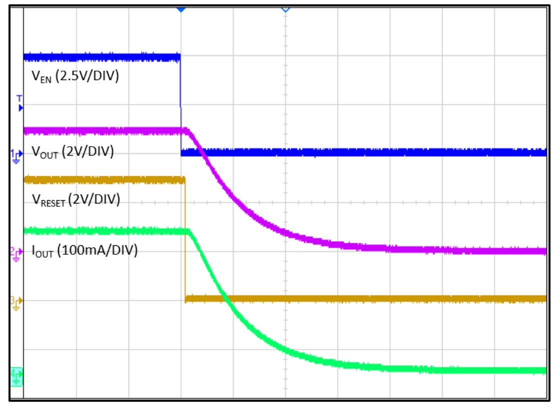
Unless otherwise stated, the test conditions are the same as Chapter 7.5. $C_{IN} = C_{OUT} = 1\mu F$, $T_A = 25^{\circ}C$.



Time (1ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 16.6Ohm, C_{Delay} = 0.1µF

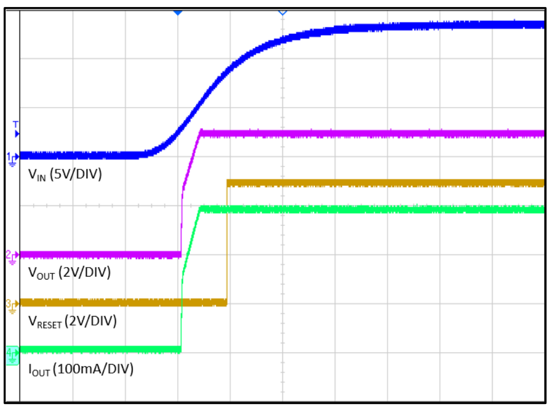
Figure 17. Startup with EN



Time (20µs/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 16.6Ohm, C_{Delay} = 0.1µF

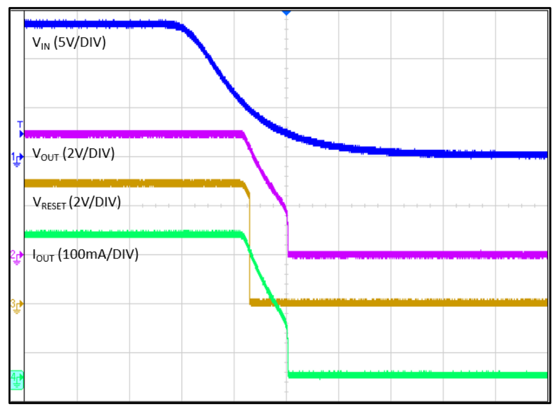
Figure 18. Shutdown with EN



Time (5ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 16.6Ohm, C_{Delay} = 0.1µF

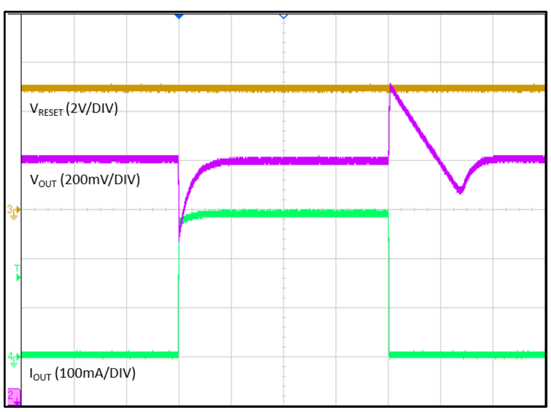
Figure 19. Startup with V_{IN}



Time (5ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, R_{LOAD} = 16.6Ohm, C_{Delay} = 0.1µF

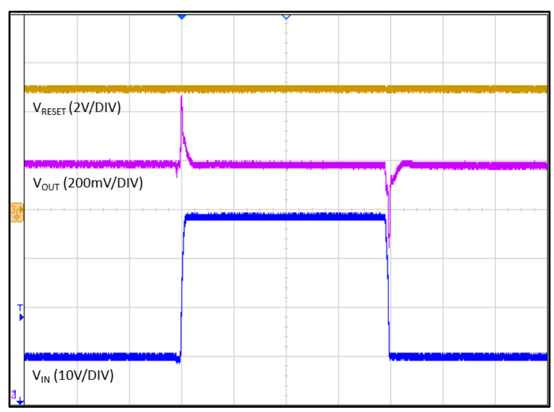
Figure 20. Shutdown with V_{IN}



Time (200µs/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, Slew Rate↑↓ = 0.1A/µs

Figure 21. Load Transient 1 <-> 300mA



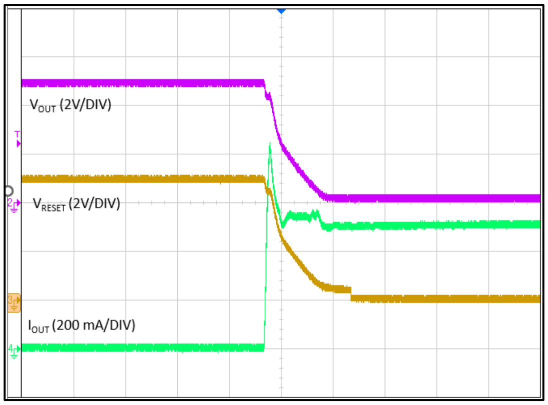
Time (500µs/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, I_{OUT} = 200mA, Slew Rate↑↓ = 1V/µs

Figure 22. Line Transient 13.5 <-> 40V

Typical Waveforms (Continued)

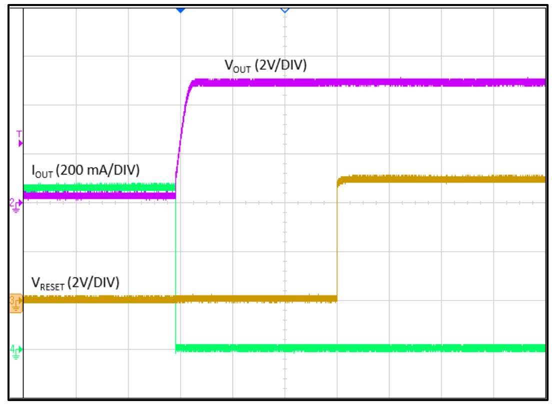
Unless otherwise stated, the test conditions are the same as Chapter 7.5. C_{IN} = C_{OUT} = 1μF, T_A = 25˚C.



Time (200μs/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V

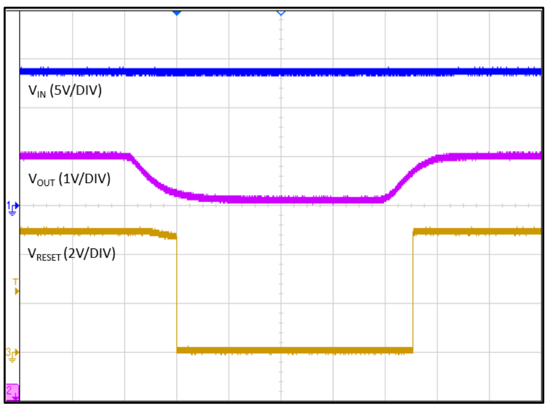
Figure 23. Short Circuit Entry



Time (1ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, C_{DELAY} = 0.1μF

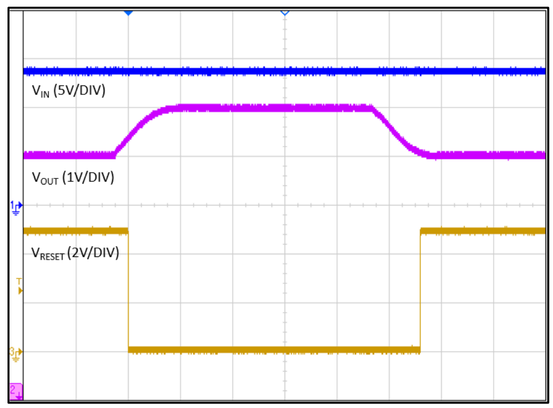
Figure 24. Short Circuit Recovery



Time (10ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, V_{OUT} = 5V <-> 4V

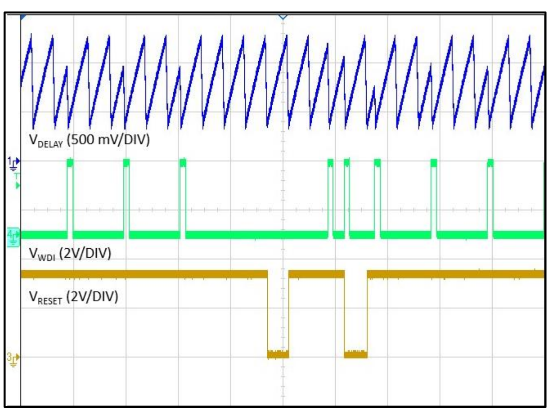
Figure 25. V_{OUT} UV



Time (10ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V, V_{OUT} = 5V <-> 6V

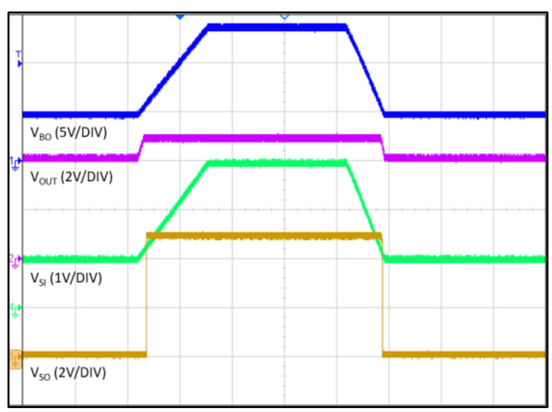
Figure 26. V_{OUT} OV



Time (45ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 13.5V

Figure 27. Watchdog



Time (45ms/DIV)

LN220435AQ1, Fixed V_{OUT} = 5V, V_{IN} = 4.5V <->13.5V

Figure 28. V_{BAT} Sense

8 Functional Description

8.1 Overview

LN22043Q1 is a low quiescent current, low dropout linear regulator (LDO) with a wide input voltage range of 3V to 40V. The series provides fixed 3.3V or 5V outputs and delivers up to 300mA output current. Typical shutdown current of LN22043Q1 is less than 1.5µA, while the quiescent current under no-load condition is 16µA.

Watchdog function can provide an independent monitor for microcontrollers. Window watchdog mode can monitor whether the frequency of watchdog service signal (WDI) is within a preset range. Different fault conditions of missing pulse in open window and receiving pulse in close window can both be reported on RESET pin. The duration of watchdog window can be set by delay capacitor.

LN22043Q1 provides a battery voltage sense function. By integrating an independent switch and a dedicated BEN pin, V_{BAT} sense function can be achieved by a simple peripheral circuit, without sacrificing system quiescent consumption.

LN22043Q1 also features power good indicator, over current protection and over temperature shutdown with auto restart.

The product family are available in DFN12(3X3) package with wettable flanks.

8.2 Funtional Dragram

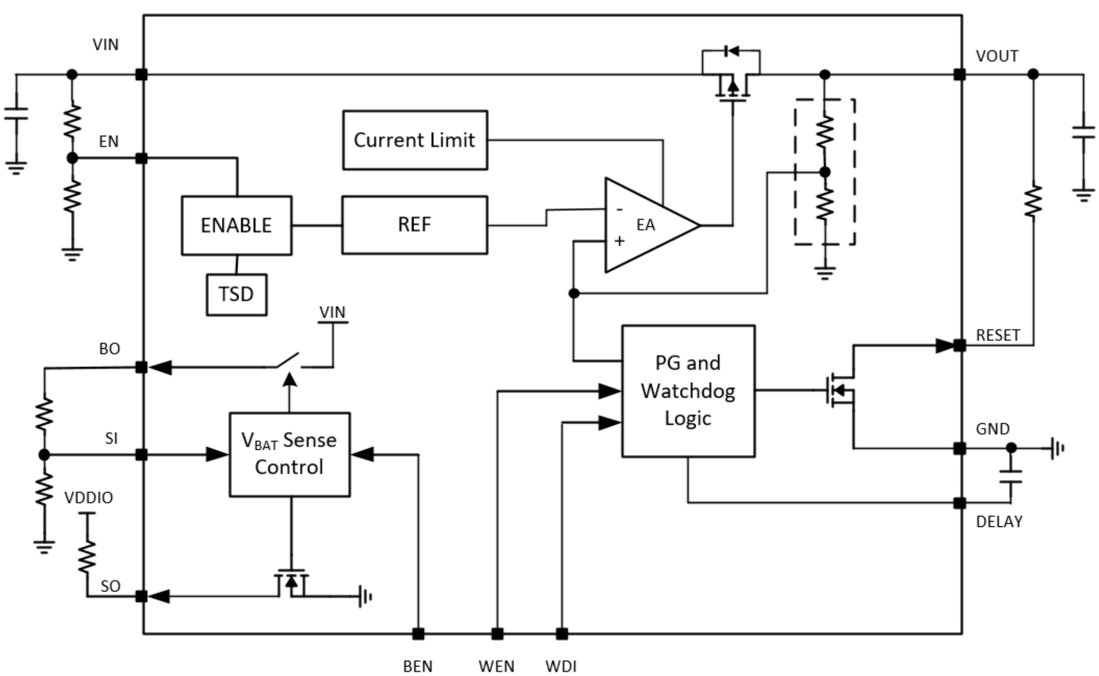


Figure 29. LN22043Q1 Functional Diagram

8.3 Funtional Description

8.3.1 Vbat Sense Function

LN22043Q1 provides a battery voltage sense function. By integrating an independent switch and a dedicated BEN pin, V_{BAT} sense function can be achieved by a simple peripheral circuit, without sacrificing system quiescent consumption.

Only one or two pairs of resistor divider is needed to implement battery voltage sense, working procedures are described as follows, and schematic is shown in figure 30.

1) When BEN is enabled, BO pin is pullup to VIN though an internal switch.
2) V_{BAT} can be sensed by connecting a voltage divider between BO and GND and connect the center of the divider to SI pin. When the SI voltage drops below threshold V_{SI-L}, battery under-voltage is reported, and the SO will be pulled low. The use of external voltage divider makes this function very flexible in the applications.
   V_{IN} rising threshold:
   $$V_{IN-R} = \left(1 + \frac{R_{SIT}}{R_{SIB}}\right) \times V_{SI-H} \quad (1)$$
   V_{IN} falling threshold:
   $$V_{IN-F} = \left(1 + \frac{R_{SIT}}{R_{SIB}}\right) \times V_{SI-L} \quad (2)$$
3) Another pair of voltage divider can also be connected to BO pin and the divided signal can be connected an ADC of MCU for precise analog sensing.
4) Extreme low system IQ can be achieved by turning off BO pin through BEN.

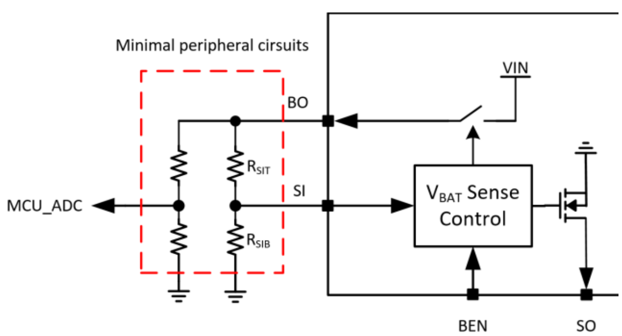


Figure 30. V_{BAT} Sense Function

The typical timing for SI comparator is shown in figure 31.

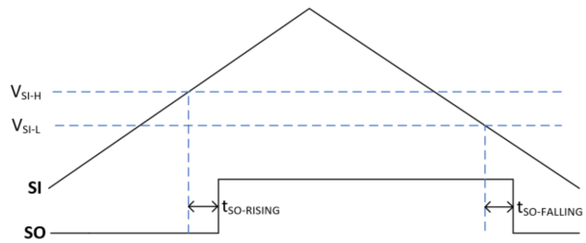


Figure 31. SI Timing

8.3.2 Watchdog Function

8.3.2.1 Function Description

Independent watchdog is a basic requirement in most reliable systems, which can provide an independent monitor circuit for microcontrollers, and reset MCU when software runaway. Window watchdog integrated in LN22043Q1 can monitor whether the frequency of watchdog service signal (WDI) is within a preset range.

In window watchdog mode, there is a close window and an open window, WDI signal must be served in the open window; Missing pulse in open window and receiving pulse in close window can both trigger fault window and be reported on RESET pin. The duration of watchdog window can be set by delay capacitor.

The operation of window watchdog is descripted as follow, and the timing diagram of watchdog is shown in Figure 32.

1) When watchdog function is enabled through WEN pin, voltage on DELAY pin is discharged from $V_{D-CLAMP}$ to V_{DL}, it enters open window status, and then DELAY pin begins to charge and discharge.
2) When WDI pin detects a trigger in open window, it switches to close window immediately, and then a complete cycle of charge and discharge procedure is implemented on DELAY pin, the voltage goes from V_{DL} to V_{DH} and then back to V_{DL}. During the close window, WDI must keep quiet.
3) After the closed window, the watchdog will come back to the open window status again and wait for the next WDI signal. When the next WDI signal comes, it will go back to step 2), and the procedure repeats.
4) Two types of faults can be reported during above procedure:
   Fault 1: The WDI signal is not received during the open window; watchdog turns to fault window after open window complete and reports low signal on RESET pin, the time duration of RESET low voltage equals one complete cycle to make sure MCU is properly reset. After the fault window, watchdog will go back to open window and repeat step 2).
   Fault 2: The WDI signal is received during the close window, it enters fault window immediately, the voltage on the DELAY pin is discharged to V_{DL} first and then followed by a complete cycle of charge and discharge procedure. The time duration of RESET low voltage may be a little longer than one complete cycle depends on the WDI signal position. After the fault window, watchdog will go back to open window and repeat step 2).
5) After watchdog function is disabled, voltage on DELAY pin is charged to $V_{D-CLAMP}$ and RESET will not be pulled low due to failed WDI signal.

8.3.2.2 Watchdog timing

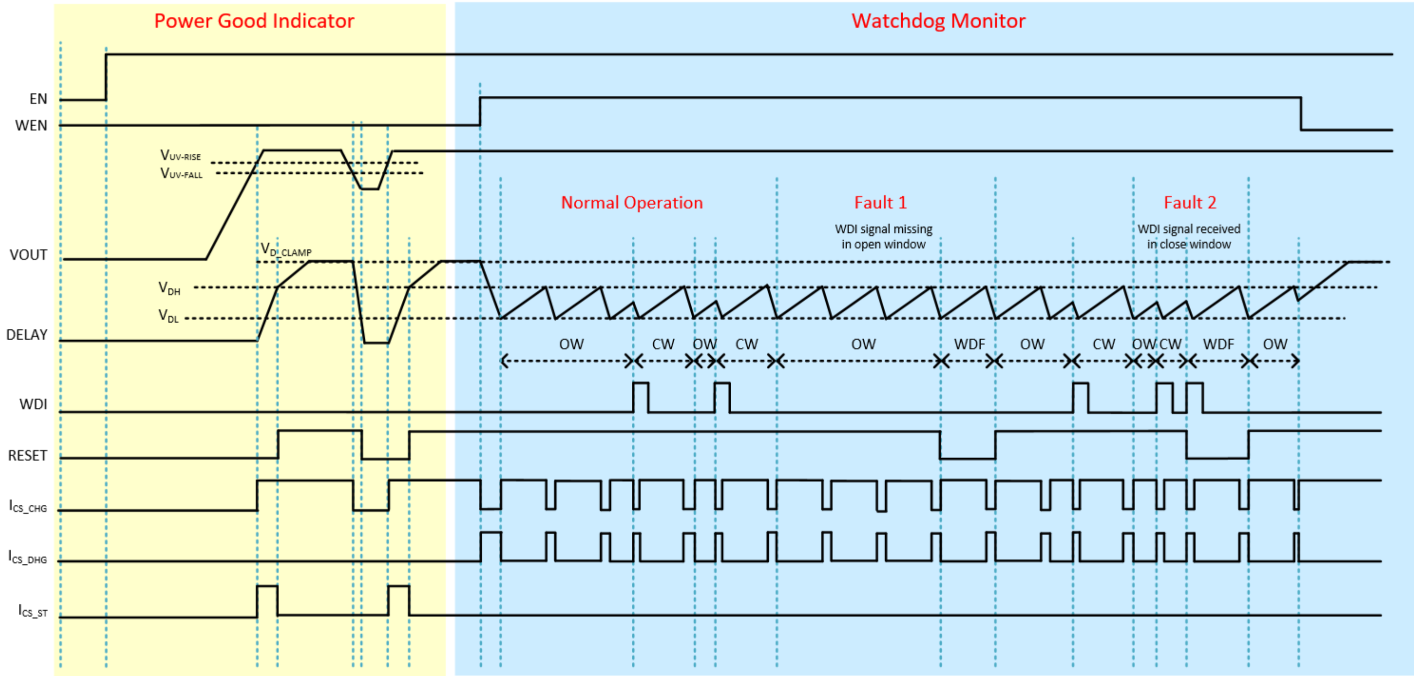


Figure 32. Window Watchdog

8.3.2.3 Calculation of Timing

The duration of the watchdog window can be programmed by connecting an external capacitor to ground at the DELAY pin. Voltage on the DELAY pin will be charged and discharged repeatedly between V_{DH} and V_{DL}. Close window lasts for about one charging and discharging cycle, while open window is three cycles, so the ratio between open window and closed window duration is fixed as 3:1. Different capacitance will influence the charging and discharging time, and then determine the watchdog period.

The voltage difference between V_{DH} and V_{DL} is defined as V_{D-HYS}.

$$V_{D-HYS} = V_{DH} - V_{DL} \tag{3}$$

Open window lasts for 3 charging and discharging cycles, so the duration is:

$$t_{OW} = 3 \times V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}}\right) \tag{4}$$

Close window duration maybe a little different depends on the WDI signal position. If WDI signal occurs when the DELAY pin volage is V_{DL}, then the close window duration is one complete charging and discharging period, the minimum close window duration is:

$$t_{CW-MIN} = V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}}\right) \tag{5}$$

While if the WDI occurs when the DELAY pin volage is at V_{DH}, then the close window should go through a discharging time first, and then followed by another charging and discharging period. So, the maximum close window duration is:

$$t_{CW-MAX} = V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}} + \frac{1}{I_{CS-DHG}}\right) \quad (6)$$

After WDI signal is effectively triggered, to avoid a watchdog fault, the next WDI signal must come after the maximum close window, and before the open window time out, so the period of the WDI signal should be in below range.

$$t_{CW-MAX} < t_{WDI} < t_{OW} + t_{CW-MIN} \quad (7)$$

Taking the spec variation of the device and capacitor into consideration, the recommended WDI signal period can be set as two complete charge and discharge cycles, then the watchdog WDI signal period and frequency are calculated as below:

$$t_{WDI-NOM} = 2 \times V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}}\right) \quad (8)$$

$$f_{WDI-NOM} = \frac{1}{t_{WDI-NOM}} = \frac{1}{2 \times V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}}\right)} \quad (9)$$

If something is wrong with the MCU, and WDI comes within the close window or after the open window, the watchdog fault is triggered, RESET pin will be pulled to low. Depends on when the fault happens, the fault window duration is a little different which is similar to the close window calculation method.

$$t_{WDF-MAX} = V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}} + \frac{1}{I_{CS-DHG}}\right) \quad (10)$$

$$t_{WDF-MIN} = V_{D-HYS} \times C_{delay} \times \left(\frac{1}{I_{CS-CHG}} + \frac{1}{I_{CS-DHG}}\right) \quad (11)$$

8.3.3 V_{OUT} UV and OV Monitor Function

The RESET pin is open drain output, so the RESET pin needs to be pulled up to a voltage source by a resistor externally. When V_{OUT} is not in the desired range, RESET pin outputs low voltage to reset MCU.

When EN is high and V_{OUT} rises above the power good threshold $V_{UV-RISE}$, to make sure that MCU is properly reset, the RESET pin isn't pulled up directly. Instead, the DELAY pin starts to output a current (I_{CS-CHG}+ I_{CS-ST}) to charge the external delay capacitor, only after the voltage on the DELAY pin rises across V_{DH}, RESET is pulled up.

The external delay capacitor is selected based on the desired MCU delay time t_{Delay} and is calculated based on:

$$\mathrm{C_{Delay}} = \frac{(I_{CS-CHG} + I_{CS-ST}) \times \mathrm{t_{Delay}}}{\mathrm{V_{DH}}} \quad (12)$$

When EN is high but V_{OUT} is below the power good threshold $V_{UV-FALL}$, the DELAY pin will discharge the voltage of delay capacitor within microsecond level through an internal resistor, and after the voltage on the DELAY pin is below V_{DL}, RESET is pulled down.

LN22043Q1 also integrates an over voltage monitor function. When V_{OUT} rises above the threshold $V_{OV\text{-}RISE}$, the DELAY pin also will quickly discharge the DELAY pin to V_{DL} and then RESET is pulled down. When the OV state disappears, the DELAY pin will be recharged to V_{DH} and then the RESET pin will be released again.

8.3.4 Output capacitor stable region

LN22043Q1 can operate stably in the wide range of 0.47uF to 200uF and 0Ω to100Ω of equivalent resistance (ESR).

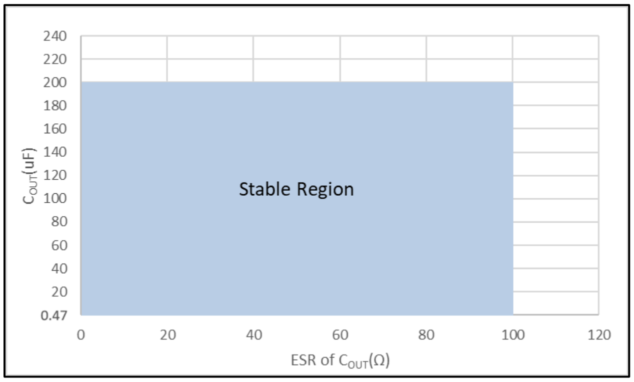


Figure 33. Stable Region

8.3.5 Accurate EN control

An accurate threshold is placed at $V_{EN\text{-}H}$, when EN voltage rises above this threshold, it turns on the LDO. This accurate threshold serves to provide an accurate system V_{IN} UVLO level. In the application, an enable divider can be added between VIN and GND. The LDO can thus be turned on and off at programmable precise input voltages. The V_{IN} UVLO threshold can be determined by:

$$V_{IN-Rising} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times V_{EN-H} \quad (13)$$

$$V_{IN-Falling} = \left(1 + \frac{R_{ENT}}{R_{ENB}}\right) \times V_{EN-L} \quad (14)$$

8.3.6 Over-Current Protection

LN22043Q1 features over-current protection to keep the device in a safe operating area when the circuit overload or output short to ground. When the over-current protection is triggered, the device output current is clamped to the current limit.

8.3.7 Thermal Shutdown and Auto-Recovery

LN22043Q1 features thermal shutdown and auto-recovery as a protection from over-heating. When the junction temperature exceeds 164˚C, the device turns off the output to reduce thermal dissipation. It automatically restarts the output after junction temperature drops back below 148 ˚C.

9 Typical Applications

9.1 Applicaition Diagram with Full Features

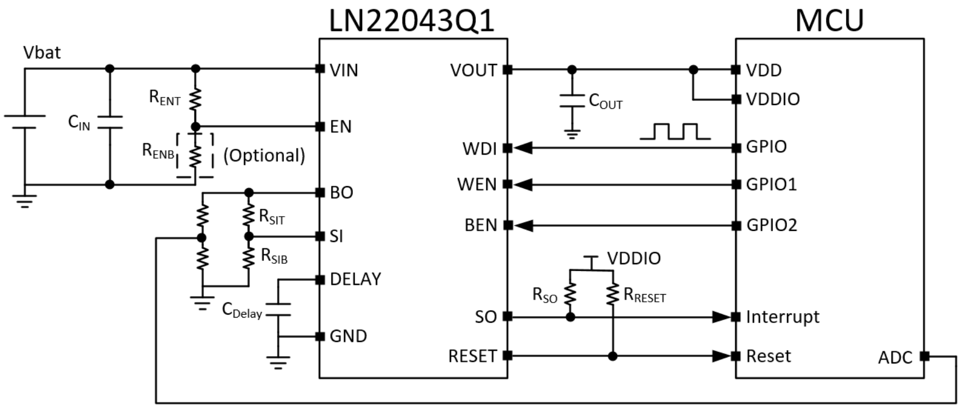


Figure 34. Typical Application

9.2 Design Requirements

For this design example, use the parameters listed in table 1 as the input parameters.

Table 1 Design Parameters

Design Parameter	Example Value
Input voltage range	6V to 16V
Output voltage	5V
Output current	200mA
V_{IN} startup threshold	5.5V
V_{BAT} Sense falling threshold	6V
Power good delay time	2.5ms

9.3 Detailed Design Procedure

The following design procedure applies to Figure 34 and Table 1.

9.3.1 R_{ENT} and R_{ENB} Select

When the system confirms the V_{IN} startup threshold, use equation (15) to calculate the value of R_{ENT} to R_{ENB}.

$$R_{ENT} = \left(\frac{V_{IN-Rising}}{V_{EN-H}} - 1\right) \times R_{ENB} \quad (15)$$

Where $V_{IN-Rising}$ is the V_{IN} startup threshold.

To reduce the input quiescent current, the recommended resistance value of R_{ENB} is between 100kΩ to 1MΩ. For example, if the R_{ENB} select a resistance of 510kΩ, then the R_{ENT} requires the selection of a 1.4MΩ resistance. Use equation (14) to calculate the $V_{IN-Falling}$ threshold is 4.6V.

9.3.2 R_{SIT} and R_{SIB} Select

When the system confirms the sense input trip threshold, use equation (16) to calculate the value of R_{SIT} to R_{SIB}.

$$R_{SIT} = \left(\frac{V_{IN-F}}{V_{SI-L}} - 1\right) \times R_{SIB} \tag{16}$$

Where V_{IN-F} is the target V_{BAT} falling threshold.

Typically, R_{SIB} is recommended to choose a resistance between 10kΩ to 1MΩ. For example, if the R_{SIB} select a resistance of 24.9kΩ, then R_{SIT} requires the selection of a 110kΩ resistance. Use equation (1) to calculate the SO error clearance threshold is 6.7V.

9.3.3 Power Good Delay Capacitor Select

When the system confirms the PG delay time, use equation (12) to calculate the PG delay capacitor.

$$C_{Delay} = 93.8nF$$

Considering the derating of the capacitor, the recommended PG delay capacitor is 100nF.

9.3.4 Calculation of Watchdog Serve Frequency

After confirming the PG delay capacitor, use equation (8) ~ (9) to calculate the recommended watchdog WDI signal period and frequency.

Use equation (8) to calculate the recommended WDI signal period:

$$t_{WDI-NOM} = 44.2ms$$

Use equation (9) to calculate the recommended WDI signal frequency:

$$f_{WDI-NOM} = 22.64Hz$$

Please note that both PG delay time and watchdog period are determined by delay capacitor, it is not necessary to calculate the C_{Delay} by PG delay time, if the WDI frequency is more important, then users can also use equation (8) ~ (9) to choose the capacitor value first and calculate the PG delay time later. Sometimes users must make a tradeoff between the two specifications.

9.3.5 Estimating Junction Temperature

The power dissipation for the regulator is calculated as below:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \tag{17}$$

For the application of the 16V maximum input voltage, the maximum power dissipation for the regulator is 2.2W.

Referring to chapter 7.4, the thermal resistance of the LEN EVM is 26°C/W. The junction temperature calculation equation is as below:

$$\Delta T_{Rise} = P_D \times R_{\theta JA-EVM} \tag{18}$$

Use equation (18) to calculate the maximum temperature rising is 57.2°C. The regulator can operate at maximum temperature of 85°C without triggering over temperature protection.

10 Layout

10.1 Layout Guidelines

To minimize the impact of parasitic parameters and improve the PSRR, EMC and thermal performance, it is recommended the following layout principles are applied to LN22043Q1 series products.

Number	Name	Layout Guideline
1	**VIN**	Place a ceramic capacitor C_{IN} of at least 1µF between VIN and GND. C_{IN} should be as close as possible to the VIN and GND pins. An additional ceramic capacitor in small package (such as 0603) is highly recommended.
2	**EN**	Connect to VIN directly, to VIN through a divider, or to a logic control signal.
3	**BO**	Connect to SI divider. If not used, keep this pin floating.
4	**SI**	Connect to the center leg of the voltage divider between BO and GND. The ground connection of voltage divider should be located to GND pin as close as possible. If not used, connect to the BO pin.
5	**GND**	It is recommended to connect to a GND plane.
6	**DELAY**	Place a ceramic capacitor between DELAY and GND. The capacitor should be as close as possible to DELAY and GND pins. If not used, keep this pin floating.
7	**RESET**	Connect to a voltage not greater than V_{OUT} through a pull-up resistor. If not used, left this pin floating is recommended.
8	**SO**	Connect to a voltage not greater than V_{OUT} through a pull-up resistor. If not used, left this pin floating is recommended.
9	**BEN**	Connect to the MCU GPIO interface.
10	**WEN**	Connect to the MCU GPIO interface.
11	**WDI**	Connect to the MCU GPIO interface.
12	**VOUT**	Place a ceramic capacitor C_{OUT} of at least 0.47µF between VOUT and GND. C_{OUT} should be as close as possible to the VOUT and GND pins.
	Thermal pad	It is recommended to connect the thermal pad to a complete ground plane through an array of 0.2mm thermal vias for heat sinking.

10.2 Layout Example

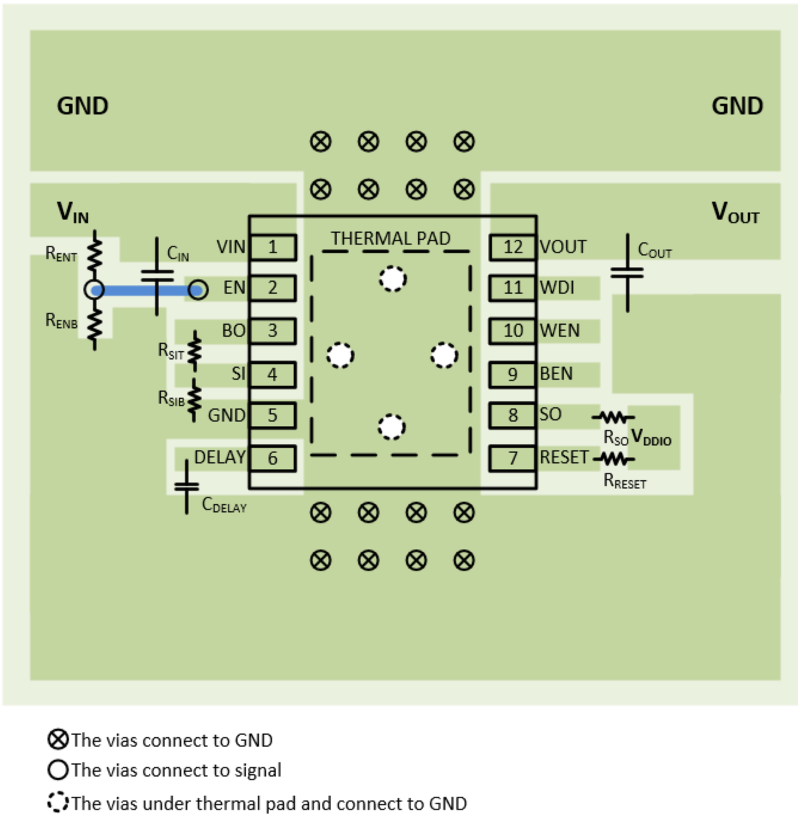
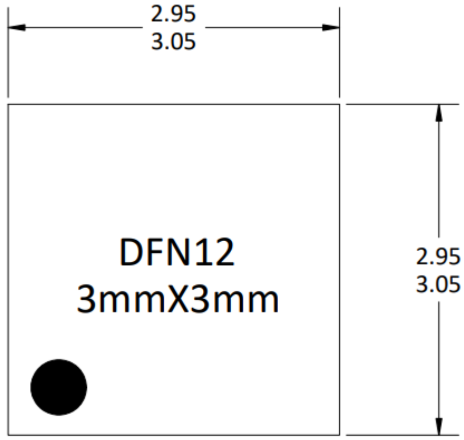


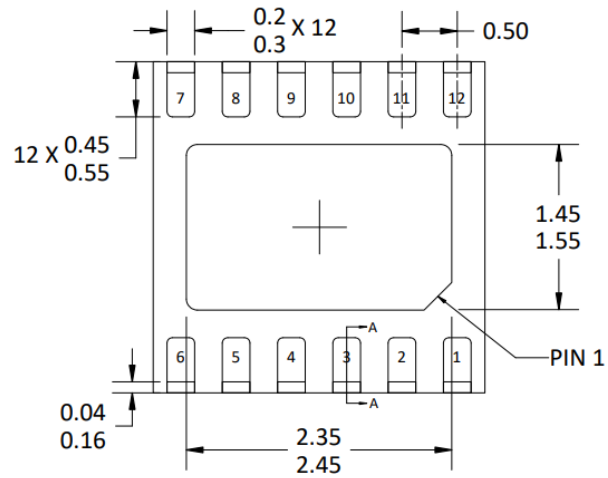
Figure 35. LN22043Q1 Layout Example

11 Package Information

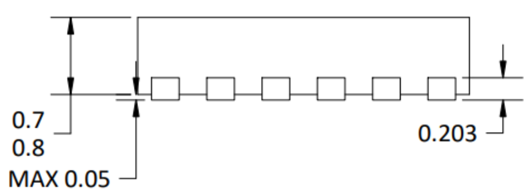
11.1 Package Outline



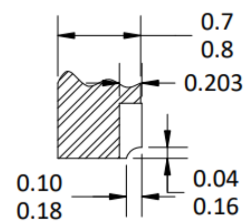
TOP VIEW



BOTTOM VIEW



SIDE VIEW



SECTION A-A

Notes:

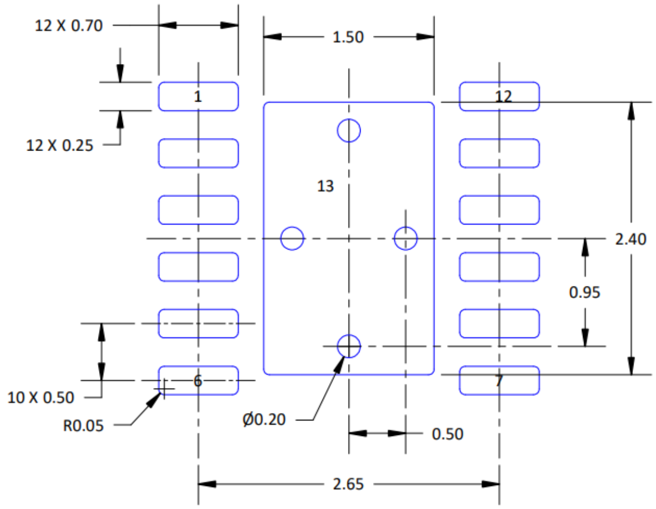
1. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

2. Both package length and width do not include mold flash.

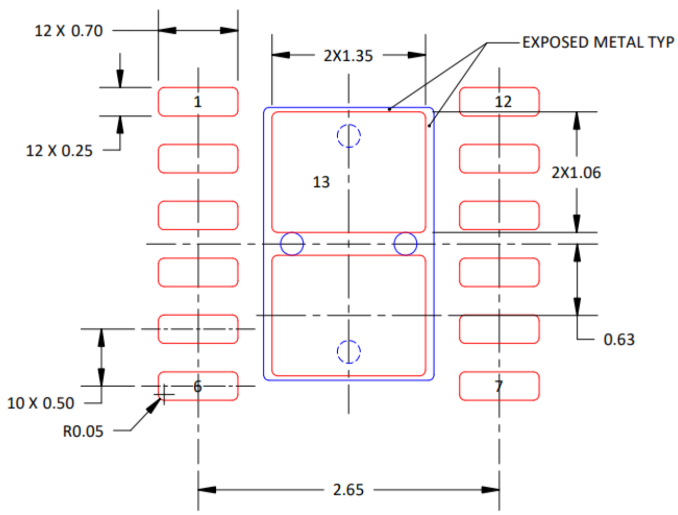
3. Unremoved flash between leads & package end flash shall not exceed 0.15mm from bottom body per side.

4. Features may not be present.

11.2 Footprint Example

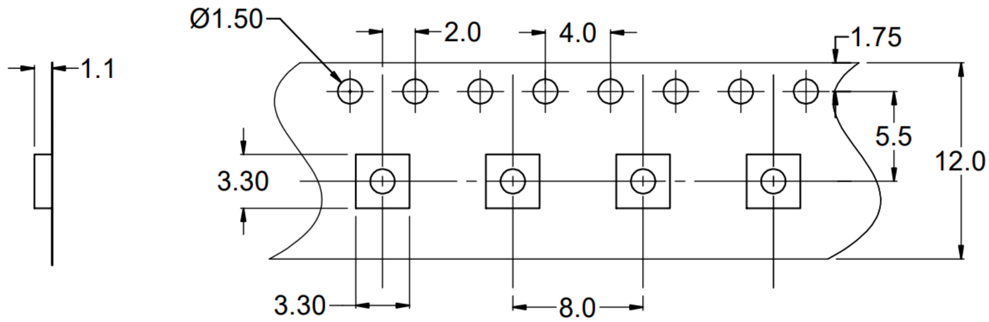


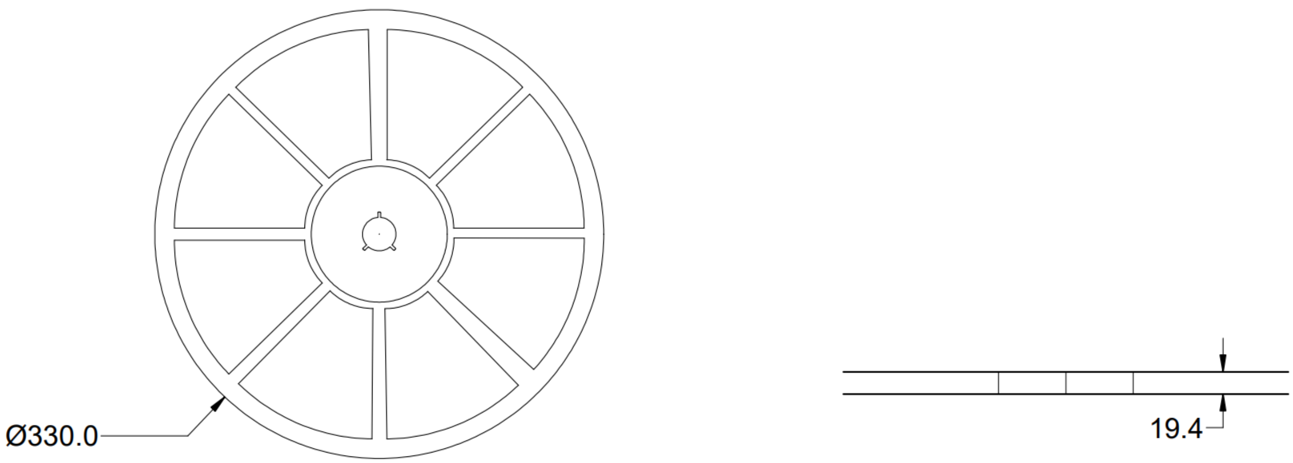
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X

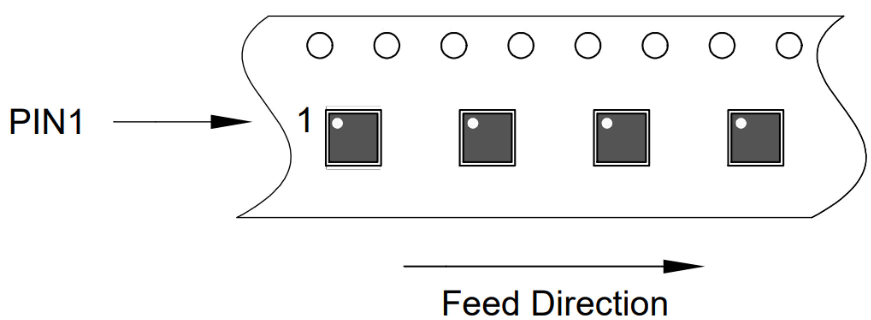


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
FOR PAD 13
80% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

11.3 Tape and Reel Information







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