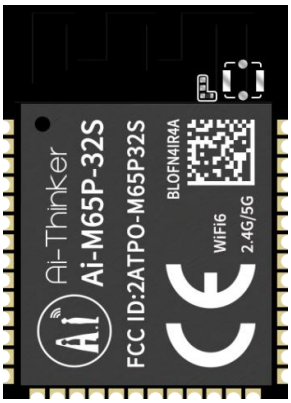
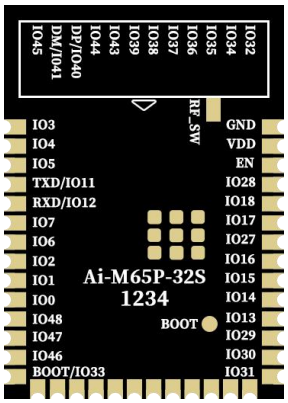
Ai-M65P-32S Specification





Product Series: Wi-Fi Series

Product Model: Ai-M65P-32S

Version: V1.1.0

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1 Product Overview

The Ai-M65P-32S module is based on the Bouffalo Lab BL618DG RF chip and supports IEEE 802.11a/b/g/n/ac/ax standards. It features dual-band 2.4GHz and 5GHz Wi-Fi 6, with both bands supporting 20MHz/40MHz bandwidths and 1024-QAM modulation. It also supports BT/BLE and IEEE 802.15.4. Wi-Fi and Bluetooth coexist using a shared antenna. The module integrates two high-performance RISC-V CPUs and offers a rich set of peripherals, including Timer, UART, I2C, SPI, PWM, IPC, SEC_Eng, EMAC, KeyScan, IR, Audio, I2S, Touch, CAM, MJPEG Encoder, MJPEG Decoder, OSD, Display, ADC, SDIO 3.0 (Host & Device), USB 2.0, and DMA, meeting the requirements of diverse applications in AIoT, new energy, and other fields.

For power management, the BL618DG integrates one DC-DC converter and two LDO regulators. Only a single external 3.3V power supply is required, simplifying the external power supply design. The BL618DG also supports secure boot, image encryption and signing, and firmware anti-rollback, addressing security requirements in smart home appliances, IoT, new energy, and other applications. The product offers five key advantages: strong signal performance, low power consumption, high integration, security and reliability, and a compact package.

Figure 1 shows the BL618DG main chip architecture.

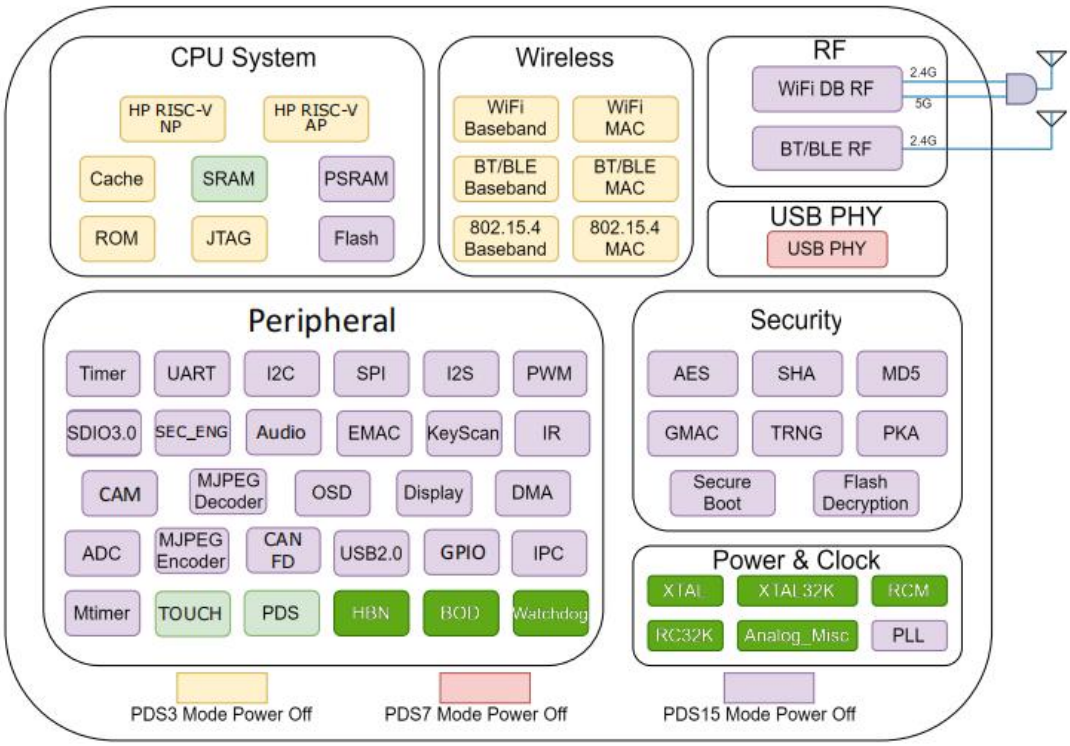


Figure 1 Main Chip Architecture Diagram

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1.1 Features

Wi-Fi

- 2.4GHz/5GHz operating frequency bands; supports MCS0 to MCS11
- Wi-Fi 6 (IEEE 802.11a/b/g/n/ac/ax)
- Supports 20MHz/40MHz bandwidth and 1T1R
- Supports WPS/WEP/WPA/WPA2/WPA3
- Supports LDPC, STBC, beamforming, DL/UL OFDMA, MU-MIMO, TWT (Target Wake Time), SR (Spatial Reuse), and ER (Extended Range)
- Supports aggregation (AMPDU and AMSDU), Immediate Block Ack, fragmentation, and defragmentation
- Supports IEEE 802.11e QoS WMM (Wi-Fi Multimedia), IEEE 802.11w PMF (Protected Management Frames), IEEE 802.11z TDLS, IEEE 802.11h DFS/TPC, and IEEE 802.11r
- Supports STA, SoftAP, STA + SoftAP, and Sniffer modes
- Integrated RF balun and PA/LNA
- Receiver sensitivity: -99 dBm@802.11b, 1Mbps
- Transmit power: 22 dBm@802.11b, 1Mbps

BLE

- Bluetooth® 5.3 dual mode (BT + BLE)
- Receiver sensitivity: -99 dBm@1Mbps
- High-power mode: 20dBm@1Mbps
- Supports multiple data rates: 2Mbps/1Mbps/500kbps/125kbps
- Supports IEEE 802.15.4 (Matter/Zigbee/Thread)
- Supports coexistence of Wi-Fi, BT/BLE, and Zigbee
- Wi-Fi and Bluetooth share the same antenna. The chip exposes a separate Bluetooth RF pin, and Bluetooth and 2.4GHz Wi-Fi are switched through the RF switch inside the module, enabling simultaneous Bluetooth and Wi-Fi connectivity.

Microcontroller Subsystem

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- High-performance RISC-V AP and NP processors, with clock frequencies of 640MHz for the AP and 480MHz for the NP
- Supports FPU

Security

- Secure Boot (supports firmware encryption & signing)
- Secure debug
- Anti-Rollback
- XIP On-The-Fly AES decryption (OTFAD)
- TrustZone
- AES-ECB/CBC/CTR/GMAC/XTS modes
- SHA-1/224/256/384/512
- TRNG (True Random Number Generator)
- PKA (Public Key Accelerator) for RSA/ECC
- Total 4096 bits eFuse

Peripherals

- Supports Timer, UART, I2C, SPI, PWM, IPC, SEC_Eng, EMAC, KeyScan, IR, Audio, I2S, Touch, CAM, MJPEG Encoder, MJPEG Decoder, OSD, Display, ADC, SDIO 3.0 (Host & Device), USB 2.0, DMA, etc.

Memory

- Total 852KB SRAM
  - 320KB OCRAM
  - 320KB WRAM
  - 128KB MRAM
  - 16KB XRAM
  - 64KB BT/BLE RAM
  - 4KB HBN RAM
- Supports internal/external NOR Flash

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- Supports in-package PSRAM

Development Environment

- Supports secondary development, integrated with Windows and Linux development environments

Power Characteristics

- Transmit current: TX 802.11ax, MCS11, POUT=+10dBm: -mA (average, 100% duty cycle)
- Receive current: -mA
- PDS current consumption (Wi-Fi connected): -μA
- HBN current consumption: 38μA (For lower HBN power consumption, please contact Ai-Thinker. HBN power consumption varies for different RF configurations, with a minimum of 8μA.)

Physical Characteristics

- Package: SMD-40
- Module dimensions (L × W × H): 25.50 × 18.00 × 3.10mm
- Antenna type: onboard antenna or IPEX Gen 4 connector optional
- Operating temperature: -20 – 85°C
- Storage conditions: -20 – 125°C, < 90% RH

Electrical Characteristics

- Supply voltage: 2.97 – 3.63V (typical value 3.3V)
- Supply current: > 500mA
- Communication interface: standard UART
- Available I/Os: 37 GPIOs exposed by default
- Protection: built-in ESD protection circuit

Note: For features not marked, please refer to the official BL618DG chip datasheet.

1.2 Application Scenarios

- Audio/Video Multimedia
- Internet of Things (IoT)
- Mobile Devices
- Smart Home
- Central Control Unit

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2 Key Specifications

Table 1 summarizes the key electrical and physical parameters of the Ai-M65P-32S module.

Table 1 Key Specifications

Model	Ai-M65P-32S
Package	SMD-40
Dimensions	25.50 × 18.00 × 3.10mm
Antenna Type	Onboard antenna/IPEX Gen 4 connector optional
Frequency Range	2400 – 2483.5MHz, 5180 – 5825MHz
Operating Temperature	-20 – 85℃
Storage Conditions	-20 – 125℃, < 90% RH
Power Supply Range	Supply voltage: 2.97 – 3.63V, typical 3.3V; supply current > 500mA
Available I/Os	37 by default
UART Rate	115200bps by default
Security	WPS/WEP/WPA/WPA2/WPA3
Flash	4MByte by default (up to 16MByte supported)

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3 Electrical Characteristics

3.1 Recommended Operating Conditions

Table 2 lists the recommended operating electrical parameters of the Ai-M65P-32S module. Operating outside these ranges may cause device damage.

Table 2 Recommended Operating Conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Supply Voltage	2.97	3.3	3.63	V
I	Supply Current	500	-	-	mA

3.2 I/O DC Electrical Characteristics

Table 3 lists the I/O DC characteristics of the Ai-M65P-32S module. These parameters are mainly used for external interface level matching and GPIO circuit design.

Table 3 I/O DC Electrical Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
VIH	High-level Input Voltage	2	-	-	V
VIL	Low-level Input Voltage	-	-	0.8	V
VOH	High-level Output Voltage	-	0.9 × VDDIO	-	V
VOL	Low-level Output Voltage	-	0.1 × VDDIO	-	V

3.3 Electrostatic Discharge

Figure 2 shows the ESD protection diagram. Ai-M65P-32S is an ESD-sensitive device and requires special precautions during handling.



Figure 2 ESD Protection Diagram

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3.4 Wi-Fi RF Performance

Table 4 lists the Wi-Fi performance parameters of the Ai-M65P-32S module. The RF performance parameters are measured under typical test conditions. Actual performance may be affected by the antenna, power supply, PCB layout, test environment, and other factors.

Table 4 Wi-Fi RF Performance

Description	Typ			Unit
Frequency Range	2400 – 2483.5			MHz
2.4GHz Output Power				
Mode	**Min**	**Typ**	**Max**	**Unit**
802.11b, 1Mbps	-	22	-	dBm
802.11b, 11Mbps	-	22	-	dBm
802.11g, 6Mbps	-	18	-	dBm
802.11g, 54Mbps	-	17	-	dBm
802.11n, HT20 (MCS7)	-	17	-	dBm
802.11n, HT40 (MCS7)	-	17	-	dBm
802.11ax, HE20 (MCS9)	-	16	-	dBm
802.11ax, HE40 (MCS9)	-	16	-	dBm
802.11ax, HE20 (MCS11)	-	15	-	dBm
802.11ax, HE40 (MCS11)	-	15	-	dBm
2.4GHz Receiver Sensitivity				
Mode	**Min**	**Typ**	**Max**	**Unit**
802.11b, 1Mbps	-	-99	-	dBm
802.11b, 11Mbps	-	-88	-	dBm
802.11g, 6Mbps	-	-92	-	dBm
802.11g, 54Mbps	-	-77	-	dBm
802.11n, HT20 (MCS7)	-	-74	-	dBm
802.11n, HT40 (MCS7)	-	-72	-	dBm

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802.11ax, HE20 (MCS9)	-	-69	-	dBm
802.11ax, HE40 (MCS9)	-	-69	-	dBm
802.11ax, HE20 (MCS11)	-	-66	-	dBm
802.11ax, HE40 (MCS11)	-	-63	-	dBm
Description	**Typ**			**Unit**
Frequency Range	5180 – 5825			MHz
5GHz Output Power				
Mode	**Min**	**Typ**	**Max**	**Unit**
802.11a, 6Mbps	-	20	-	dBm
802.11a, 54Mbps	-	17	-	dBm
802.11n, HT20 (MCS7)	-	15	-	dBm
802.11n, HT40 (MCS7)	-	15	-	dBm
802.11ax, HE20 (MCS9)	-	13	-	dBm
802.11ax, HE40 (MCS9)	-	13	-	dBm
802.11ax, HE20 (MCS11)	-	10	-	dBm
802.11ax, HE40 (MCS11)	-	10	-	dBm
5GHz Receiver Sensitivity				
Mode	**Min**	**Typ**	**Max**	**Unit**
802.11a, 6Mbps	-	-90	-	dBm
802.11a, 54Mbps	-	-75	-	dBm
802.11n, HT20 (MCS7)	-	-72	-	dBm
802.11n, HT40 (MCS7)	-	-70	-	dBm
802.11ax, HE20 (MCS9)	-	-67	-	dBm
802.11ax, HE40 (MCS9)	-	-67	-	dBm
802.11ax, HE20 (MCS11)	-	-64	-	dBm
802.11ax, HE40 (MCS11)	-	-60	-	dBm

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3.5 BLE RF Performance

Table 5 lists the BLE performance parameters of the Ai-M65P-32S module. The RF performance parameters are measured under typical test conditions. Actual performance may be affected by the antenna, power supply, PCB layout, test environment, and other factors.

Table 5 BLE RF Performance

Description	**Typ**			**Unit**
Frequency Range	2400 – 2483.5			MHz
Output Power				
Rate Mode	**Min**	**Typ**	**Max**	**Unit**
1Mbps	-	20	-	dBm
2Mbps	-	20	-	dBm
Receiver Sensitivity				
Rate Mode	**Min**	**Typ**	**Max**	**Unit**
1Mbps Sensitivity @ 30.8% PER	-	-99	-	dBm
2Mbps Sensitivity @ 30.8% PER	-	-97	-	dBm

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Table 6 lists the regulatory requirements for common countries and regions. The module requires an external MCU to adjust the transmit power and operating frequency, which must be configured by the user in strict compliance with the regulations of the relevant country or region. The configurable 5GHz transmit power range is -dBm, while the configurable 2.4GHz transmit power range is -17 to +12dBm.

Table 6 RF Regulatory Limits by Country / Region

Country / Region	Regulation	Operating Band	Power Limit
Mainland China	Document No. 129 (2021)	2400 – 2483.5MHz	EIRP ≤ 20dBm
Mainland China	Document No. 129 (2021)	5180 – 5825MHz	EIRP ≤ -dBm
European Union	CE	2400 – 2483.5MHz	EIRP ≤ 20dBm
European Union	CE	5180 – 5825MHz	EIRP ≤ -dBm
North America	FCC	2400 – 2483.5MHz	EIRP ≤ 30dBm
North America	FCC	5180 – 5825MHz	EIRP ≤ -dBm

Notes:

- ERP (dBm) = Pt (dBm) − Cable Loss (dB) + Antenna Gain (dBd)
- EIRP (dBm) = Pt (dBm) − Cable Loss (dB) + Antenna Gain (dBi)

According to the sample code on Ai-Thinker's official website, the procedures for configuring transmit power and operating frequency are as follows:

* @param [in] radio Pointer to radio data structure

* @param [in] output_pwr_in_dbm Output power - in dBm

* @param [in] rf_freq_in_hz RF frequency - in Hertz

static inline ral_status_t ral_set_tx_cfg(const ral_t* radio, const int8_t output_pwr_in_dbm,

const uint32_t rf_freq_in_hz)

For questions regarding the above configuration, please contact Ai-Thinker.

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3.6 Power Consumption

Table 7 lists the power consumption data of the Ai-M65P-32S module in different modes. The following power consumption data are measured under a 3.3V power supply and 25℃ ambient temperature.

- The P_{OUT} power for all transmit modes is measured at the antenna interface.
- All transmission data are measured at 100% duty cycle in continuous transmit mode.

Table 7 Power Consumption

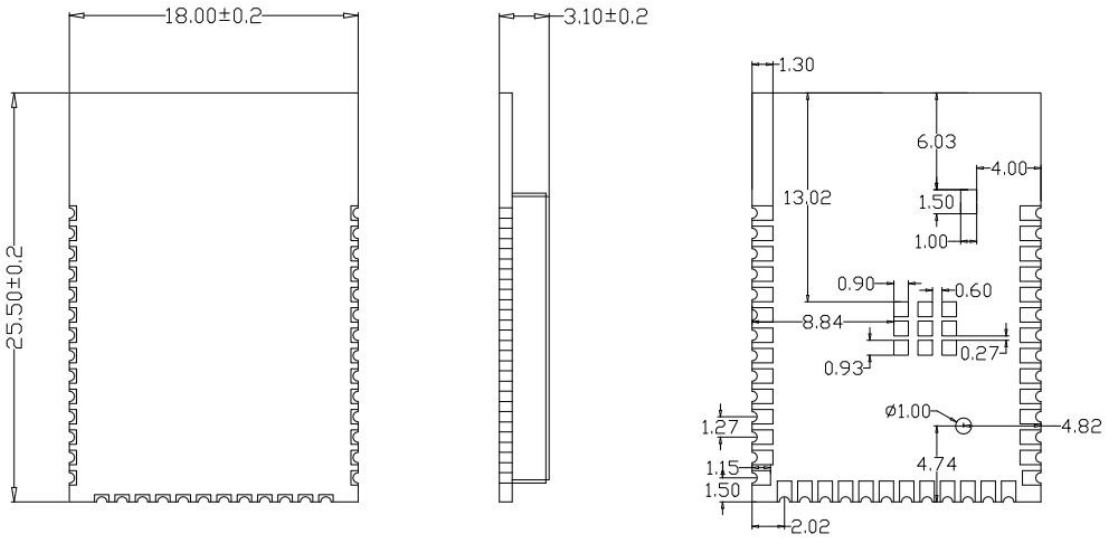
Mode	Min	Avg	Max	Unit
TX 802.11b, 11Mbps, POUT=+22dBm	-	-	-	mA
TX 802.11g (2.4GHz), 54Mbps, POUT=+17dBm	-	-	-	mA
TX 802.11n (2.4GHz), MCS7, POUT=+17dBm	-	-	-	mA
TX 802.11ax (2.4GHz), MCS9, POUT=+16dBm	-	-	-	mA
RX 802.11b (2.4GHz), Packet Length 1500 Bytes	-	-	-	mA
RX 802.11g (2.4GHz), Packet Length 1500 Bytes	-	-	-	mA
RX 802.11n (2.4GHz), Packet Length 1500 Bytes	-	-	-	mA
RX 802.11ax (2.4GHz), Packet Length 1500 Bytes	-	-	-	mA
TX 802.11a (5GHz), 54Mbps, POUT=+17dBm	-	-	-	mA
TX 802.11n (5GHz), MCS7, POUT=+15dBm	-	-	-	mA
TX 802.11ax (5GHz), MCS9, POUT=+13dBm	-	-	-	mA
RX 802.11a (5GHz), Packet Length 1500 Bytes	-	-	-	mA
RX 802.11n (5GHz), Packet Length 1500 Bytes	-	-	-	mA
RX 802.11ax (5GHz), Packet Length 1500 Bytes	-	-	-	mA
Deep-Sleep	-	-	-	μA

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4 Mechanical Specifications

4.1 Module Dimensions

Figure 3 shows the outline dimensions of the Ai-M65P-32S module. The outline dimensions (L × W × H) are 25.50 × 18.00 × 3.10mm. The dimensional tolerance is ±0.20mm.



Top View Side View Bottom View

Figure 3 Module Dimensions (Unit: mm)

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4.2 Shield Cover Marking Information

Figure 4 shows the shield cover marking information of the Ai-M65P-32S module. Each character corresponds to module configuration information such as chip brand, Flash size, and temperature version.

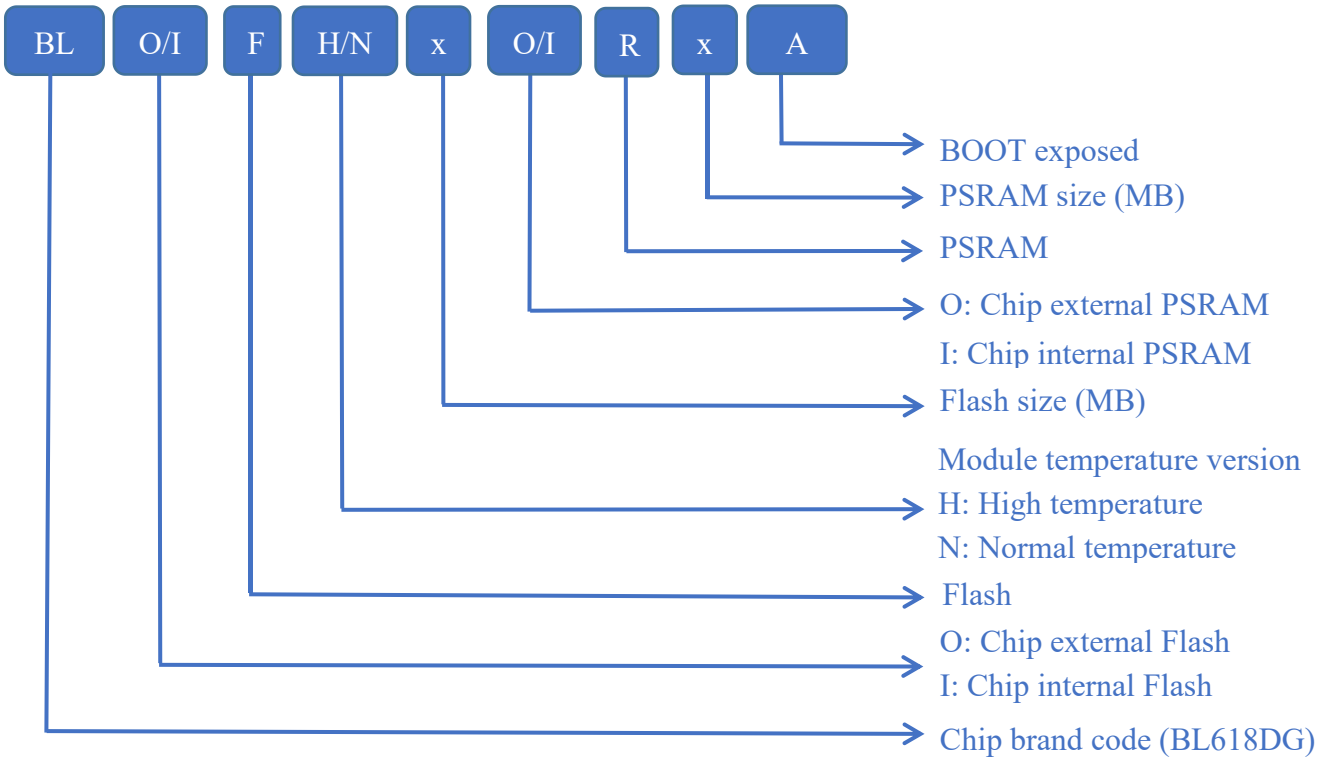


Figure 4 Shield Cover Marking Information

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4.3 External Antenna Connector Dimensions

Figure 5 shows the engineering drawing of the IPEX Gen 4 connector used with Ai-M65P-32S.

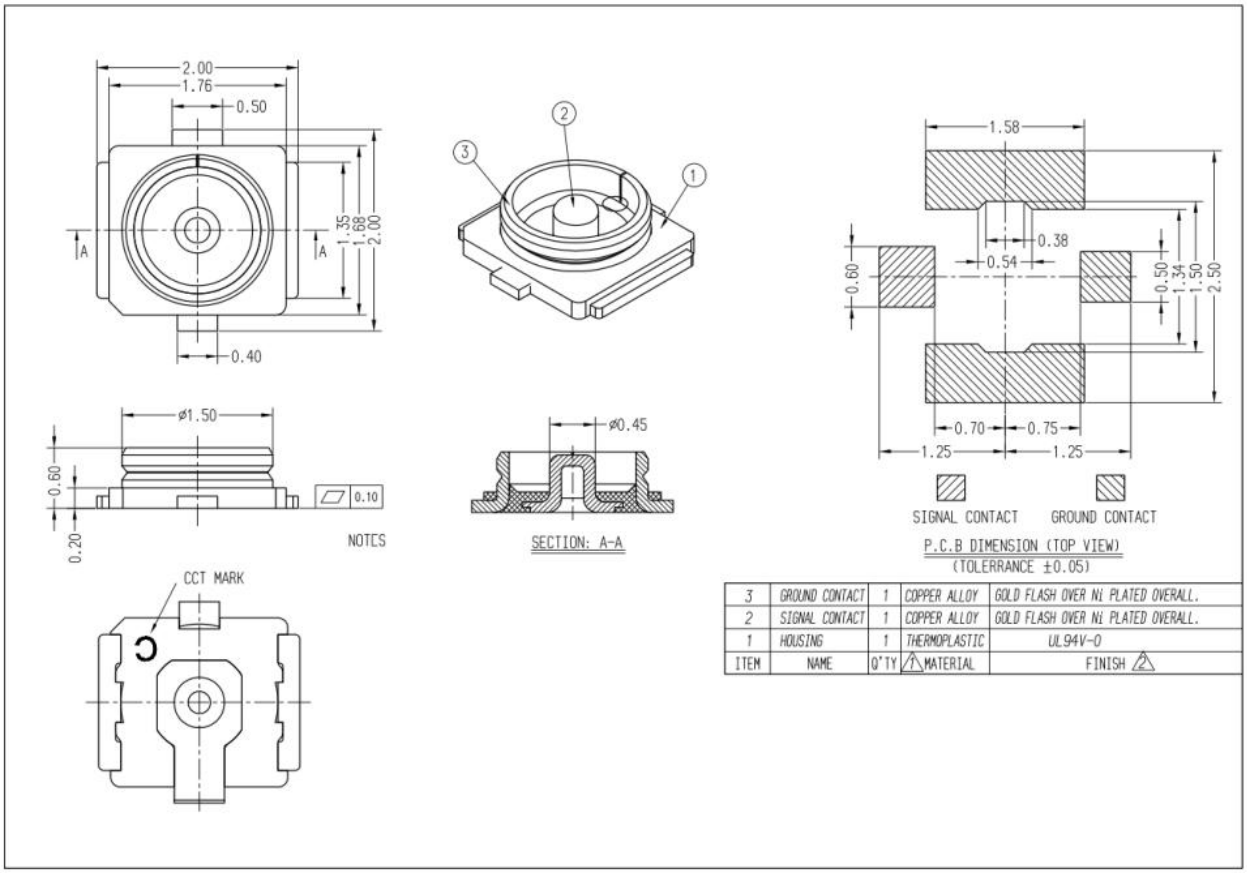
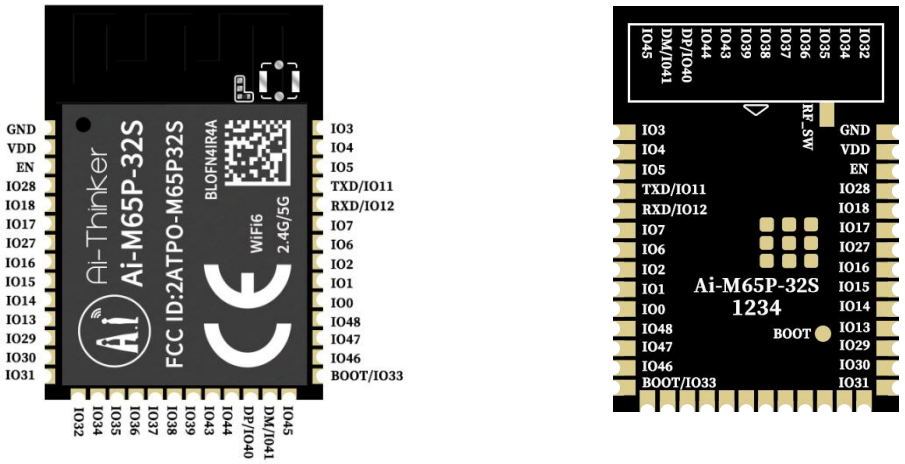


Figure 5 External Antenna Connector Dimensions (Unit: mm)

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5 Pin Definition

Figure 6 shows the top and bottom views of the Ai-M65P-32S module's pin layout, with a total of 40 pins exposed.



Top View Bottom View

Figure 6 Pin Diagram

Table 8 defines the pin functions of the Ai-M65P-32S module, including pin number, pin name, and function description.

Table 8 Pin Function Definition

No.	Name	Function
1	GND	Ground
2	VDD	3.3V supply (VDD); the external power supply output current is recommended to be above 500mA.
3	EN	Chip enable pin; active high.
4	IO28	SPI3_SS/pdm_clk_o/I2S_BCLK/CANFD2_RX/I2C0_SDA/I2C2_SCL/UART_SIG4/E0_TXD[0]/CAM0_VSYNC/ADC1_3/dsi_dp_clk/SWGPIO[28]/pwm2_mc_out_c0p/pwm2_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_DB7/data16/R0/spdt_p/main_jtag_tms/main_-cjtag_tmsc/PEC_28/rf_epa_gpio[4]/ant_switch_cntI[3]/epta_wI_act/epta_wI_act/gnt/chip_clk_out[0]
5	IO18	SPI0_MISO/pdm_clk_o/I2S_DI/I2S_RCLK_O/CANFD0_RX/I2C1_SDA/I2C2_SCL/UART_SIG6/E0_MDC/CAM0_DATA3/ADC0_3/touch_ch[6]/SWGPIO[18]/pwm1_mc_out_c2p/pwm1_mc_out_c1p/wl_jtag_tdo/UART

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		3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_CSn/data6/B6/spdt_p/main_jtag_tdo/PEC_18/rf_epa_gpio[2]/ant_switch_cntl[1]/epta_bt_pri/epta_bt_pri/chip_clk_out[2]
6	IO17	SPI0_SCLK/pdm_0_in/I2S_FS/CANFD2_TX/I2C0_SCL/I2C2_SDA/UART_SIG5/E0_MDIO/CAM0_DATA2/ADC1_2/touch_ch[5]/SWGPIO[17]/pwm1_mc_out_c1p/pwm1_mc_out_c0n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_WRn/data5/B5/spdt_n/main_jtag_tck/main_-cjtag_tckc/PEC_17/rf_epa_gpio[1]/ant_switch_cntl[0]/epta_bl_act/epta_bl_act/chip_clk_out[1]
7	IO27	SPI2_MOSI/pdm_0_in/I2S_DO/I2S_RCLK_O/CANFD1_TX/I2C1_SCL/I2C2_SDA/UART_SIG3/E0_REF_CLK/CAM0_HSYNC/ADC1_11/dsi_dn_clk/SWGPIO[27]/pwm1_mc_out_c3p/pwm2_mc_out_c1n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_DB6/data15/G7/spdt_n/main_jtag_tdi/PEC_27/rf_epa_gpio[3]/ant_switch_cntl[2]/chip_clk_out[3]
8	IO16	SPI0_SS/pdm_clk_o/I2S_BCLK/CANFD2_RX/I2C0_SDA/I2C2_SCL/UART_SIG4/E0_TX_EN/CAM0_DATA1/ADC0_2/touch_ch[4]/SWGPIO[16]/pwm1_mc_out_c0p/pwm1_mc_out_c0p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/data4/B4/spdt_p/main_jtag_tms/main_-cjtag_tmsc/PEC_16/rf_epa_gpio[0]/ant_switch_req/epta_wl_act/epta_wl_act/gnt/chip_clk_out[0]; this pin is assigned to RF_SW control by default and is unavailable for other use in the default configuration. Leave it floating.
9	IO15	SPI3_MOSI/pdm_0_in/I2S_DO/I2S_RCLK_O/CANFD1_TX/I2C1_SCL/I2C2_SDA/UART_SIG3/CAM0_DATA0/ADC1_1/touch_ch[3]/SWGPIO[15]/irrx/pwm2_mc_out_c3p/pwm2_mc_out_c3n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/data3/B3/spdt_n/main_jtag_tdi/PEC_15/rf_epa_gpio[7]/ant_switch_cntl[6]/chip_clk_out[3]
10	IO14	SPI3_MISO/pdm_clk_o/I2S_DI/I2S_RCLK_O/CANFD1_RX/I2C1_SDA/I2C2_SCL/UART_SIG2/E1_MDC/vref_ext[1]/touch_ch[2]/SWGPIO[14]/irrx/pwm2_mc_out_c2p/pwm2_mc_out_c3p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_DCn/DBI_TypeC_DCn/data2/B2/spdt_p/main_jtag_tdo/PEC_14/rf_epa_gpio[6]/ant_switch_cntl[5]/epta_bt_pri/chip_clk_out[2]

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11	IO13	SPI3_SCLK/pdm_0_in/I2S_FS/CANFD0_TX/I2C0_SCL/I2C2_SDA/UART_SIG1/E1_MDIO/ADC0_1/dc_tp_18/C_-EXT/SWGPIO[13]/irrx/pwm2_mc_out_c1p/pwm2_mc_out_c2n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_RDn/DBI_TypeC_SDA0/data1/B1/spdt_n/main_jtag_tck/main_cjtag_tckc/PEC_13/rf_epa_gpio[5]/ant_switch_cntl[4]/epta_bl_act/epta_bl_act/chip_clk_out[1]
12	IO29	SPI3_SCLK/pdm_0_in/I2S_FS/CANFD2_TX/I2C0_SCL/I2C2_SDA/UART_SIG5/E0_TXD[1]/CAM0_CLK/ADC0_4/dsi_dn2/SWGPIO[29]/pwm2_mc_out_c1p/pwm2_mc_out_c2n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/data17/R1/spdt_n/main_jtag_tck/main_cj-tag_tckcPEC_29/rf_epa_gpio[5]/ant_switch_cntl[4]/epta_bl_act/epta_bl_act/chip_clk_out[1]
13	IO30	SPI3_MISO/pdm_clk_o/I2S_DI/I2S_RCLK_O/CANFD0_RX/I2C1_SDA/I2C2_SCL/UART_SIG6/E0_RXD[0]/CAM0_DATA4/ADC1_4/AUADC_4/dsi_-dp2/SWGPIO[30]/irrx/pwm2_mc_out_c2p/pwm2_mc_out_c3p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/data18/R2/spdt_p/main_jtag_tdo/PEC_30/rf_epa_gpio[6]/ant_switch_cntl[5]/epta_bt_pri/epta_bt_pri/chip_clk_out[2]
14	IO31	SPI3_MOSI/pdm_0_in/I2S_DO/I2S_RCLK_O/CANFD0_TX/I2C1_SCL/I2C2_SDA/UART_SIG7/E0_RXD[1]/CAM0_DATA5/ADC0_5/AUADC_5/dsi_-dn3/SWGPIO[31]/irrx/pwm2_mc_out_c3p/pwm2_mc_out_c3n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/data19/R3/spdt_n/main_jtag_tdi/PEC_31/rf_epa_gpio[7]/ant_switch_cntl[6]/chip_clk_out[3]
15	IO32	SPI0_SS/pdm_clk_o/I2S_BCLK/CANFD1_RX/I2C0_SDA/I2C2_SCL/UART_SIG8/E0_RX_DV/CAM0_DATA6/vref_ext[2]/dsi_dp3/SWGPIO[32]/irrx/pwm1_mc_out_c0p/pwm1_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/data20/R4/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_32/rf_epa_gpio[0]/ant_switch_req/epta_wl_act/epta_wl_act/gnt/chip_clk_out[0]
16	IO34	Data2/SPI0_MISO/SFlash_CS/I2S_DI/I2S_RCLK_O/CANFD2_RX/I2C1_SDA/I2C2_SCL/UART_SIG10/SWGPIO[34]/SDIO_DAT2/pwm1_mc_out_c2p/pwm1_mc_out_c3p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_p/main_jtag_tdo/PEC_34/rf_epa_gpio[2]/ant_switch_cntl[1]/epta_bt_pri/epta_bt_pri/chip_clk_out[2];

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		in the external Flash version, this I/O is shared with the internal Flash and is not brought out.
17	IO35	Data3/SPI0_MOSI/SFlash_D0/I2S_DO/I2S_RCLK_O/CANFD2_TX/I2C1_SCL/I2C2_SDA/UART_SIG11/SWGPIO[35]/SDIO_DAT3/pwm1_mc_out_c3p/pwm1_mc_out_c3n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_n/main_jtag_tdi/PEC_35/rf_epa_gpio[3]/ant_switch_cntl[2]/chip_clk_out[3]; in the external Flash version, this I/O is shared with the internal Flash and is not brought out.
18	IO36	CMD/SPI1_SS/SFlash_D1/I2S_BCLK/CANFD0_RX/I2C0_SDA/I2C2_SCL/UART_SIG0/SWGPIO[36]/SDIO_CMD/pwm2_mc_out_c0p/pwm1_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_36/rf_epa_gpio[4]/ant_switch_cntl[3]/epta_wl_act/epta_wl_act/gnt/chip_clk_out[0]; in the external Flash version, this I/O is shared with the internal Flash and is not brought out.
19	IO37	CLK/SPI1_SCLK/SFlash_D2/I2S_FS/CANFD0_TX/I2C0_SCL/I2C2_SDA/UART_SIG1/SWGPIO[37]/SDIO_CLK/pwm2_mc_out_c1p/pwm1_mc_out_c2n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_n/main_jtag_tck/main_cj-tag_tckc/PEC_37/rf_epa_gpio[5]/ant_switch_cntl[4]/epta_bl_act/epta_bl_act/chip_clk_out[1]; in the external Flash version, this I/O is shared with the internal Flash and is not brought out.
20	IO38	Data0/SPI1_MISO/SFlash_D3/I2S_DI/I2S_RCLK_O/CANFD1_RX/I2C1_SDA/I2C2_SCL/UART_SIG2/SWGPIO[38]/SDIO_DAT0/pwm2_mc_out_c2p/pwm1_mc_out_c3p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_p/main_jtag_tdo/PEC_38/rf_epa_gpio[6]/ant_switch_cntl[5]/epta_bt_pri/epta_bt_pri/chip_clk_out[2]; in the external Flash version, this I/O is shared with the internal Flash and is not brought out.
21	IO39	Data1/SPI1_MOSI/SFlash_CLK/I2S_DO/I2S_RCLK_O/CANFD1_TX/I2C1_SCL/I2C2_SDA/UART_SIG3/SWGPIO[39]/SDIO_DAT1/pwm2_mc_out_c3p/pwm1_mc_out_c3n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_R

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		OW_I/Key_Scan_Drive_COL_O/spdt_n/main_jtag_tdi/PEC_39/rf_epa_gpio[7]/ant_switch_cntl[6]/chip_clk_out[3]; in the external Flash version, this I/O is shared with the internal Flash and is not brought out.
22	IO43	Data2/SPI2_MOSI/SFlash_CS/I2S_DO/I2S_RCLK_O/CANFD0_TX/I2C1_SCL/I2C2_SDA/UART_SIG7/SWGPIO[43]/SDIO_DAT2/pwm1_mc_out_c3p/pwm2_mc_out_c1n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/data22/R6/spdt_n/main_jtag_tdi/PEC_43/rf_epa_gpio[3]/ant_switch_cntl[2]/chip_clk_out[3]
23	IO44	Data3/SPI3_SS/SFlash_D0/I2S_BCLK/CANFD1_RX/I2C0_SDA/I2C2_SCL/UART_SIG8/SWGPIO[44]/SDIO_DAT3/pwm2_mc_out_c0p/pwm2_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/data23/R7/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_44/rf_epa_gpio[4]/ant_switch_cntl[3]/epta_wl_act/epta_wl_act/gnt/chip_clk_out[0]
24	DP/IO40	SPI2_SS/pdm_0_in/I2S_BCLK/CANFD2_RX/I2C0_SDA/I2C2_SCL/UART_SIG4/USB_DP/SWGPIO[40]/pwm1_mc_out_c0p/pwm2_mc_out_c0p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_40/rf_epa_gpio[0]/ant_switch_req/epta_wl_act/epta_wl_act/gnt/chip_clk_out[0]
25	DM/IO41	SPI2_SCLK/pdm_clk_o/I2S_FS/CANFD2_TX/I2C0_SCL/I2C2_SDA/UART_SIG5/USB_DM/SWGPIO[41]/pwm1_mc_out_c1p/pwm2_mc_out_c0n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/spdt_n/main_jtag_tck/main_cj-tag_tckc/PEC_41/rf_epa_gpio[1]/ant_switch_cntl[0]/epta_bl_act/epta_bl_act/chip_clk_out[1]
26	IO45	CMD/SPI3_SCLK/SFlash_D1/I2S_FS/CANFD1_TX/I2C0_SCL/I2C2_SDA/UART_SIG9/SWGPIO[45]/SDIO_CMD/pwm2_mc_out_c1p/pwm2_mc_out_c2n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART30_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/PCLK/spdt_n/main_jtag_tck/main_cj-tag_tckc/PEC_45/rf_epa_gpio[5]/ant_switch_cntl[4]/epta_bl_act/epta_bl_act/chip_clk_out[1]
27	BOOT/IO33	SPI0_SCLK/I2S_FS/CANFD1_TX/I2C0_SCL/I2C2_SDA/UART_SIG9/E0_RX_ERR/CAM0_DATA7/SWGPIO[33]/pwm1_mc_out_c1p/pwm1_mc_out_c2n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Sca

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		n_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/data21/R5/spdt_n/main_jtag_tck/main_cj-tag_tckc/PEC_33/rf_epa_gpio[1]/ant_switch_cntl[0]/epta_bl_act/chip_clk_out[1]
28	IO46	CLK/SPI3_MISO/SFlash_D2/I2S_DI/I2S_RCLK_O/CANFD2_RX/I2C1_SDA/I2C2_SCL/UART_SIG10/SWGPIO[46]/SDIO_CLK/pwm2_mc_out_c2p/pwm2_mc_out_c3p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/HS/spdt_p/main_jtag_tdo/PEC_46/rf_epa_gpio[6]/ant_switch_cntl[5]/epta_bt_pri/chip_clk_out[2]
29	IO47	Data0/SPI3_MOSI/SFlash_D3/I2S_DO/I2S_RCLK_O/CANFD2_TX/I2C1_SCL/I2C2_SDA/UART_SIG11/SWGPIO[47]/SDIO_DAT0/pwm2_mc_out_c3p/pwm2_mc_out_c3n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/VS/spdt_n/main_jtag_tdi/PEC_47/rf_epa_gpio[7]/ant_switch_cntl[6]/chip_clk_out[3]
30	IO48	Data1/SPI0_SS/SFlash_CLK/I2S_BCLK/CANFD0_RX/I2C0_SDA/I2C2_SCL/UART_SIG0/SWGPIO[48]/SDIO_DAT1/pwm1_mc_out_c0p/pwm1_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/DE/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_48/rf_epa_gpio[0]/ant_switch_req/chip_clk_out[0]
31	IO0	SPI0_SS/pdm_clk_o/I2S_BCLK/CANFD0_RX/I2C0_SDA/I2C2_SCL/UART_SIG0/E1_REF_CLK/CAM0_DATA0/ADC0_6/SWGPIO[0]/irtx/pwm1_mc_out_c0p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_DB0/DISP_QSPI_SCL/PCLK/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_0/rf_epa_gpio[0]/ant_switch_req/epta_wl_act/gnt/chip_clk_out[0]
32	IO1	SPI0_SCLK/pdm_0_in/I2S_FS/CANFD0_TX/I2C0_SCL/I2C2_SDA/UART_SIG1/E1_TXD[0]/CAM0_DATA1/ADC1_6/SWGPIO[1]/irrx/pwm1_mc_out_c1p/pwm1_mc_out_c0n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_DB1/DISP_QSPI_CSn/HS/spdt_n/main_jtag_tck/main_cj-tag_tckcPEC_1/rf_epa_gpio[1]/ant_switch_cntl[0]/epta_bl_act/chip_clk_out[1]
33	IO2	SPI0_MISO/pdm_clk_o/I2S_DI/I2S_RCLK_O/CANFD1_RX/I2C1_SDA/I2C2_SCL/UART_SIG2/E1_TXD[1]/CAM0_DATA2/ADC0_7/SWGPIO[2]/irrx/irtx/pwm1_mc_out_c2p/pwm1_mc_out_c1p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_DB2/DISP_QSPI_SDA0/VS/spdt_p/main_jtag_tdo/PEC_2/r

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		f_epa_gpio[2]/ant_switch_cntl[1]/epta_bt_pri/chip_clk_out[2]
34	IO6	SPI1_MISO/pdm_clk_o/I2S_DI/I2S_RCLK_O/CANFD0_RX/I2C1_SDA/I2C2_SCL/UART_SIG6/E1_TX_EN/CAM0_CLK/ADC1_8/touch_ch[0]/SWGPIO[6]/irrx/irtx/pwm2_mc_out_c2p/pwm1_mc_out_c3p/wl_jtag_tdo/UART3_TXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_DB6/VS/spdt_p/main_jtag_tdo/PEC_6/rf_epa_gpio[6]/ant_switch_cntl[5]/epta_bt_pri/chip_clk_out[2]
35	IO7	SPI1_MOSI/pdm_0_in/I2S_DO/I2S_RCLK_O/CANFD0_TX/I2C1_SCL/I2C2_SDA/UART_SIG7/E1_RX_DV/CAM0_DATA4/ADC0_9/touch_ch[1]/SWGPIO[7]/irrx/irtx/pwm2_mc_out_c3p/pwm1_mc_out_c3n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_DB7/DE/spdt_n/main_jtag_tdi/PEC_7/rf_epa_gpio[7]/ant_switch_cntl[6]/chip_clk_out[3]
36	IO12	SPI3_SS/I2S_BCLK/CANFD0_RX/I2C0_SDA/I2C2_SCL/UART_SIG0/ADC1_0/AUADC_1/SWGPIO[12]/irrx/pwm2_mc_out_c0p/pwm2_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_CSn/DBI_TypeC_CSn/data0/B0/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_12/rf_epa_gpio[4]/ant_switch_cntl[3]/epta_wl_act/epta_wl_act/gnt/chip_clk_out[0]
37	IO11	SPI2_MOSI/I2S_DO/I2S_RCLK_O/CANFD2_TX/I2C1_SCL/I2C2_SDA/UART_SIG11/ADC0_0/AUADC_0/SWGPIO[11]/irrx/pwm1_mc_out_c3p/pwm2_mc_out_c1n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_WRn/DBI_TypeC_SCL/spdt_n/main_jtag_tdi/PEC_11/rf_epa_gpio[3]/ant_switch_cntl[2]/chip_clk_out[3]
38	IO5	SPI1_SCLK/pdm_0_in/I2S_FS/CANFD2_TX/I2C0_SCL/I2C2_SDA/UART_SIG5/E1_RX_ERR/CAM0_VSYNC/ADC0_8/AUADC_7/xtal_-ext_clk_18/xtal32k_out/SWGPIO[5]/irrx/irtx/pwm2_mc_out_c1p/pwm1_mc_out_c2n/wl_jtag_tclk/wl_cjtag_tckc/ep_jtag_tclk/UART3_CTS/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_P/DBI_TypeB_DB5/DISP_QSPI_SDA3/HS/spdt_n/main_jtag_tck/main_cj-tag_tckc/PEC_5/rf_epa_gpio[5]/ant_switch_cntl[4]/epta_bl_act/chip_clk_out[1]
39	IO4	SPI1_SS/pdm_clk_o/I2S_BCLK/CANFD2_RX/I2C0_SDA/I2C2_SCL/UART_SIG4/E1_RXD[1]/CAM0_HSYNC/ADC1_7/AUADC_-6/xtal32k_in/SWGPIO[4]/irrx/irtx/pwm2_mc_out_c0p/pwm1_mc_out_c2p/wl_jtag_tms/wl_cjtag_-tmsc/ep_jtag_tms/UART3_RTS/Key_Scan_In_ROW_I/Key

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		_Scan_Drive_COL_O/DBI_TypeB_DB4/DISP_QSPI_SDA2/PCLK/spdt_p/main_jtag_tms/main_cj-tag_tmsc/PEC_4/rf_epa_gpio[4]/ant_switch_cntl[3]/epta_wl_act/gnt/chip_clk_out[0]
40	IO3	SPI0_MOSI/pdm_0_in/I2S_DO/I2S_RCLK_O/CANFD1_TX/I2C1_SCL/I2C2_SDA/UART_SIG3/E1_RXD[0]/CAM0_DATA3/vref_ext[0]/SWGPIO[3]/irrx/irtx/pwm1_mc_out_c3p/pwm1_mc_out_c1n/wl_jtag_tdi/UART3_RXD/Key_Scan_In_ROW_I/Key_Scan_Drive_COL_O/AUDAC_PWM_N/DBI_TypeB_DB3/DISP_QSPI_SDA1/DE/spdt_n/main_jtag_tdi/PEC_3/rf_epa_gpio[3]/ant_switch_cntl[2]/chip_clk_out[3]
/	RF_SW	RF switch control pin for switching between 2.4 GHz Wi-Fi and BT inside the module. It is controlled by IO16 by default and should be left floating. If a pin conflict requires the use of a different I/O configuration, please contact Ai-Thinker.

Notes:

1. For the external-Flash version, IO34, IO35, IO36, IO37, IO38, and IO39 are unavailable.

2. The module's SDIO interfaces are IO43, IO44, IO45, IO46, IO47, and IO48. Length-matched routing and impedance matching are required when using SDIO communication.

3. IO16 is assigned to the module's internal RF_SW control pin (RF switch control pin) by default. It is unavailable for other use in the default configuration and is recommended to be left unconnected. To control the internal RF_SW using another I/O, please contact Ai-Thinker. (Only even-numbered I/Os can be configured for this purpose, and the selected I/O must also be connected to the RF_SW pad on the rear of the module.)

4. Soldering the module's bottom ground pad to ground is recommended to improve interference immunity.

5. For further descriptions of pin functions, please contact Ai-Thinker.

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6 Schematic

Figure 7 shows the schematic of the Ai-M65P-32S module.

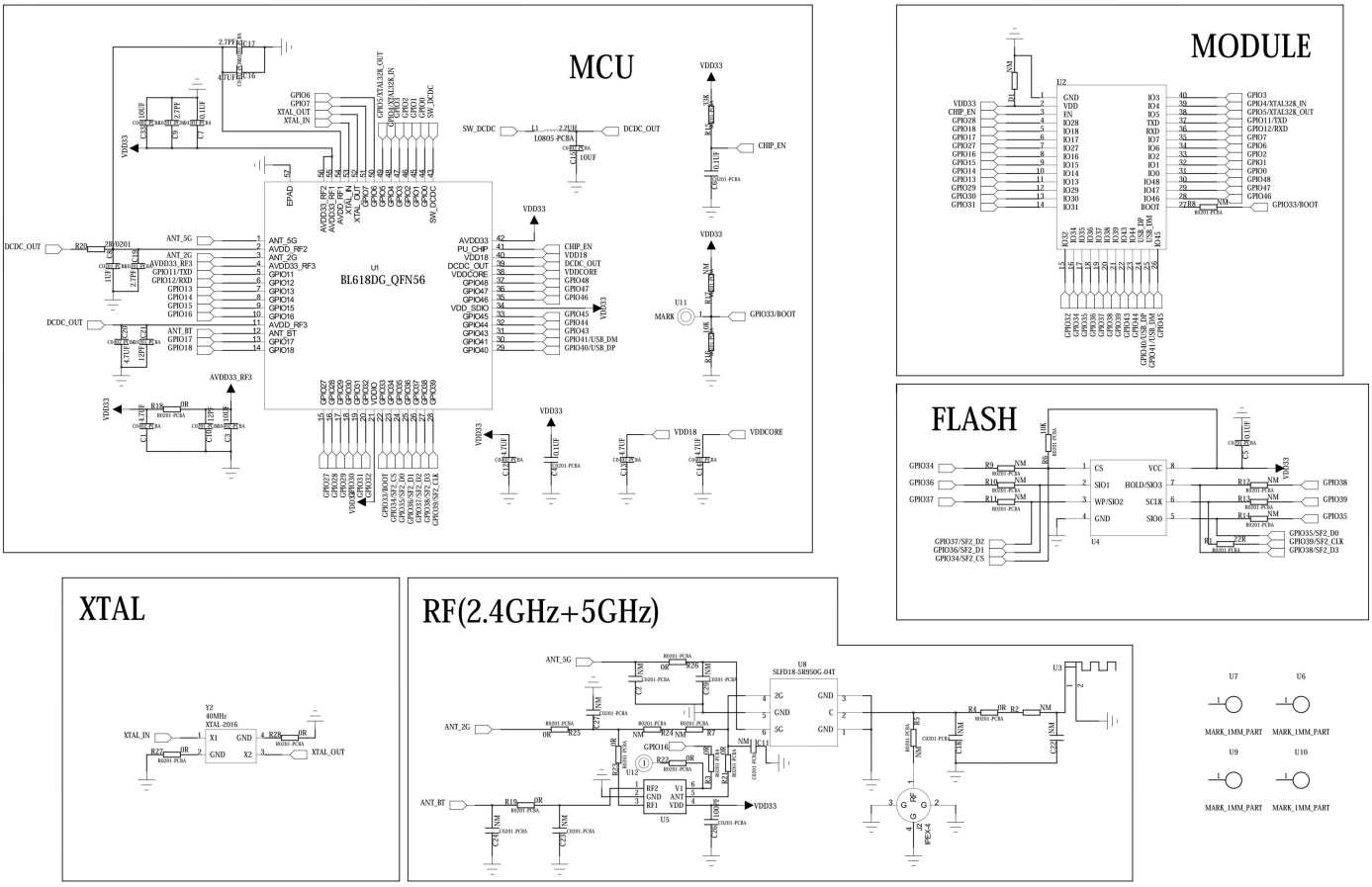


Figure 7 Schematic

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7 Antenna Parameters

7.1 Antenna Test Prototype

Figure 8 shows the antenna test prototype of the Ai-M65P-32S module.

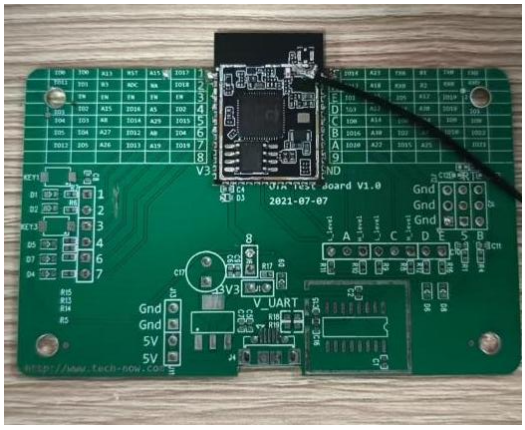


Figure 8 Antenna Test Prototype

7.2 Antenna S-Parameters

Figure 9 shows the antenna S-parameter results of the Ai-M65P-32S module measured by a network analyzer, including three RF characteristic curves: Smith chart, S11 return loss and VSWR.

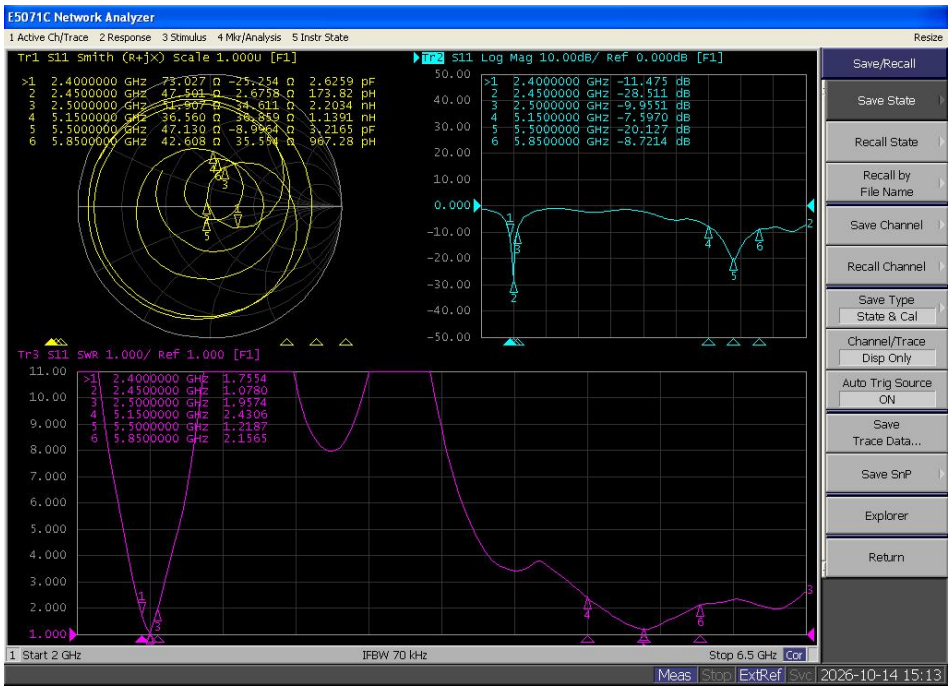


Figure 9 Antenna S-Parameters

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7.3 Antenna Gain and Efficiency

Table 9 shows the measured gain and radiation efficiency parameters of the Ai-M65P-32S module's antenna at each frequency point within the 2400 – 2500MHz and 5180 – 5850MHz operating bands.

Table 9 Antenna Gain and Efficiency

No.	1	2	3	4	5	6	7	8	9	10	11
Frequency (MHz)	2400	2410	2420	2430	2440	2450	2460	2470	2480	2490	2500
Gain (dBi)	0.46	0.80	0.73	0.55	0.26	0.29	-0.14	0.00	0.52	0.46	0.67
Efficiency (%)	43.83	45.06	44.89	46.03	44.11	43.14	42.04	43.11	43.81	41.82	43.52
Frequency (MHz)	5150	5250	5350	5450	5550	5650	5750	5850	-	-	-
Gain (dBi)	4.38	4.55	4.90	5.21	4.24	5.32	6.55	4.83	-	-	-
Efficiency (%)	63.37	68.76	62.35	71.80	62.74	69.68	65.79	65.13	-	-	-

7.4 Antenna Radiation Pattern

Figure 10 shows the 3D radiation pattern and planar cut patterns of the Ai-M65P-32S module's antenna at a typical 2.4GHz frequency point.

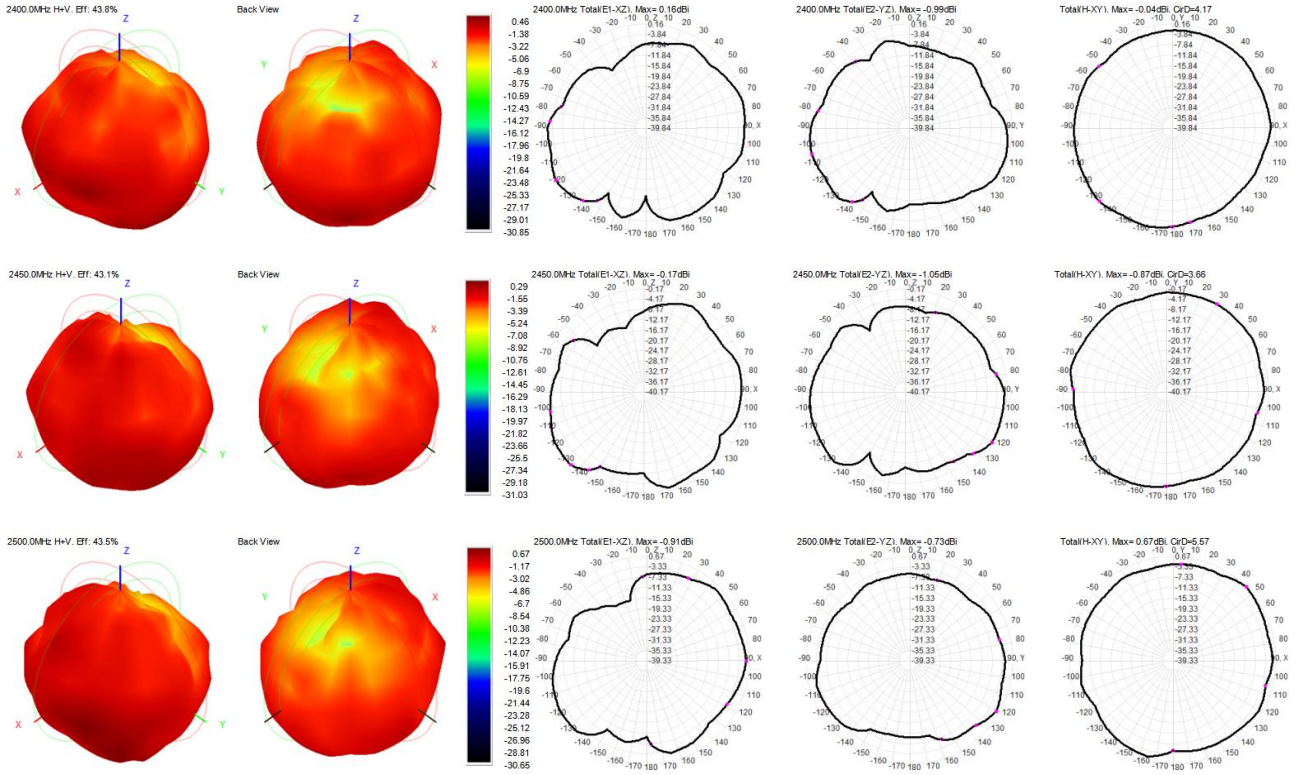


Figure 10 Antenna Radiation Pattern (2.4GHz)

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Figure 11 shows the 3D radiation pattern and planar cut patterns of the Ai-M65P-32S module's antenna at a typical 5GHz frequency point.

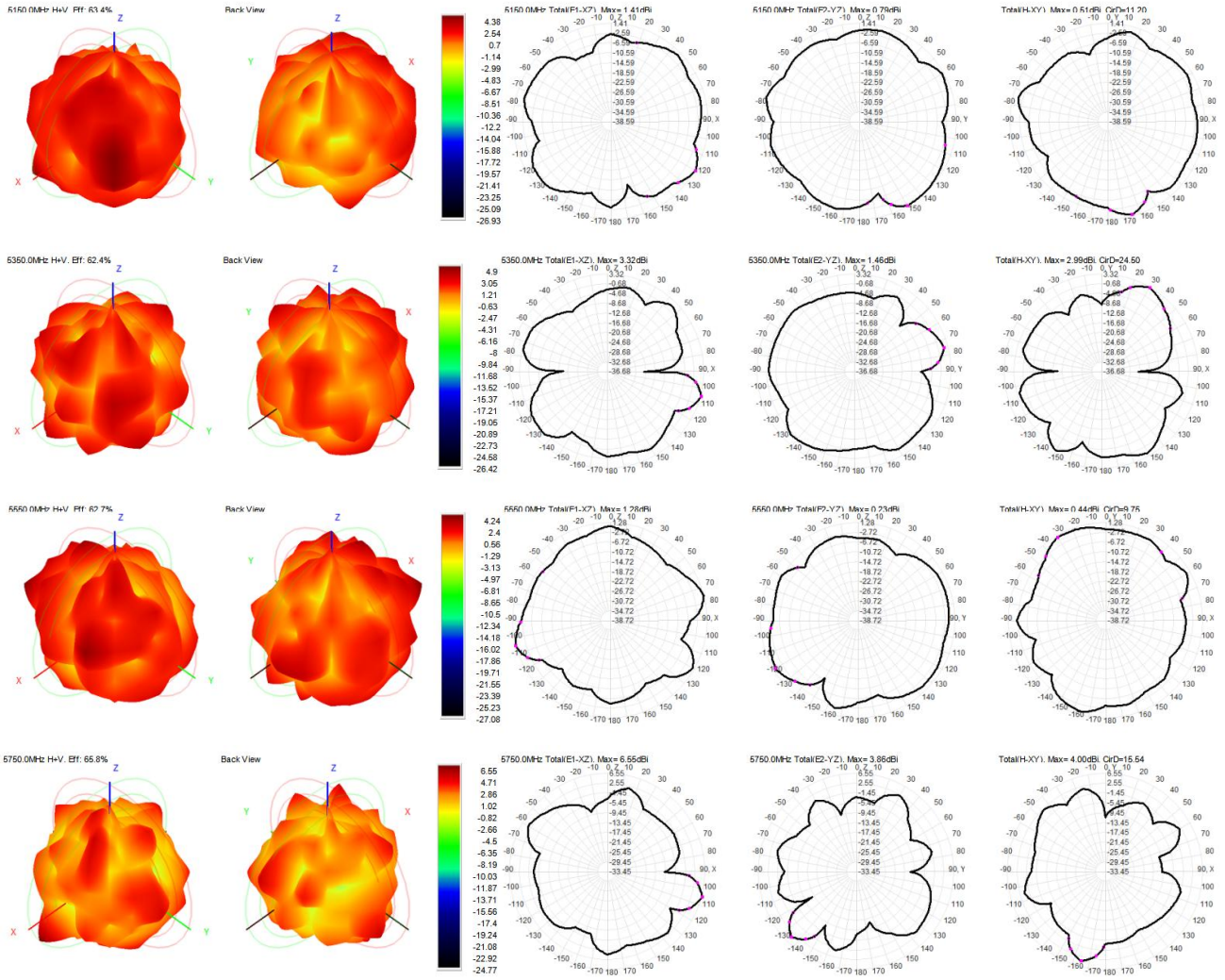


Figure 11 Antenna Radiation Pattern (5GHz)

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8 Design Guide

8.1 Application Reference Circuit

Figure 12 shows the hardware application reference circuit for the Ai-M65P-32S module, illustrating the serial communication, power supply, enable, and program download interface connections.

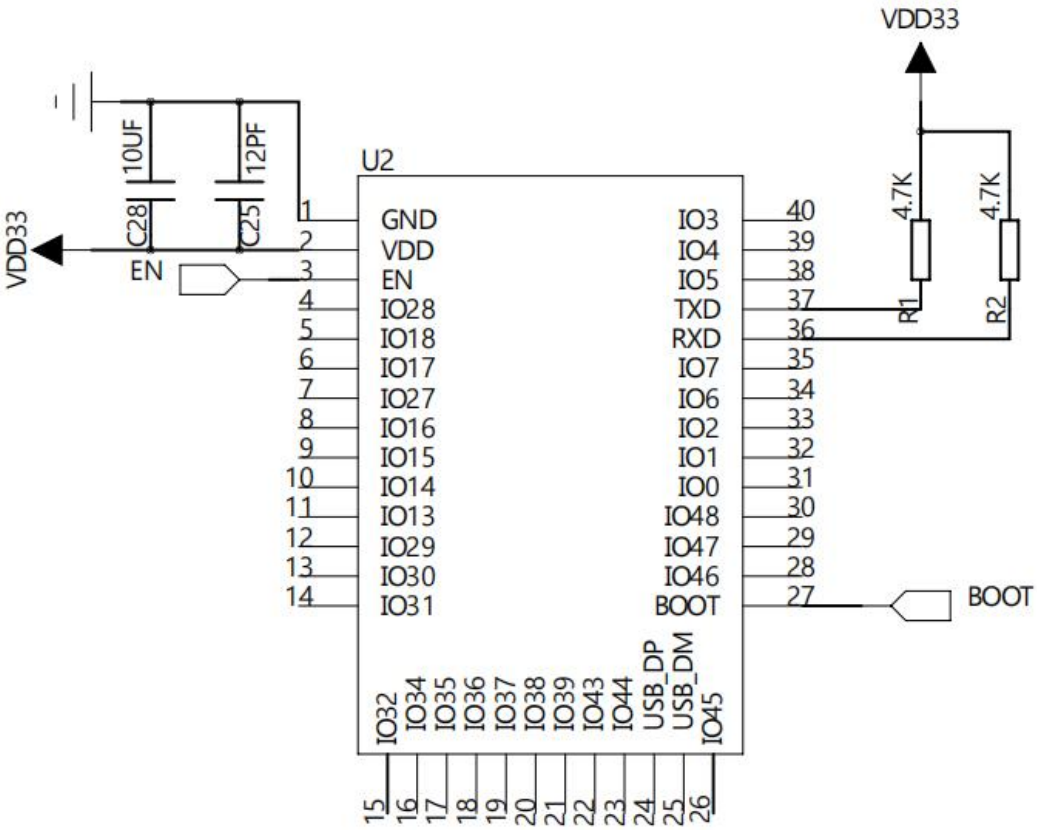


Figure 12 Application Reference Circuit

Notes on the Application Reference Circuit:

- VDD supply voltage: 2.97 – 3.63V. The external power supply output current is recommended to be above 500mA.
- The BOOT pin for all modules in this series is located on the test point on the back of the module. For module versions with marking suffix “A”, the chip’s BOOT configuration pin is exposed to the edge castellated pad, corresponding to module pin IO33. Module versions without the “A” suffix do not have this pin exposed.
- For module versions with marking suffix “A”, both IO33 (castellated pad) and the back test point pad can be used as the download BOOT pin. It is recommended to prioritize IO33 (castellated pad) as the download interface configuration pin, and it is not recommended to use this IO as a regular GPIO. If this IO must be used, the external circuit’s power-on startup timing must meet the timing requirements of the BOOT pin.

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8.2 Recommended PCB Footprint Dimensions

Figure 13 shows the recommended PCB footprint dimensions of the Ai-M65P-32S module. The pad dimensions (L × W) are 2.60 × 0.90mm. The center-to-center spacing between adjacent pads is 1.27mm.

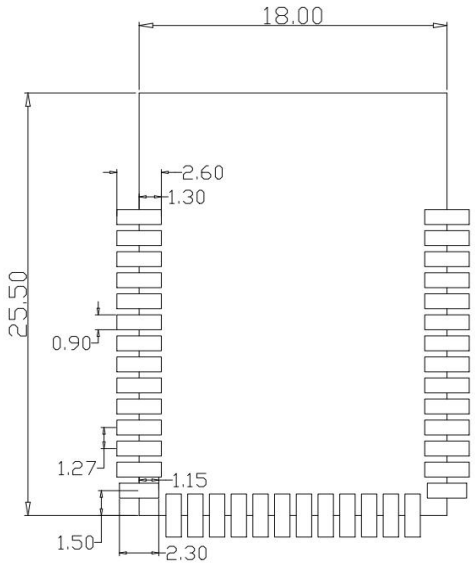


Figure 13 Recommended PCB Footprint Dimensions (Unit: mm)

8.3 Antenna Layout Requirements

Figure 14 illustrates the antenna layout. For the installation position on the mainboard, the following 2 options are recommended.

Option 1: Place the module at the mainboard edge, with the antenna area extending beyond it.

Option 2: Place the module at the mainboard edge, with a clearance cutout at the antenna position.

- To ensure optimal performance of the onboard antenna, metal objects must not be placed near the antenna, and the antenna should be kept away from high-frequency devices.

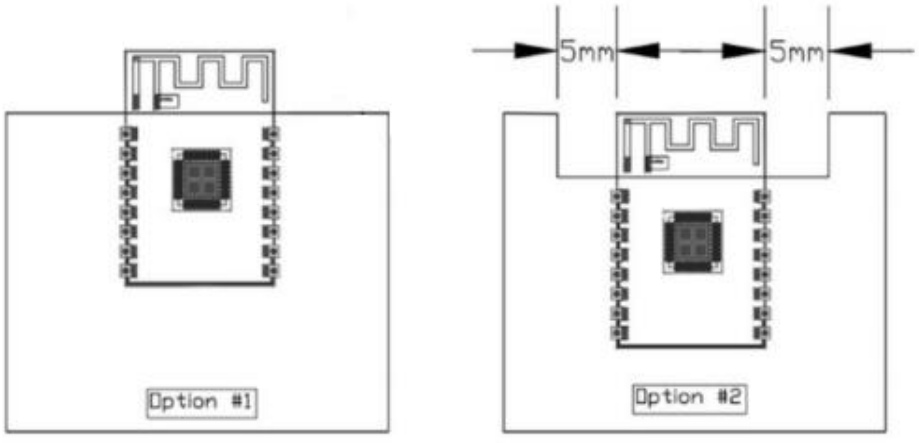


Figure 14 Antenna Layout Diagram

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8.4 Power Supply

Figure 15 shows a DC-DC buck power supply circuit converting 12V to 3.3V, with a maximum output current of 2A.

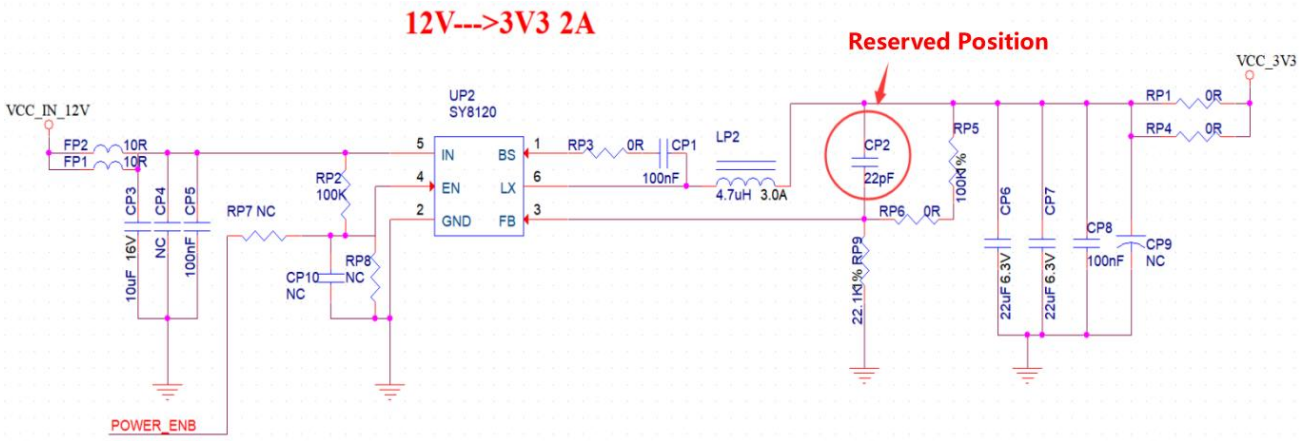


Figure 15 DC-DC Buck Circuit

Notes on the DC-DC Buck Circuit:

- Recommended VDD voltage: 3.3V; recommended current ≥ 500mA.
- An LDO is recommended for power supply; if using DC-DC, the ripple should be controlled within 30mV.
- For the DC-DC power supply circuit, it is recommended to reserve space for dynamic response capacitors to optimize output ripple under large load transients.
- It is recommended to add ESD protection devices to the power interface.

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8.5 GPIO

Figure 16 shows a 3.3V and 5V bidirectional UART level-shifting circuit, which supports bidirectional serial communication across different voltage levels.

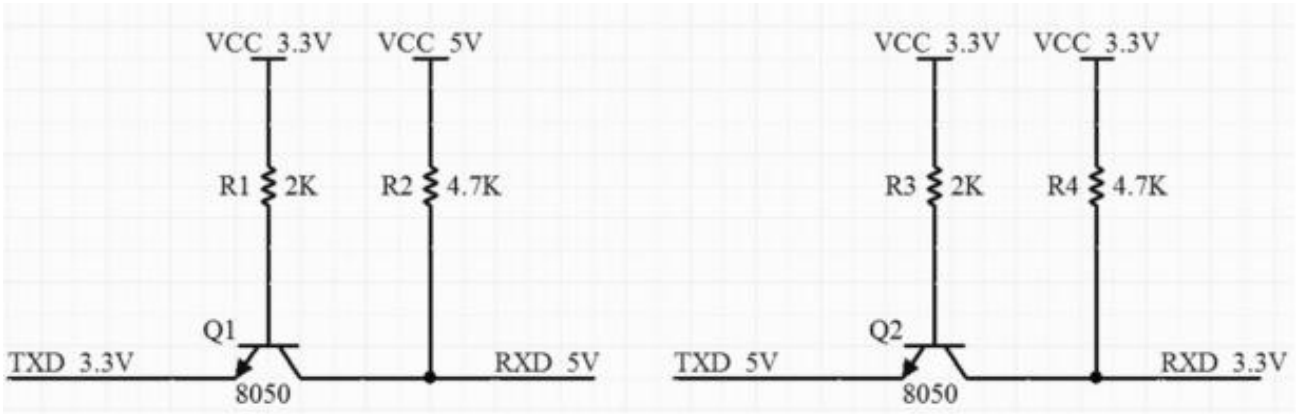


Figure 16 Level-Shifting Circuit

Notes on the Level-Shifting Circuit:

- Some I/O pins are brought out from the module. To use these I/O pins, it is recommended to connect a 10 – 100Ω resistor in series with each I/O pin. This helps suppress overshoot, stabilize signal levels, and benefits both EMI and ESD protection.
- The pull-up or pull-down configuration for special I/O pins must refer to the instructions in the specification, as it affects the module boot configuration.
- The module I/O pins level is 3.3V. If the host controller I/O voltage level does not match the module, a level-shifting circuit should be added.
- If an I/O pin is directly connected to a peripheral interface or pin headers, it is recommended to reserve space for an ESD protection device near the connector on the I/O trace.

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9 Storage Conditions

Products sealed in moisture barrier bags should be stored in a non-condensing atmosphere at < 40℃ and < 90% RH.

The moisture sensitivity level (MSL) of the module is level 3.

The module must be used within 168 hours after vacuum bag removal under conditions of 25±5℃ and 60% RH. Otherwise, the module requires baking before being returned to production.

10 Reflow Soldering Profile

Figure 17 shows the module reflow soldering process profile. The process is divided into four stages: ramp-up zone, preheat/soak zone, reflow soldering zone and cooling zone.

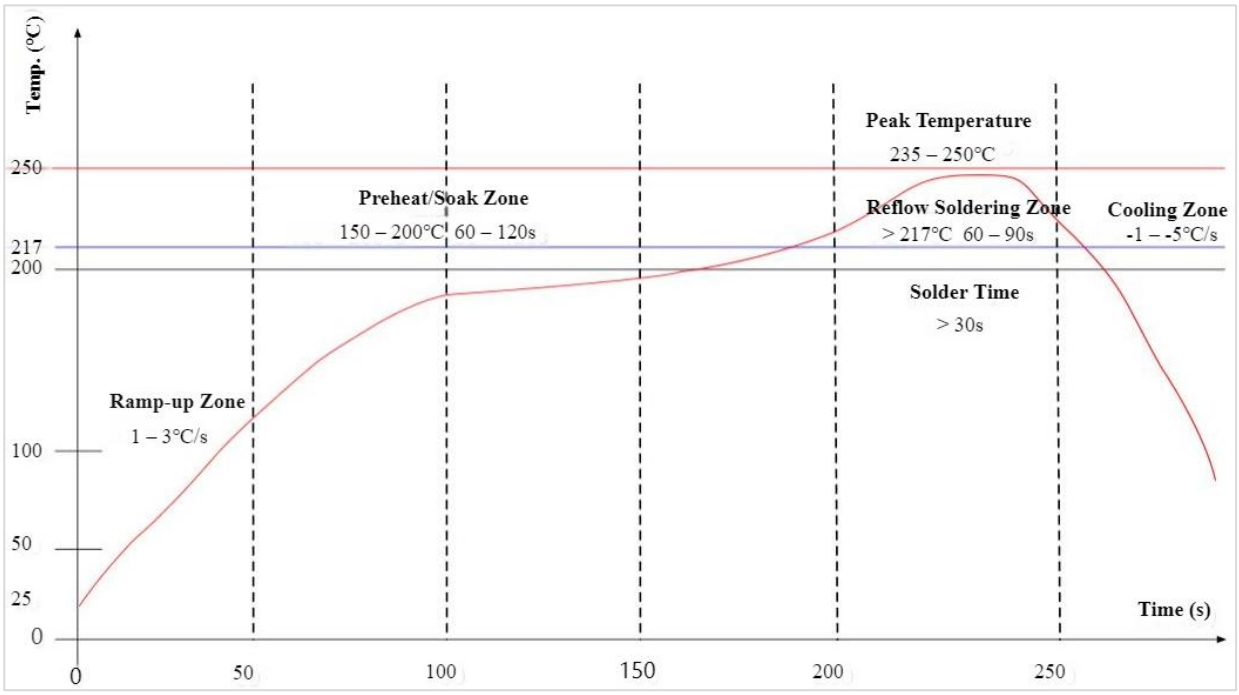


Figure 17 Reflow Soldering Profile

Reflow Soldering Profile Description:

- Ramp-up zone – Temperature: 25 – 150℃, Time: 60 – 90s, Ramp rate: 1 – 3℃/s
- Preheat/soak zone – Temperature: 150 – 200℃, Time: 60 – 120s
- Reflow soldering zone – Temperature: > 217℃, Time: 60 – 90s, Peak temperature: 235 – 250℃, Time: 30 – 70s
- Cooling zone – Temperature: peak temperature to 180℃, Cooling rate: -1 – -5℃/s
- Solder – Sn-Ag-Cu lead-free solder alloy (SAC305)

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11 Packaging Information

Figure 18 shows the packaging of the Ai-M65P-32S module. The module is packed in tape-and-reel, 800 pcs/reel.



Figure 18 Tape and Reel Packaging Diagram

12 Contact Us

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