RTL8762EMF-VS-CG

BLUETOOTH LOW ENERGY SOC

PRELIMINARY DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

ELECTROSTATIC DISCHARGE (ESD) WARNING

This product can be damaged by Electrostatic Discharge (ESD). When handling, care must be taken. Damage due to inappropriate handling is not covered by warranty.

Do not open the protective conductive packaging until you have read the following, and are at an approved anti-static workstation.

- Use an approved anti-static mat to cover your work surface
- Use a conductive wrist strap attached to a good earth ground
- Always discharge yourself by touching a grounded bare metal surface or approved anti-static mat before picking up an ESD-sensitive electronic component
- If working on a prototyping board, use a soldering iron or station that is marked as ESD-safe
- Always disconnect the microcontroller from the prototyping board when it is being worked on

REVISION HISTORY

Revision	Release Date	Summary
0.6	2022/04/28	1. Preliminary release.
0.7	2022/05/05	Modify power on sequence description.
0.8	2022/06/24	Modify feature list description.
0.9	2022/10/04	Modify feature list description.
0.91	2023/01/06	Modify Chapter 11.9 RF RX sensitivity description.

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1. General Description

1.1. *Overview*

The RTL8762EMF-VS-CG (hereinafter also called RTL8762E) is ultra-low-power system on-chip solutions for Bluetooth 5.2 low energy and 2.4GHz proprietary multi-application that combine the excellent performance of a leading RF transceiver with a low-power ARM Cortex-M0+, power management unit, ADC, and smart I/O distribution controller.

In addition, RTL8762E supports an analog MIC interface that integrates a sigma-delta ADC, programmable gain amplifier, and microphone bias circuit for voice command application. The RTL8762E also embeds an IR transceiver, hardware key-scan, and Quad-decoder on a single IC within a QFN package.

1.2. *MCU Platform*

The embedded ARM Cortex-M0+ CPU enables developers to achieve 32-bit performance at an 8-bit price point, bypassing the step to 16-bit devices. By using a single-cycle multiply option and a 2-stage pipeline, the ARM Cortex-M0+ makes program execution simple and highly efficient.

Serial Wire Debug (SWD) interface provided as part of the Debug Access Port (DAP), in conjunction with the Basic Branch Buffer (BBB). This offers a flexible and powerful mechanism for non-intrusive program code debugging. Developers can easily add breakpoints in the code and perform single-step debugging.

The RTL8762E memory architecture includes 272kByte ROM, 104kByte RAM, and with maximum 8M-bit MCM Flash.

Flash Address Space is a virtual space that is mapped to external Flash to extend the code space in XIP (eXecute In Place) mode.

2. Features

General

- Ultra-low power consumption with intelligent PMU
- Supports Bluetooth 5.2 core specification and 2.4GHz proprietary feature multi-protocol independently
- Supports 2Mbps LE
- LE advertising Extensions
- LE Long Range
- Additional Adv channel
- Channel Selection #2
- High Duty Cycle Non-Connectable Adv
- Integrated MCU to execute Bluetooth protocol stack
- Supports multiple level Low Energy states
- Supports LE L2CAP Connection Oriented Channel Support
- Supports LE low duty directed advertising
- Supports LE data length extension feature
- Supports OTA (Over-the-Air) programming mechanism for firmware upgrade
- Supports GAP, ATT/GATT, SMP, L2CAP
- Generic Applications for GAP Central, Peripheral, Observer and Broadcaster Roles
- Supports True Random Number Generator (TRNG)
- Supports AES128 and AES256 feature

Platform

- ARM Cortex-M0+ CPU (Maximum 40MHz)
- Serial flash controller with 8kB 4-way cache
- Total 104kB SRAM, 272kB ROM
- 64B EFuse for manufacturer use
- Embedded MCM 8Mb flash

Bluetooth Transceiver

- RX sensitivity: -97dBm BLE1M (minimum)
- TX power: +7.5dBm (maximum)
- Fast AGC control to improve receiving dynamic range
- Supports Bluetooth Low Energy PHY

Peripheral Interfaces

- Flexible general purpose IOs: 26 (maximum)
- Hardware key-scan and quad-decoder
- Embedded IR transceiver
- Real-time counters (RTC)
- Supports generic 4-wire SPI master/slave
- Supports external 4-channel low power comparator
- Supports external 2-channel capacitive sensor inputs
- 400ksps, 10-bit, 4-channel AUXADC
- Timers x 8
- I2C x 2
- PWM x 8
- UART x 2
- I2S/PCM interface for external audio codec
- Supports one DMIC (PDM mono)
- Supports external 40MHz XTAL without capacitor (in limited condition)

- Support embedded internal 32kHz RCOSC to keep BLE link (in limited condition)

Package

- RTL8762EMF-VS-CG: 40-pin 5x5mm^2 QFN, internal MCM with 8Mb Flash

3. Applications

- Mesh Product

4. System & Power Block Diagrams

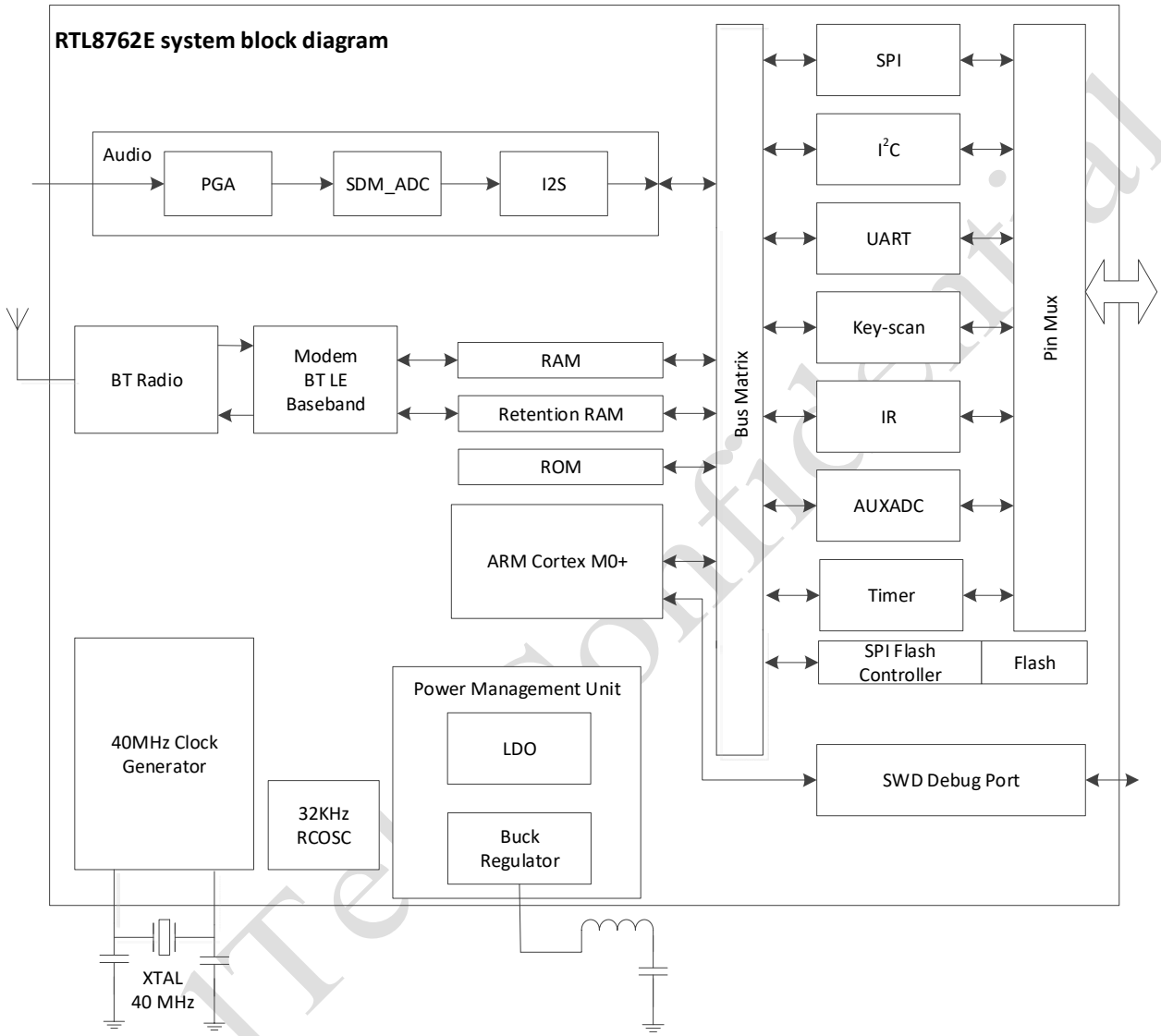

Figure 1. System Block Diagram

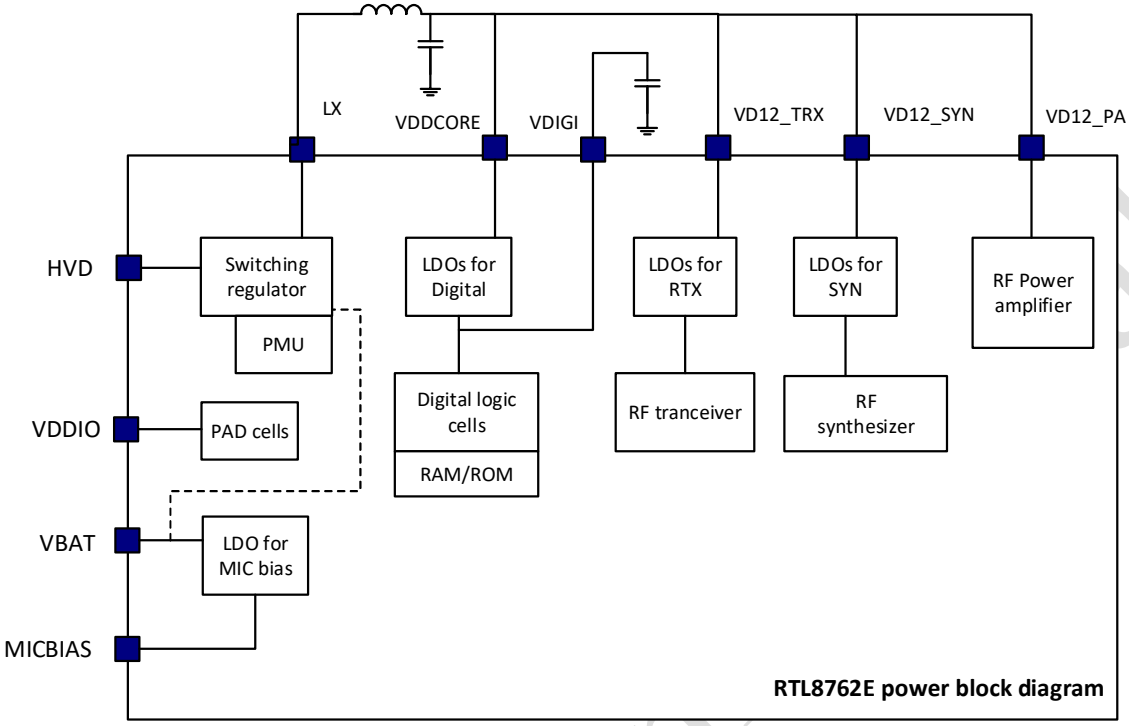

Figure 2. Power Block Diagram

4.1. *Power on Sequence-SWR Mode*

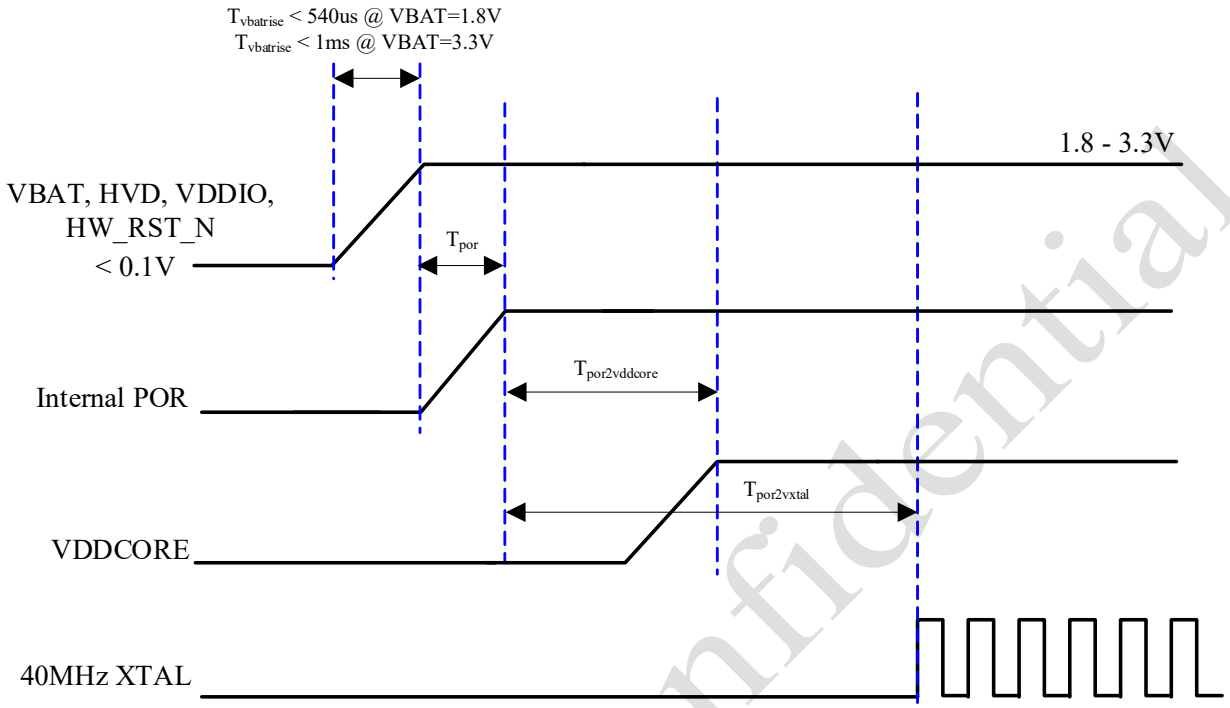

Figure 3. Power on Sequence-SWR Mode

Table 1. Power on Sequence Timing-SWR Mode

Parameter	Minimum	Typical	Maximum	Unit
T_{por}	-	0.2	0.5	ms
$T_{por2vddcore}$	-	20	40	ms
$T_{por2vxtal}$	-	40	80	ms

***Note:**

1. HW_RST_N power on time should be equal or slower than VBAT/HVD/VDDIO.
2. When booting, the initial voltage of VBAT/VDDIO/HVD would be less than 0.1V.

5. Pin Assignments

5.1. *RTL8762EMF-VS-CG Pin Assignments*

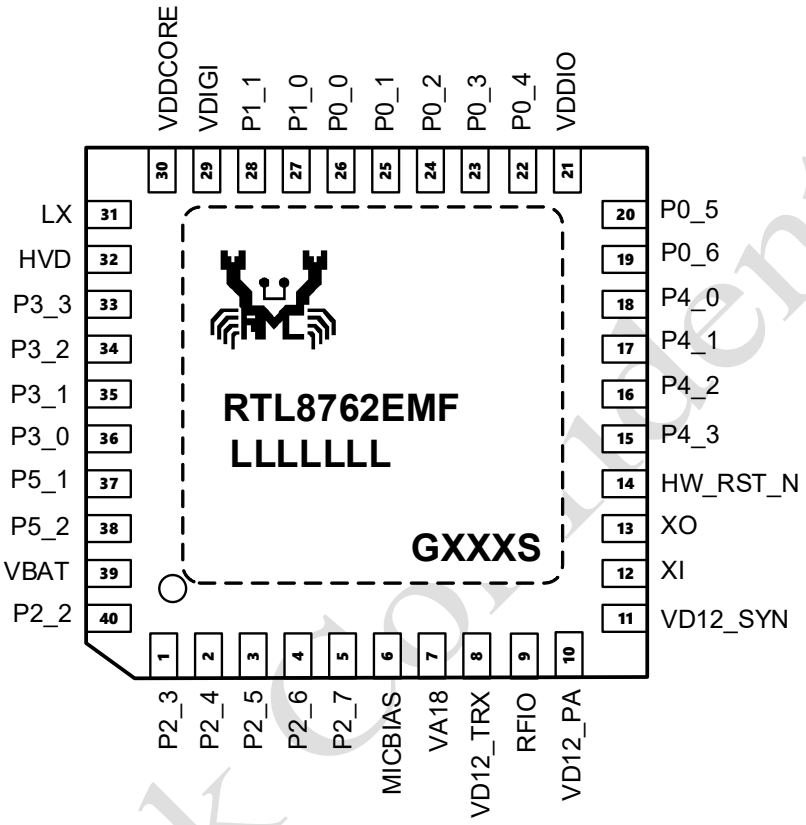

Figure 4. RTL8762EMF-VS-CG Pin Assignments

5.2. *Package Identification*

Green package is indicated by the 'G' in GXXXV (Figure 4).

6. Pin Descriptions

The following signal type codes are used in the tables:

I: Input O: Output

P: Power A: Analog

6.1. *RF Interface*

Table 2. RF Interface

Symbol	Type	Pin Number	Description
-	-	EMF-VS	-
RFIO	A	9	BT RX / BT TX interface.

6.2. *XTAL and System Interface*

Table 3. XTAL and System Interface

Symbol	Type	Pin Number	Description
-	-	EMF-VS	-
XI	A	12	40MHz crystal input.
XO	A	13	40MHz crystal output or external 40MHz clock input.
HW_RST_N	I	14	Hardware reset pin, low active.

6.3. *General Purpose IOs*

Table 4. General Purpose IOs

Symbol	Type	Pin Number	Description
-	-	EMF-VS	-
P0_0	IO	26	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_1	IO	25	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_2	IO	24	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.

Symbol	Type	Pin Number	Description
-	-	EMF-VS	-
P0_3	IO	23	LOG_UART TX. Power on trap: Pull-up for normal operation Pull-down to bypass executing program code in flash (PAD internal pull-up by default).
P0_4	IO	22	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_5	IO	20	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P0_6	IO	19	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P1_0	IO	27	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. SWDIO (default).
P1_1	IO	28	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. SWDCLK (default).
P2_2	IO	40	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 0. Capacitive sensor input 0.
P2_3	IO	1	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 1. Capacitive sensor input 1.
P2_4	IO	2	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P2_5	IO	3	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.

Symbol	Type	Pin Number	Description
-	-	EMF-VS	-
P2_6	IO	4	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 2. Analog MIC input_N. (RTL8762ESF-CG QFN24 can't support)
P2_7	IO	5	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. AUXADC input 3. Analog MIC input_P. (RTL8762ESF-CG QFN24 can't support)
P3_0	IO	36	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. HCI_UART_TX (default).
P3_1	IO	35	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down. HCI_UART_RX (default).
P3_2	IO	34	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P3_3	IO	33	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_0	IO	18	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_1	IO	17	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_2	IO	16	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P4_3	IO	15	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.

Symbol	Type	Pin Number	Description
-	-	EMF-VS	-
P5_1	IO	37	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.
P5_2	IO	38	General purpose IO, refer to Table 8 Pin Multiplexer, page 19. 8mA driving capability. With wakeup function. With internal strong/weak pull-up and pull-down.

6.4. *Power Pins*

Table 5. Power Pins

Symbol	Type	Pin Number	Description
		EMF-VS	
VA18	P	7	ADC reference voltage (decouple).
VD12_TRX	P	8	Supply 1.2V power for RF transceiver.
VD12_PA	P	10	Supply 1.2V power for PA.
VD12_SYN	P	11	Supply 1.2V power for synthesizer.
VDDIO	P	21	Supply 1.8V~3.3V power for digital IO PADs.
VDDCORE	P	30	Supply 1.2V power to LDO for digital core.
VDIGI	P	29	1.0V digital power decouple.
HVD	P	32	Supply 1.8V~3.3V power for Switching regulator input.
LX	P	31	Switching regulator output.
VBAT	P	39	Battery voltage input.
P5_0	P	6	Microphone bias. Pin share as GPIO when microphone bias is not used.

7. Bluetooth/2.4GHz Radio

7.1. *RF Transceiver*

The RTL8762E includes an embedded GFSK RF transceiver with ultra-low power consumption, and is fully compatible with the Bluetooth low energy wireless system, and can be flexibly applied to developing proprietary 2.4GHz wireless communication protocol. The block diagram is shown in Figure 5.

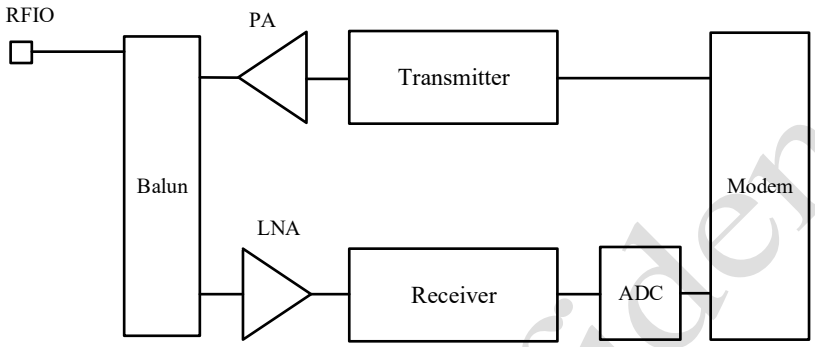

Figure 5. RF Transceiver Block Diagram

7.2. *Modem*

In the transmit path, the modem combines with the RF transmitter to generate a GFSK signal. In the receiver path, the modem receives a baseband GFSK signal from an analog to digital converter (ADC), and decodes the bit data via channel filtering, synchronizing, and demodulating.

An RF automatic calibration scheme is implemented in the modem to compensate for transistor characteristic variations in the CMOS process, and for ambient temperature differences.

7.3. *Transmitter*

The transmitter convert baseband signals to 2.4GHz unlicensed Industrial, Scientific and Medical (ISM) band GFSK modulated signals. The up-converted GFSK signal is amplified by the integrated power amplifier.

7.4. *Front-End*

To minimize external BOM requirements, the RTL8762E is single-ended RF mode and TX/RX path sharing the same RFIO pin with an integrated Balun. For antenna matching and harmonic signal reduction, a PI matching network is required in the RF path.

7.5. *2.4GHz Proprietary*

The supported 2.4GHz proprietary features of the module are listed as follow:

- Frequency band: 2348MHz~2530MHz, 1MHz step
- Modulation: 1Mbps/2Mbps GFSK
- Coding: whitening, CRC
- Configurable packet format
- Roles: proprietary TX (PTX), proprietary RX (PRX)
- Modes: one-shot/continuous PRX, one-shot/periodic/GPIO triggered PTX, auto acknowledge (ACK)
- DMA data transfer
- Power Spectrum Detection (PSD)

8. Clock Management

For optimal power consumption and performance, the RTL8762E offers high and low frequency clocks. The high frequency clock is generated by an external 40MHz crystal oscillator (XTAL). The low frequency clock is generated by a 32kHz RCOSC.

In normal mode the high frequency clock is kept running to provide clock to the CPU, Bluetooth core, and the peripheral block. In low power mode the high frequency clock is turned off for power saving. The 32kHz low frequency clock remains on to provide clock to the RTC (Real Time Counter), BT core, and PMU.

8.1. *40MHz XTAL Oscillator*

The RTL8762E has a built-in 40MHz crystal oscillation circuit to provide a stable, controllable system clock. With the help of the internal built-in capacitor, the clock offset could be fine-tuned in the mass production process. The maximum internal cap is 20pF typically, and it is suggested to follow Realtek crystal design specification and QVL, the external capacitor, C_1 and C_2, could be replaced by an internal capacitor, reducing the BOM cost, minimizing the PCB dimensions, and adding flexibility for clock fine tuning.

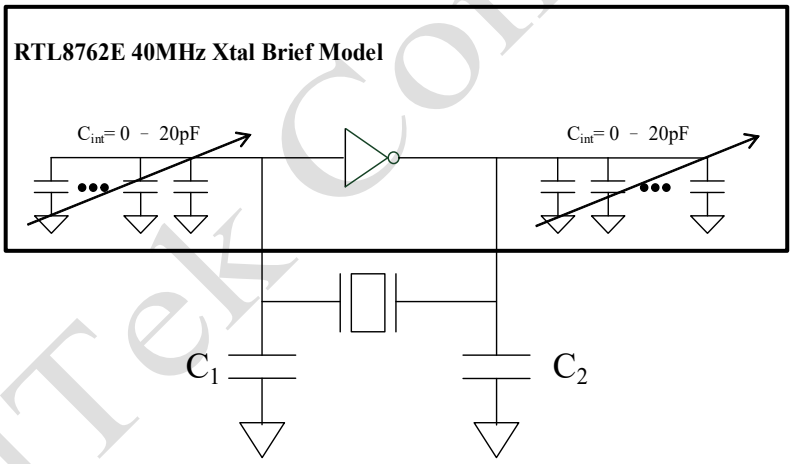

Figure 6. 40MHz Crystal Oscillation Schematic

Example:

For a crystal with spec C_L=9pF

C_L= [(C_1 x C_2) / (C_1+C_2)] + (C_{int} / 2) + $C_{parasitic}$, the parasitic capacitor $C_{parasitic}$ could be observed on the PCB trace and IC SMT soldering pad….etc.

As a rule of thumb, "C_1 + C_{int}" is typically 12~15pF, hence the external capacitor C_1 and C_2 can possibly be replaced by the internal capacitor C_{int}, which could be 20pF at the maximum setting to cover the need for external capacitors.

Table 6. 40MHz XTAL Specification

Parameter	Minimum	Typical	Maximum
Frequency (MHz)	-	40	-
Frequency tolerance (ppm)	-	-	±10
Frequency stability (ppm)	-	-	±10
Load capacitance (pF)	7	9	-
Maximum Drive Level (μW)	100 @ C_L=7/9pF	-	-
Equivalent Series Resistance (Ohm)	-	-	50Ω@7pF 40Ω@9pF
Shunt Capacitance (pF)	-	-	2
Insulation Resistance (MOhm)	500	-	-

***Note:** Total tolerance is ±20 ppm.

8.2. *Internal 32kHz RC Oscillator*

The RTL8762E has a built-in internal 32kHz RCOSC used as a low speed clock source. With a run-time self-calibration algorithm and limited user environment, and temperature variation of less than 1°C per second, the BLE link could be maintained via the internal 32kHz RC Oscillator.

9. Power Management Unit (PMU)

The RTL8762E is supplied with 1.8V to 3.3V by a single power source. For more flexibility of peripheral usage, IO voltage (VDDIO) can be different from VBAT (but VDDIO should be less than or equal to VBAT). There is a high-efficiency BUCK regulator to provide power to the digital core circuit and radio circuit.

The RTL8762E defines three PMU power states for various conditions.

Active Mode: All clock and power is turned on. All functions operate in this mode.

Deep LPS Mode: High-speed clock and core domain power is turned off. The CPU stops running. Data can be retained in retention SRAM.

Power Down Mode: Except in an 'always-on' power domain, all clock sources and power are turned off. Power down mode can only be woken by GPIO pins.

10. Peripheral Interface Descriptions

The RTL8762E series peripheral descriptions are shown in the table below.

Table 7. Peripheral Interface Descriptions

Physical Address	IP Function
0x4000_0000 - 0x4000_0FFF	SYS Control
0x4000_1000 - 0x4000_17FF	GPIO
0x4000_2000 - 0x4000_2FFF	Timer
0x4001_3000 - 0x4001_37FF	IR RC
0x4000_4000 - 0x4000_47FF	Quad Decoder
0x4000_5000 - 0x4000_57FF	Key Scan
0x4000_8000 - 0x4000_8FFF	Enhanced Timer
0x4000_9000 - 0x4000_97FF	Cap Touch
0x4001_0000 - 0x4001_0FFF	AUXADC
0x4001_1000 - 0x4001_13FF	UART_0
0x4001_2000 - 0x4001_23FF	UART_1
0x4001_3000 - 0x4001_33FF	SPI_0
0x4001_3400 - 0x4001_37FF	SPI_1
0x4001_4000 - 0x4001_4FFF	AES engine
0x4001_5000 - 0x4001_53FF	I2C_0
0x4001_5400 - 0x4001_57FF	I2C_1
0x4002_9000 - 0x4002_9FFF	I2S_0
0x4004_0000-0x4004_03FF	SPI0_HS
0x4008_0000-0x4008_3FFF	SPIC0

10.1. *Pin Multiplexer*

All GPIO pins in the RTL8762E are configurable via the built-in pin multiplexer (PINMUX). Table 8 shows all GPIO pin configurations. Figure 7 shows the PINMUX and GPIO PADs control path. In the RTL8762E, all pins have an internal pull-up and pull-down resistor for controlling GPIO_PU and GPIO_PD.

Table 8. Pin Multiplexer (PINMUX)

0	IDEL	25	qdec_phase_a_z	50	SPI0_CLK (master only)	75	KEY_COL_17	100	SDI (CODEC - slave)	125	ADCDAT (SPORT0)
1		26	qdec_phase_b_z	51	SPI0_MO (master only)	76	KEY_COL_18	101	SDO (CODEC - slave)	126	DACDAT (SPORT0)
2		27		52	SPI0_MI (master only)	77	KEY_COL_19	102		127	MCLK
3		28		53	SPI2W_DATA (master only)	78	KEY_ROW_0	103			
4		29	UART1_TX	54	SPI2W_CLK (master only)	79	KEY_ROW_1	104			
5	I2C0_CLK	30	UART1_RX	55	SPI2W_CS (master only)	80	KEY_ROW_2	105			
6	I2C0_DAT	31	UART1_CTS	56	SWD_CLK	81	KEY_ROW_3	106	BT_COEX_I_0		
7	I2C1_CLK	32	UART1_RTS	57	SWD_DIO	82	KEY_ROW_4	107	BT_COEX_I_1		
8	I2C1_DAT	33	IRDA_TX	58	KEY_COL_0	83	KEY_ROW_5	108	BT_COEX_I_2		
9	PWM2_P	34	IRDA_RX	59	KEY_COL_1	84	KEY_ROW_6	109	BT_COEX_I_3		
10	PWM2_N	35	UART0_TX	60	KEY_COL_2	85	KEY_ROW_7	110	BT_COEX_O_0		
11	ENPWM0_P	36	UART0_RX	61	KEY_COL_3	86	KEY_ROW_8	111	BT_COEX_O_1		
12	ENPWM0_N	37	UART0_CTS	62	KEY_COL_4	87	KEY_ROW_9	112	BT_COEX_O_2		
13	PWM0	38	UART0_RTS	63	KEY_COL_5	88	KEY_ROW_10	113	BT_COEX_O_3		
14	PWM1	39	SPI1_SS_N_0 (master only)	64	KEY_COL_6	89	KEY_ROW_11	114	PTA_I2C_CLK (slave only)		
15	PWM2	40	SPI1_SS_N_1 (master only)	65	KEY_COL_7	90	DWGPIO	115	PTA_I2C_DAT (slave only)		
16	PWM3	41	SPI1_SS_N_2 (master only)	66	KEY_COL_8	91		116	PTA_I2C_INT_OUT		
17	PWM4	42	SPI1_CLK (master only)	67	KEY_COL_9	92		117	EN_EXPA		
18	PWM5	43	SPI1_MO (master only)	68	KEY_COL_10	93		118	EN_EXLNA		
19	ENPWM0	44	SPI1_MI (master only)	69	KEY_COL_11	94		119	ANT_SW0		
20	ENPWM1	45	SPI0_SS_N_0 (slave)	70	KEY_COL_12	95		120	ANT_SW1		
21	qdec_phase_a_x	46	SPI0_CLK (slave)	71	KEY_COL_13	96	DMIC1_CLK	121	ANT_SW2		
22	qdec_phase_b_x	47	SPI0_SO (slave)	72	KEY_COL_14	97	DMIC1_DAT	122	ANT_SW3		
23	qdec_phase_a_y	48	SPI0_SI (slave)	73	KEY_COL_15	98	LRC_I (CODEC - slave)	123	LRC (SPORT0)		
24	qdec_phase_b_y	49	SPI0_SS_N_0 (master only)	74	KEY_COL_16	99	BCLK_I (CODEC - slave)	124	BCLK (SPORT0)		

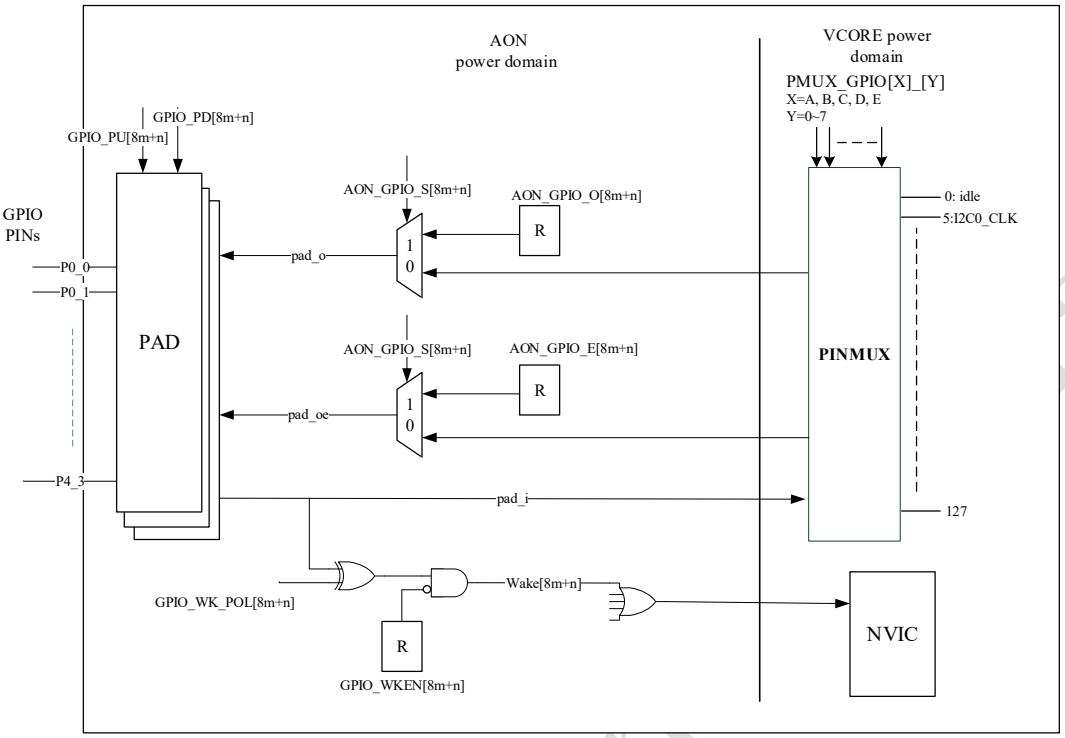

Figure 7. PINMUX and GPIO PADs Control Path

10.2. *Real-Time Counter (RTC)*

There are 32-bits counters with four individual comparators. The counter is clocked by an internal 32kHz RCOSC with 12-bit pre-scalar. The comparators output can interrupt the CPU and wake up the chip from DLPS mode. The RTC block diagram is shown below.

Features:

- 12-bits pre-scale counter
- 32-bits read only RTC counter
- Internal 32kHz RCOSC clock resource
- 4 independent comparators (with interrupt)
- 1 tick interrupt
- RTC counter overflow interrupt

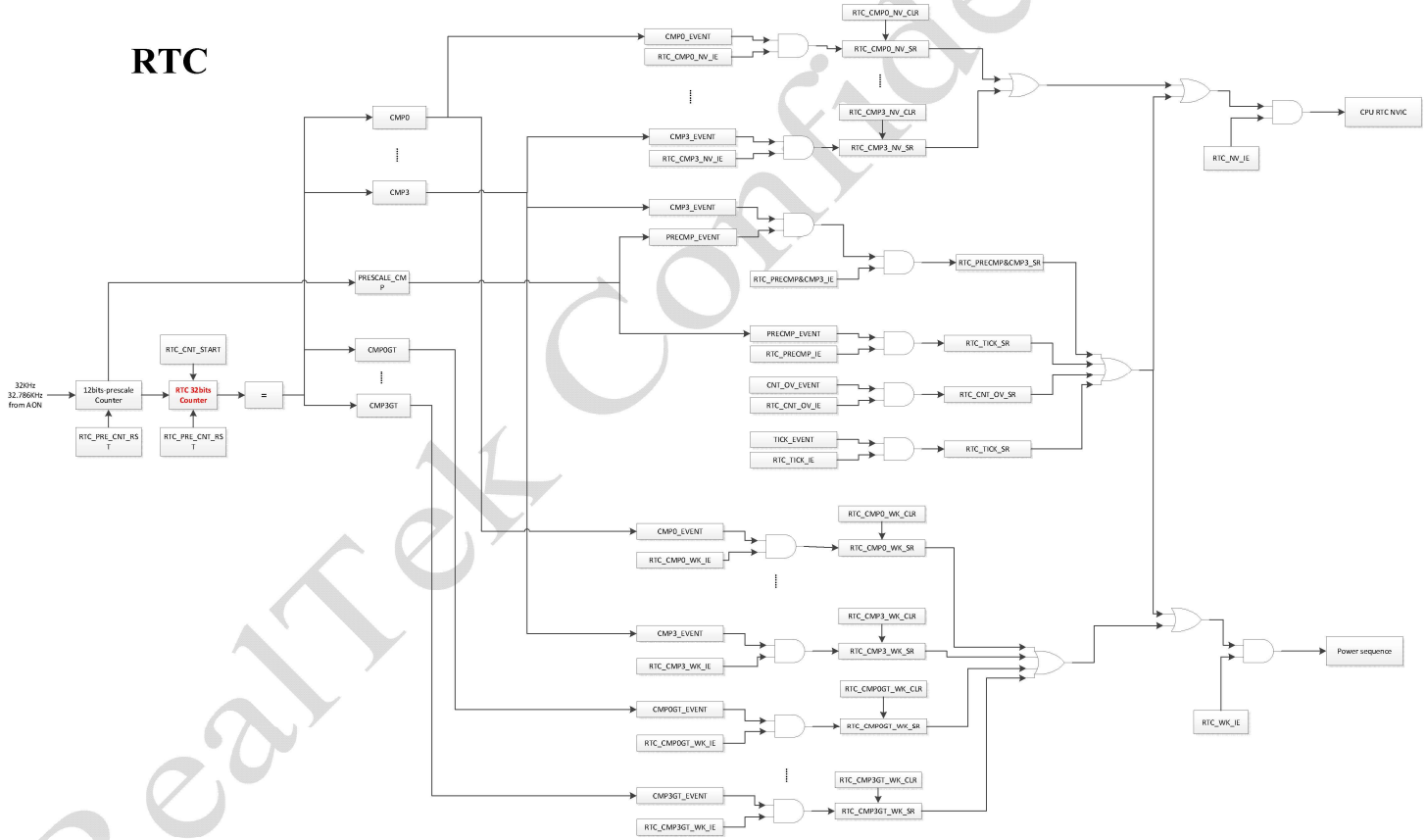

Figure 8. RTC Block Diagram

10.3. *PWM/Hardware Timer (TIM)*

The RTL8762E supports eight PWM/TIM modules.

Features:

- 6 independent Timers (2 Timers are dedicated for Internal usage)
- Timer clock source 40MHz clock
- 3 mode (free run/user define/PWM)
- 32bits counter
- Complementary PWM output & Dead zone (only Timer2, Timer3)
- PWM output state read back (<100kHz)

Table 9. Hardware Timer (Base Address: 0x4000_2000)

Address Range (Base +)	Function
0x00 to 0x10	Timer 0 Registers
0x14 to 0x24	Timer 1 Registers
0x28 to 0x38	Timer 2 Registers
0x3c to 0x4c	Timer 3 Registers
0x50 to 0x60	Timer 4 Registers
0x64 to 0x74	Timer 5 Registers
0xb0 to 0xcc	TimerNLoadCount2 Registers

10.4. *Enhance Timer (ENTIM)*

The RTL8762E supports two Enhance timer channel.

Features:

- 2 independent timers
- Timer clock source 40MHz clock
- 3 mode (free run/User-define PWM auto/manual)
- 32bits counter
- 2 mode counting methods (increase for free run/decrease for User-define PWM auto/manual)
- Optional PWM output initial polarity: High/Low
- Support all (100%) high/low PWM output
- Complementary PWM output & Dead zone (only Enhance timer0)
- 3 trigger (GPIO/ LE Slave role Acc_hit/ LE Master role Tx_on) mode latch current counter value
- Latch FIFO Depth: 4

10.5. *GPIO Control*

The RTL8762E provides a highly flexible GPIO module for developers. There are 32 GPIOs assigned to IO PADs. The mapping table is shown in Table 10. The GPIO function could be assigned to the IO PAD via the pin mux register.

Features:

- 32 GPIOs
- Input/output function
- 32 Independence interrupts
- 3 interrupt trigger conditions (level/edge/dual-edge)
- Hardware interrupt de-bounce

Table 10. GPIO Mapping Table

Pin Name	DW GPIO	Pin Name	DW GPIO	Pin Name	DW GPIO	Pin Name	DW GPIO	Pin Name	DW GPIO
P0_0	GPIO[0]	P1_0	GPIO[8]	P2_0	GPIO[16]	P3_0	GPIO[24]	P4_0	GPIO[13]
P0_1	GPIO[1]	P1_1	GPIO[9]	P2_1	GPIO[17]	P3_1	GPIO[25]	P4_1	GPIO[29]
P0_2	GPIO[2]	P1_6	GPIO[14]	P2_2	GPIO[18]	P3_2	GPIO[26]	P4_2	GPIO[30]
P0_3	GPIO[3]	P1_7	GPIO[15]	P2_3	GPIO[19]	P3_3	GPIO[27]	P4_3	GPIO[31]
P0_4	GPIO[4]	-	-	P2_4	GPIO[20]	P3_4	GPIO[28]	MICBIAS	GPIO[10]
P0_5	GPIO[5]	-	-	P2_5	GPIO[21]	P3_5	GPIO[29]	P5_1	GPIO[11]
P0_6	GPIO[6]	-	-	P2_6	GPIO[22]	P3_6	GPIO[30]	P5_2	GPIO[12]
P0_7	GPIO[7]	-	-	P2_7	GPIO[23]	-	-	-	-

10.6. *Quadrature Decoder*

A three axis (X, Y, and Z-axis) quadrature decoder is built into the RTL8762E, including a smart interrupt mechanism to reduce firmware loading. The RTL8762E embeds the input de-bounce circuitry with the programmable timer.

Features:

- 2 input quadrature decoder
- 3 independent axis (X,Y, Z)
- Hardware de-bounce timer
- Configurable sample rate
- 16bits-counter
- Underflow/overflow interrupt

10.7. *Hardware Key Scan*

The RTL8762E supports a Configurable 12 rows * 20 columns key matrix with key scan engine. Each IO PAD could be configured as any row or column pin of Key Scan to reduce complexity of PCB routing.

Features:

- Configurable matrix, max matrix (12 rows * 20 columns)
- Configurable matrix scan clock（10kHz-128kHz, frequency must be 5MHz/N. N: integer）
- Configurable de-bounce time
- Configurable scan interval time
- Configurable all-key release
- 26 depth Key FIFO
- Key filter (one key)

- scan clock= system clock(5MHz)/(SCAN_DIV+1), SCAN_DIV 11bits
- delay clock= scan clock/(DELAY_DIV+1), DELAY_DIV 6bits
- debounce time= (1~2^9)*(1/delay clock)
- scan interval time= (1~2^9)*(1/delay clock)
- release time = (1~2^9)*(1/delay clock)

10.8. *IR Controller*

The IR module provides a flexible way of transmitting and receiving IR code used in remote controls. It can both send and receive IR waveforms within IR carriers.

IR Transmitter Feature:

- Clock source: IR_CLK =40MHz
- Programmable IR carrier frequency=IR_CLK /N. (N: integer) (frequency range:5kHz-2MHz)
- Programmable IR carrier cycle high/low period (step:1/IR clock)
- Programmable IR carrier cycle number (above 1000)
- Hardware output waveform control
- TX FIFO Depth: 32

IR Receiver Feature:

- Programmable sample clock
- Automatic/manual trigger mode
- Hardware waveform sample (not interfered with by software tasks)
- RX FIFO Depth: 32

10.9. *SPI*

There are two individual SPI interfaces in the RTL8762E. SPI0 supports master and slave mode. SPI1 supports master mode only.

SPI0 Master Features:

- Supports Clock Mode 0-3 (CPOL, CPHA)
- 4 transmit mode: TX only, RX only, Full-duplex, EEPROM
- SPI0 source clock (40MHz)
- SPI0 SPI_CLK frequency = (SPI0 source clock)/N, N is any even value between 2 and 65534.
- Supports 4 to 32bits data frame
- 3 Hardware CS
- TX FIFO width 32bits, depth 16
- RX FIFO width 32bits, depth 16
- DMA transfer supported

SPI0 Slave Features:

- Support Mode 0-3 (CPOL, CPHA)
- Max input SPI_CLK: 8MHz
- Support 4/8/16bits data frame
- TX FIFO width 16bits, depth 64
- RX FIFO width 16bits, depth 64
- DMA transfer supported

SPI1 Master Features:

- Supports Clock Mode 0-3 (CPOL, CPHA)
- 4 transmit mode: TX only, RX only, Full-duplex, EEPROM
- SPI1 source clock (40MHz)
- SPI1 SPI_CLK frequency = (SPI1 source clock)/N, N is any even value between 2 and 65534.
- Supports 4 to 32bits data frame
- 3 Hardware CS support
- TX FIFO width 32bits, depth 16
- RX FIFO width 32bits, depth 16
- DMA transfer supported

10.10. *I2C*

There are two separate I2C interfaces in the RTL8762E. Each I2C interface is comprised of Serial Data Line (SDA) and Serial Clock Line (SCL). Both I2C interfaces can be configured to master or slave mode.

Features:

- Master/Slave mode
- Supports 7/10 bits I2C address
- Configurable I2C address (slave mode)
- Standard speed (0-100kHz), Fast speed (100kHz-400kHz), Fast-mode Plus (1 Mbit/s).
- TX FIFO width 8bits, depth 24
- RX FIFO width 8bits, depth 40
- DMA supported

10.11. *UART*

There are two hardware UARTs (UART0, UART1). UART1 is dedicated for log output. The UARTs have the same hardware features.

The RTL8762E provides multiple UART baud-rates configured by register setting. The common band-rate example is shown in Table 11 below. The UART clock error between two devices should be less than +-2.5%.

Features:

- Supports 7/8 Data Format
- 1/2 bit Stop bit
- Configurable parity bit: odd/even
- Programmable baud rate (max. baud rate 4,000,000)
- Hardware flow control
- RX line idle state detect
- DMA supported
- 1-wire supported

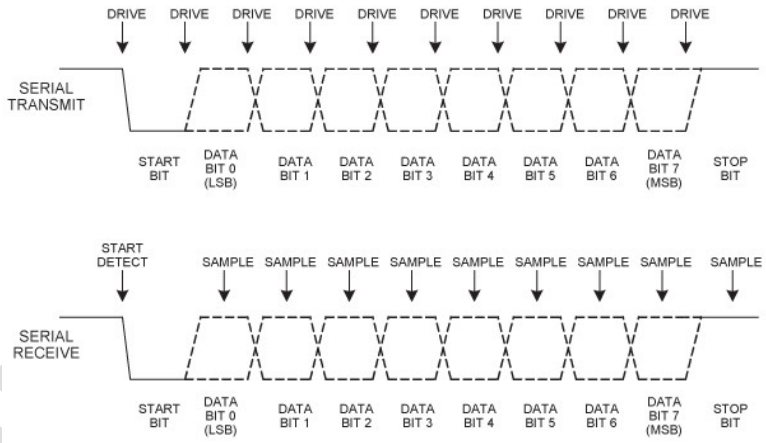

Figure 9. UART Waveform

Table 11. UART BaudRate

BaudRate (bps)	Error (%)	BaudRate (bps)	Error (%)
1200	-0.23	460800	0.17
9600	<0.01	500000	<0.01
14400	<0.01	921600	0.18
19200	<0.01	1000000	<0.01
28800	<0.01	1382400	0.17
38400	<0.01	1444400	-0.31
57600	<0.01	1500000	<0.01

BaudRate (bps)	Error (%)	BaudRate (bps)	Error (%)
76800	0.01	1843200	-0.35
115200	<0.01	2000000	0.02
128000	0.02	2764800	0.14
153600	-0.10	3000000	0.06
230400	0.03	4000000	0.03

10.12. *Direct Memory Access Controller (DMA)*

DMA features:

- 4 DMA Channels
- Independent interrupts and control bit for every channel
- 4 transfer mode: Memory to memory, memory to peripheral, peripheral to memory, peripheral to peripheral
- Multi-block supported (Channel 0 to 1)
- Safe abort/suspend transfer
- Transferred items counter (single block)
- Hardware handshake interface for peripheral

10.13. *AUXADC*

The RTL8762E provides a built in (maximum 4 channels, the maximum number of ADC channels depends on the package type) 10bits, 400kbps AUXADC for external analog signal sensing and internal VBAT voltage monitoring. The functional block is shown in Figure 10.

- A 10bits, max 400ksps AUXADC with 4 channel sharing
- Flexible sampling schedule table for multi-channel sampling
- Divided mode: Supports 0~min(VBAT, VDDIO) input range with internal resistor divider
- Internal VBAT voltage sensing
- Supports single-ended mode and differential mode

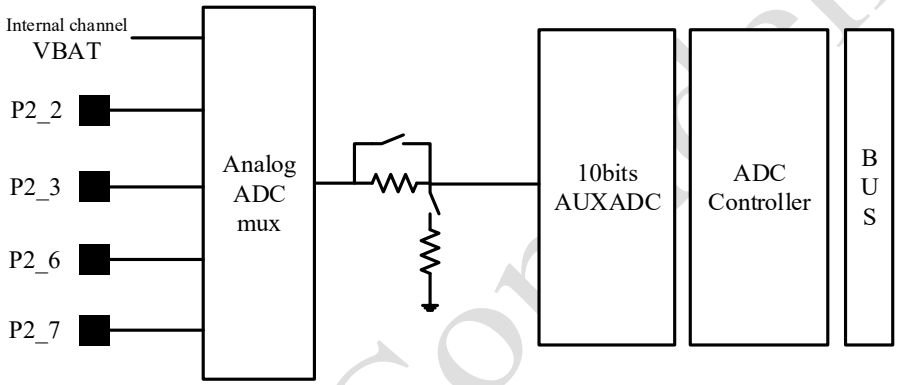

Figure 10. AUXADC Functional Block

10.14. *Proximity Sensor*

The RTL8762E series embed proximity sensor function, with 2 channel capacitive sensor inputs (RTL8762ESF-CG can't support this feature), which is used to sense finger touch on your design. When a finger put on the external touch sensor, such as a mental pad or wire, the controller uses changes in capacitance to detect such activity. A CapSense-Based Sensor is more reliable and convenient compared to mechanical buttons, as it does not involve moving parts and requires little force to operate.

Feature List

- Support 2 capacitive sensor channels (P2_2 & P2_3)
- Automatic scan period change:
  - Fast mode, fast response time
  - Slow mode, low power consumption
- Programmable touch judgement mode
  - Difference threshold judgement mode
  - Absolute threshold judgement mode
- Active noise immunity
  - Support SNR information monitor
  - Adjustable environmental noise threshold for each channel
- Automatic environment capacitance tracking and calibration
  - Support hardware baseline initial automatically
  - Support automatic baseline and threshold update for tracking environmental changing
- Programmable button de-bounce function
- Support interrupt control
  - Programmable interrupt enable for every interrupt source
  - Software readable interrupt status and raw status register
- Low power consumption
- Application
  - Power on/off key
  - Short and long press key
  - Slide key

10.15. *Audio Digital Interface*

There is a I2S/PCM interface for audio output applications. The sampling rate of I2S/PCM can be from 8kHz to 48kHz to support middle quality I2S DAC.

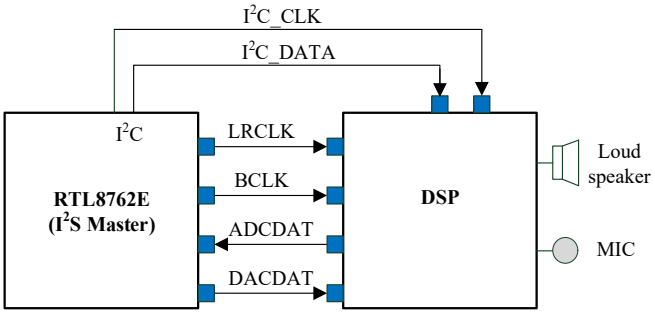

Figure 11. I2S Connection in Master Mode

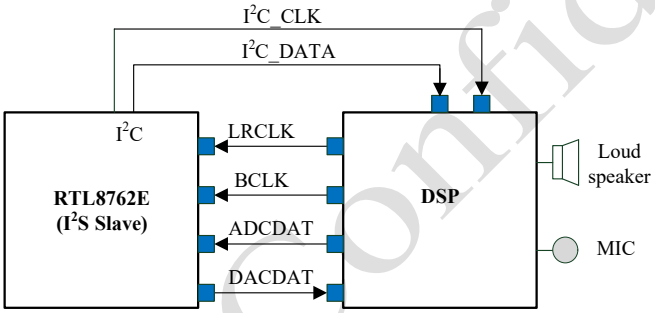

Figure 12. I2S Connection in Slave Mode

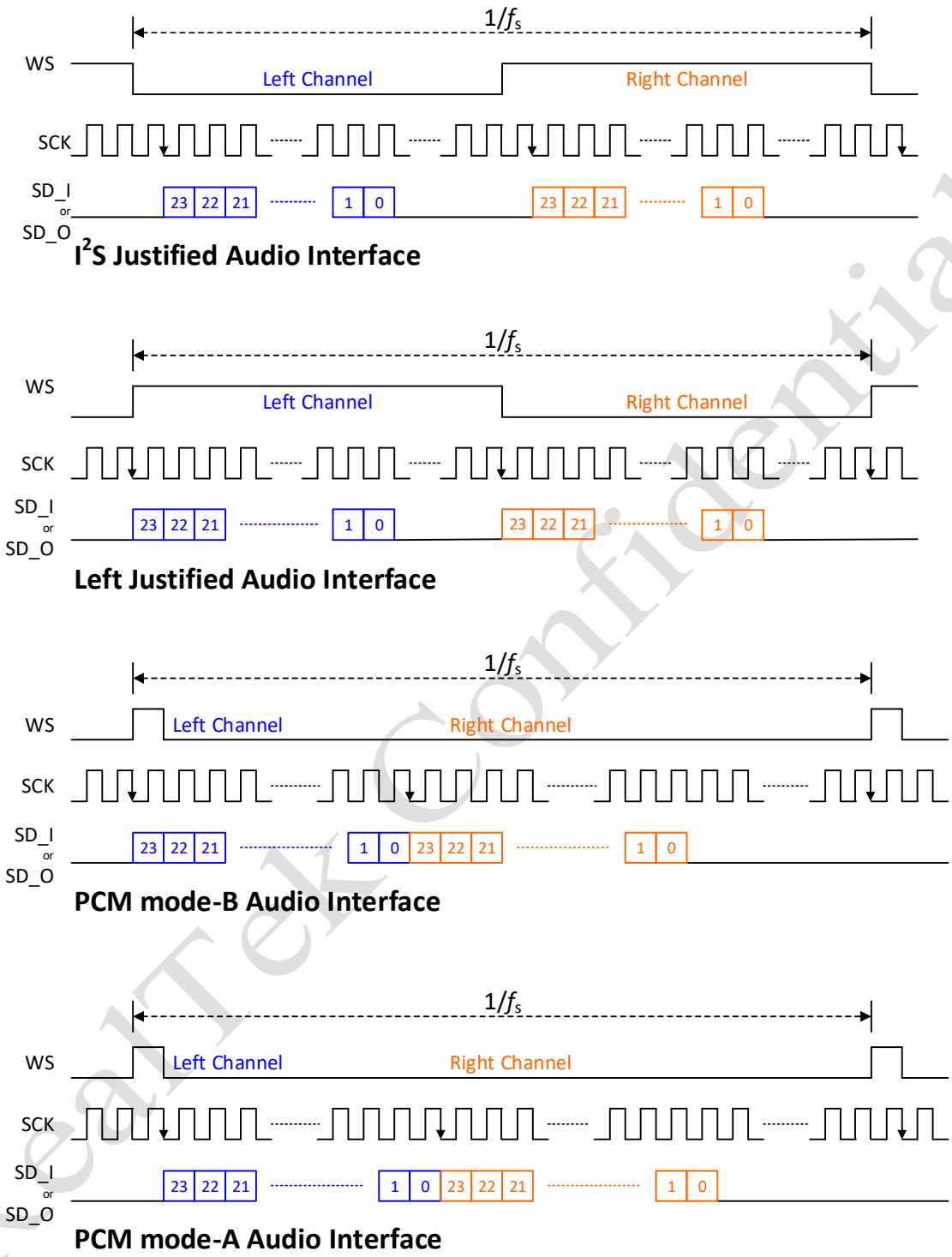

Figure 13. 24-bit Timing Diagram

***Note:** 'SCK' may be inverted at any time if required.

11. Electrical and Thermal Characteristics

11.1. *Temperature Limit Ratings*

Table 12. Temperature Limit Ratings

Parameter	Minimum	Maximum	Units
Storage Temperature	-55	+125	°C
Ambient Operating Temperature	-40	+105	°C

11.2. *Absolute Maximum Ratings*

Table 13. Absolute Maximum Ratings

Symbol	Parameter	Minimum	Typical	Maximum	Units
VBAT	Single power source for whole chip	-0.3	-	3.65	V
VDDCORE VD12_PA VD12_TRX VD12_SYN	1.2V Core and RFAFE Supply Voltage	-0.3	-	1.36	V
VDIGI	Digital core voltage	-0.3	-	1.25	V
VDDIO	Power for digital IO PADs	-0.3	-	3.65	V
HVD	Power for switching regulator	-0.3	-	3.65	V

***Note**: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and refers to the instantaneous value, not the average or final value. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum ratings for prolonged periods may affect the reliability of the device.

11.3. *Power Supply DC Characteristics*

Table 14. Recommended Power Supply DC Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
VBAT	Single power source for whole chip	-	1.8	3	3.6	V
VDDCORE VD12_PA VD12_TRX VD12_SYN	1.2V Core Supply Voltage RFAFE Supply Voltage	Active Mode	1.0	1.2	1.32	V
		DLPS Mode	0.6	0.67	-	V
VDIGI	Digital core voltage	Active Mode	0.9	1.0	1.21	V
		DLPS Mode	0.6	0.67	-	
VDDIO[Note]	Power for digital IO PADs	-	1.8	-	3.6	V
HVD	Power for switching regulator	-	1.8	-	3.6	V

***Note:** VDDIO ≤ VBAT

11.4. *Power Supply Transient Characteristics*

Table 15. Power Supply Transient Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Units
$V_{VDDCORE\_P2P\_1.8V}$	Ripple peak-to-peak on VDDCORE/VD12_PA/ SYN/TRX	Perform TX/RX duration, VBAT = 1.8V, TX Output Power = 0dBm, Ambient Temp. = 25˚C	-	40	50	mV
$V_{VDIGI\_P2P\_1.8V}$	Ripple peak-to-peak on VDIGI	Perform TX/RX duration, VBAT = 1.8V, TX Output Power = 0dBm, Ambient Temp. = 25˚C	-	25	30	mV

***Note**: All values listed in this section tested by EVB while using inductor part no. ZWP-0603-2R2K, 2.2uH±10%, R_{dc} 0.56Ω and capacitor part no. 0603X475K100CT, 4.7uF±10%, 10V, X5R, Y for switching regulator.

11.5. *Switching Regulator Characteristics*

Condition: VBAT=3V, VDDIO=3V, ambient temperature: 25°C

Table 16. Switching Regulator Characteristics

Parameter	Condition	Minimum	Typical	Maximum	Unit
Input voltage	-	1.8	3	3.6	V
Output voltage	-	-	1.2	1.36	V
Output current	Only for RTL8762E internal use	-	-	50	mA
Recommended input capacitor	X5R	4.7	-	10	µF
Recommended output inductor	1. Power inductor 2. +-20%	-	2.2	-	µH
Recommended output capacitor	X5R	-	4.7	-	µF

11.6. *ESD Characteristics*

Table 17. ESD Characteristics

Parameter	Condition	Susceptibility
HBM	All pins, test method: JESD22	+/-2kV

11.7. *AUXADC Characteristics*

Condition: VBAT/HVD=3V, VDDIO=3V, ambient temperature: 25°C

Table 18. AUXADC Characteristics

AUX Mode	Conditions	Minimum	Typical	Maximum	Unit
Resolution	Bypass mode	-	10	-	bit

AUX Mode	Conditions	Minimum	Typical	Maximum	Unit
ENOB	-	-	8.8	-	bit
Sampling Rate	-	-	400	1000	kHz
Offset	with FT calibration	-	20	-	mV
Input Voltage Range	External channel (Divided mode)	0.2	-	*Note	V
	External channel (Bypass mode)	0.05	-	0.9	V
	Internal channel (VBAT)	1.8	-	3.6	V
Input Impedance	Bypass mode	-	8.7	-	MOhm
	Resistor divider mode	-	500	-	kOhm
Sampling Capacitance	Bypass mode	-	0.5	-	pF
	Resistor divider mode	-	0.5	-	pF

Note: ADC input pin voltage should be less than min(VBAT, VDDIO) at all times.

11.8. *Microphone Interface Characteristics*

These include PGA, sigma-delta ADC, and MIC Bias characteristics.

Condition: VBAT/HVD =3V, VDDIO=3V, ambient temperature: 25°C

Table 19. Microphone Interface Characteristics

AUDIO Mode	Conditions	Minimum	Typical	Maximum	Unit
Resolution	-	-	-	16	bit
Input Sample Rate	-	8	-	48	kHz
Mode	-	-	Differential /Single-end	-	-
Signal to Noise Ratio (Single-ended mode)	Fin=1kHz B/W=20Hz - 20kHz A-weighted THD+N < 0.1 % 500mVrms input 0 dB gain	-	92.5	-	dBA
Signal to Noise Ratio (differential mode)	Fin=1kHz B/W=20Hz - 20kHz A-weighted THD+N < 0.1 % 1Vrms input 0 dB gain	-	93.3	-	dBA
Signal to Noise Ratio (Single-ended mode)	Fin=1kHz B/W=20Hz - 20kHz A-weighted THD+N < 0.5 % 5mVrms input 40 dB gain	-	53.6	-	dBA
Signal to Noise Ratio (differential mode)	Fin=1kHz B/W=20Hz - 20kHz A-weighted THD+N < 0.5 % 10mVrms input 40 dB gain	-	65.8	-	dBA
Digital Gain	-	-17.625		30	dB
Gain Step	-	-	0.375	-	dB
MIC Boost Gain	0/20/30/40 dB	0	-	40	dB
Input Full-Scale at Maximum Gain (Single-ended mode)	Gain = 40 dB	-	15.5	-	mVpp
Input Full-Scale at Maximum Gain (Differential)	Gain = 40 dB	-	31	-	mVpp
Input Full-Scale at Maximum Gain (Single-ended mode)	Gain = 0 dB	-	1.55	-	Vpp
Input Full-Scale at Minimum Gain (Differential)	Gain = 0 dB	-	3.1	-	Vpp
3dB Bandwidth	-	-	20	-	kHz
Microphone Mode	Input impedance	-	6	10	kOhm

AUDIO Mode	Conditions	Minimum	Typical	Maximum	Unit
Input Impedance	Input capacitance	-	-	20	pF
THD+N @-3dBFS output (Single-ended mode)	AVDD=1.8V, Gain=20 dB	-	0.03	-	%
THD+N @-3dBFS output (Differential mode)	AVDD=1.8V, Gain=20 dB	-	0.01	-	%
THD+N @-3dBFS output (Single-ended mode)	AVDD=1.8V, Gain=0 dB	-	0.011	-	%
THD+N @-3dBFS output (Differential mode)	AVDD=1.8V, Gain=0 dB	-	0.0095	-	%
MIC Bias	3-bits resolution	1.5	1.8	2.2	V

***Note:** Measured with the RTK EVB.

11.9. *Radio Characteristics*

Condition: VBAT/HVD =3V, VDDIO=3V, ambient temperature: 25°C

Table 20. General Radio Characteristics

Parameter	Condition	Minimum	Typical	Maximum
Frequency Range (MHz)	-	2402	-	2480

Table 21. RX Performance

Parameter	Condition	Minimum	Typical	Maximum
Sensitivity (dBm) (LE 1M/LE 2M/LR2[*4]/LR8[*4])	PER ≤ 30.8%	-98/-95/-101/-107[*1]	-97/-94/-100/-106	-92/-89/-95/-100[*3]
Maximum Input Level (dBm) (LE 1M/LE 2M/LR2/LR8)	PER ≤ 30.8%	-	-1/-1/-1/-1	-
C/I (LE 1M/LR2/LR8)	$C/I_{co\text{-}channel}$ (dB)	21/17/12	-	-
	C/I_{+1MHz} (dB)	15/11/6	-	-
	C/I_{-1MHz} (dB)	15/11/6	-	-
	C/I_{+2MHz} (dB)	-17/-21/-26	-	-
	C/I_{-2MHz} (dB)	-15/-19/-24	-	-
	C/I_{+3MHz} (dB)	-27/-31/-36	-	-
	C/I_{Image} (dB)	-9/-13/-18	-	-
	$C/I_{Image+1MHz}$ (dB)	-15/-19/-24	-	-
	$C/I_{Image-1MHz}$ (dB)	-15/-19/-24	-	-
C/I LE 2M	$C/I_{co\text{-}channel}$ (dB)	21	-	-
	C/I_{+2MHz} (dB)	15	-	-
	C/I_{-2MHz} (dB)	15	-	-
	C/I_{+4MHz} (dB)	-17	-	-
	C/I_{-4MHz} (dB)	-15	-	-
	C/I_{+6MHz} (dB)	-27	-	-
	C/I_{Image} (dB)	-9	-	-

Parameter	Condition	Minimum	Typical	Maximum
	$C/I_{Image+2MHz}$ (dB)	-15	-	-
	$C/I_{Image-2MHz}$ (dB)	-15	-	-
Blocker Power (dBm)	30~2000MHz, Wanted signal level =-67dBm	-30	-	-
	2003~2399MHz, Wanted signal level =-67dBm	-35	-	-
	2484~2997MHz, Wanted signal level =-67dBm	-35	-	-
	3000MHz~12.75GHz, Wanted signal level =-67dBm	-30	-	-
Max PER Report Integrity	Wanted signal: -30dBm	-	50%	-
Max Intermodulation level (dBm)	Wanted signal (f0): -64dBm Worst intermodulation level @2f1-f2=f0, |f1-f2|=n MHz, n=3, 4, 5…	-50	-	-

***Note 1:** Measured with the RTK EVB.

***Note 2:** Depends on PCB design and registers setting.

***Note 3:** Spur channels may have extra degradation due to clock interference at 2420, 2440, 2460 and 2480MHz.

****Note 4*:** LR2 is the abbreviation *of* LE Coded (S=2). LR8 is the abbreviation of LE Coded (S=8).

Table 22. TX Performance

Parameter	Condition	Minimum	Typical	Maximum
Maximum Output Power (dBm)	-	5	7.5	10.5
Adjacent Channel Power Ratio (dBm) LE 1M	+2MHz	-	-	-20
	-2MHz	-	-	-20
	>=+3MHz	-	-	-30
	<=-3MHz	-	-	-30
Adjacent Channel Power Ratio (dBm) LE 2M	+4MHz	-	-	-20
	-4MHz	-	-	-20
	>=+6MHz	-	-	-30
	<=-6MHz	-	-	-30
Modulation Characteristics (LE 1M/LE 2M/LR8[*2])	$\Delta f1_{avg}$ (kHz)	-	250/500/250	-
	Δf2max (kHz)	185/370/185	-	-
	$\Delta f2_{max}$ Pass Rate (%)	-	100	-
	$\Delta f2_{avg} / \Delta f1_{avg}$	-	0.88	-
Carrier Frequency Offset and Drift (LE 1M/LE 2M/LR8)	Average Fn (kHz)	-	12.5/12.5/12.5	-
	Drift Rate (kHz/50μs)	-	10/10/10	-
	Avg Drift (kHz/50μs)	-	10/10/10	-
	Max Drift (kHz/50μs)	-	20/20/19.2	-
Output power of second harmonic (dBm)	-	-	-50[*1]	-
Output power of third harmonic (dBm)	-	-	-50[*1]	-

Parameter	Condition	Minimum	Typical	Maximum

***Note 1:** Tested by EVB with RF PI network.

***Note 2:** LR8 is the abbreviation of LE Coded (S=8).

11.10. *Digital IO Pin DC Characteristics*

Table 23. Digital IO Pin DC Characteristics

Parameter	Condition	Minimum	Typical	Maximum	Unit
Input high voltage	VDDIO=3.3V	2	3.3	3.6	V
Input low voltage	VDDIO=3.3V	-	0	0.9	V
Output high voltage	VDDIO=3.3V	2.97	-	3.3	V
Output low voltage	VDDIO=3.3V	0	-	0.33	V
Input high voltage	VDDIO=1.8V	1.3	1.8	2.1	V
Input low voltage	VDDIO=1.8V	-	0	0.5	V
Output high voltage	VDDIO=1.8V	1.62	-	1.8	V
Output low voltage	VDDIO=1.8V	0	-	0.18	V
Pull high and pull low resistor	VDDIO=3.3V Strong pull/weak pull	-	10/100	-	kOhm
	VDDIO=1.8V Strong pull/weak pull	-	20/200	-	
Input high current	PAD configured as input mode	-	-	0.1	µA
Input low current	PAD configured as input mode	-	-	0.1	µA

11.11. *UART Characteristics*

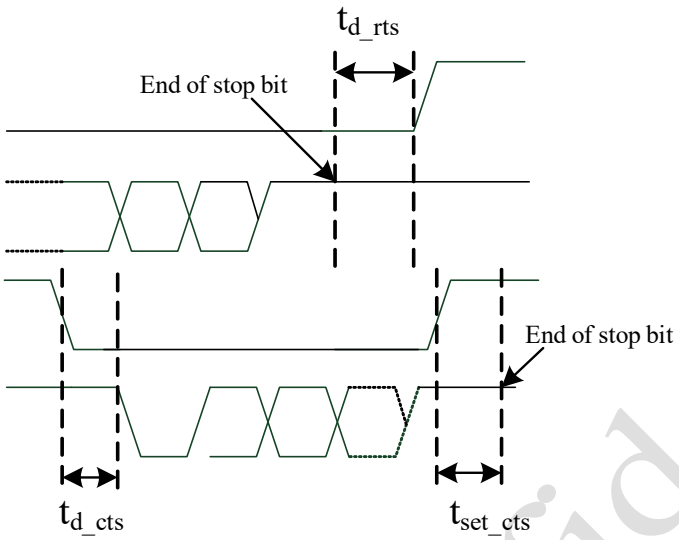

Figure 14. UART Characteristics

Table 24. UART Timing Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Timing between RX Stop bit and RTS go high when RX FIFO is full (symbol time)	t_{d_rts}	-	-	0.5	ns
Timing between CTS go low and device send first bit	t_{d_cts}	-	-	25	ns
Timing between CTS go high and TX send stop bit	t_{set_cts}	75	-	-	ns

11.12. *I2C Timing Characteristics*

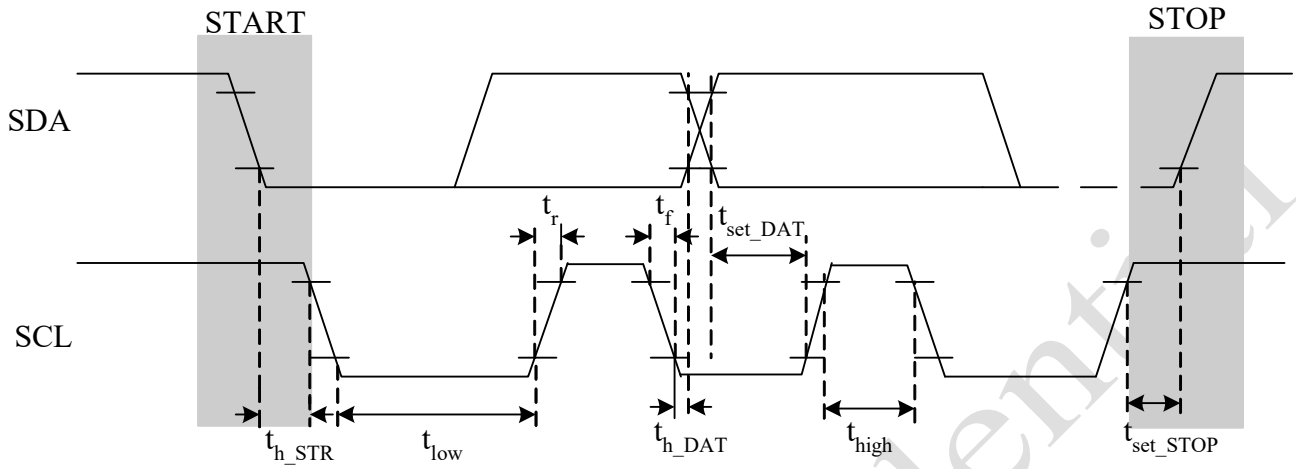

Figure 15. I2C Interface Timing Diagram

Table 25. I2C Timing Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SCL clock frequency	-	-	-	400	kHz
High period of SCL	t_{high}	600	-	-	ns
Low period of SCL	t_{low}	1300	-	-	ns
Hold time of START	t_{h_STR}	600	-	-	ns
Hold time of DATA	t_{h_DAT}	0	-	-	ns
Setup time of STOP	t_{set_STOP}	600	-	-	ns
Setup time of DATA	t_{set_DAT}	100	-	-	ns
Rise time of SCL and SDA (with 4.7k ohm resistor pulled high)	t_r	See note	-	-	ns
Fall time of SCA and SDA	t_f	See note	-	-	ns

***Note:** Depends on the external bus pull up resistor.

11.13. *Power Consumption*

11.13.1. Low Power Mode Power Consumption

Measurement Condition:

(a) VBAT/HVD =3V, VDDIO=3V, ambient temperature: 25°C

(b) Internal MCM with Z-bit 8Mb Flash

(c) Measured with RTK EVB and 3225-type 40MHz crystal @ C_L=9pF

Table 26. Low Power Mode Power Consumption

Parameter	Always on Registers	32kHz RCOSC	Retention SRAM	CPU	Wake-up Method	Current Consumption (Typical)
Power Down	On	Off	Off	Off	Wake-up by GPIO	1.9 uA
Deep LPS	On	On	Retention	Off	Wake-up by GPIO, Timer	3.9 uA

11.13.2. Active Mode Power Consumption

Measurement Condition:

(a) VBAT/HVD =3V, VDDIO=3V, ambient temperature: 25°C

(b) Internal MCM with Z-bit 8Mb Flash

(c) Measured with RTK EVB and 3225-type 40MHz crystal @ C_L=9pF

Table 27. Active Mode Power Consumption

Power Mode	Current Consumption (Typical)
Active RX mode	5.3 mA
Active TX mode (TX power: -20 dBm)	4.1 mA
Active TX mode (TX power: 0 dBm)	5.9 mA
Active TX mode (TX power: 4 dBm)	6.8 mA
Active TX mode (TX power: 7.5 dBm)	13.1 mA
Advertising (adv_interval: 1s, payload: 23Bytes, 0dBm)	16.5 uA

12. Mechanical Dimensions

12.1. *RTL8762EMF-VS-CG: Plastic Quad Flat No-Lead Package 40 Leads 5x5mm² Outline*

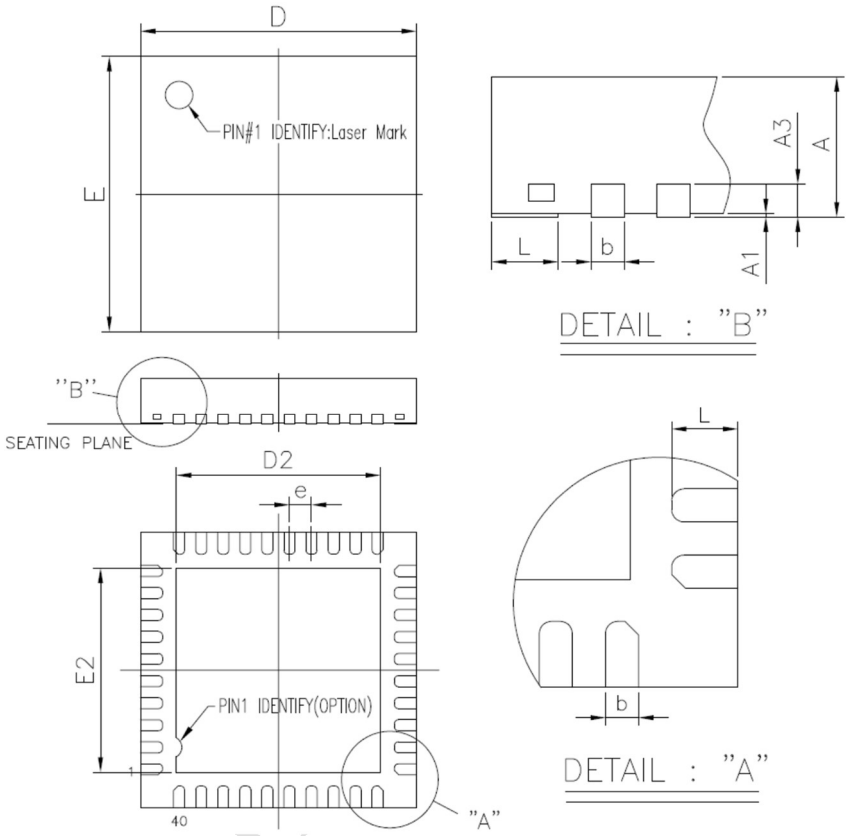

Figure 16. RTL8762EMF-VS-CG: Plastic Quad Flat No-Lead Package 40 Leads 5x5mm² Outline

12.2. *RTL8762EMF-VS-CG Mechanical Dimensions Notes*

Symbol	Dimension in mm			Dimension in inch		
	Minimum	Nominal	Maximum	Minimum	Nominal	Maximum
A	0.80	0.85	0.90	0.031	0.033	0.035
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3		0.20 REF			0.008 REF	
b	0.15	0.20	0.25	0.006	0.008	0.010
D/E		5.00 BSC			0.197 BSC	
D2/E2	3.45	3.60	3.75	0.136	0.142	0.148
e		0.40 BSC			0.016 BSC	
L	0.30	0.40	0.50	0.012	0.016	0.020

***Notes:**

1. CONTROLLING DIMENSION: MILLIMETER (mm).
2. REFERENCE DOCUMENT: JEDEC MO-220.

13. Reflow Profile

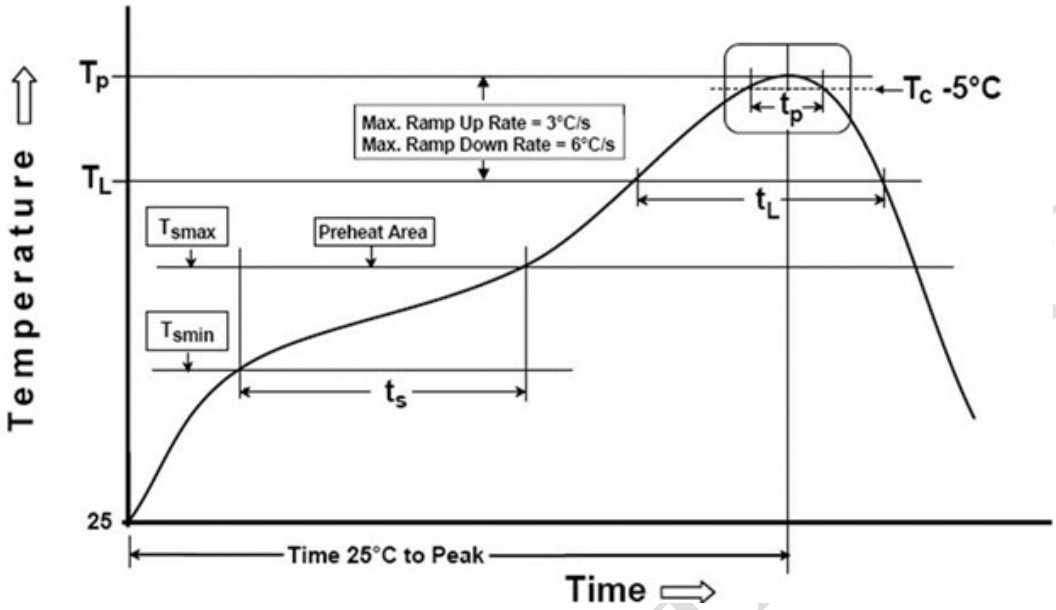

Figure 17. Reflow Profile

Table 28. Reflow Profile

Stage	Note	Pb-Free Assembly
Average ramp-up rate	T_L to Tp	3°C/ second max.
Preheat	Temperature min (T_{smin})	150°C
	Temperature max (T_{smax})	200°C
	Time (t_{smin} to t_{smax})	60 – 120 seconds
Time maintained above	Temperature(T_L)	217°C
	Time (t_L)	60 – 150 seconds
Peak package body temperature (Tp)		See following table. Tp must not exceed the specified classification temp in the following table.
Time(tp) within 5°C of the specified classification temperature (Tc)		30 seconds
Ramp-down rate (Tp to T_L)		6°C / seconds max.
Time 25°C to peak temperature		8 minutes max.

Table 29. Pb-Free Process -Classification Temperatures (T_c)

Package Thickness	Volume < 350 mm^3	Volume 350 – 2000 mm^3	Volume > 2000 mm^3
< 1.6 mm	260°C	260°C	260°C
1.6 – 2.5 mm	260°C	250°C	245°C
> 2.5 mm	260°C	245°C	245°C

14. Ordering Information

Table 30. Ordering Information

Part Number	Package
RTL8762EMF-VS-CG	QFN-40, 5x5mm^2 Outline, 'Green' Package

Note: See section 5 Pin Assignments, page 8 for package identification.

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