# CH32H417/H416/H415 Datasheet

V1.4

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## Overview

CH32H417 is an interconnected general-purpose microcontroller designed based on QingKe RISC-V5F and RISC-V3F dual cores. CH32H417 integrates USB 3.2 Gen1 controller and transceiver, 100M Ethernet MAC and PHY, SerDes high-speed isolated transceiver, Type-C/PD controller and PHY, provides SD/EMMC controller SDMMC, 500MBytes universal high-speed interface UHSIF, DVP, SWPMI, PIOC, FMC, DFSDM, LTDC, GPHA, DMA Controller, multi-timers, 8 UARTs, I3C, 4 groups of I2C, 2 groups of QSPI, 4 groups of SPI, 2 groups of I2S, 3 groups of CAN and other peripheral resources. Built-in 5M sampling rate dual 12-bit ADC unit, 20M sampling rate 10-bit high-speed HSADC unit, 16-channel touch-key, dual DAC unit, 3 groups of OPA, voltage CMP and other analog resources, support 10M/100M Ethernet communication. It supports USB 2.0 and USB 3.0, USB Host and USB Device, Type-C and PDUSB fast charging, SerDes high-speed isolation and remote transmission, and dual-core division of labor to improve the efficiency of network protocol processing and communication response speed.

## Feature

- **Core**
- Dual-core structure: QingKe RISC-V5F and RISC-V3F
- Fast programmable interrupt controller + hardware interrupt stack
- V5F up to 400MHz, V3F up to 150MHz
- **Memory**
- 896KB volatile data storage area SRAM (include 128KB ITCM and 256KB DTCM)
- 960KB program memory area CodeFlash
- 56KB System BootLoader storage area
- 256B user-defined information storage area
- **Power management and low-power:**
- System power supply $V_{DD33}$ rated: 3.3V
- Regular GPIO power supply $V_{DDIO}$, rated 3.3V, supports 1.8V
- High-speed GPIO supply $V_{IO18}$, selectable 1.2/1.8/2.5/3.3V
- $V_{BAT}$ power supply independently powering RTC, LSE
- Low-power modes: Sleep, Stop
- **System clock and reset:**
- Built-in factory-adjusted 25MHz RC oscillator
- Built-in RC oscillator of about 40kHz
- High-speed oscillator supports external 25MHz crystal
- Low-speed oscillator supports external 32kHz crystal
- Power-on/power-off reset, programmable voltage monitor
- **2 groups of 16 general DMA controllers:**
- A total of 16 channels, supporting ring buffer management
- **2 groups of 12-bit ADC:**
- Analog input range: $V_{SS}$~$V_{DDIO}$
- 16 external signal channels +2 internal signal channels
- The sampling rate is up to 5Msps, supports dual ADC
- **16-bit TouchKey channel detection**
- **1 group of 10-bit HSADC:**
- Analog input range: $V_{SS}$~$V_{DDIO}$
- 7 external signal channels
- Sampling rate up to 20Msps
- **2 groups of 12-bit DAC**
- **32-bit width 125MHz Universal High-speed Interface UHSIF**
- **150MHz DVP**
- **200MHz SD/EMMC controller: Support single/dual edge**

- **SDIO master/slave interface: support SD/SDIO/MMC port**
- **1-wire protocol main interface SWPMI**
- **Programmable protocol I/O controller PIOC:**
- Programmable, supporting a variety of 1-wire/2-wire interfaces.
- Support 1-wire RGB chip multi-stage series connection
- **Ethernet controller MAC and 10M/100M PHY:**
- MAC and 100M PHY are fully integrated, and the periphery only needs capacitance
- Support Auto-MDIX line automatic conversion and polarity adaptation
- Provide RGMII interface, which can connect external 1000M PHY.
- Built-in pre-assigned globally unique MAC address
- **5Gbps SuperSpeed USB 3.0 controller and PHY**
- Support SuperSpeed Host and Device modes
- Support drive USB 3.0 HUB
- High-speed integrated design, measured 450Mbytes per second.
- **480Mbps high-speed USB 3.0 controller and PHY**
- Support high-speed/full-speed Host and Device modes
- Support 1024-byte packets
- Support USART or I2C pin mapping
- **Full-speed USB 2.0 controller and PHY**
- Support full-speed/low-speed Host and Device mode
- Support OTG function
- **Remote SerDes controller and PHY**
- Support high-voltage signal isolation transmission at kilovolt level
- Support 100 meters of differential network cable remote transmission
- **Random Number Generator RNG**
- **USB PD and Type-C controller and PHY**
- Support DRP, Sink and Source application, support PDUSB
- Support PD3.2 and EPR, support 100W or 240W fast charging
- **Analog voltage comparator CMP**
- 2 input channels, output to peripherals or I/O
- **3 groups of OPA/PGA/CMP**
- Multiple input channels and output channels
- Low dropout voltage, multi-step gain, support high-speed mode
- **Multi-group timers:**
- 2×16-bit advanced timers
- 4×16-bit and 4×32-bit general-purpose timers
- 2×16-bit Basic Timers
- 2×16-bit low-power timers
- 2 Watchdog timers: (independent watchdog and window watchdog)
- 2×32-bit SysTick
- **RTC: 32-bit independent timer**
- **8 groups of USART: Support LIN**
- **4 groups of I2C interfaces**
- **I3C interface**
- **4 groups of SPI interfaces (SPI2, SPI3 for I2S1, I2S2)**
- **2 groups of QuadSPI interfaces**
- **3 groups of CAN interfaces (2.0B active)**
- **Digital Filter for ΣΔ Modulator DFSDM**
- **Serial Audio Interface SAI**
- **LCD-TFT Display Controller LTDC**
- **Graphics Processing Hardware Accelerator GPHA**
- **Flexible Memory Controller FMC:**
- Support FSMC interface and SDRAM interface.
- Support external expansion of low-cost PSRAM.
- **Fast GPIO port:**
- 6 groups of GPIO ports, 95 I/O ports
- Mapping 16 external interrupts
- **ECDC encryption module:**
- Support AES128/192/256 algorithm
- Support SM4 algorithm
- **Debug mode:**
- Support 1-wire (default) and 2-wire debugging modes
- **Package form: QF**

| Product model / Resource differences | | CH32H417 | | | CH32H416 | CH32H415 |
|---|---|---|---|---|---|---|
| | | QEU6 | MEU6 | WEU6 | RDU6 | REU6 |
| Chip pin number | | 128 | 88 | 68 | 60 | 60 |
| Nonzero wait Code FLASH | | 960KB | 960KB | 960KB | 480KB | 960KB |
| SRAM | Core 1 HS ITCM | 128KB | 128KB | 128KB | 128K | 128KB |
| | Core 1 HS DTCM | 256KB | 256KB | 256KB | 256K | 256KB |
| | Shared code and data area | 512KB | 512KB | 512KB | 512K | 512KB |
| GPIO port number | | 95 | 65 | 50 | 48 | 54 |
| Timer | ADTM (16-bit) | 2 | 2 | 2 | 2 | 2 |
| | GPTM (16-bit) | 4 | 4 | 4 | 4 | 4 |
| | GPTM (32-bit) | 4 | 4 | 4 | 4 | 4 |
| | Basic (16-bit) | 2 | 2 | 2 | 2 | 2 |
| | LPTIM | 2 | 2 | 2 | 2 | 2 |
| | Watchdog | WWDG+IWDG | | | WWDG+IWDG | WWDG+IWDG |
| | SysTick 32-bit | 2 | 2 | 2 | 2 | 2 |
| RTC | | √ | √ | √ | √ | √ |
| ADC/ TKey | Units | 2 | 2 | 2 | 2 | 2 |
| | Channels | 16+4 | 9+4 | 7+4 | 16+4 | 15+4 |
| HSADC | Units | 1 | 1 | 1 | 1 | 1 |
| | Channels | 7 | 4 | 4 | 7 | 4 |
| DAC (Unit) | | 2 | 2 | 1 (DAC2) | 2 | 2 |
| OPA | | 3 | 2 (OPA1/3) | 2 (OPA1/3) | 3 | 2 (OPA1/3) |
| CMP | | 1 | 1 | 1 | 1 | 1 |
| DFSDM | | 1 | 1 | 1 | 1 | 1 |
| RNG | | 1 | 1 | 1 | 1 | 1 |
| LTDC | | 1 | 1 | 1 | 1 | 1 |
| GPHA | | 1 | 1 | 1 | 1 | 1 |
| DVP | | 1 | 1 | 1 | 1 | 1 |
| USART | | 8 | 8 | 7 | 7 | 8 |
| SPI/I2S | | 4/2 | 4/2 | 3/2 | 3/2 | 4/2 |
| QSPI | | 2 | 1 (QSPI2) | 1 (QSPI2) | 1 (QSPI2) | - |
| I2C | | 4 | 4 | 4 | 4 | 4 |
| I3C | | 1 | 1 | 1 | 1 | 1 |
| UHSIF | | 1 | 1 | 1[(1)] | - | - |
| CAN[(5)] | | 3 | 3 | 3 | 3 | 3 |
| SDIO | | 1 | - | - | - | 1 |
| SDMMC | | 1 | 1 | 1 | 1 | - |
| SAI | | 1 | 1 | 1 | 1 | 1 |
| SWPMI | | 1 | 1 | 1 | 1 | 1 |
| PDUSB | USBFS/OTG_FS | 1 | 1 | - | 1 | 1 |
| | USBHS (USB | 1 | 1 | 1 | 1 | 1 |

| Product model / Resource differences | | CH32H417 | | | CH32H416 | CH32H415 |
|---|---|---|---|---|---|---|
| | | QEU6 | MEU6 | WEU6 | RDU6 | REU6 |
| | 2.0) | | | | | |
| | USBSS (USB 3.0) | 1 | 1 | 1 | 1 | - |
| | USBPD Type-C | 1 | 1 | - | 1<br>Built-in Rd(4) | 1 |
| SerDes(4) | | 1 | 1 | - | - | - |
| Ethernet(5) | | MAC+10/100M PHY | MAC+10/100M PHY | MAC+10/100M PHY | - | - |
| FMC | FSMC | 1 | 1(2) | 1(2) | - | - |
| | SDRAM | 1 | 1 | 1(3) | - | - |
| PIOC | | 1 | 1 | 1 | 1 | 1 |
| Package form | | QFN128 | QFN88 | QFN68 | QFN60X6 | QFN60X6 |

*Note:*

*1. Incomplete, only supports most functions.*

*2. Incomplete, only supports 8-bit and 16-bit.*

*3. Incomplete, only supports 8-bit and 16-bit.*

*4. CH32H416RdU6 has a controllable RD pull-down resistor defined by the Type-C specification, which is about 5.1kΩ.*

*5. For products with lot number 5 bit 0, GPHA, Ethernet, SerDes, CAN functions are not provided.*

# Chapter 1 Specification Information

## 1.1 System Structure

The microcontroller is designed on the basis of the RISC-V instruction set, and its architecture integrates 2 QingKe microprocessor cores, arbitration unit, DMA module, SRAM storage and other components through multiple bus groups to achieve interaction. A general-purpose DMA controller is integrated to reduce the CPU load and improve access efficiency, and a multi-level clock management mechanism is applied to reduce the power consumption of peripherals, while both the data protection mechanism, the clock automatically switches to protect the measures to increase system stability. The following diagram shows the overall internal architecture of the series chip.

Figure 1-1-1 CH32H417 system block diagram

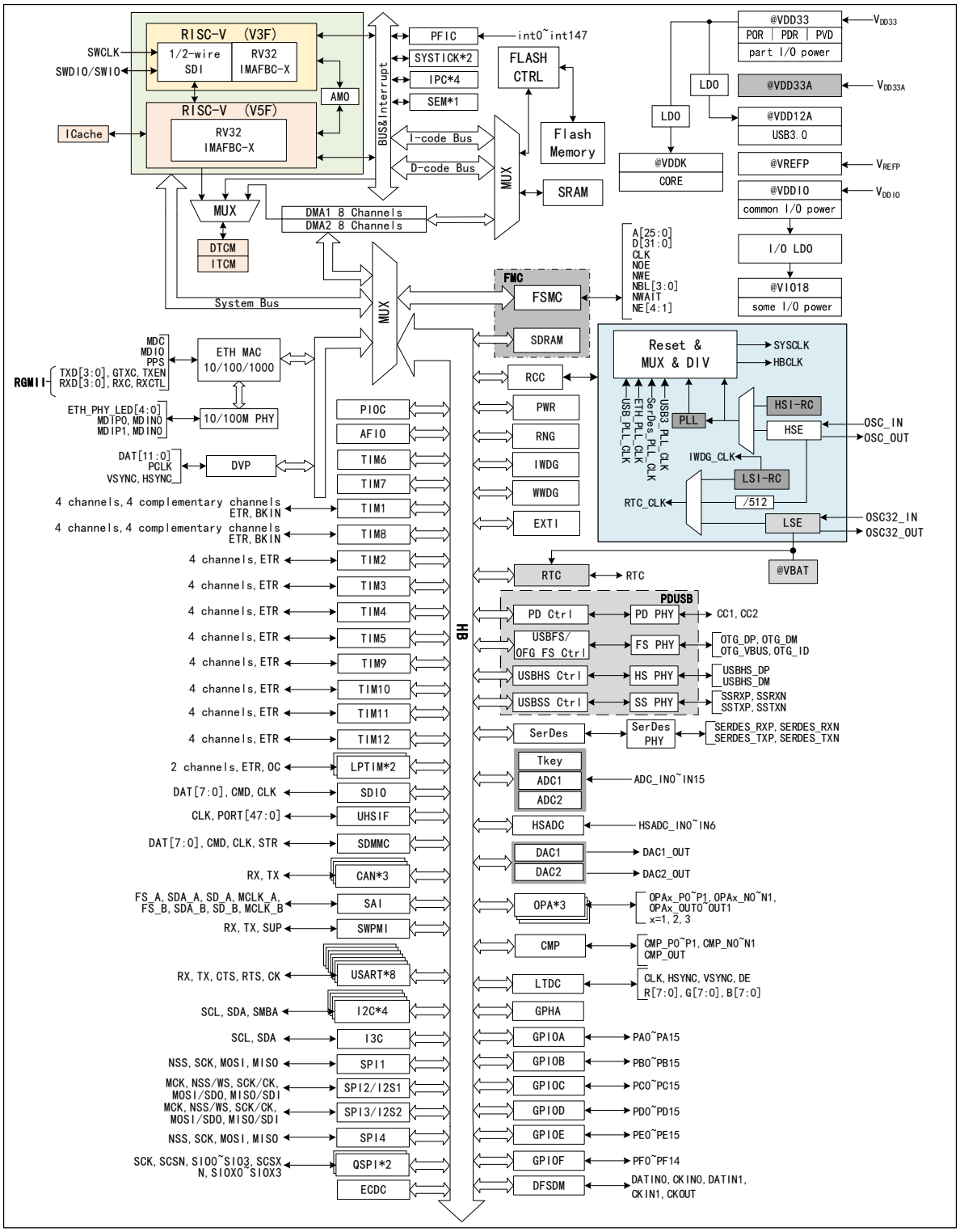


Figure 1-1-2 CH32H416 system block diagram

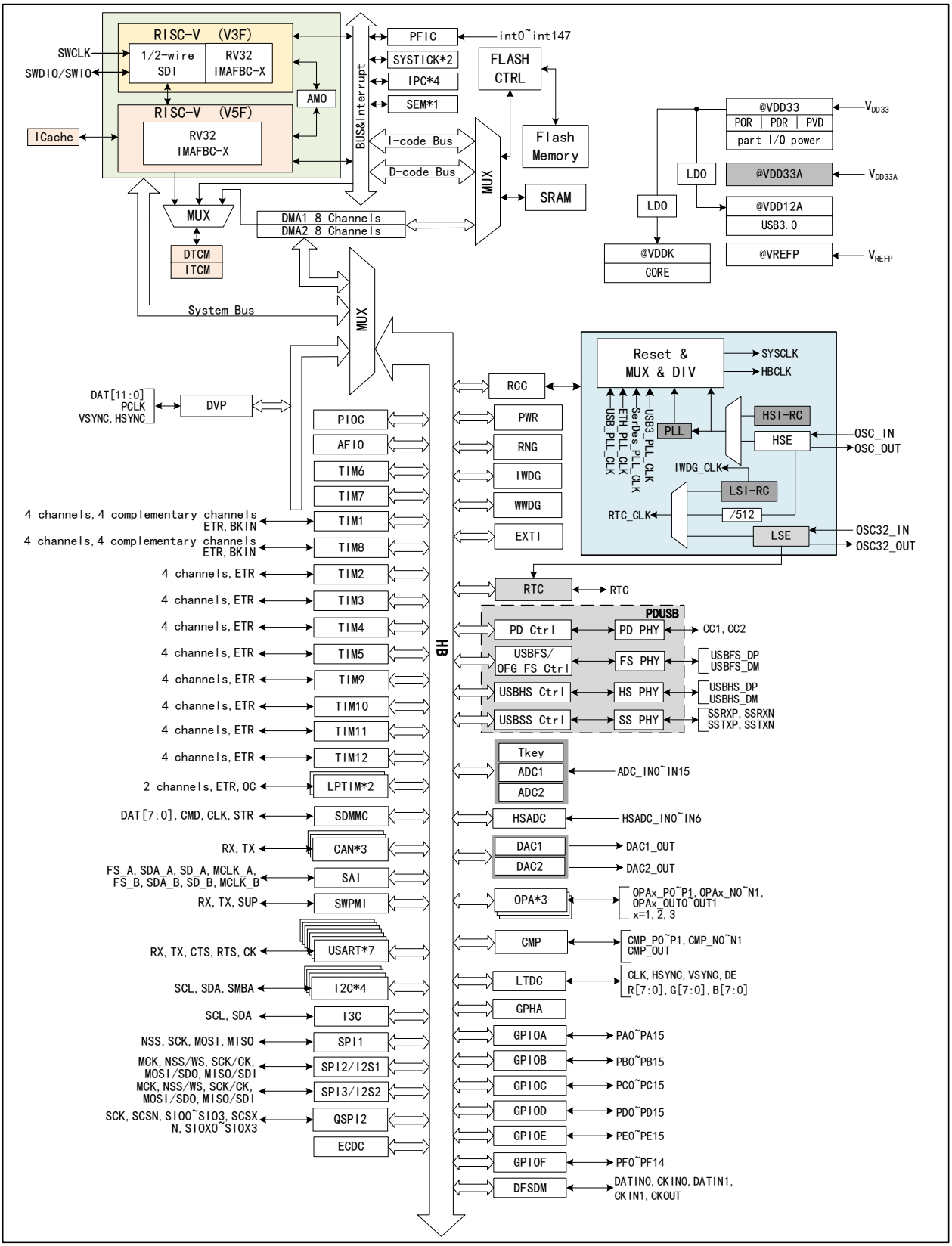
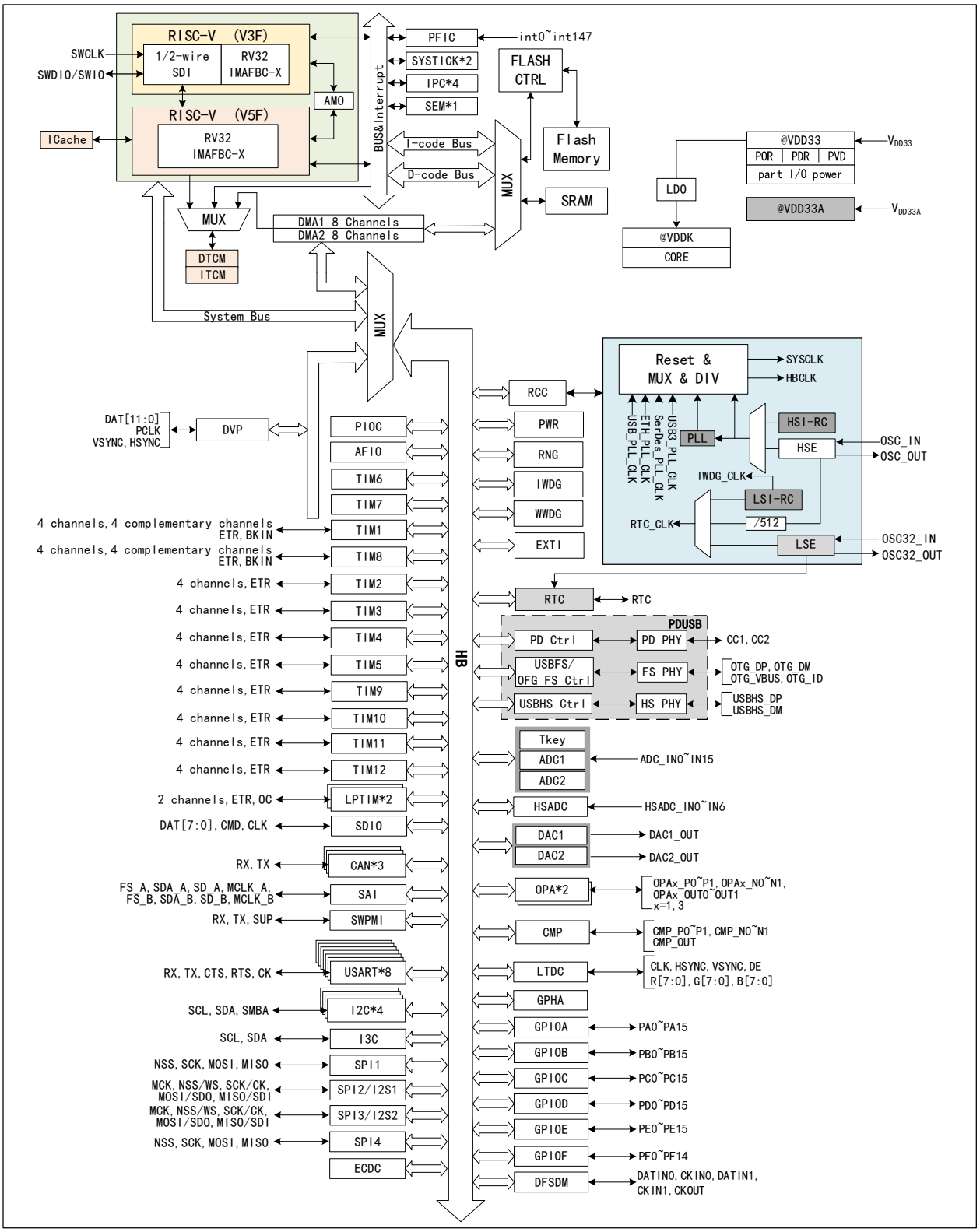
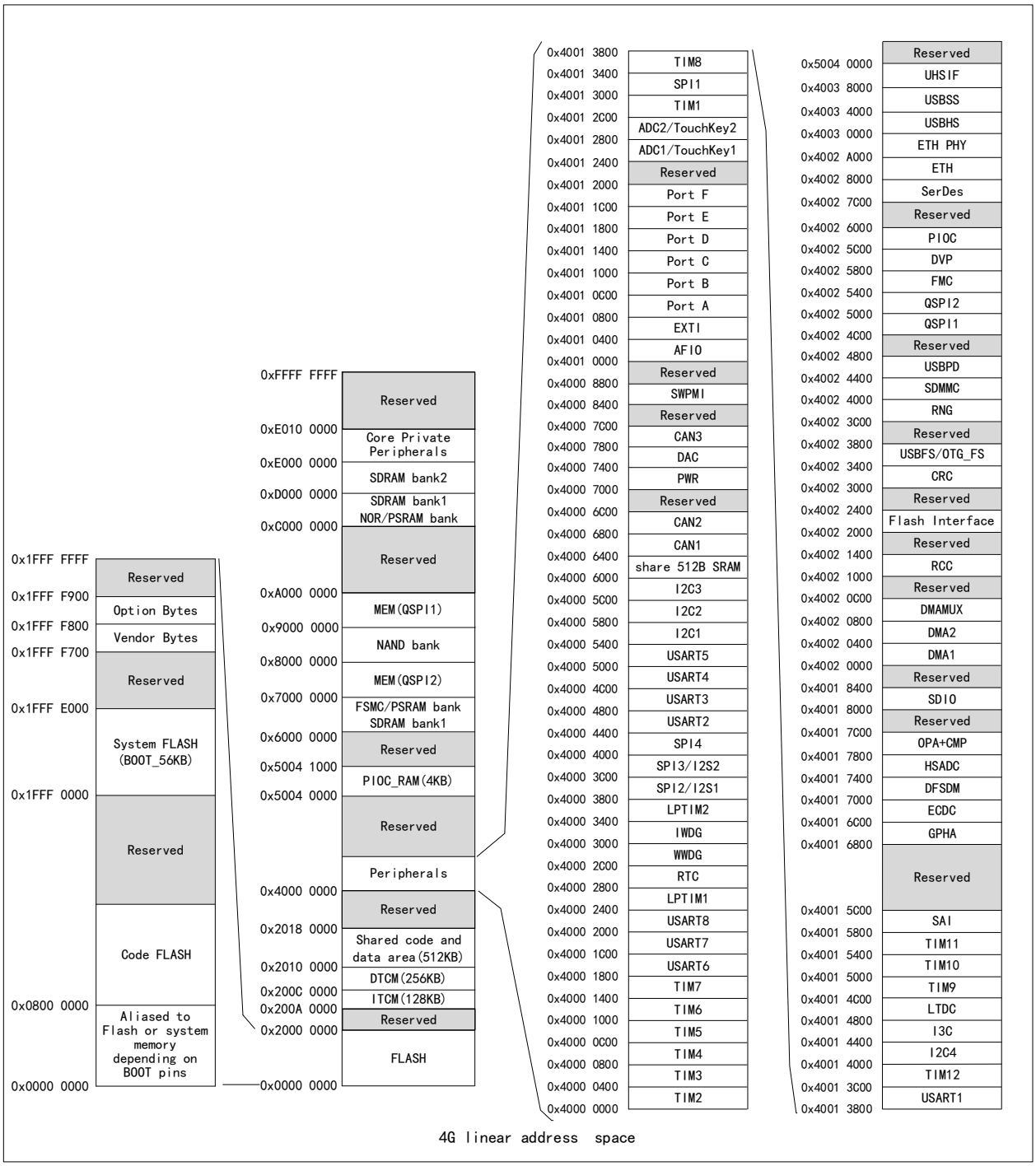


Figure 1-1-3 CH32H416 system block diagram



# 1.2 Memory Map

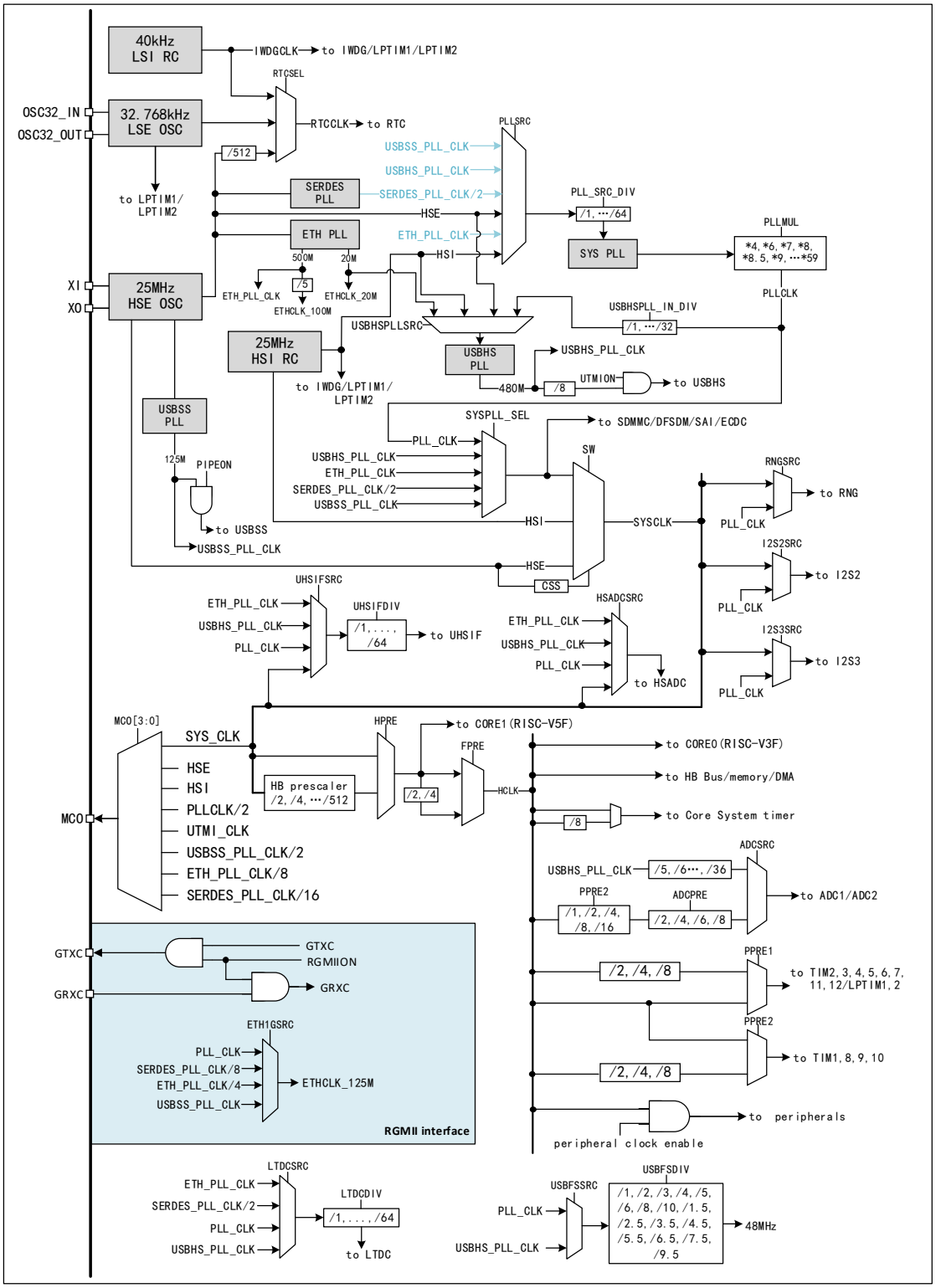
Figure 1-2 Memory address map



## 1.3 Clock Tree

4 groups of clock sources are introduced into the system: internal high frequency RC oscillator (HSI), internal low frequency RC oscillator (LSI), external high frequency oscillator (HSE), external low frequency oscillator (LSE).

Figure 1-3 Clock tree block diagram




*Note: The blue-marked sections in the above diagram apply only to chips with a fifth digit greater than 0 in the lot number.*

## 1.4 Functional Description

### 1.4.1 Dual Core: RISC-V5F Processor and RISC-V3F Processor

The chip integrates a dual core architecture: RISC-V5F (CORE1) and RISC-V3F (CORE0). Both processors support the instruction set RV32IMAFBC-X, are internally managed in a modular fashion, and contain units such as the fast programmable interrupt controller PFIC, memory protection, branch prediction mode, and extended instruction support. Externally multiple buses are connected to external unit modules to enable interaction between external function modules and the core.

The processor with its minimal instruction set, multiple operating modes, and modular custom extensions can be flexibly applied to different scenarios of microcontroller design, such as small area low-power embedded scenarios, high performance application operating system scenarios, etc.

RISC-V5F processor:

- Disordered multi-transmit architecture
- Built-in 32KB instruction cache
- High main frequency, high performance, focus on computing
- Provide a non-maskable interrupt NMI
- 4-channel Physical Memory Protection (PMP)
- 4-channel hardware breakpoints
- 8-level interrupt nesting
- Programmable Fast Interrupt Controller (PFIC)
- Custom extension Instructions
- Hardware Stacks

RISC-V3F processor:

- Sequential single-transmit architecture
- 3-stage pipeline
- Low mains frequency, low-power consumption, focus on control
- Provide a non-maskable interrupt NMI
- 4-channel physical memory protection (PMP)
- 4-channel hardware breakpoints
- 2-level interrupt nesting
- Programmable Fast Interrupt Controller (PFIC)
- Custom extension instructions
- Hardware Stacks

### 1.4.2 On-chip Memory

Built-in SRAM with a total capacity of 896K bytes, partly used in data area and partly used in zero-waiting code area, data is lost after power failure. The SRAM is divided into 3 blocks: 128KB ITC core 1 tightly coupled zero wait code area, 256KB DTCM core 1 tightly coupled zero wait data area, and the remaining 512KB shared code and data area. In addition, the core 1 also has a 32KB high-speed instruction cache.

The 512KB shared area can be configured as zero-waiting code area and data area of RISC-V3F, and it is suggested to allocate it flexibly in units of 128KB as required.

As an option, 128KB of ITCM and 256KB of DTCM, totaling 384KB, can be configured as the code area of RISC-V5F, in which DTCM as the code area will increase one clock waiting when a jump occurs.

RISC-V3F can wait for access to ITCM or DTCM according to HCLK clock.

RISC-V5F and RISC-V3F can wait for access to the 512KB shared area according to HCLK clock zero.

Built-in 256-byte system nonvolatile configuration information storage area is used to store the manufacturer's configuration words, which are solidified before leaving the factory and cannot be modified by users.

Built-in 256-byte user-defined information storage area for user option bytes storage.

The sizes of user area and BOOT area are read by the DBMODE bit in R32_FLASH_CFGR0 register:

When DBMODE=1: Built-in 960K byte non-zero waiting program flash memory area (Code FLASH), that is, the user area, is used for user application and constant data storage, with an equivalent frequency of about 25MHz. Built-in maximum 56K byte system storage area (System FLASH), i.e. BOOT area, is used for system bootstrap storage, and a built-in bootloader loader.

When DBMODE = 0: Built-in 480K bytes non-zero wait program flash memory storage area (Code FLASH), i.e., user area, for user's application program and constant data storage, equivalent frequency is about 12.5MHz. built-in maximum 28K bytes system storage area (System FLASH), i.e., BOOT area, for system boot program storage, built-in bootloader.

### 1.4.3 Power Supply Scheme

(1) CH32H417

- $V_{DD33}$ = 2.4~3.6V: To power some I/O pins and system voltage regulator LDO, including built-in USB2.0 and Ethernet PHY. At the same time, $V_{DD33}$ supplies power to the built-in system voltage regulator LDO and outputs a regulated power supply on the $V_{DD12A}$ and $V_{DDK}$ pins. It is recommended to connect 0.1uF high-frequency capacitors to each externally. The main $V_{DD33}$ (adjacent to the Ethernet signal pin) also needs to be connected to another 4.7uF capacitor in parallel. When used for USB2.0 or Ethernet, the $V_{DD33}$ range is recommended to be 3.2~3.45V.
- $V_{DD33A}$ = 1.8~3.6V: To power the analog part of ADC, temperature sensor, HSADC, OPA, CMP, DAC and PLL, it is recommended to connect an external high-frequency capacitor with 0.1uF capacity. When using OPA or DAC, $V_{DD33A}$ and $V_{DDIO}$ are recommended to be the same voltage; when not using OPA or DAC, $V_{DD33A}$ can be higher than $V_{DDIO}$ voltage. $V_{DD33A}$ is recommended to be not less than 3.0V when using HSADC, and not less than 2.4V when using ADC and DAC.
- $V_{DD12A}$ = 1.18~1.28V: To power the built-in USB 3.0 module, it is recommended to connect an external 0.1uF parallel 4.7uF capacity high frequency capacitor. During normal operation, the VDD12A voltage is generated by the system voltage regulator LDO powered by VDD33. In order to minimize the heat generated by the LDO of the chip, it can be supplied with an external power supply (which can be generated by an external DC-DC), and it is recommended that the external voltage be slightly higher than the output voltage of the internal LDO.
- $V_{DDIO}$ = 1.8~3.6V: Power supply for some of the regular I/O pins determines the pin output high voltage amplitude, at the same time, $V_{DDIO}$ through the built-in I/O pins LDO regulator power supply in the $V_{IO18}$ pin output regulated power supply, it is recommended that each external 0.1uF high-frequency capacitance, the main $V_{DDIO}$ (adjacent to the $V_{IO18}$) also need to be another 4.7uF capacitor connected in parallel. the $V_{DDIO}$ voltage cannot be higher than the $V_{DD33}$ voltage, and $V_{DDIO}$ voltage cannot be higher than $V_{DD33A}$ voltage.

- $V_{IO18}$ = 1.1~3.6V: Power supply for some of the high-speed I/O pins determines the pin output high-voltage amplitude, it is recommended that each external 0.1uF high-frequency capacitor, the main $V_{IO18}$ (adjacent to $V_{DDIO}$) also need to be connected in parallel with another 4.7uF capacitor. During normal operation, the $V_{IO18}$ voltage is generated by the I/O pin LDO regulator powered by $V_{DDIO}$ and can be dynamically configured by software to 1.2V, 1.8V, 2.5V, 3.3V or off; the default voltage of the $V_{IO18}$ after power-up can be selected by the pull-down resistor connected externally to the XO pin, refer to Table 3-2; when there is no need to support the low-voltage, the $V_{IO18}$ can be shorted fixedly to the $V_{DDIO}$.
- $V_{REFP}$ = 2.4~3.6V: For the reference voltage of ADC, HSADC, DAC, it is recommended to connect an external high-frequency capacitor with 0.1uF capacity. $V_{REFP}$ must not be higher than $V_{DD33A}$ voltage.
- $V_{BAT}$ = 1.8~3.6V: Optional backup power supply, when $V_{DD33}$ and $V_{DD33A}$ are turned off, the internal power switcher switches $V_{BAT}$ to be used to power the RTC, external low frequency oscillator alone.
- $V_{DDK}$ = 1.17~1.27V: To power the core circuits, it is recommended that each be externally connected to a 0.1uF high-frequency capacitor, and that an additional 4.7uF capacitor be connected in parallel to the main $V_{DDK}$ (adjacent to $V_{DD33}$). During normal operation, the $V_{DDK}$ voltage is generated by the system voltage regulator LDO powered by $V_{DD33}$. In order to minimize the heat generated by the LDO of the chip, this power supply can be supplied externally (it can be generated by an external DC-DC), and it is recommended that the voltage supplied externally be slightly higher than the value of the output voltage of the internal LDO.

The above power supply pins with the same name must be shorted, voltage relationship: $V_{DD33} \geq V_{DD33A} \geq V_{DDIO} \geq V_{IO18}$; and $V_{DD33A} \geqslant V_{REFP}$.

(2) CH32H416

- $V_{DD33}$ = 2.4~3.6V: To power some I/O pins and system voltage regulator LDO, including built-in USB2.0 and Ethernet PHY. At the same time, $V_{DD33}$ supplies power to the built-in system voltage regulator LDO and outputs a regulated power supply on the $V_{DD12A}$ and $V_{DDK}$ pins. It is recommended to connect 0.1uF high-frequency capacitors to each externally. The main $V_{DD33}$ (adjacent to the Ethernet signal pin) also needs to be connected to another 4.7uF capacitor in parallel. When used for USB2.0 or Ethernet, the $V_{DD33}$ range is recommended to be 3.2~3.45V.
- $V_{DD33A}$ = 1.8~3.6V: To power the analog part of ADC, temperature sensor, HSADC, OPA, CMP, DAC and PLL, it is recommended to connect an external high-frequency capacitor with 0.1uF capacity. When using HSADC, it is recommended that $V_{DD33A}$ should not be less than 3.0V, and when using ADC and DAC, $V_{DD33A}$ should not be less than 2.4V.
- $V_{DD12A}$ = 1.18~1.28V: To power the built-in USB 3.0 module, it is recommended to connect an external 0.1uF parallel 4.7uF capacity high frequency capacitor. During normal operation, the $V_{DD12A}$ voltage is generated by the system voltage regulator LDO powered by $V_{DD33}$. In order to minimize the heat generated by the LDO of the chip, it can be supplied with an external power supply (which can be generated by an external DC-DC), and it is recommended that the external voltage be slightly higher than the output voltage of the internal LDO.
- $V_{REFP}$ = 2.4~3.6V: For the reference voltage of ADC, HSADC, DAC, it is recommended to connect an external high-frequency capacitor with 0.1uF capacity. $V_{REFP}$ must not be higher than $V_{DD33A}$ voltage.
- $V_{DDK}$ = 1.17~1.27V: To power the core circuits, it is recommended that each be externally connected to a 0.1uF high-frequency capacitor, and that an additional 4.7uF capacitor be connected in parallel. During normal operation, the $V_{DDK}$ voltage is generated by the system voltage regulator LDO powered by $V_{DD33}$. In order to minimize the heat generated by the LDO of the chip, this power supply can be supplied externally (it

can be generated by an external DC-DC), and it is recommended that the voltage supplied externally be slightly higher than the value of the output voltage of the internal LDO.

The above power supply pins with the same name must be shorted, voltage relationship: $V_{DD33}$ = $V_{DD33A}$ and $V_{DD33A} \geq V_{REFP}$.

(3) CH32H415

- $V_{DD33}$ = 2.4~3.6V: To power some I/O pins and system voltage regulator LDO, including built-in USB2.0. At the same time, $V_{DD33}$ supplies power to the built-in system voltage regulator LDO and outputs a regulated power supply on the $V_{DD12A}$ and $V_{DDK}$ pins. It is recommended to connect 0.1uF high-frequency capacitors to each externally. The main $V_{DD33}$ (adjacent to the $V_{DDK}$) also needs to be connected to another 4.7uF capacitor in parallel. When used for USB2.0 or Ethernet, the $V_{DD33}$ range is recommended to be 3.2~3.45V.
- $V_{DD33A}$ = 1.8~3.6V: To power the analog part of ADC, temperature sensor, HSADC, OPA, CMP, DAC and PLL, it is recommended to connect an external high-frequency capacitor with 0.1uF capacity. When using HSADC, it is recommended that $V_{DD33A}$ should not be less than 3.0V, and when using ADC and DAC, $V_{DD33A}$ should not be less than 2.4V.
- $V_{DDK}$ = 1.17~1.27V: To power the core circuits, it is recommended that each be externally connected to a 0.1uF high-frequency capacitor, and that an additional 4.7uF capacitor be connected in parallel. During normal operation, the $V_{DDK}$ voltage is generated by the system voltage regulator LDO powered by $V_{DD33}$. In order to minimize the heat generated by the LDO of the chip, this power supply can be supplied externally (it can be generated by an external DC-DC), and it is recommended that the voltage supplied externally be slightly higher than the value of the output voltage of the internal LDO.

The above power supply pins with the same name must be shorted, voltage relationship: $V_{DD33}$ = $V_{DD33A}$.

### 1.4.4 Power Supply Detector

The power-on reset (POR)/ power-off reset (PDR) circuit is integrated in the chip, which is always in working state. When $V_{DD33}$ is lower than the set threshold ($V_{POR/PDR}$), the device is placed in a reset state without using an external reset circuit.

In addition, the system has a programmable voltage monitor (PVD), which needs to be turned on by software to compare the voltage magnitude of the $V_{DD33}$ supply with the set threshold $V_{PVD}$. Refer to Chapter 3 for $V_{POR/PDR}$ and $V_{PVD}$ values.

### 1.4.5 System Voltage Regulator LDO

After resetting, the system voltage regulator is automatically switched on. There are 2 modes of operation depending on the application mode.

- On mode: Normal running operation, providing stable core power.
- Low-power mode: Low-power operation of the regulator when the CPU is in Standby mode.

### 1.4.6 Low-power Mode

The system supports 2 low-power modes, which can achieve the best balance under the conditions of low power consumption, short start-up time and multiple wake-up events.

- Sleep mode (SLEEP)

In sleep mode, only the CPU clock stops, but all peripheral clocks are powered normally and the peripherals are in

working state. This mode is the shallowest low-power mode, but can achieve the fastest wake-up.

Exit condition: Any interruption or wake-up event.

- Stop mode (STOP)

The stop mode combines the clock control mechanism of peripherals on the basis that both cores V3F and V5F go into deep sleep, and makes the voltage regulator run in a lower power consumption state.

Both V3F and V5F enter this mode: the high frequency clock (HSE/HSI/PLL) domain is turned off, the contents of SRAM and register are kept, and the state of I/O pin is kept. The system can continue to run after this mode wakes up, and HSI is the default system clock.

Exit conditions: any wake-up event (EXTI signal), external reset signal on RST and IWDG reset. Among them, EXTI signal includes one of 95 external I/O ports, RTC alarm clock, SWPMI wake-up signal, LPTIM wake-up signal, I3C wake-up signal, USART wake-up signal, USBPD wake-up signal, Ethernet wake-up signal, USBFS wake-up signal and USBHS wake-up signal.

### 1.4.7 CRC Calculation Unit

The CRC (Cyclic Redundancy Check) Calculation Unit generates a CRC code from a 32-bit data word using a fixed polynomial generator. In numerous applications, CRC-based techniques are used to verify the consistency of data transmission or storage. Within the scope of the EN/IEC 60335-1 standard, which provides a means of detecting errors in flash memory, the CRC calculation unit can be used to compute the signature of software in real time and compare it with the signature generated at the time of linking and generating that software.

### 1.4.8 Programmable Fast Interrupt Controller (PFIC)

The chip has a built-in Programmable Fast Interrupt Controller (PFIC) that supports up to 256 interrupt vectors, providing flexible interrupt management with minimal interrupt latency. The 2 cores in the chip manage 32 private interrupts of each core and share other interrupts. 117 peripheral interrupt sources can be allocated through the configuration register of PFIC. The shared interrupt source can only generate interrupt requests to the assigned core.

- Support hardware interrupt stack (HPE) without instruction overhead
- Provide 4 table-free interrupts (VTF)
- Vector table support address or instruction mode
- Core RISC-V3F supports up to configurable level 2 interrupt nesting
- Core RISC-V5F supports up to configurable level 8 interrupt nesting
- Support low-power sleep and wake-up management

### 1.4.9 External Interrupt/Event Controller (EXTI)

The external interrupt/event controller contains a total of 27 edge detectors for generating interrupt/event requests. Each interrupt line can be configured independently of its trigger event (rising or falling edge or double edge) and can be individually masked; a pending register maintains the status of all interrupt requests. EXTI can detect that the pulse width is smaller than the clock cycle of the internal HB. Up to 95 general purpose I/O ports are optionally connected to 16 external interrupt lines.

### 1.4.10 General DMA Controller

The chip has 2 sets of general-purpose DMA controllers built-in, which manages a total of 16 channels, of which

DMA1 contains 8 channels and DMA2 contains 8 channels. It can flexibly handle high-speed data transfers between memory to memory, peripheral to memory and memory to peripheral, supporting the ring buffer approach. Supports reconfiguration of DMA request lines between peripherals and DMA, and supports software triggering; by configuring related registers, each channel of the DMA can choose to support requests to related peripherals; can configure access priority, transmission length, transmission source and destination address, etc.

DMA is used for the main peripherals including: General-purpose/advanced-control timers TIMx, ADC, DAC, I2S, USART, I2C, SPI, SDIO, SAI, DFSDM, SWPMI, I3C, QSPI, FMC.

*Note: DMA1, DMA2 and CPU access to system SRAM after arbiter arbitration.*

### 1.4.11 Clock and Boot

The system clock source HSI is turned on by default. After no clock is configured or reset, the internal 25MHz RC oscillator is used as the default CPU clock. Then, an external 25MHz clock or PLL clock can be selected. When the clock safety mode is turned on, if the HSE is used as the system clock (direct or indirect), when an external clock failure is detected, the system clock will automatically switch to the internal RC oscillator, and the HSE and PLL will be automatically turned off; for the low-power mode of the clock that turns off, the system will automatically switch to the internal RC oscillator after wake-up. If a clock interrupt is enabled, the software can receive the corresponding interrupt.

### 1.4.12 RTC

The RTC and the backup register are in the backup power supply area within the system, which is powered by the $V_{DD33}$ when the $V_{DD33}$ is valid, and automatically switched to the power supply by the $V_{BAT}$ pin when the $V_{DD33}$ is invalid.

The RTC real-time clock is a set of 32-bit programmable counters with a time base that supports 20-bit prescaling and is used for long-time measurement. The clock reference comes from a high-speed external clock division (HSE/512), an external crystal low frequency oscillator (LSE), or an internal low-power RC oscillator (LSI). Among them, there is also a backup power supply area in LSE, so when LSE is selected as RTC, the setting and time of RTC can remain unchanged after the system resets or wakes up from Stop mode.

### 1.4.13 Analog-to-digital Converter (ADC) and Touch-key Capacitance Detection

The chip has two 12-bit analog/digital converters (ADCs), which use up to 16 external channels and 2 internal channels to sample, and the sampling rate can reach 5Msps. The chip provides programmable channel sampling time, can achieve single, continuous, scan or interrupt conversion, and supports dual ADC conversion mode. Provides analog watchdog function allows very precise monitoring of one or more selected channels for monitoring channel signal voltages, provides configurable analog watchdog reset function to reset the system when monitored voltage exceeds a threshold. Supports external event-triggered transitions. Trigger sources include internal signals from on-chip timers and external pins. Supports operation using DMA.

The internal channels of ADC are ADC_IN16~ADC_IN17 respectively. The temperature sensor is connected to the IN16 input channel; The internal reference voltage $V_{REFINT}$ is connected to the IN17 input channel.

The touch-key capacitance detection unit provides up to 16 detection channels and reuses the external channels of the ADC module. The detection result is converted into the output result by the ADC module, and the touch-key state is identified by the user software.

### 1.4.14 HSADC (High-speed Analog/Digital Converter)

The chip has a built-in 10-bit high-speed analog/digital converter (HSADC), providing samples from up to 7 external channels, with sampling rates up to 20Msps, which can achieve continuous conversion and support DMA operation.

### 1.4.15 DAC (Digital/Analog Converter)

The chip has built-in two 12-bit voltage output digital/analog converters (DACs), which convert 2 digital signals into 2 analog voltage signals and output them. It supports independent or synchronous conversion of dual DAC channels, supports left or right alignment of 12-bit data, supports 12-bit or 8-bit data, and supports external event trigger conversion. It can realize triangular wave and noise generation. Supports DMA function.

### 1.4.16 Timer and Watchdog

Timers in the system include advanced-control timers, general-purpose timers, basic timers, watchdog timers and system time base timers, please refer to Table 1-1 for details.

Table 1-1 Timer comparison

| Timer | | Resolution | Count type | Time base | DMA | Function |
|---|---|---|---|---|---|---|
| ADTM | TIM1<br>TIM8 | 16-bit | Up<br>Down<br>Up/down | 16-bit frequency divider | Support | PWM complementary output, single pulse output<br>Input capture<br>Output comparison<br>Timing count |
| GPTM | TIM2<br>TIM3<br>TIM4<br>TIM5 | 16-bit | Up<br>Down<br>Up/down | 16-bit frequency divider | Support | PWM generation, single pulse output<br>Input capture<br>Output comparison<br>Timing count |
| | TIM9<br>TIM10<br>TIM11<br>TIM12 | 32-bit | Up<br>Down<br>Up/down | 32-bit frequency divider | Support | PWM generation, single pulse output<br>Input capture<br>Output comparison<br>Timing count |
| Basic timer | TIM6<br>TIM7 | 16-bit | Up | 16-bit frequency divider | Support | Timing count |
| Low-power timer | LPTIM1<br>LPTIM2 | 16-bit | Up | 3-bit frequency divider | Not support | Timing count |
| Window Watchdog | | 7-bit | Down | 4 frequency divider | Not support | Timing<br>Reset system (Normal working) |
| Independent Watchdog | | 12-bit | Down | 7 frequency divider | Not support | Timing<br>Reset system (Normal + low power consumption operation) |
| System timebase timer 1 | | 32-bit | Up/down | SYSCLK or SYSCLK/8 | Not support | Timing |
| System timebase | | 32-bit | Up/down | SYSCLK or | Not | Timing |

| | | | | | |
|---|---|---|---|---|---|
| timer 2 | | | SYSCLK/8 | support | |

- Advanced-control timer (TIM1/8)

The Advanced Timer Module consists of two 16-bit auto-loading increment/decrement counters (TIM1 and TIM8) with 16-bit programmable prescalers. In addition to the full general-purpose timer functionality, it can be viewed as a three-phase PWM generator assigned to 6 channels, with complementary PWM outputs with deadband insertion, allowing the timer to be updated for repeated counting cycles after a specified number of counter cycles, a braking function, and more. Many of the features of the Advanced Timer are the same as the General Purpose Timer, and the internal structure is the same, so the Advanced Timer can operate in concert with other TIM timers through the Timer Link function to provide synchronization or event linking capabilities.

- General-purpose timer (TIM2/3/4/5/9/10/11/12)

The general-purpose timer module includes 4×16-bit automatic re-installable timers (TIM2, TIM3, TIM4 and TIM5) and 4 32-bit automatic re-installable timers (TIM9, TIM10, TIM11 and TIM12), which are used to measure the pulse width or generate pulses, PWM waves of specific frequency, etc. Can be used in fields such as automation control and power supply.

TIM2/3/4/5/9/10/11/12 each has 4 independent channels, each supporting input capture, output comparison, PWM generation and single pulse mode output. It can also work with advanced timers through the timer link function to provide synchronization or event link function. In debug mode, the counter can be frozen while the PWM output is disabled, thereby cutting off the switches controlled by these outputs. Any general-purpose timer can be used to generate PWM output. Each timer has an independent DMA request mechanism.

- Basic timer (TIM6/7)

The basic timer module contains 2×16-bit automatic re-installable timers (TIM6 and TIM7) for counting and generating interrupts or DMA requests in update events. TIM6 and TIM7 support 16-bit programmable prescalers. A synchronization circuit that can provide clocks for digital-to-analog conversion (DAC) can be triggered. The basic timers are independent of each other and do not share any resources.

- Low-power timer (LPTIM1/LPTIM2)

LPTIM is a 16-bit upstream count timer, with a 3-bit programmable prescaler, supporting 8 frequency division coefficients (1, 2, 4, 8, 16, 32, 64, 128). Supports continuous/single trigger mode, can select software or hardware input trigger, supports PWM output, and supports I/O polarity configurable.

LPTIM has a variety of optional clock sources, the internal clock source is the LSE, LSI, HSI or PB1 clock, and the external clock source is the external clock on the LPTIM input, LPTIM can operate without the internal clock source, so LPTIM can be used as a 'pulse counter'. In addition, LPTIM can wake up the system from the low-power mode, so LPTIM is very suitable for realizing the 'time-out function' with very low power consumption.

- Independent watchdog (IWDG)

The independent watchdog is a free-running 12-bit decrement counter that supports 7 frequency division coefficients. The clock is provided by an internally independent RC oscillator (LSI) of about 40 kHz; because the LSI is independent of the main clock, it can be run in stop mode. IWDG can work completely independently outside the main program, so it is used to reset the entire system in the event of a problem, or to provide timeout management for the application as a free timer. The option byte can be configured to be a software or hardware startup watchdog. In debug mode, the counter can be frozen.

- Window watchdog (WWDG)

The window watchdog is a 7-bit decrement counter and can be set to run freely. Can be used to reset the entire system when a problem occurs. It is driven by the main clock and has the function of early warning interrupt; in debug mode, the counter can be frozen.

- System time base timer (SysTick)

QingKe microprocessor core comes with two 32-bit optional increment or decrement counters, which is used to generate SYSTICK exceptions (exception number: 12), which can be specially used in real-time operating systems to provide 'heartbeat' rhythm for the system, or can be used as two standard 32-bit counter. It has automatic reload function and programmable clock source.

### 1.4.17 Universal Synchronous/Asynchronous Receiver Transmitter (USART)

The chip provides 8 sets of universal synchronous/asynchronous transceivers (USART1/2/3/4/5/6/7/8). It supports full-duplex asynchronous serial communication, synchronous unidirectional communication as well as half duplex single line communication, also LIN (Local Interconnect Network), compatible IrDA SIR ENDEC transmission codec specification, as well as modem (CTS/RTS hardware flow control) operation, and also supports multi-processor communication. It uses a fractional baud rate generator system and supports continuous communication by DMA operation.

### 1.4.18 Serial Peripheral Interface (SPI)

The chip provides 4 serial peripheral SPI interface (SPI1/2/3/4), support master or slave operation, dynamic switching. Support multi-master mode, full-duplex or half-duplex synchronous transmission, support basic SD card and MMC mode. Programmable clock polarity and phase, data bit width provides 8- or 16-bit selection, hardware CRC generation/check for reliable communication, and continuous communication support for DMA operation.

### 1.4.19 I2S (Audio) Interface

Up to 2 sets of standard I2S interfaces (multiplexed with SPI2 and SPI3) operate in master or slave mode. The software can be configured to transmit frames for 16/24/32-bit packets, supports audio sampling frequency from 8kHz to 562.2kHz, and supports 4 audio standards. In main mode, its main clock can be output to an external DAC or CODEC (decoder) at a fixed 256x audio sampling frequency, supporting DMA.

### 1.4.20 QSPI Interface

The chip has built-in 2 sets of dedicated QuadSPI, connect single, dual or quad (one data line) SPI FLASH memory media. The main features are:

- 3 functional modes: indirect mode, state polling mode and memory mapped mode
- Dual Flash mode, by accessing 2 FLASHs in parallel
- Integrated FIFO for transmit and receive
- SDR mode support
- Fully programmable frame format for indirect and memory-mapped modes
- Fully programmable opcodes for indirect and memory-mapped modes
- Generates DMA trigger signals when FIFO threshold is reached and transmission is complete
- Generates interrupts when FIFO threshold is reached, timeout occurs, operation is complete, and an access

error occurs Generates interrupts on FIFO threshold, timeout, operation completion, and access error

### 1.4.21 I2C Bus

The chip provides 4 I2C bus interfaces, capable of working in multi-master or slave mode, performing all I2C bus specific timing, protocols, arbitration, etc. Both standard and fast communication speeds are supported and it is also compatible with SMBus 2.0.

The I2C interface provides 7-bit or 10-bit addressing, and supports dual slave addressing in 7-bit Slave mode. It integrates built-in hardware CRC generator/checker. It also supports DMA operation and supports SMBus bus version 2.0/PMBus bus.

### 1.4.22 I3C Bus

The I3C bus is a 2-wire serial single-ended multi-branch bus designed to improve the traditional I2C bus. The I3C interface is responsible for handling communication between the device and other devices connected to the I3C bus. It itself supports both as a master and a slave, and when used as a controller, it can enhance the functionality of the I2C interface while maintaining a certain degree of backward compatibility. The main features include:

- Support master/slave device
- Support MIPI I3C specification v1.1
- Support multi-host function
- Support DMA
- Support In-Band Interrupt (IBI) function
- Built-in error detection and recovery
- I3C SCL bus clocking up to 12.5MHz
- Support dynamically assigned addresses, direct and broadcast Common Command Code (CCC), and private read/write transfers

### 1.4.23 USB PD and Type-C Controller (USB PD)

Built-in USB Power Delivery controller and PD physical layer transceiver PHY support USB Type-C master-slave detection, automatic BMC codec and CRC, and CC pin supports hardware edge control.

Support USB PD2.0 and PD3.0 and PD3.2 power transmission, support SPR and EPR, support 100W or 240W fast charging, support PD power receiving terminal Sink and PD power supply terminal Source and DRP application. Support PDUSB, UFP, DFP and DRD applications.

Among them, the CC pins PB3/CC1R and PB4/CC2R of CH32H416RdU6 chip have built-in controllable RD pull-down resistors 5K1 defined by the Type-C specification.

### 1.4.24 Universal Serial Bus USB2.0 Full-speed Host/Device Controller (USBFS/OTG_FS)

USB2.0 full-speed host controller and device controller (USBFS), complies with USB2.0 full-speed standard. Provides 16 configurable USB device endpoints and a set of host endpoints. Supports control/batch/synchronous/interrupt transmission, dual buffer mechanism, USB bus suspend/recover operation, and provides standby/wake-up function.

The OTG_FS is a dual role USB controller that supports both host-side and device-side functionality and is compatible with the On-The-Go Supplement to the USB 2.0 specification. The controller can also be configured to support host-side only or device-side only functionality, compatible with the USB 2.0 Full Speed specification. Key

features include:

- Supports the OTG protocol defined as an optional item in the (Physical Layer of the OTG_FS Controller) USB On-The-Go Supplement, Revision 1.3 specification
- Configurable through software for USB full-speed hosts, USB full-speed/low-speed devices, and USB dual-role devices
- Provide power-saving features
- Support control transfers, bulk transfers, interrupt transfers, real-time/synchronous transfers
- Provide bus reset, hang, wake-up, and resume
- Support packets up to 64 bytes, built-in FIFO, support interrupt and DMA

### 1.4.25 Universal Serial Bus USB2.0 High-speed Host/Device Controller (USBHS)

The USB2.0 high-speed controller has dual roles of host controller and device controller, and has a built-in USB-PHY physical layer transceiver with 480Mbps. When used as a host controller, it supports low-speed, full-speed and high-speed USB devices. When used as a device controller, it can be flexibly set to low-speed, full-speed or high-speed modes to suit a variety of applications. The main features include:

- Support USB 2.1, USB 2.0, USB 1.1, USB 1.0 protocol specifications
- Support USB Host function and USB Device function
- Support control transfer, lot transfer, interrupt transfer, real-time/synchronous transfer
- Provide bus reset, suspend, wake-up and resume functions
- Host support USB HUB
- Non-0 endpoints support up to 1024-byte packets, built-in FIFO, support for interrupts and DMA
- Support USART or I2C pin mapping. The host can be used for 2-wire debugging

### 1.4.26 Universal Serial Bus USB2.0 SuperSpeed Host/Device Controller (USBSS)

The USB3.0 SuperSpeed controller has the dual role of host controller and device controller. It has a built-in ultra-high-speed USBPHY physical layer transceiver, which can realize the USB3.0 interface product functions and supports 5Gbps USBSS ultra-high-speed signal.

This controller module provides a link layer register access interface for application code to manage device connection and disconnection, bus status, and power mode. It provides a host (HOST) function access interface and a device (DEVICE) function access interface, which is used to implement various data transmission and upper-layer protocols for the USB3.0 protocol specification. The main features include:

- Support USB 3.0 protocol specification and USB 3.2 Gen1
- Support USB Host function and USB Device function
- Power management mode supports U1/U2/U3 low-power state
- Support driving USB 3.0 HUB
- Support control transmission, lot transmission, interrupt transmission, real-time/synchronous transmission
- Non-0 endpoints support packets up to 1024 bytes and burst mode
- Support DMA to directly access the data in the buffer of each endpoint
- Self-developed controller and transceiver, high-speed integrated design, measured 450Mbytes per second

### 1.4.27 Serial-parallel Interchange Controller and Transceiver (SerDes)

The chip has built-in SerDes module that supports signal isolation and long-distance transmission, and supports 1.5Gbps high-speed differential signals (SERDES_RXP, SERDES_RXN, SERDES_TXP, SERDES_TXN pins).

Long-distance data transmission can be carried out through a differential peer-to-peer transmission media in the optical fiber module or network cable. The main features include:

- Programmable transmission data rate, supports up to 1.5Gbps
- Supports network transformer high-voltage signal isolation, also supports capacitive low-voltage isolation
- Built-in 8bit/10bit codec and CRC checksum, support serial number matching
- Built-in FIFO, support send/receive double-buffer mode
- Support DMA function, access address support byte alignment
- Provide a variety of transmission interrupt flags and status, and timely feedback information to the application layer
- Differential transceiver, can directly drive fiber optic modules

### 1.4.28 Controller Area Network (CAN)

The chip has 3 sets of CAN interfaces, compatible with specifications 2.0A and 2.0B (active), with a baud rate of up to 1Mbits/s, and supports time-triggered communication function. Standard frames with 11-bit identifiers can be received and sent, or extended frames with 29-bit identifiers can be received and sent. With 3 sending mailboxes and two 3-level deep receiving FIFO.

### 1.4.29 Digital Video Port (DVP)

DVP (Digital Video Port) is used to connect the camera module to obtain image data stream. It provides 8/10/12-bit parallel interface communication, and supports up to 150MHz pixel clock input frequency. It supports image data organized in the original row and frame format, such as YUV, RGB, etc., and also supports compressed image data such as JPEG format, which can receive high-speed parallel data streams output by external 8-bit, 10-bit, and 12-bit camera modules. During reception, it mainly relies on VSYNC and HSYNC signal synchronization. Supports image cropping function.

### 1.4.30 Random Number Generator (RNG)

The chip has a built-in hardware random number generator, based on continuous analog noise, which provides a 32-bit random number through internal analog circuitry.

### 1.4.31 Ethernet Controller and Transceiver (MAC+PHY)

The chip has a built-in Gigabit Ethernet controller (MAC) that complies with IEEE802.3-2002 standards, which acts as the data link layer. Its Link speed supports up to 1Gbps, supports Gigabit, 100Mbps, and 10Mbps speeds with auto-negotiation, and provides an RGMII interface to connect to external PHY chips. When applying, the development of network products is achieved by combining the TCP/IP protocol stack.

The CH32H417 chip also has a built-in 10/100Mbps Ethernet PHY physical layer transceiver. Single chip can realize Ethernet communication. The main features include:

- Conforms to IEEE 802.3 protocol specification and design
- Provide RGMII interface to connect external Ethernet PHY transceiver
- Support full-duplex operation and 10/100/1000Mbps data transmission rate
- Hardware Automatic IPv4 and IPv6 packet integrity check, IP/ICMP/UDP/TCP packet checksum calculation and auto-filling
- Multiple MAC address filtering modes
- Support LED
- SMI interface to configure and manage the external PHYs

- Support Ethernet controller MAC + built-in 10/100Mbps PHY
- Optional Ethernet controller MAC + external 1Gbps PHY
- Support Auto-MDIX switching of RX/TX and automatic identification of positive and negative signal lines

### 1.4.32 SIDO Host/Device Controller

The SDIO host interface provides the operation interface of multimedia card (MMC), SD memory card, SDIO card and CE-ATA device. Supports 3 different data bus modes: 1-bit (default), 4-bit and 8-bit. In 8-bit mode, the clock for data transmission over this interface can reach up to 100MHz. Currently, this interface is fully compatible with multimedia card system specification 4.5 (forward compatible), SDIO card specification 2.0, SD memory card specification 2.0, and CE-ATA digital protocol specification 1.1. The main features include:

- Support SD card, SDIO card and MMC card
- Support 1-bit, 4-bit and 8-bit bus modes
- Maximum communication clock up to 100MHz
- Compatible with MMC specification 4.5 (forward compatible)
- Compatible with SD card Specification 2.0, SDIO card specification 2.0
- Not compatible with SPI and QSPI

### 1.4.33 SD/EMMC Host/Device Controller (SDMMC)

The chip integrates one SDMMC controller with host/slave interfaces, supporting a maximum transmission clock of 200MHz. It accommodates 1-wire, 4-wire, and 8-wire communication modes, along with single-edge and dual-edge sampling. External devices such as SD/TF cards and eMMC cards can be connected. The application code can flexibly set various commands, response packets, valid data packets, and double buffer length switching limits for data transmission and reception.

- Support SD physical layer 1.0 and 2.0 specifications, and UHS-I SDR50, DDR50 and SDR104 modes of SD3.0 specification
- Conform to the 4.4 and 4.5.1 specifications of EMMC card; supports HS200 and HS400 of EMMC card 5.0 specification
- Communication modes support 1-wire, 4-wire, and 8-wire modes
- Maximum communication clock: single edge up to 200MHz, dual edge up to 180MHz
- Support double-edge sampling
- Flexible and configurable packet lengths, command formats, and response states
- Provide hardware to stop the clock function automatically at the interval of data block
- Support SD card, SDIO card, EMMC card and other devices that conform to the SD interface protocol
- Support SDIO slave interface, which can complete the data exchange of the chip that supports the SDIO host interface.
- DMA double buffer function

### 1.4.34 Programmable Protocol I/O Controller (PIOC)

The programmable protocol I/O controller is based on a dedicated thin instruction set RISC core with a single clock cycle. It runs at the main frequency of the system. It has a program ROM with 2K instructions, 49 SFR registers and PWM timing/counter, and supports protocol control of 2 I/O pins.

- RISC core, optimized single-cycle bit-operated instruction set, full static instruction set
- Reuse 4K-byte system SRAM as 2K-word capacity program ROM, supports program pause and dynamic

loading

- Provide 33-byte bi-directional and uni-directional registers each, provides 6-level independent Stack
- Support 2 general-purpose bi-directional I/O protocol control and input level change detection
- Support 1-wire and 2-wire interfaces with multiple protocol specifications by dynamically loading different protocol programs
- Support 1024 levels of serial connection of 1-wire ARGB chip

### 1.4.35 Serial Audio Interface (SAI)

The chip has a built-in set of serial audio interfaces (SAI), which supports I2S standard, LSB or MSB alignment, PCM/DSP, TDM and AC'97 and other audio protocols. It is suitable for mono and stereo applications and supports SPDIF output. In order to achieve the flexibility and configurability of the SAI interface, SAI includes 2 sets of control modules in A/B, each set of modules containing up to 4 I/O pins (SD, SCK, FS and MCLK).

The SAI can be configured in any combination of master/slave, transmit/receive, and depending on the audio submodule synchronous/asynchronous configuration, its mode of operation can be set to full duplex/simplex.

- Support a wide range of audio protocols such as I2S standard, LSB or MSB alignment, PCM/DSP, TDM and AC'97
- Provide 2 groups of independent control modules, each audio submodule can be configured as any combination of Master/Slave, Transmit/Receive, and both have an 8-word FIFO
- The 2 groups of control modules, A and B, can be in synchronous or asynchronous mode, and the master/slave configurations are independent of each other
- Up to 16 Slots, each Slot supports a size of 8-bit, 10-bit, 16-bit, 20-bit, 24-bit, or 32-bit data
- Support SPDIF output
- Frame Synchronization Configuration (active level, active length and offset)
- Support LSB or MSB data transfer
- Support Stereo/Mono audio functionality with mute mode
- Serial Clock Selection Edge Selection (SCK)
- Each audio submodule has 2 independent DMA interfaces supporting slave mode at frequencies up to 4MHz
- Error flag bits and interrupt sources:

- FIFO overflow and underflow
- Frame synchronization advance detection in slave mode
- Frame synchronization lag detection in slave mode
- AC'97 codec is not ready.
- Clock configuration error

### 1.4.36 Single-wire Protocol Master Interface (SWPMI)

Single-wire Protocol Master Interface (SWPMI) is a full-duplex single-wire communication technology. This technology implements single-wire protocol (SWP) communication based on the ETSITS102613 standard specification.

In SWPMI, data can be transmitted in 2 physical ways: The first is to realize data transmission from the master device to the slave device through the voltage domain (S1 signal); the second is to realize data transmission from the slave device to the master device through the current domain (S2 signal). The S1 signal is transmitted using a digital modulation method of pulse width modulation, while the S2 signal transmits data from the current change. Its main characteristics are as follows:

- Support full-duplex communication mode
- Support automatic handling of fill bits
- Support automatic SWP bus state management
- Provide send-back mode for testing
- Support automatic handling of start of frame (SOF) and automatic handling of end of frame (EOF)
- Support bit rate configurable up to 2 Mbit/s and interrupt configurable
- Provide CRC error, underflow, overflow, and recovery from device monitoring flags
- Support CRC-16 calculation, generation, and checking

### 1.4.37 Universal High-Speed Interface (UHSIF)

The chip has a built-in set of universal high-speed interfaces UHSIF, the transmission clock can reach up to 125MHz, supports 8-bit, 16-bit or 32-bit data width, and the theoretical maximum speed is 500Mbytes/s.

### 1.4.38 OPA

The chip has 3 sets of independently configured low offset voltage op amps (OPA1/2/3) built-in, and can also be used as voltage comparators. The inputs and outputs of each op amp can be selected for multiple channels by changing configurations. OPA1 also has an additional internal output channel directly connected to the input terminal of CMP CMP_P2. All 3 OPAs support programmable gain op amps (PGAs), support high-speed mode, and can increase the slew rate by setting high-speed mode.

### 1.4.39 CMP

A set of rail-to-rail universal voltage comparators that support optional hysteresis characteristics and digital filtering. The inputs of the voltage comparator CMP_P0~CMP_P1 and CMP_N0~CMP_N1 are respectively connected to the GPIO, while the other inputs CMP_P2 and CMP_N2 are connected to the output channels of OPA1 and DAC2 within the chip, respectively; the voltage comparison results can be selected by the configuration bit CMP_MODE or multiplexed into the internal sampling channel of the TIM (the control that releases I/O for other purposes).

### 1.4.40 LCD-TFT Display Controller (LTDC)

LCD-TFT (Liquid Crystal Display-Thin Film Transistor) Display Controller (LTDC) mainly provides parallel digital RGB and horizontal synchronization, vertical synchronization, pixel clock and data enabled signals, which can be used as output signals to different LCD and TFT panel interfaces. Its main characteristics are:

- Provide 24-bit RGB parallel pixel output: 8 bits per pixel (RGB888)
- Provide 2 display layers containing proprietary 8*256-bit FIFOs
- Support Color Look-Up Tables (CLUT) with up to 256 colors per layer
- Support Programmable timing of different display panels
- Support programmable background colors
- Support programmable polarity of HSYNC, VSYNC and data enable signals
- Up to 8 input color formats per display layer: ARGB8888, RGB888, RGB565, ARGB1555, ARGB4444, L8 (8-bit luminance or CLUT), AL44 (4-bit alpha + 4-bit luminance), AL88 (8-bit alpha + 8-bit luminance)
- Support flexible blending between 2 layers using alpha values (per pixel or constant)
- Support color keying (transparent colors)
- Support programmable window position and size
- Support thin-film transistor (TFT) color displays
- Support up to 3 programmable interrupt times

### 1.4.41 Graphics Processing Hardware Accelerator (GPHA)

GPHA is a DMA specially used for image processing. Provides indexed color mode and direct color mode, supporting all classic color coding schemes, supporting 4 bits per pixel to up to 32 bits. In addition, the GPHA module also comes with its own proprietary color lookup table (CULT). Its main characteristics are:

- Support single HB master device bus architecture
- HB slave programming interface supports 8/16/32-bit access (except 32-bit CLUT access)
- Support programmable source and target area sizes and offsets
- Support user-programmable source address and target address
- Support adjustable Alpha values (source, fixed, modulated)
- Support mixing of up to 2 sources
- Support programmable source and target color formats, up to 11 color formats and up to 32 bits per pixel
- Support 2 internal memories for storing CLUTs in indirect color mode
- Support programmable CLUT size, either by automatic loading of CLUTs by the CPU or by programmed CLUTs
- Support internal timer to control the bandwidth of the HB
- Support 3 modes of operation are supported: register-to-memory, memory-to-memory with pixel format conversion, memory-to-memory with pixel format conversion and blending.
- Support filling a specified part or all of the target image with a specific color.
- Support copying part or all of the source image to the corresponding part or all of the target image.
- Support pixel format conversion copying from part or all of a source image to part or all of a target image
- Support blending parts and/or all of 2 source images with different pixel formats, and then copying the result to a part or all of the target image with a different color format
- Support aborting, suspending GPHA running
- Support for generating an interrupt in case of a bus error or access conflict
- Support for generating an interrupt on process completion

### 1.4.42 Flexible Memory Controller (FMC)

The FMC module incorporates a configurable static memory controller (FSMC), synchronous dynamic random-access memory (SDRAM), and an HB interface. It supports devices such as SRAM, SDRAM, PSRAM, NOR, and NAND. The module converts internal HB transmission signals into compatible external communication protocols and flexibly configures sampling delay times to meet the timing requirements of various devices.

In addition, the FSMC controller can also be used to interface with most graphics LCD controllers. It supports Intel 8080 and Motorola 6800 modes, making it easy to build simple graphics application environments or high-performance solutions for specialized acceleration controllers.

The main features of the FMC module are:

- Support connection to SRAM, SDRAM, PSRAM, NOR, and NAND devices
- Support burst mode for faster access to NOR, PSRAM, and SDRAM
- Support programmable continuous clock outputs for asynchronous and synchronous access
- Support sequential access to 8/16/32-bit data
- Support independent chip select control and independent configuration for each memory area
- Support write enable and byte channel select outputs
- Support external asynchronous wait control
- Support 16*32-bit deep write FIFOs
- SDRAM supports cacheable 6*32-bit deep read FIFO (6*14-bit address tag)

- Support DMA mode for accessing storage devices

### 1.4.43 Digital Filter for ΣΔ Modulator (DFSDM)

The DFSDM is a high-performance module dedicated to connecting external ΣΔ modulators to MCUs. It includes 2 external digital serial interfaces and 2 digital filters with flexible ΣΔ digital processing options, providing up to 24-bit ADC final resolution. DFSDM also features selectable parallel data stream inputs from the internal ADC peripheral or device memory. Key features are:

- Provide 2 multiplexed input digital serial channels
- 2 internal digital parallel channels support optional inputs
- Support adjustable digital signal processing
- Support up to 24-bit output data resolution
- Support signed Data format
- Support automatic data offset correction (offset values are stored in registers by the user)
- Include 2 conversion modes: single conversion mode and continuous conversion mode
- Conversions can be turned on synchronously by software trigger, internal timer, external event, or by using the first DFSDM filter
- Support analog watchdog
- Built-in short-circuit detector to detect saturated analog input values (lower and upper limits)
- Support generating breaks when analog watchdog events and short-circuit monitoring events occur
- Built-in extreme value detector
- Support Interrupt and DMA

### 1.4.44 Encryption Module (ECDC)

The chip has built-in packet cipher algorithm module, which supports two packet cipher algorithms, AES and SM4, as well as electronic cipher book (ECB) and counter (CTR) modes. The module completes an encryption and decryption process with 128-bit data size as the basic unit, providing DMA encryption and decryption of data in memory and a single encryption and decryption mode of SFR registers. Its main characteristics are:

- ECB and CTR modes for 128-bit key of SM4 algorithm
- ECB and CTR modes for 128/192/256-bit key of AES algorithm
- Support direct encryption and decryption of a single 128-bit block of data in the way of writing SFR by software
- Support DMA (memory to memory) encryption and decryption of software-specified data blocks.

### 1.4.45 General-purpose Input/Output Interface (GPIO)

The chip has built-in 6 groups of GPIO ports (PA0~PA15, PB0~PB15, PC0~PC15, PD0~PD15, PE0~PE15, PF0~PF14), totaling 95 GPIO pins. Most of the pins can be configured by software as outputs (push-pull or open-drain), inputs (with or without pull-ups or pull-downs), or multiplexed peripheral function ports.

Pins PA9 to PA12, PC13 to PC15, and PE3 to PE6 are powered by $V_{DD33}$, rated at 3.3V. Among them, pins PC13 to PC15 are automatically switched to be powered by $V_{BAT}$ when $V_{DD33}$ is powered down.

Pins PA0 to PA8, PB2 to PB7, PB15, PC4 to PC5, PD8, PE2, PF6 to PF10 are powered by $V_{DDIO}$, rated 3.3V power supply, and support 1.8V, 2.5V, and 3.3V power supply.

High-speed pins PA13 to PA15, PB0 to PB1, PB10 to PB14, PC0 to PC3, PC6 to PC12, PD0 to PD7, PD9 to PD15, PE0 to PE1, PE7 to PE15, PF0 to PF5, and PF11 to PF14 are powered by $V_{IO18}$, with built-in voltage

regulator for the I/O pins, and support 1.2V, 1.8V, 2.5V, 3.3V and supports dynamic power supply voltage switching, and supports XO pin to configure the default voltage after power-on. Please refer to [12:9] fields of PWR_CTLR register in *CH32H417RM* for specific configuration information.

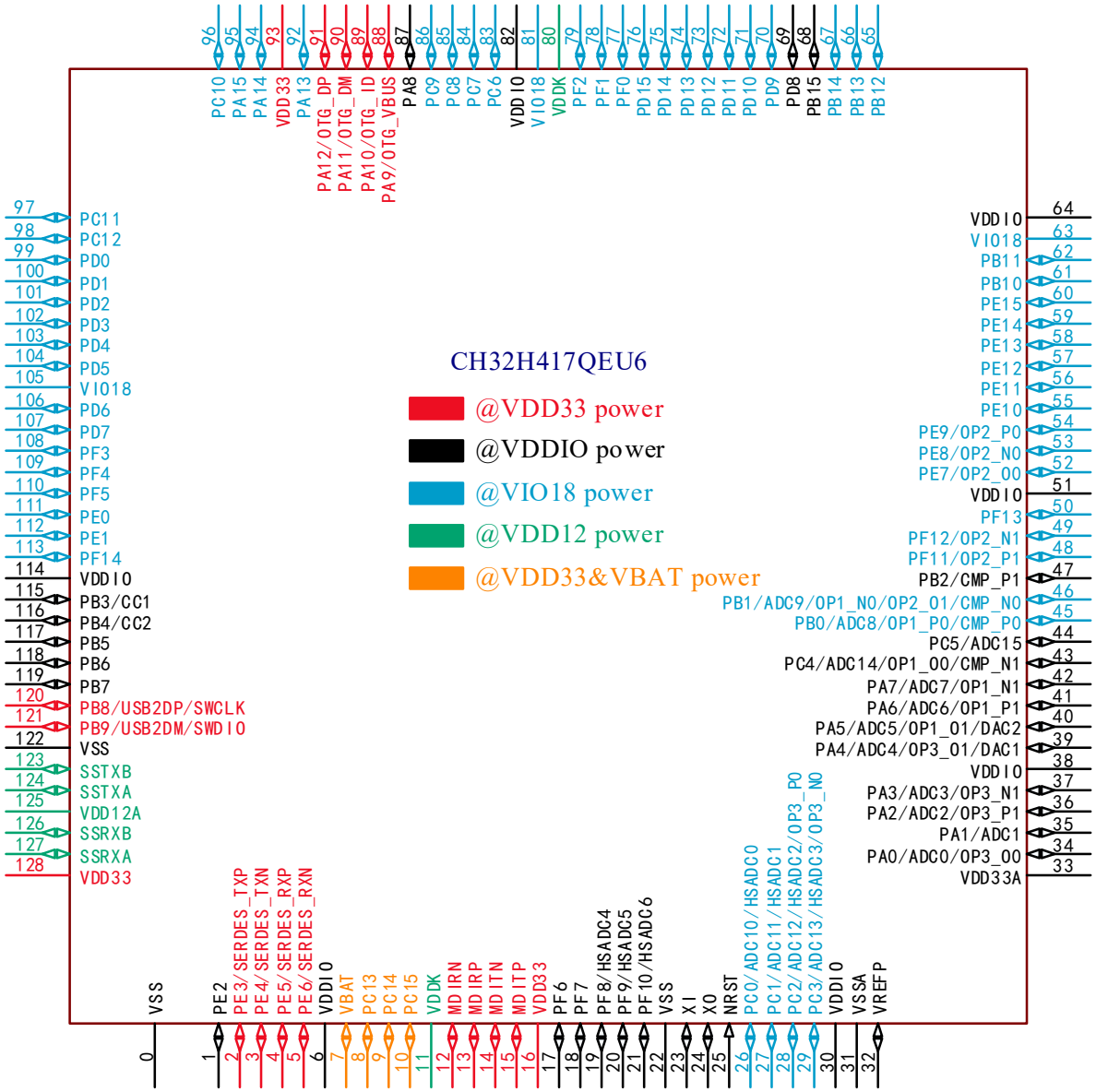
### 1.4.46 Serial Debug Interface (SDI)

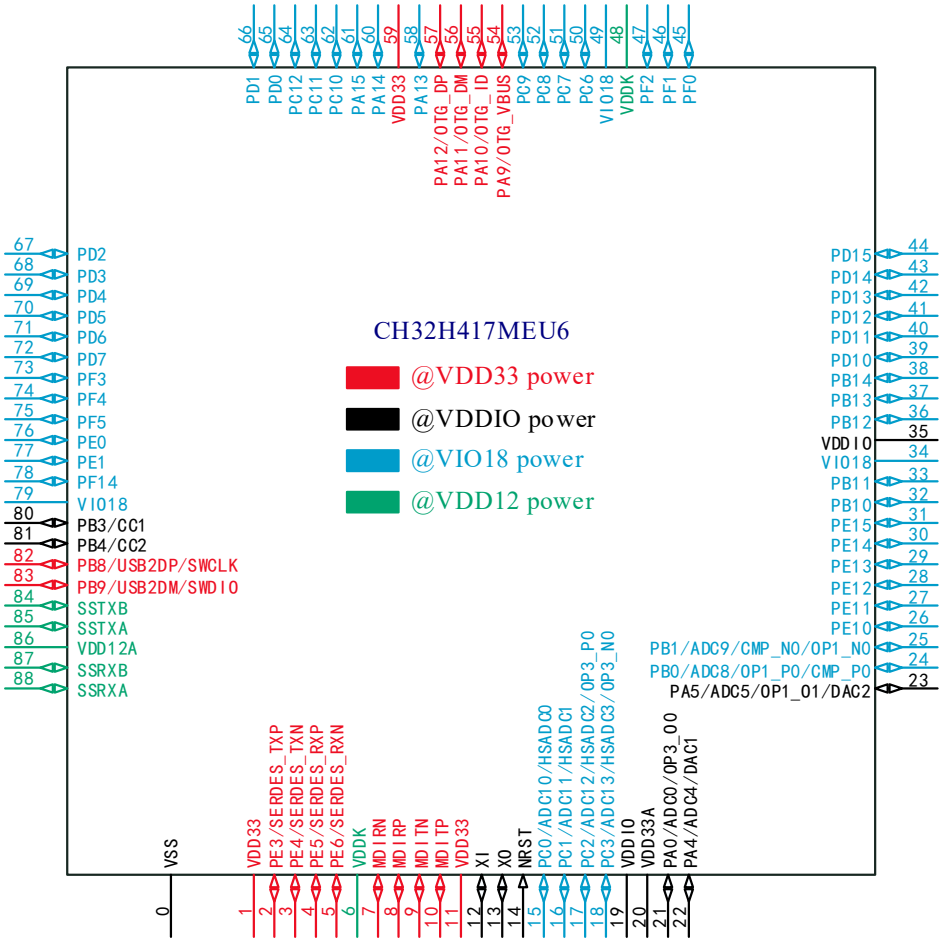
The core comes with a 1-wire SDI Serial Debug Interface and a 2-wire SDI Serial Debug Interface. The system supports 2 debugging modes: 1-wire debugging is the default debugging mode, which corresponds to the SWIO pin (Single Wire Input Output), while 2-wire debugging corresponds to the SWDIO and SWCLK pins, which can be used to increase the speed of downloading. The default debugging interface pins are turned on after the system is powered on or reset, and the SDI can be turned off as needed after the main program is run.

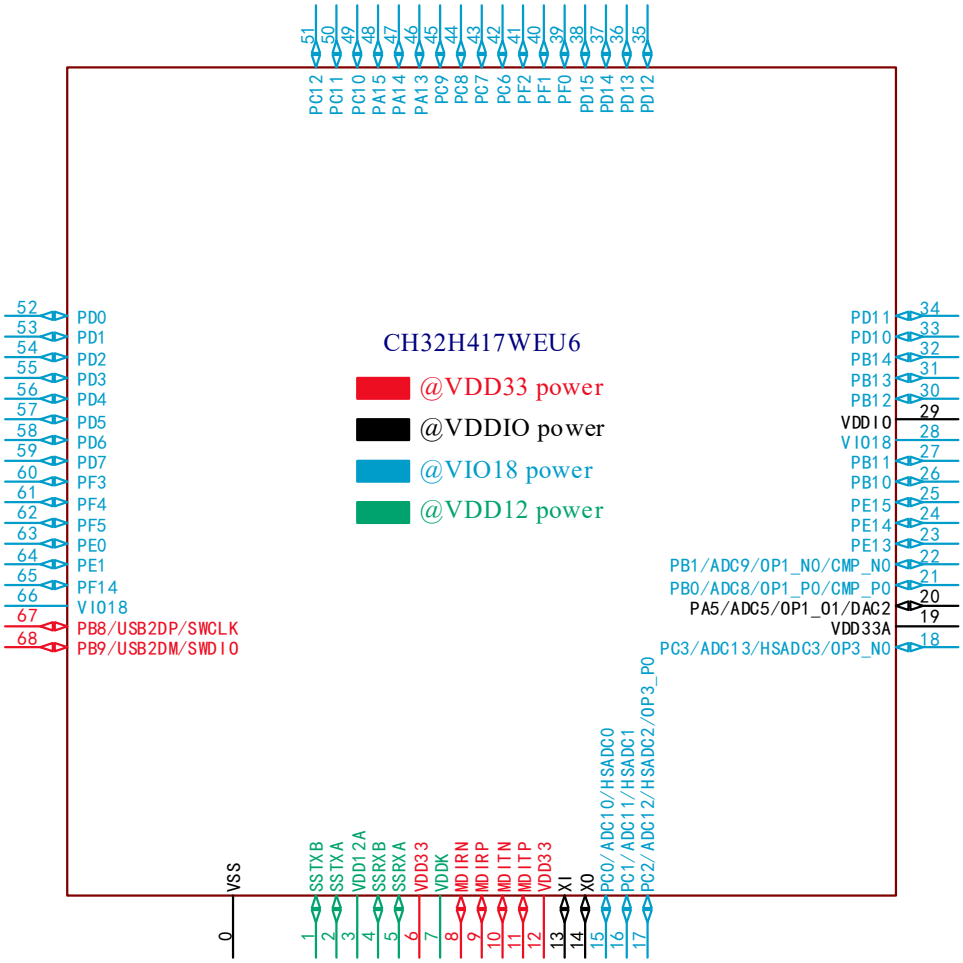
# Chapter 2 Pinouts and Pin Definition

## 2.1 Pinouts

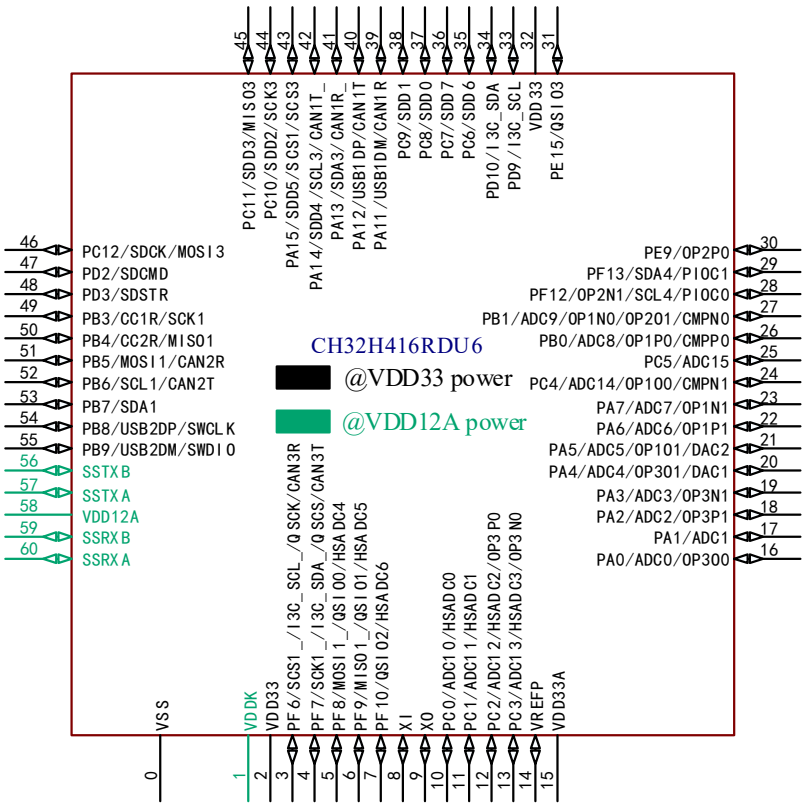
### 2.1.1 CH32H417 Pinouts



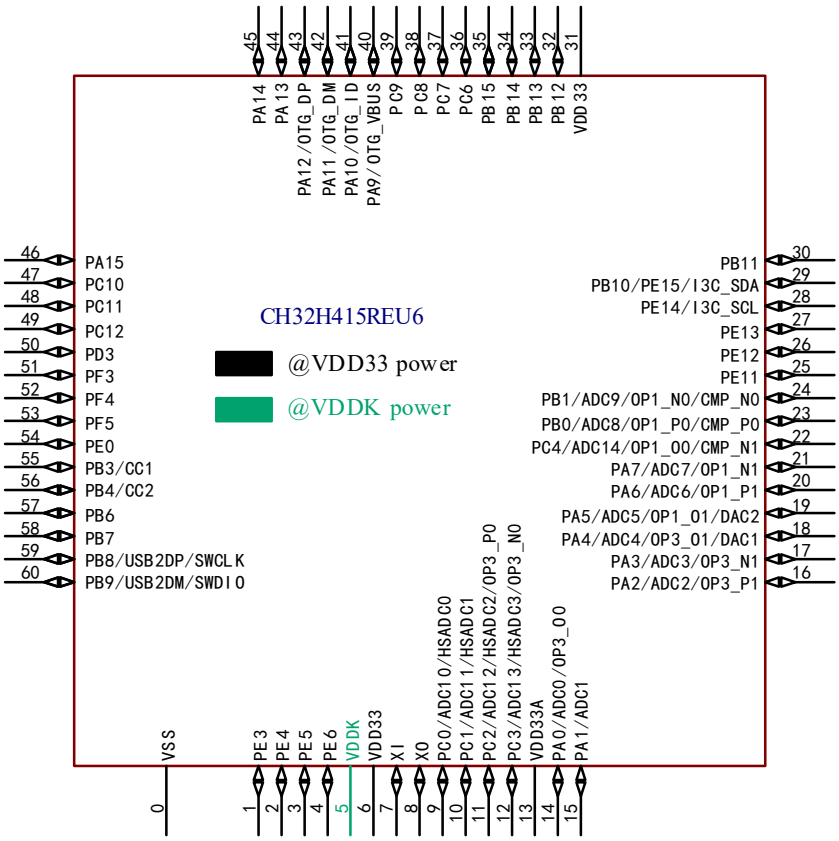

CH32H417MEU6
@VDD33 power
@VDDIO power
@VIO18 power
@VDD12 power
PD1
PD0
PC12
PC11
PC10
PA15
PA14
VDD33
PA13
PA12/OTG_DP
PA11/OTG_DM
PA10/OTG_ID
PA9/OTG_VBUS
PC9
PC8
PC7
PC6
VIO18
VDDK
PF2
PF1
PF0
PD2
PD3
PD4
PD5
PD6
PD7
PF3
PF4
PF5
PE0
PE1
PF14
VIO18
PB3/CC1
PB4/CC2
PB8/USB2DP/SWCLK
PB9/USB2DM/SWDIO
SSTXB
SSTXA
VDD12A
SSRXB
SSRXA
PD15
PD14
PD13
PD12
PD11
PD10
PB14
PB13
PB12
VDDIO
VIO18
PB11
PB10
PE15
PE14
PE13
PE12
PE11
PE10
PB1/ADC9/CMP_NO/OP1_NO
PB0/ADC8/OP1_PO/CMP_PO
PA5/ADC5/OP1_O1/DAC2
VSS
VDD33
PE3/SERDES_TXP
PE4/SERDES_TXN
PE5/SERDES_RXP
PE6/SERDES_RXN
VDDK
MDIRN
MDIRP
MDITN
MDITP
VDD33
XI
XO
NRST
PC0/ADC10/HSADC0
PC1/ADC11/HSADC1
PC2/ADC12/HSADC2/OP3_PO
PC3/ADC13/HSADC3/OP3_NO
VDDIO
VDD33A
PA0/ADC0/OP3_OO
PA4/ADC4/DAC1


CH32H417WEU6
@VDD33 power
@VDDIO power
@VIO18 power
@VDD12 power
PC12
PC11
PC10
PA15
PA14
PA13
PC9
PC8
PC7
PC6
PF2
PF1
PF0
PD15
PD14
PD13
PD12
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PF3
PF4
PF5
PE0
PE1
PF14
VIO18
PB8/USB2DP/SWCLK
PB9/USB2DM/SWDIO
PD11
PD10
PB14
PB13
PB12
VDDIO
VIO18
PB11
PB10
PE15
PE14
PE13
PB1/ADC9/OP1_NO/CMP_NO
PB0/ADC8/OP1_PO/CMP_PO
PA5/ADC5/OP1_O1/DAC2
VDD33A
PC3/ADC13/HSADC3/OP3_NO
VSS
SSTXB
SSTXA
VDD12A
SSRXB
SSRXA
VDD33
VDDK
MDIRN
MDIRP
MDITN
MDITP
VDD33
XI
XO
PC0/ADC10/HSADC0
PC1/ADC11/HSADC1
PC2/ADC12/HSADC2/OP3_PO

### 2.1.2 CH32H416 Pinouts



### 2.1.3 CH32H415 Pinouts




*Note: The alternate functions in the pin diagram are abbreviated.*

Example: ADC_: (ADC0:ADC_IN0)

HSADC_: (HSADC4:HSADC_IN4)

DAC_: (DAC1:DAC_OUT1)

USB2DP: USBHS_DP

USB2DN: USBHS_DN

SSRXA: USBSS_RXA

SSRXB: USBSS_RXB

SSTXA: USBSS_TXA

SSTXB: USBSS_TXB

OP: OPA_(OP1_P1:OPA1_P1, OP1_N1:OPA1_N1, OP1_O1:OPA1_OUT1)

## 2.2 Pin Description

Note that the pin function descriptions in the table below are for all functions and do not refer to specific chip models. Peripheral resources may vary from model to model, so please check the availability of this function against the chip model resource table before viewing.

Table 2-1-1 CH32H417 Pin definitions

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| 0 | 0 | 0 | $V_{SS}$ | P | - | $V_{SS}$ | | |
| 6 | 1 | - | $V_{DD33}$ | P | - | $V_{DD33}$ | | |
| - | - | 1 | PE2 | I/O | FT | PE2 | USART5_RX(AF4)/SPI4_SCK(AF5)/ SAI_MCLK_A(AF6)/USART6_CK(AF8)/ SDRAM_CLK(AF9)/FSMC_A23(AF12)/ DVP_D2(AF13)/LTDC_R6(AF14) | |
| - | 2 | 2 | PE3 | I/O/ SDP | - | PE3 | SERDES_TXP/TIM8_CH1(AF0)/ SDRAM_DQM2(AF1)/TIM4_CH1(AF2)/ TIM12_CH1(AF3)/PIOC_IO0(AF5)/ SAI_SD_B(AF6)/SDRAM_CS_N0(AF9)/ USART5_TX(AF11)/FSMC_A19(AF12)/ DVP_D3(AF13) | |
| - | 3 | 3 | PE4 | I/O/ SDP | - | PE4 | SERDES_TXN/TIM8_CH2(AF0)/ TIM4_CH2(AF2)/TIM12_CH2(AF3)/ PIOC_IO1(AF4)/SPI4_NSS(AF5)/ SAI_FS_A(AF6)/SDRAM_CS_N1(AF9)/ FSMC_A20(AF12)/DVP_D4(AF13)/ LTDC_B0(AF14) | |
| - | 4 | 4 | PE5 | I/O/ SDP | - | PE5 | SERDES_RXP/TIM8_CH3(AF0)/ TIM4_CH3(AF2)/TIM12_CH3(AF3)/ TIM9_CH3(AF4)/SPI4_MISO(AF5)/ SAI_SCK_A(AF6)/SDRAM_CKE0(AF9)/ SDRAM_D27(AF10)/FSMC_A21(AF12)/ DVP_D6(AF13)/LTDC_G0(AF14) | |
| - | 5 | 5 | PE6 | I/O/ SDP | - | PE6 | SERDES_RXN/TIM8_CH4(AF0)/ TIM1_BKIN2(AF1)/TIM4_CH4(AF2)/ TIM12_CH4(AF3)/TIM9_CH4(AF4)/ SPI4_MOSI(AF5)/SAI_SD_A(AF6)/ SDRAM_CKE1(AF7)/USART8_CK(AF8)/ SDRAM_D28(AF10)/CMP_OUT(AF11)/ FSMC_A22(AF12)/DVP_D7(AF13)/ LTDC_G1(AF14) | |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| - | - | 6 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | | |
| - | - | 7 | $V_{BAT}$ | P | - | $V_{BAT}$ | | |
| - | - | 8 | PC13(4)-RTC | I/O | - | PC13(5) | RTC(AF1)/FSMC_A5(AF12)/ SDRAM_A5(AF12) | |
| - | - | 9 | PC14(4)-OSC32_IN | I/O/A | - | PC14(5) | OSC32_IN/SDRAM_CKE1(AF9)/ FSMC_D16(AF12)/SDRAM_D16(AF12) | |
| - | - | 10 | PC15(4)-OSC32_OUT | I/O/A | - | PC15(5) | OSC32_OUT/SDRAM_RAS_N(AF9)/ FSMC_D17(AF12)/SDRAM_D17(AF12) | |
| 7 | 6 | 11 | $V_{DDK}$ | P | - | $V_{DDK}$ | Main $V_{DDK}$ | |
| 8 | 7 | 12 | MDIRN(6) | ETH | - | MDIRN | | |
| 9 | 8 | 13 | MDIRP(6) | ETH | - | MDIRP | | |
| 10 | 9 | 14 | MDITN(6) | ETH | - | MDITN | | |
| 11 | 10 | 15 | MDITP(6) | ETH | - | MDITP | | |
| 12 | 11 | 16 | $V_{DD33}$ | P | - | $V_{DD33}$ | Main $V_{DD33}$ | |
| - | - | 17 | PF6 | I/O | FT | PF6 | CAN3_RX(AF2)/SPI1_NSS(AF3)/ QSPI2_SCK(AF4)/I3C_SCL(AF5)/ SAI_SD_B(AF6)/USART8_RX(AF7)/ TIM10_CH3(AF9)/QSPI1_SIO3(AF10)/ FSMC_D18(AF12)/SDRAM_D18(AF12)/ TIM11_CH1(AF13) | |
| - | - | 18 | PF7 | I/O | FT | PF7 | CAN3_TX(AF2)/SPI1_SCK(AF3)/ QSPI2_SCSN(AF4)/I3C_SDA(AF5)/ SAI_MCLK_B(AF6)/USART8_TX(AF7)/ TIM10_CH4(AF9)/QSPI1_SIO2(AF10)/ FSMC_D19(AF12)/SDRAM_D19(AF12)/ TIM11_CH2(AF13) | |
| - | - | 19 | PF8 | I/O | - | PF8 | HSADC_IN4/SPI1_MOSI(AF3)/ QSPI2_SIO0(AF4)/SAI_SCK_B(AF6)/ USART8_RTS(AF7)/QSPI2_SIO0(AF8)/ TIM10_CH1(AF9)/TIM11_CH3(AF13) QSPI1_SIO0(AF10)/FSMC_D20(AF12)/SDRAM_D20(AF12)/ | |
| - | - | 20 | PF9 | I/O/A | - | PF9 | HSADC_IN5/SPI1_MISO(AF3)/ QSPI2_SIO1(AF4)/SAI_FS_B(AF6)/ USART8_CTS(AF7)/TIM10_CH2(AF9)/ USART8_RTS(AF11)/ QSPI1_SIO1(AF10)/FSMC_D21(AF12)/SD | |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | RAM_D21(AF12)/TIM11_CH4(AF13) | |
| - | - | 21 | PF10 | I/O/A | - | PF10 | HSADC_IN6/QSPI2_SIO2(AF4)/ USART8_CK(AF7)/TIM10_ETR(AF8)/ USART8_CTS(AF11)/FSMC_D22(AF12)/SDRAM_D22(AF12)/DVP_D11(AF13)/ LTDC_DE(AF14) | |
| - | - | 22 | $V_{SS}$ | P | - | $V_{SS}$ | | |
| 13 | 12 | 23 | XI | I/A | - | XI | | |
| 14 | 13 | 24 | XO | O/A | - | XO | | |
| - | 14 | 25 | NRST | I | - | NRST | | |
| 15 | 15 | 26 | PC0 | I/O/A | - | PC0 | ADC_IN10/HSADC_IN0/ TIM8_BKIN(AF0)/ETH_MDC(AF1)/ DFSDM_CKIN0(AF3)/FSMC_D4(AF4)/ PIOC_IO1(AF5)/SAI_MCLK_A(AF7)/ I2C2_SCL(AF9)/QSPI2_SIO3(AF10)/ LTDC_G2(AF11)/SDRAM_WE_N(AF12)/ LTDC_R5(AF14)/SDRAM_CAS_N(AF15) | UHSIF_CLK_1 |
| 16 | 16 | 27 | PC1 | I/O/A | - | PC1 | ADC_IN11/HSADC_IN1/ TIM8_CH1N(AF0)/ETH_MDIO(AF1)/ TIM5_CH1(AF2)/DFSDM_DATIN0(AF3)/ FSMC_D5(AF4)/SPI2_MOSI(AF5)/ I2S1_SDO(AF5)/SAI_SD_A(AF7)/ PIOC_IO0(AF7)/I2C2_SDA(AF9)/ QSPI2_SCSXN(AF10)/SDIO_CK(AF11)/LTDC_G5(AF14)/SDRAM_WE_N(AF15) | UHSIF_PORT0_2/ UHSIF_PORT0_3/ UHSIF_PORT3_1 |
| 17 | 17 | 28 | PC2 | I/O/A | - | PC2 | ADC_IN12/HSADC_IN2/OPA3_P0/ TIM8_CH2N(AF0)/ETH_PPS(AF1)/ TIM5_CH2(AF2)/DFSDM_CKIN1(AF3)/ FSMC_D6(AF4)/SPI2_MISO(AF5)/ I2S1_SDI(AF5)/DFSDM_CKOUT(AF6)/ SAI_SCK_A(AF7)/PIOC_IO1(AF8)/ I2C2_SMBA(AF9)/ QSPI2_SIOX0(AF10)/ SDRAM_CS_NO(AF12)/ SDRAM_DQM0(AF15) | UHSIF_PORT1_2/ UHSIF_PORT1_3/ UHSIF_PORT4_1 |
| 18 | 18 | 29 | PC3 | I/O/A | - | PC3 | ADC_IN13/HSADC_IN3/ OPA3_N0/TIM8_CH3N(AF0)/ TIM5_CH3(AF2)/DFSDM_DATIN1(AF3)/ FSMC_D7(AF4)/SPI2_MOSI(AF5)/ | UHSIF_PORT2_2/ UHSIF_PORT2_3/ UHSIF_PORT5_1 |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | I2S1_SDO(AF5)/SAI_FS_A(AF7)/ QSPI2_SIOX1(AF10)/ SDRAM_D16(AF11)/FSMC_D16(AF11)/ SDRAM_CKE0(AF12)/ SDRAM_DQM1(AF15) | |
| - | 19 | 30 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | | |
| - | - | 31 | $V_{SSA}$ | P | - | $V_{SSA}$ | | |
| - | - | 32 | $V_{REFP}$ | P | - | $V_{REFP}$ | | |
| 19 | 20 | 33 | $V_{DD33A}$ | P | - | $V_{DD33A}$ | | |
| - | 21 | 34 | PA0 | I/O/A | - | PA0 | ADC_IN0/OPA3_OUT0/ TIM2_CH1_ETR(AF1)/TIM5_CH1(AF2)/ TIM8_ETR(AF3)/QSPI2_SIOX2(AF4)/ IO2W_IO0(AF5)/TIM9_CH1(AF6)/ USART2_CTS(AF7)/USART6_TX(AF8)/ SDIO_CMD(AF9)/FSMC_D23(AF12)/ SDRAM_D23(AF12)/LTDC_R0(AF14)/ SDRAM_DQM2(AF15) | |
| - | - | 35 | PA1 | I/O/A | - | PA1 | ADC_IN1/TIM2_CH2(AF1)/ TIM5_CH2(AF2)/QSPI2_SIOX3(AF4)/ TIM9_CH2(AF6)/USART2_RTS(AF7)/ USART6_RX(AF8)/QSPI1_SIO3(AF9)/ FSMC_D24(AF12)/SDRAM_D24(AF12)/ LTDC_R2(AF14) | |
| - | - | 36 | PA2 | I/O/A | - | PA2 | ADC_IN2/OPA3_P1/TIM2_CH3(AF1)/ TIM5_CH3(AF2)/USART6_CK(AF3)/ TIM9_CH3(AF4)/USART2_TX(AF7)/ FSMC_D25(AF12)/SDRAM_D25(AF12)/ LTDC_R1(AF14) | |
| - | - | 37 | PA3 | I/O/A | - | PA3 | ADC_IN3/OPA3_N1/TIM2_CH4(AF1)/ TIM5_CH4(AF2)/TIM9_CH4(AF4)/ USART2_RX(AF7)/TIM10_CH3(AF8)/ LTDC_B2(AF9)/FSMC_D26(AF12)/ SDRAM_D26(AF12)/LTDC_B5(AF14) | |
| - | - | 38 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | | |
| - | 22 | 39 | PA4 | I/O/A | - | PA4 | ADC_IN4/DAC1_OUT/OPA3_OUT1/ TIM5_ETR(AF2)/TIM9_ETR(AF4)/ SPI1_NSS(AF5)/SPI3_NSS(AF6)/ I2S2_WS(AF6)/USART2_CK(AF7)/ TIM10_CH4(AF9)/FSMC_D27(AF12) | |

| Pin No. | | | Pin name | Pin type(1) | I/O characte ristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | SDRAM_D27(AF12)/DVP_HSYNC(AF13) / LTDC_VSYNC(AF14) | |
| 20 | 23 | 40 | PA5 | I/O/A | - | PA5 | ADC_IN5/DAC2_OUT/OPA1_OUT1/ TIM2_CH1_ETR(AF1)/ TIM1_BKIN2(AF2)/TIM8_CH1N(AF3)/ SPI1_SCK(AF5)/TIM10_ETR(AF9)/ DVP_VSYNC(AF11)/FSMC_D28(AF12)/ SDRAM_D28(AF12)/LTDC_R4(AF14) | |
| - | - | 41 | PA6 | I/O/A | - | PA6 | ADC_IN6/OPA1_P1/TIM1_BKIN(AF1)/ TIM3_CH1(AF2)/TIM8_BKIN(AF3)/ SPI1_MISO(AF5)/SDRAM_DQM2(AF6)/ TIM10_CH1(AF9)/CMP_OUT(AF10)/ LTDC_HSYNC(AF11)/DVP_PCLK(AF13)/ LTDC_G2(AF14) | |
| - | - | 42 | PA7 | I/O/A | - | PA7 | ADC_IN7/OPA1_N1/TIM1_CH1N(AF1)/ TIM3_CH2(AF2)/TIM8_CH1N(AF3)/ SPI1_MOSI(AF5)/TIM10_CH2(AF9)/ SDRAM_WE_N(AF12)/ LTDC_VSYNC(AF14)/ | |
| - | - | 43 | PC4 | I/O/A | - | PC4 | ADC_IN14/OPA1_OUT0/CMP_N1/ CAN3_RX(AF6)/I3C_SCL(AF7)/ SDRAM_CS_N0(AF12)/LTDC_R7(AF14) | |
| - | - | 44 | PC5 | I/O/A | - | PC5 | ADC_IN15/CAN3_TX(AF6)/ I3C_SDA(AF7)/SDRAM_CKE0(AF12)/ CMP_OUT(AF13)/LTDC_DE(AF14) | |
| 21 | 24 | 45 | PB0 | I/O/A | - | PB0 | ADC_IN8/OPA1_P0/CMP_P0/MCO(AF0)/ TIM1_CH2N(AF1)/TIM3_CH3(AF2)/ TIM8_CH2N(AF3)/TIM5_CH4(AF4)/ DFSDM_CKOUT(AF6)/SDRAM_DQM3( AF7)/USART6_CTS(AF8)/LTDC_R3(AF9) / FSMC_D29(AF12)/SDRAM_D29(AF12)/ TIM12_ETR(AF13)/LTDC_G1(AF14) | UHSIF_PORT3_2/ UHSIF_PORT3_3/ UHSIF_PORT6_1 |
| 22 | 25 | 46 | PB1 | I/O/A | - | PB1 | ADC_IN9/OPA1_N0/OPA2_OUT1/ CMP_N0/TIM1_CH3N(AF1)/ TIM3_CH4(AF2)/TIM8_CH3N(AF3)/ TIM12_CH1(AF5)/SDRAM_BA0(AF7)/ DFSDM_DATIN1(AF6)/LTDC_R6(AF9)/ | UHSIF_PORT4_2/ UHSIF_PORT4_3/ UHSIF_PORT7_1 |

| Pin No. | | | Pin name | Pin type(1) | I/O characte ristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | FSMC_D30(AF12)/SDRAM_D30(AF12)/ LTDC_G0(AF14) | |
| - | - | 47 | PB2 | I/O/A | FT | PB2 | CMP_P1/DFSDM_CKIN1(AF4)/ TIM12_CH2(AF5)/SAI_SD_A(AF6)/ SPI3_MOSI(AF7)/I2S2_SDO(AF7)/ QSPI1_SCK(AF9)/FSMC_D31(AF12) SDRAM_D31(AF12)/TIM11_ETR(AF13) | |
| - | - | 48 | PF11 | I/O/A | - | PF11 | OPA2_P1/UHSIF_CLK/ I2C4_SMBA(AF2)/SDRAM_RAS_N(AF12 ) | |
| - | - | 49 | PF12 | I/O/A | - | PF12 | OPA2_N1/UHSIF_PORT0/ I2C4_SCL(AF2)/PIOC_IO0(AF3)/ SDRAM_CAS_N(AF12)/ TIM12_CH3(AF13) | |
| - | - | 50 | PF13 | I/O | - | PF13 | UHSIF_PORT1/I2C4_SDA(AF2)/ PIOC_IO1(AF5)/DVP_PCLK(AF11)/ TIM12_CH4(AF13) | |
| - | - | 51 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | | |
| - | - | 52 | PE7 | I/O/A | - | PE7 | OPA2_OUT0/UHSIF_PORT2/ TIM1_ETR(AF1)/USART8_RX(AF7)/ QSPI1_SIOX0(AF10)/FSMC_D4(AF12)/S DRAM_D4(AF12) | |
| - | - | 53 | PE8 | I/O/A | - | PE8 | OPA2_N0/UHSIF_PORT3/ TIM1_CH1N(AF1)/USART8_TX(AF7)/ SDIO_D0(AF8)/QSPI1_SIOX1(AF10)/ FSMC_D5(AF12)/SDRAM_D5(AF12) | |
| - | - | 54 | PE9 | I/O/A | - | PE9 | OPA2_P0/UHSIF_PORT4/ TIM1_CH1(AF1)/DFSDM_CKOUT(AF3)/ SDIO_D1(AF8)/QSPI1_SIOX2(AF10)/ FSMC_D6(AF12)/SDRAM_D6(AF12) | |
| - | 26 | 55 | PE10 | I/O | - | PE10 | UHSIF_PORT5/TIM1_CH2N(AF1)/ SDRAM_D17(AF3)/SDIO_D2(AF8)/ QSPI2_SCK(AF7)/ QSPI1_SIOX3(AF10)/FSMC_D7(AF12)/S DRAM_D7(AF12)/SDRAM_BA1(AF15) | UHSIF_PORT5_2/ UHSIF_PORT5_3 |
| - | 27 | 56 | PE11 | I/O | - | PE11 | UHSIF_PORT6/TIM1_CH2(AF1)/ SDRAM_D18(AF3)/SPI4_NSS(AF5)/ QSPI2_SCSN(AF7)/SDIO_D3(AF8)/ FSMC_D8(AF12)/SDRAM_D8(AF12)/ | UHSIF_PORT6_2/ UHSIF_PORT6_3 |

| Pin No. | | | Pin name | Pin type(1) | I/O characte ristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | LTDC_G3(AF14)/SDRAM_A0(AF15) | |
| - | 28 | 57 | PE12 | I/O | - | PE12 | UHSIF_PORT7/TIM1_CH3N(AF1)/ SDRAM_D19(AF3)/SPI4_SCK(AF5)/ QSPI2_SIO0(AF7)/SDIO_D4(AF8)/ FSMC_D9(AF12)/SDRAM_D9(AF12)/ CMP_OUT(AF13)/LTDC_B4(AF14)/ SDRAM_A1(AF15) | UHSIF_PORT7_2/ UHSIF_PORT7_3 |
| 23 | 29 | 58 | PE13 | I/O | - | PE13 | UHSIF_PORT8/TIM1_CH3(AF1)/ TIM12_CH2(AF2)/SPI4_MISO(AF5)/ QSPI2_SIO1(AF7)/SDIO_D5(AF8)/ FSMC_D10(AF12)/SDRAM_D10(AF12)/ LTDC_DE(AF14)/SDRAM_A2(AF15) | |
| 24 | 30 | 59 | PE14 | I/O | - | PE14 | UHSIF_PORT9/TIM1_CH4(AF1)/ TIM12_CH3(AF2)/I3C_SCL(AF3)/ SPI4_MOSI(AF5)/QSPI2_SIO2(AF7)/ SDIO_D6(AF8)/FSMC_D11(AF12)/ SDRAM_D11(AF12)/LTDC_CLK(AF13)/ SDRAM_A3(AF14) | |
| 25 | 31 | 60 | PE15 | I/O | - | PE15 | UHSIF_PORT10/TIM1_BKIN(AF1)/ TIM12_CH4(AF2)/I3C_SDA(AF3)/ QSPI2_SIO3(AF7)/SDIO_D7(AF8)/ USART5_CK(AF11)/FSMC_D12(AF12)/ SDRAM_D12(AF12)/CMP_OUT(AF13)/ LTDC_R7(AF14)/SDRAM_A4(AF15) | |
| 26 | 32 | 61 | PB10 | I/O | - | PB10 | UHSIF_PORT11/SDRAM_A5(AF0)/ TIM2_CH3(AF1)/TIM9_CH2(AF2)/ LPTIM2_CH1(AF3)/I2C2_SCL(AF4)/ SPI2_SCK(AF5)/I2S1_CK(AF5)/ FSMC_A19(AF6)/USART3_TX(AF7)/ SDIO_CMD(AF8)/USART6_CK(AF9)/ QSPI2_SCSXN(AF11)/ FSMC_A10(AF12)/SDRAM_A10(AF12)/ LTDC_G4(AF14) | SDMMC_D2_1(8) |
| 27 | 33 | 62 | PB11 | I/O | - | PB11 | UHSIF_PORT12/SDRAM_A6(AF0)/ TIM2_CH4(AF1)/FSMC_A20(AF2)/ LPTIM2_ETR(AF3)/I2C2_SDA(AF4)/ USART3_RX(AF7)/SDIO_CK(AF8)/ TIM9_CH4(AF9)/QSPI2_SIOX0(AF11)/ FSMC_A11(AF12)/SDRAM_A11(AF12)/ | SDMMC_D3_1(8) |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | LTDC_G5(AF14) | |
| 28 | 34 | 63 | $V_{IO18}$ | P | - | $V_{IO18}$ | Main $V_{IO18}$ | |
| 29 | 35 | 64 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | Main $V_{DDIO}$ | |
| 30 | 36 | 65 | PB12 | I/O | - | PB12 | UHSIF_PORT13/SDRAM_A7(AF0)/ TIM1_BKIN(AF1)/TIM8_BKIN(AF2)/ FSMC_A21(AF3)/I2C2_SMBA(AF4)/ SPI2_NSS(AF5)/I2S1_WS(AF5)/ DFSDM_DATIN1(AF6)/ USART3_CK(AF7)/TIM9_CH3(AF8)/ CAN2_RX(AF9)/LTDC_VSYNC(AF10)/ QSPI2_SIOX1(AF11)/ FSMC_A12(AF12)/SDRAM_A12(AF12)/ CMP_OUT(AF13)/USART7_RX(AF14)/ DVP_PCLK(AF15) | |
| 31 | 37 | 66 | PB13 | I/O | - | PB13 | UHSIF_PORT14/SDRAM_A8(AF0)/ TIM1_CH1N(AF1)/TIM8_BKIN2(AF2)/ LPTIM2_OC(AF3)/TIM9_ETR(AF4)/ SPI2_SCK(AF5)/I2S1_CK(AF5)/ DFSDM_CKIN1(AF6)/ USART3_CTS(AF7)/DVP_HSYNC(AF8)/ CAN2_TX(AF9)/ETH_PHY_LED3(AF10)/ QSPI2_SIOX0(AF11)/ FSMC_A13(AF12)/DVP_D2(AF13)/ USART7_TX(AF14)/FSMC_A22(AF15) | SDMMC_D0_1(8) |
| 32 | 38 | 67 | PB14 | I/O | - | PB14 | UHSIF_PORT15/FSMC_A23(AF0)/ TIM1_CH2N(AF1)/TIM9_CH1(AF2)/ TIM8_CH2N(AF3)/USART1_TX(AF4)/ SPI2_MISO(AF5)/I2S1_SDI(AF5)/ LTDC_G0(AF6)/USART3_RTS(AF7)/ USART6_RTS(AF8)/SDIO_D0(AF9)/ ETH_PHY_LED4(AF10)/ QSPI2_SIOX1(AF11)/ FSMC_A14(AF12)/SDRAM_BA0(AF12)/ USART7_CK(AF13)/LTDC_CLK(AF14)/ DVP_VSYNC(AF15) | |
| - | - | 68 | PB15 | I/O | FT | PB15 | TIM1_CH3N(AF1)/TIM9_CH2(AF2)/ TIM8_CH3N(AF3)/USART1_RX(AF4)/ SPI2_MOSI(AF5)/I2S1_SDO(AF5)/ USART6_CTS(AF8)/SDIO_D1(AF9)/ | |

| Pin No. | | | Pin name | Pin type(1) | I/O characte ristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | FSMC_A15(AF12)/SDRAM_BA1(AF12)/ LTDC_G7(AF14) | |
| - | - | 69 | PD8 | I/O | FT | PD8 | USART3_TX(AF7)/FSMC_D13(AF12)/ SDRAM_D13(AF12)/LTDC_B7(AF14) | |
| - | - | 70 | PD9 | I/O | - | PD9 | SDRAM_A9(AF0)/I3C_SCL(AF5)/ USART3_RX(AF7)/FSMC_D14(AF12)/ SDRAM_D14(AF12) | UHSIF_CLK_3 |
| 33 | 39 | 71 | PD10 | I/O | - | PD10 | UHSIF_PORT16/SDRAM_A10(AF0)/ DFSDM_CKOUT(AF3)/ LPTIM2_ETR(AF4)/I3C_SDA(AF5)/ USART3_CK(AF7)/RGMII_TXD3(AF10)/ FSMC_D15(AF12)/SDRAM_D15(AF12)/ LTDC_B3(AF14) | SDMMC_STR_1 |
| 34 | 40 | 72 | PD11 | I/O | - | PD11 | UHSIF_PORT17/SDRAM_A11(AF0)/ LPTIM1_ETR(AF1)/LPTIM2_CH2(AF3)/I 2C4_SMBA(AF4)/TIM5_ETR(AF6)/ USART3_CTS(AF7)/QSPI1_SIO0(AF9)/ RGMII_TXD2(AF10)/LTDC_R4(AF11)/ FSMC_A16(AF12)/USART1_CK(AF14) | SDMMC_SDCK_1 SDMMC_SLVCK_ 1 |
| 35 | 41 | 73 | PD12 | I/O | - | PD12 | UHSIF_PORT18/SDRAM_A12(AF0)/ LPTIM1_CH1(AF1)/TIM4_CH1(AF2)/ LPTIM2_CH1(AF3)/I2C4_SCL(AF4)/ CAN3_RX(AF5)/TIM5_CH1(AF6)/ USART3_RTS(AF7)/QSPI1_SIO1(AF9)/ RGMII_TXD1(AF10)/LTDC_R3(AF11)/ FSMC_A17(AF12)/DVP_D4(AF13)/ USART1_RX(AF14) | SDMMC_STS_1 SDMMC_CMD_1 |
| 36 | 42 | 74 | PD13 | I/O | - | PD13 | UHSIF_PORT19/SDRAM_D0(AF0)/ LPTIM1_OC(AF1)/TIM4_CH2(AF2)/ LTDC_R2(AF3)/I2C4_SDA(AF4)/ CAN3_TX(AF5)/TIM5_CH2(AF6)/ QSPI1_SIO3(AF9)/ RGMII_TXD0(AF10)/FSMC_A18(AF12)/ DVP_D5(AF13)/USART1_TX(AF14) | |
| 37 | 43 | 75 | PD14 | I/O | - | PD14 | UHSIF_PORT20/SDRAM_D1(AF0)/ LPTIM1_CH2(AF1)/TIM4_CH3(AF2)/ TIM5_CH3(AF6)/LTDC_B1(AF8)/ QSPI1_SIO2(AF9)/ RGMII_TXEN(AF10)/ | |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | FSMC_D0(AF12)/SDRAM_D0(AF12)/ DVP_D6(AF13)/USART1_RTS(AF14) | |
| 38 | 44 | 76 | PD15 | I/O | - | PD15 | UHSIF_PORT21/SDRAM_D2(AF0)/ TIM4_CH4(AF2)/TIM5_CH4(AF6)/ LTDC_G2(AF7)/RGMII_GTXC(AF10)/ FSMC_D1(AF12)/SDRAM_D1(AF12)/ DVP_D7(AF13)/USART1_CTS(AF14) | |
| 39 | 45 | 77 | PF0 | I/O | - | PF0 | UHSIF_PORT22/SDRAM_D3(AF2)/ SDRAM_CS_N1(AF4)/ QSPI2_SCK(AF5)/USART4_CTS(AF7)/ ETH_PHY_LED0(AF10)/ LTDC_R1(AF11)/DVP_D11(AF12)/ LTDC_R7(AF14) | |
| 40 | 46 | 78 | PF1 | I/O | - | PF1 | UHSIF_PORT23/SDRAM_D4(AF2)/ QSPI2_SCSN(AF5)/ SAI_MCLK_A(AF6)/USART4_CK(AF7)/ LTDC_B0(AF8)/ETH_PHY_LED1(AF10)/ FSMC_INT2(AF12)/LTDC_CLK(AF14) | |
| 41 | 47 | 79 | PF2 | I/O | - | PF2 | UHSIF_PORT24/SDRAM_D5(AF2)/ TIM8_ETR(AF3)/ QSPI2_SIO0(AF5)/USART4_RTS(AF7)/ ETH_PHY_LED2(AF10)/ SDRAM_CLK(AF12)/LTDC_G7(AF14) | |
| - | 48 | 80 | $V_{DDK}$ | P | - | $V_{DDK}$ | | |
| - | 49 | 81 | $V_{IO18}$ | P | - | $V_{IO18}$ | | |
| - | - | 82 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | | |
| 42 | 50 | 83 | PC6 | I/O | - | PC6 | SDMMC_D6(8)/UHSIF_PORT25/ SDRAM_D6(AF0)/ TIM3_CH1(AF2)/TIM8_CH1(AF3)/ FSMC_D8(AF4)/SPI2_MCK(AF5)/ USART4_TX(AF7)/SDIO_D6(AF9)/ SWPMI_IO(AF11)/RGMII_RXD3(AF12)/ DVP_D0(AF13)/LTDC_HSYNC(AF14) | SDMMC_D6_1(8) |
| 43 | 51 | 84 | PC7 | I/O | - | PC7 | SDMMC_D7(8)/UHSIF_PORT26/ SDRAM_D7(AF0)/ TIM3_CH2(AF2)/TIM8_CH2(AF3)/ FSMC_D9(AF4)/SPI3_MCK(AF6)/ USART4_RX(AF7)/SDIO_D7(AF9)/ SWPMI_TX(AF11)/RGMII_RXD2(AF12)/ | SDMMC_D7_1(8) |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | DVP_D1(AF13)/LTDC_G6(AF14) | |
| 44 | 52 | 85 | PC8 | I/O | - | PC8 | SDMMC_D0/UHSIF_PORT27/ SDRAM_D8(AF0)/ TIM3_CH3(AF2)/TIM8_CH3(AF3)/ FSMC_D13(AF4)/TIM9_ETR(AF6)/ USART4_CK(AF7)/USART7_RTS(AF8)/ SWPMI_RX(AF11)/RGMII_RXD1(AF12)/ DVP_D2(AF13)/LTDC_G4(AF14) | |
| 45 | 53 | 86 | PC9 | I/O | - | PC9 | SDMMC_D1(8)/UHSIF_PORT28/ SDRAM_D9(AF0)/ TIM3_CH4(AF2)/TIM8_CH4(AF3)/ I2C3_SDA(AF4)/SPI3_MISO(AF5)/ I2S2_SDI(AF5)/TIM9_CH1(AF6)/ FSMC_D14(AF7)/USART7_CTS(AF8)/ QSPI1_SIO0(AF9)/LTDC_G3(AF10)/ SWPMI_SUP(AF11)/ RGMII_RXD0(AF12)/DVP_D3(AF13)/ LTDC_B2(AF14)/SAI_MCLK_B(AF15) | SDMMC_D1_1(8) |
| - | - | 87 | PA8 | I/O | FT | PA8 | TIM1_CH1(AF1)/TIM8_BKIN2(AF3)/ I2C3_SCL(AF4)/ SDRAM_DQM3(AF6)/ USART1_CK(AF7)/ USART8_RX(AF11)/CMP_OUT(AF12)/ LTDC_B3(AF13)/LTDC_R6(AF14) | |
| - | 54 | 88 | PA9 | I/O/A | FT | PA9 | OTG_VBUS/SDRAM_D10(AF0)/ TIM1_CH2(AF1)/ I2C3_SMBA(AF4)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART1_TX(AF7)/ SDRAM_D20(AF8)/DVP_D0(AF13)/ LTDC_R5(AF14) | |
| - | 55 | 89 | PA10 | I/O/A | FT | PA10 | OTG_ID/SDRAM_D11(AF0)/ TIM1_CH3(AF1)/USART6_CK(AF6)/ USART1_RX(AF7)/SDRAM_D21(AF8)/ FSMC_A6(AF10)/SDRAM_A6(AF10)/ LTDC_B4(AF12)/DVP_D1(AF13)/ LTDC_B1(AF14) | |
| - | 56 | 90 | PA11 | I/O/A | FT | PA11 | OTG_DM/SDRAM_D12(AF0)/ TIM1_CH4(AF1)/USART3_CK(AF4)/ SPI2_NSS(AF5)/I2S1_WS(AF5)/ | |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | USART6_RX(AF6)/USART1_CTS(AF7)/ SDRAM_D22(AF8)/CAN1_RX(AF9)/ FSMC_A7(AF10)/SDRAM_A7(AF10)/ LTDC_R4(AF14) | |
| - | 57 | 91 | PA12 | I/O/A | FT | PA12 | OTG_DP/SDRAM_D13(AF0)/ TIM1_ETR(AF1)/USART3_RTS(AF4)/ SPI2_SCK(AF5)/I2S1_CK(AF5)/ USART6_TX(AF6)/USART1_RTS(AF7)/ SDRAM_D23(AF8)/CAN1_TX(AF9)/ FSMC_A8(AF10)/SDRAM_A8(AF10)/ TIM1_BKIN2(AF12)/LTDC_R5(AF14)/ | |
| 46 | 58 | 92 | PA13 | I/O | - | PA13 | UHSIF_PORT29/SDRAM_D14(AF0)/ SPI3_MOSI(AF1)/I2S2_SDO(AF1)/ SDRAM_BA1(AF3)/USART3_TX(AF4)/ CAN_RX(AF5)/I2C3_SDA(AF7)/ LTDC_B2(AF8)/FSMC_A9(AF10)/ SDRAM_A9(AF10)/SAI_SD_B(AF13)/ | |
| - | 59 | 93 | $V_{DD33}$ | P | - | $V_{DD33}$ | | |
| 47 | 60 | 94 | PA14 | I/O | - | PA14 | SDMMC_D4(8)/UHSIF_PORT30/ SDRAM_D15(AF0)/SPI3_SCK(AF1)/ I2S2_CK(AF1)/SDRAM_A0(AF3)/ USART3_RX(AF4)/CAN_TX(AF5)/ I2C3_SCL(AF7)/USART8_CK(AF11)/ RGMII_RXDV(AF12)/ SAI_SCK_B(AF13)/LTDC_B6(AF14)/ LTDC_R0(AF15) | SDMMC_D4_1(8) |
| 48 | 61 | 95 | PA15 | I/O | - | PA15 | SDMMC_D5(8)/UHSIF_PORT31/ FSMC_NBL3(AF0)/ SDRAM_DQM3(AF0)/ TIM2_CH1_ETR(AF1)/ RGMII_RXC(AF3)/USART3_CTS(AF4)/ SPI1_NSS(AF5)/SPI3_NSS(AF6)/ I2S2_WS(AF6)/I2C3_SMBA(AF7)/ USART6_RTS(AF8)/LTDC_R3(AF9)/ LTDC_B4(AF10)/USART8_TX(AF11)/ SDRAM_A1(AF12)/SAI_FS_B(AF13)/ LTDC_B6(AF14)/LTDC_CLK(AF15) | SDMMC_D5_1(8) |
| 49 | 62 | 96 | PC10 | I/O | - | PC10 | SDMMC_D2(8)/UHSIF_PORT32/ FSMC_NBL2(AF0)/ | SDMMC_STS_2/ SDMMC_STS_3/ |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | SDRAM_DQM2(AF0)/ TIM9_CH2(AF2)/SDRAM_D24(AF3)/ SPI3_SCK(AF6)/I2S2_CK(AF6)/ USART3_TX(AF7)/USART6_TX(AF8)/ QSPI1_SIO1(AF9)/LTDC_B1(AF10)/ SWPMI_RX(AF11)/DVP_D8(AF13)/ LTDC_R2(AF14)/LTDC_HSYNC(AF15) | SDMMC_CMD_2/ SDMMC_CMD_3/ UHSIF_PORT32_2/ UHSIF_PORT32_3 |
| 50 | 63 | 97 | PC11 | I/O | - | PC11 | SDMMC_D3(8)/UHSIF_PORT33/ FSMC_NBL1(AF0)/ SDRAM_DQM1(AF0)/ TIM9_CH4(AF2)/SDRAM_D25(AF3)/ SPI3_MISO(AF6)/I2S2_SDI(AF6)/ USART3_RX(AF7)/USART6_RX(AF8)/ QSPI1_SCSXN(AF9)/DVP_D4(AF13)/ LTDC_B4(AF14)/LTDC_VSYNC(AF15) | SDMMC_STR_2/ SDMMC_STR_3/ UHSIF_PORT33_2/ UHSIF_PORT33_3 |
| 51 | 64 | 98 | PC12 | I/O | - | PC12 | SDMMC_SDCK/SDMMC_SLVCK/ UHSIF_PORT34/FSMC_NBL0(AF0)/ SDRAM_DQM0(AF0)/TIM9_CH3(AF2)/ SDRAM_D26(AF3)/SPI3_MOSI(AF6)/ I2S2_SDO(AF6)/USART3_CK(AF7)/ USART7_TX(AF8)/DVP_D9(AF13)/ LTDC_R6(AF14)/LTDC_DE(AF15) | SDMMC_SDCK_2/ SDMMC_SDCK_3/ SDMMC_SLVCK_2/ SDMMC_SLVCK_3/ UHSIF_PORT34_2/ UHSIF_PORT34_3 |
| 52 | 65 | 99 | PD0 | I/O | - | PD0 | UHSIF_PORT35/SDRAM_D10(AF1)/ USART6_RX(AF8)/CAN1_RX(AF9)/ FSMC_D2(AF12)/SDRAM_D2(AF12)/ LTDC_B1(AF14)/LTDC_R3(AF15) | SDMMC_D0_2/ SDMMC_D0_3/ UHSIF_PORT35_2/ UHSIF_PORT35_3 |
| 53 | 66 | 100 | PD1 | I/O | - | PD1 | UHSIF_PORT36/SDRAM_D11(AF1)/ USART6_TX(AF8)/CAN1_TX(AF9)/ FSMC_D3(AF12)/SDRAM_D3(AF12)/ LTDC_R4(AF15) | SDMMC_D1_2(8)/ SDMMC_D1_3(8)/ UHSIF_PORT36_2/ UHSIF_PORT36_3 |
| 54 | 67 | 101 | PD2 | I/O | - | PD2 | SDMMC_STS/SDMMC_CMD/ UHSIF_PORT37/SDRAM_D12(AF1)/ TIM3_ETR(AF2)/USART7_RX(AF8)/ LTDC_B7(AF9)/FSMC_A25(AF11)/ DVP_D11(AF13)/LTDC_B2(AF14)/ LTDC_R5(AF15) | SDMMC_D2_2(8)/ SDMMC_D2_3(8)/ UHSIF_PORT37_2/ UHSIF_PORT37_3 |
| 55 | 68 | 102 | PD3 | I/O | - | PD3 | SDMMC_STR/UHSIF_PORT38/ SDRAM_D13(AF1)/TIM11_CH1(AF2)/ | SDMMC_D3_2(8)/ SDMMC_D3_3(8)/ |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | DFSDM_CKOUT(AF3)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART2_CTS(AF7)/ USART6_CK(AF8)/TIM3_CH1(AF9)/ FSMC_CLK(AF12)/DVP_D5(AF13)/ LTDC_G7(AF14)/LTDC_R6(AF15) | UHSIF_PORT38_2/ UHSIF_PORT38_3 |
| 56 | 69 | 103 | PD4 | I/O | - | PD4 | UHSIF_PORT39/SDRAM_D14(AF1)/ TIM11_CH2(AF2)/ USART2_RTS(AF7)/USART7_CK(AF8)/ TIM3_CH2(AF9)/FSMC_NOE(AF12)/ LTDC_B4(AF14)/LTDC_R7(AF15) | SDMMC_D4_2(8)/ SDMMC_D4_3(8)/ UHSIF_PORT39_2/ UHSIF_PORT39_3 |
| 57 | 70 | 104 | PD5 | I/O | - | PD5 | UHSIF_PORT40/SDRAM_D15(AF1)/ TIM11_CH3(AF2)/USART2_TX(AF7)/ TIM3_CH3(AF9)/FSMC_NWE(AF12)/ TIM11_ETR(AF13)/LTDC_B5(AF14)/ LTDC_G2(AF15) | SDMMC_D5_2(8)/ SDMMC_D5_3(8)/ UHSIF_PORT40_2/ UHSIF_PORT40_3 |
| - | - | 105 | $V_{IO18}$ | P | - | $V_{IO18}$ | | |
| 58 | 71 | 106 | PD6 | I/O | - | PD6 | UHSIF_PORT41/TIM11_CH4(AF2)/ SDRAM_CS_N0(AF3)/ DFSDM_DATIN1(AF4)/ SPI3_MOSI(AF5)/ I2S2_SDO(AF5)/SAI_SD_A(AF6)/ USART2_RX(AF7)/TIM3_CH4(AF9)/ USART5_CK(AF11)/ FSMC_NWAIT(AF12)/ DVP_D10(AF13)/LTDC_B2(AF14)/ LTDC_G3(AF15) | SDMMC_D6_2(8)/ SDMMC_D6_3(8)/ UHSIF_PORT41_2/ UHSIF_PORT41_3 |
| 59 | 72 | 107 | PD7 | I/O | - | PD7 | UHSIF_PORT42/SDRAM_CS_N1(AF3)/ USART5_RTS(AF4)/SPI1_MOSI(AF5)/ DFSDM_CKIN1(AF6)/USART2_CK(AF7)/ FSMC_NE1(AF12)/TIM11_CH3(AF13)/ LTDC_B3(AF14)/LTDC_G4(AF15) | SDMMC_D7_2(8)/ SDMMC_D7_3(8)/ UHSIF_PORT42_2/ UHSIF_PORT42_3 |
| 60 | 73 | 108 | PF3 | I/O | - | PF3 | UHSIF_PORT43/CAN3_TX(AF2)/ SDRAM_CKE0(AF4)/SPI1_MISO(AF5)/ USART4_RX(AF7)/QSPI1_SIOX2(AF9)/ DVP_D9(AF11)/FSMC_NE2(AF12)/ FSMC_NCE2(AF12)/DVP_VSYNC(AF13) /LTDC_B0(AF14)/LTDC_G5(AF15) | UHSIF_PORT43_2/ UHSIF_PORT43_3 |
| 61 | 74 | 109 | PF4 | I/O | - | PF4 | UHSIF_PORT44/LPTIM1_ETR(AF1)/ CAN3_RX(AF2)/SDRAM_CKE1(AF4)/ | UHSIF_PORT44_2/ UHSIF_PORT44_3 |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | SPI1_NSS(AF5)/USART4_TX(AF7)/ LTDC_G3(AF9)/DVP_D8(AF11)/ FSMC_NE3(AF12)/DVP_D2(AF13)/ LTDC_B2(AF14)/LTDC_G6(AF15) | |
| 62 | 75 | 110 | PF5 | I/O | - | PF5 | UHSIF_PORT45/LPTIM1_CH2(AF1)/ SDRAM_D29(AF3)/USART5_RX(AF4)/ SPI1_SCK(AF5)/QSPI1_SIOX3(AF9)/ FSMC_A0(AF12)/SDRAM_A0(AF12)/ DVP_D3(AF13)/LTDC_B3(AF14)/ LTDC_G7(AF15) | UHSIF_PORT45_2/ UHSIF_PORT45_3 |
| 63 | 76 | 111 | PE0 | I/O | - | PE0 | UHSIF_PORT46/LPTIM1_CH1(AF1)/ SDRAM_A3(AF0)/SDRAM_D30(AF3)/ USART5_TX(AF4)/ USART4_RTS(AF7)/LTDC_B4(AF9)/ DVP_D0(AF11)/FSMC_NE4(AF12)/ TIM11_CH1(AF13)/LTDC_B1(AF14)/ LTDC_B3(AF15) | UHSIF_PORT46_2/ UHSIF_PORT46_3 |
| 64 | 77 | 112 | PE1 | I/O | - | PE1 | UHSIF_PORT47/LPTIM1_OC(AF1)/ SDRAM_D31(AF3)/USART5_CTS(AF4)/ USART4_CTS(AF7)/DVP_D1(AF11)/ FSMC_A24(AF12)/TIM11_CH2(AF13)/ LTDC_R0(AF14)/LTDC_B4(AF15) | UHSIF_PORT47_2/ UHSIF_PORT47_3 |
| 65 | 78 | 113 | PF14 | I/O | - | PF14 | SDRAM_CLK(AF1)/PIOC_IO1(AF5)/ DVP_D5(AF11)/FSMC_NADV(AF12)/ LTDC_B5(AF15) | UHSIF_CLK_2 |
| 66 | 79 | - | $V_{IO18}$ | P | - | $V_{IO18}$ | | |
| - | - | 114 | $V_{DDIO}$ | P | - | $V_{DDIO}$ | | |
| - | 80 | 115 | PB3 | I/O | - | PB3 | TIM2_CH2(AF1)/CC1(AF4)/ SPI1_SCK(AF5)/SPI3_SCK(AF6)/ I2S2_CK(AF6)/SDIO_D2(AF9)/ USART8_RX(AF11)/FSMC_A1(AF12)/ SDRAM_A1(AF12)/DVP_D5(AF13)/ TIM12_ETR(AF14) | |
| - | 81 | 116 | PB4 | I/O | - | PB4 | TIM3_CH1(AF2)/CC2(AF4)/ SPI1_MISO(AF5)/ SPI3_MISO(AF6)/I2S2_SDI(AF6)/ SPI2_NSS(AF7)/I2S1_WS(AF7)/ SDIO_D3(AF9)/TIM4_ETR(AF10)/ USART8_TX(AF11)/FSMC_A2(AF12)/ | |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| | | | | | | | SDRAM_A2(AF12)/USART7_CK(AF14) | |
| - | - | 117 | PB5 | I/O | FT | PB5 | TIM10_ETR(AF0)/TIM3_CH2(AF2)/ LTDC_B5(AF3)/I2C1_SMBA(AF4)/ SPI1_MOSI(AF5)/I2C4_SMBA(AF6)/ SPI3_MOSI(AF7)/I2S2_SDO(AF7)/ SPI2_MCK(AF8)/CAN2_RX(AF9)/ FSMC_D17(AF11)/SDRAM_D17(AF11)/ SDRAM_CKE1(AF12)/DVP_D10(AF13)/ USART7_RX(AF14) | |
| - | - | 118 | PB6 | I/O | FT | PB6 | TIM10_CH1(AF0)/FSMC_A5(AF1)/ TIM4_CH1(AF2)/CAN1_RX(AF3)/ I2C1_SCL(AF4)/SPI3_MCK(AF5)/ I2C4_SCL(AF6)/USART1_TX(AF7)/ CAN2_TX(AF9)/QSPI1_SCSN(AF10)/ SDRAM_A5(AF11)/ SDRAM_CS_N1(AF12)/DVP_D5(AF13)/ USART7_TX(AF14) | |
| - | - | 119 | PB7 | I/O | FT | PB7 | TIM10_CH2(AF0)/TIM4_CH2(AF2)/ CAN1_TX(AF3)/I2C1_SDA(AF4)/ I2C4_SDA(AF6)/USART1_RX(AF7)/ USART8_CK(AF10)/FSMC_NADV(AF12) / DVP_VSYNC(AF13) | |
| 67 | 82 | 120 | PB8 | I/O/A | - | PB8 | SWCLK/USBHS_DP/TIM10_CH3(AF1)/ TIM4_CH3(AF2)/SDRAM_RAS_N(AF3)/ I2C1_SCL(AF4)/PIOC_IO0(AF5)/ I2C4_SCL(AF6)/USART6_RX(AF8)/ CAN1_RX(AF9)/SDIO_D4(AF10)/ FSMC_A3(AF12)/SDRAM_A3(AF12)/ DVP_D6(AF13)/LTDC_B6(AF14) | |
| 68 | 83 | 121 | PB9 | I/O/A | - | PB9 | SWIO/SWDIO/USBHS_DM/ TIM10_CH4(AF1)/ TIM4_CH4(AF2)/SDRAM_DQM2(AF3)/ I2C1_SDA(AF4)/SPI2_NSS(AF5)/ I2S1_WS(AF5)/I2C4_SDA(AF6)/ PIOC_IO1(AF7)/USART6_TX(AF8)/ CAN1_TX(AF9)/SDIO_D5(AF10)/ I2C4_SMBA(AF11)/FSMC_A4(AF12)/ SDRAM_A4(AF12)/DVP_D7(AF13)/ LTDC_B7(AF14) | |

| Pin No. | | | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Pin function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|---|---|
| H417WEU6 | H417MEU6 | H417QEU6 | | | | | | |
| - | - | 122 | $V_{SS}$ | P | - | $V_{SS}$ | | |
| 1 | 84 | 123 | SSTXB(7) | USB3.0 | - | SSTXB | | |
| 2 | 85 | 124 | SSTXA(7) | USB3.0 | - | SSTXA | | |
| 3 | 86 | 125 | $V_{DD12A}$ | P | - | $V_{DD12A}$ | | |
| 4 | 87 | 126 | SSRXB(7) | USB3.0 | - | SSRXB | | |
| 5 | 88 | 127 | SSRXA(7) | USB3.0 | - | SSRXA | | |
| - | - | 128 | $V_{DD33}$ | P | - | $V_{DD33}$ | | |

*Note 1: Explanation of table abbreviations:*

*I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output; A = analog signal input or output;*

*P = power supply; FT = tolerant 5V; USB3.0 = USB3.0 signal; ETH = Ethernet signal; SDP = SerDes PHY signal.*

*Note 2: The I/O pins are connected to the on-board peripherals/modules through a multiplexer that allows only one peripheral's multiplexing function (AF) to be connected to the I/O pins at a time. The multiplexer utilizes up to 16 multiplexing function inputs (AF0 to AF15), which can be configured through the GPIOx_AFLR and GPIOx_AFHR registers: after reset, the multiplexer selects for multiplexing function 0, i.e. (AF0). For more detailed information, please refer to the Multiplexing Function I/O section and the Debug Setup section of the CH32H417RM manual.*

*Note 3: The value after the remap function underline indicates the configuration value of the corresponding bit in the AFIO_PCFR1 register. For example, UHSIF_CLK_1 indicates that the corresponding bit of the register is configured as 01b.*

*Note 4: Both $V_{DD33}$ and $V_{BAT}$ can be connected to an internal analog switch to power the backup area as well as the PC13, PC14 and PC15 pins; this analog switch is only capable of passing a limited amount of current (3mA). When powered by $V_{DD33}$: PC14 and PC15 can be used for GPIO or LSE pins, PC13 can be used as a GPIO, an RTC calibration clock, an RTC alarm clock, or a seconds output; PC13, PC14, and PC15 can only operate in 2MHz mode when used as GPIO output pins, with a maximum drive load of 30pF and cannot be used as a current source (e.g., driving an LEDs). When powered by $V_{BAT}$: PC14 and PC15 can only be used for LSE pin, PC13 can be used as RTC alarm or second output.*

*Note 5: These pins are in the primary functional state when the backup area is first powered up, after that, even if reset, the state of these pins is controlled by the backup domain control registers (these registers are not reset by the primary reset system). For specific information on how to control these IO ports, refer to the Reset and Clock Control (RCC) section of the CH32H417RM manual.*

*Note 6: Supports Ethernet pin RX/TX send/receive identification and pairwise exchange, pin MDIRP/MDIRN positive/negative identification and exchange, and pin MDITP/MDITN positive/negative identification and exchange.*

*Note 7: USB3.0 pin signals support positive and negative identification and exchange, PCB alignment should refer to the USB specification for impedance matching to avoid over-hole. SSRXA/SSRXB default connection to*

*each other TXP/TXN, support cross-connect TXN/TXP, SSTXA/SSTXB default connection to each other RXP/RXN, support cross-connect RXN/RXP.*

*Note 8: When using 1-wire or 4-wire mode, the GPIO pins corresponding to unused data lines cannot be used for multiplexed output. They can be used for multiplexed input or as general-purpose GPIO outputs.*

Table 2-1-2 CH32H416 Pin definitions

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| 0 | $V_{SS}$ | P | - | $V_{SS}$ | | |
| 1 | $V_{DDK}$ | P | - | $V_{DDK}$ | | |
| 2 | $V_{DD33}$ | P | - | $V_{DD33}$ | Main $V_{DD33}$ | |
| 3 | PF6 | I/O | FT | PF6 | CAN3_RX(AF2)/SPI1_NSS(AF3)/ QSPI2_SCK(AF4)/I3C_SCL(AF5)/ SAI_SD_B(AF6)/USART8_RX(AF7)/ TIM10_CH3(AF9)/QSPI1_SIO3(AF10)/ TIM11_CH1(AF13) | |
| 4 | PF7 | I/O | FT | PF7 | CAN3_TX(AF2)/SPI1_SCK(AF3)/ QSPI2_SCSN(AF4)/I3C_SDA(AF5)/ SAI_MCLK_B(AF6)/USART8_TX(AF7)/ TIM10_CH4(AF9)/QSPI1_SIO2(AF10)/ TIM11_CH2(AF13) | |
| 5 | PF8 | I/O | - | PF8 | HSADC_IN4/SPI1_MOSI(AF3)/ QSPI2_SIO0(AF4)/SAI_SCK_B(AF6)/ USART8_RTS(AF7)/QSPI2_SIO0(AF8)/ TIM10_CH1(AF9)/TIM11_CH3(AF13) QSPI1_SIO0(AF10) | |
| 6 | PF9 | I/O/A | - | PF9 | HSADC_IN5/SPI1_MISO(AF3)/ QSPI2_SIO1(AF4)/SAI_FS_B(AF6)/ USART8_CTS(AF7)/TIM10_CH2(AF9)/ USART8_RTS(AF11)/ QSPI1_SIO1(AF10)/TIM11_CH4(AF13) | |
| 7 | PF10 | I/O/A | - | PF10 | HSADC_IN6/QSPI2_SIO2(AF4)/ USART8_CK(AF7)/TIM10_ETR(AF8)/ USART8_CTS(AF11)/DVP_D11(AF13)/ LTDC_DE(AF14) | |
| 8 | XI | I/A | - | XI | | |
| 9 | XO | O/A | - | XO | | |
| 10 | PC0 | I/O/A | - | PC0 | ADC_IN10/HSADC_IN0/ TIM8_BKIN(AF0)/ DFSDM_CKIN0(AF3)/PIOC_IO1(AF5)/ SAI_MCLK_A(AF7)/I2C2_SCL(AF9)/ QSPI2_SIO3(AF10)/LTDC_G2(AF11)/ LTDC_R5(AF14) | |
| 11 | PC1 | I/O/A | - | PC1 | ADC_IN11/HSADC_IN1/ | |

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| | | | | | TIM8_CH1N(AF0)/TIM5_CH1(AF2)/ DFSDM_DATIN0(AF3)/ SPI2_MOSI(AF5)/I2S1_SDO(AF5)/ SAI_SD_A(AF7)/PIOC_IO0(AF7)/ I2C2_SDA(AF9)/QSPI2_SCSXN(AF10)/ SDIO_CK(AF11)/LTDC_G5(AF14) | |
| 12 | PC2 | I/O/A | - | PC2 | ADC_IN12/HSADC_IN2/OPA3_P0/ TIM8_CH2N(AF0)/TIM5_CH2(AF2)/ DFSDM_CKIN1(AF3)/SPI2_MISO(AF5) /I2S1_SDI(AF5)/DFSDM_CKOUT(AF6)/ SAI_SCK_A(AF7)/PIOC_IO1(AF8)/ I2C2_SMBA(AF9)/QSPI2_SIOX0(AF10) | |
| 13 | PC3 | I/O/A | - | PC3 | ADC_IN13/HSADC_IN3/ OPA3_N0/TIM8_CH3N(AF0)/ TIM5_CH3(AF2)/DFSDM_DATIN1 (AF3)/ SPI2_MOSI(AF5)/I2S1_SDO(AF5)/ SAI_FS_A(AF7)/QSPI2_SIOX1(AF10)/ | |
| 14 | $V_{REFP}$ | P | - | $V_{REFP}$ | | |
| 15 | $V_{DD33A}$ | P | - | $V_{DD33A}$ | | |
| 16 | PA0 | I/O/A | - | PA0 | ADC_IN0/OPA3_OUT0/ TIM2_CH1_ETR(AF1)/TIM5_CH1(AF2) /TIM8_ETR(AF3)/QSPI2_SIOX2(AF4)/ IO2W_IO0(AF5)/TIM9_CH1(AF6)/ USART2_CTS(AF7)/USART6_TX(AF8)/ SDIO_CMD(AF9)/LTDC_R0(AF14) | |
| 17 | PA1 | I/O/A | - | PA1 | ADC_IN1/TIM2_CH2(AF1)/ TIM5_CH2(AF2)/QSPI2_SIOX3(AF4)/ TIM9_CH2(AF6)/USART2_RTS(AF7)/ USART6_RX(AF8)/QSPI1_SIO3(AF9)/ LTDC_R2(AF14) | |
| 18 | PA2 | I/O/A | - | PA2 | ADC_IN2/OPA3_P1/TIM2_CH3(AF1)/ TIM5_CH3(AF2)/USART6_CK(AF3)/ TIM9_CH3(AF4)/USART2_TX(AF7)/ LTDC_R1(AF14) | |
| 19 | PA3 | I/O/A | - | PA3 | ADC_IN3/OPA3_N1/TIM2_CH4(AF1)/ TIM5_CH4(AF2)/TIM9_CH4(AF4)/ USART2_RX(AF7)/TIM10_CH3(AF8)/ | |

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| | | | | | LTDC_B2(AF9)/LTDC_B5(AF14) | |
| 20 | PA4 | I/O/A | - | PA4 | ADC_IN4/DAC1_OUT/OPA3_OUT1/ TIM5_ETR(AF2)/TIM9_ETR(AF4)/ SPI1_NSS(AF5)/SPI3_NSS(AF6)/ I2S2_WS(AF6)/USART2_CK(AF7)/ TIM10_CH4(AF9)/DVP_HSYNC(AF13)/ LTDC_VSYNC(AF14) | |
| 21 | PA5 | I/O/A | - | PA5 | ADC_IN5/DAC2_OUT/OPA1_OUT1/ TIM2_CH1_ETR(AF1)/ TIM1_BKIN2(AF2)/TIM8_CH1N(AF3)/ SPI1_SCK(AF5)/TIM10_ETR(AF9)/ DVP_VSYNC(AF11)/LTDC_R4(AF14) | |
| 22 | PA6 | I/O/A | - | PA6 | ADC_IN6/OPA1_P1/TIM1_BKIN(AF1)/ TIM3_CH1(AF2)/TIM8_BKIN(AF3)/ SPI1_MISO(AF5)/TIM10_CH1(AF9)/ CMP_OUT(AF10)/LTDC_HSYNC(AF11) / DVP_PCLK(AF13)/LTDC_G2(AF14) | |
| 23 | PA7 | I/O/A | - | PA7 | ADC_IN7/OPA1_N1/TIM1_CH1N(AF1)/ TIM3_CH2(AF2)/TIM8_CH1N(AF3)/ SPI1_MOSI(AF5)/TIM10_CH2(AF9)/ LTDC_VSYNC(AF14)/ | |
| 24 | PC4 | I/O/A | - | PC4 | ADC_IN14/OPA1_OUT0/CMP_N1/ CAN3_RX(AF6)/I3C_SCL(AF7)/ LTDC_R7(AF14) | |
| 25 | PC5 | I/O/A | - | PC5 | ADC_IN15/CAN3_TX(AF6)/ I3C_SDA(AF7)/CMP_OUT(AF13)/ LTDC_DE(AF14) | |
| 26 | PB0 | I/O/A | - | PB0 | ADC_IN8/OPA1_P0/CMP_P0 /MCO(AF0)/ TIM1_CH2N(AF1)/TIM3_CH3(AF2)/ TIM8_CH2N(AF3)/TIM5_CH4(AF4)/ DFSDM_CKOUT(AF6)/USART6_CTS(AF8)/LTDC_R3(AF9)/ TIM12_ETR(AF13)/ LTDC_G1(AF14) | |
| 27 | PB1 | I/O/A | - | PB1 | ADC_IN9/OPA1_N0/OPA2_OUT1/ CMP_N0/TIM1_CH3N(AF1)/ | |

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| | | | | | TIM3_CH4(AF2)/TIM8_CH3N(AF3)/ TIM12_CH1(AF5)/ DFSDM_DATIN1(AF6)/LTDC_R6(AF9)/ LTDC_G0(AF14) | |
| 28 | PF12 | I/O/A | - | PF12 | OPA2_N1/I2C4_SCL(AF2)/ PIOC_IO0(AF3)/TIM12_CH3(AF13) | |
| 29 | PF13 | I/O | - | PF13 | I2C4_SDA(AF2)/PIOC_IO1(AF5)/ DVP_PCLK(AF11)/TIM12_CH4(AF13) | |
| 30 | PE9 | I/O/A | - | PE9 | OPA2_P0/ TIM1_CH1(AF1)/ DFSDM_CKOUT(AF3)/ SDIO_D1(AF8)/QSPI1_SIOX2(AF10)/ | |
| 31 | PE15 | I/O | - | PE15 | TIM1_BKIN(AF1)/ TIM12_CH4(AF2)/I3C_SDA(AF3)/ QSPI2_SIO3(AF7)/SDIO_D7(AF8)/ USART5_CK(AF11)/CMP_OUT(AF13)/ LTDC_R7(AF14) | |
| 32 | $V_{DD33}$ | P | - | $V_{DD33}$ | | |
| 33 | PD9 | I/O | - | PD9 | I3C_SCL(AF5)/USART3_RX(AF7)/ | |
| 34 | PD10 | I/O | - | PD10 | DFSDM_CKOUT(AF3)/ LPTIM2_ETR(AF4)/I3C_SDA(AF5)/ USART3_CK(AF7)/LTDC_B3(AF14) | SDMMC_STR_1 |
| 35 | PC6 | I/O | - | PC6 | SDMMC_D6(5)/TIM3_CH1(AF2)/ TIM8_CH1(AF3)/SPI2_MCK(AF5)/ USART4_TX(AF7)/SDIO_D6(AF9)/ SWPMI_IO(AF11)/DVP_D0(AF13)/ LTDC_HSYNC(AF14) | SDMMC_D6_1(5) |
| 36 | PC7 | I/O | - | PC7 | SDMMC_D7(5)/TIM3_CH2(AF2)/ TIM8_CH2(AF3)/SPI3_MCK(AF6)/ USART4_RX(AF7)/SDIO_D7(AF9)/ SWPMI_TX(AF11)/DVP_D1(AF13)/ LTDC_G6(AF14) | SDMMC_D7_1(5) |
| 37 | PC8 | I/O | - | PC8 | SDMMC_D0/TIM3_CH3(AF2)/ TIM8_CH3(AF3)/TIM9_ETR(AF6)/ USART4_CK(AF7)/USART7_RTS(AF8)/ SWPMI_RX(AF11)/DVP_D2(AF13)/ LTDC_G4(AF14) | |
| 38 | PC9 | I/O | - | PC9 | SDMMC_D1(5)/TIM3_CH4(AF2)/ | SDMMC_D1_1(5) |

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| | | | | | TIM8_CH4(AF3)/I2C3_SDA(AF4)/ SPI3_MISO(AF5)/I2S2_SDI(AF5)/ TIM9_CH1(AF6)/USART7_CTS(AF8)/ QSPI1_SIO0(AF9)/LTDC_G3(AF10)/ SWPMI_SUP(AF11)/DVP_D3(AF13)/ LTDC_B2(AF14)/SAI_MCLK_B(AF15) | |
| 39 | PA11 | I/O/A | FT | PA11 | OTG_DM/TIM1_CH4(AF1)/ USART3_CK(AF4)/SPI2_NSS(AF5)/ I2S1_WS(AF5)/USART6_RX(AF6)/ USART1_CTS(AF7)/CAN1_RX(AF9)/ LTDC_R4(AF14) | |
| 40 | PA12 | I/O/A | FT | PA12 | OTG_DP/TIM1_ETR(AF1)/ USART3_RTS(AF4)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART6_TX(AF6)/ USART1_RTS(AF7)/CAN1_TX(AF9)/ TIM1_BKIN2(AF12)/LTDC_R5(AF14)/ | |
| 41 | PA13 | I/O | - | PA13 | SPI3_MOSI(AF1)/I2S2_SDO(AF1)/ USART3_TX(AF4)/CAN_RX(AF5)/ I2C3_SDA(AF7)/LTDC_B2(AF8)/ SAI_SD_B(AF13)/ | |
| 42 | PA14 | I/O | - | PA14 | SDMMC_D4(5)/SPI3_SCK(AF1)/ I2S2_CK(AF1)/USART3_RX(AF4)/ CAN_TX(AF5)/I2C3_SCL(AF7)/ USART8_CK(AF11)/SAI_SCK_B(AF13)/ LTDC_B6(AF14)/LTDC_R0(AF15) | SDMMC_D4_1(5) |
| 43 | PA15 | I/O | - | PA15 | SDMMC_D5(5)/TIM2_CH1_ETR(AF1)/ USART3_CTS(AF4)/SPI1_NSS(AF5)/ SPI3_NSS(AF6)/I2S2_WS(AF6)/ I2C3_SMBA(AF7)/USART6_RTS(AF8)/ LTDC_R3(AF9)/LTDC_B4(AF10)/ USART8_TX(AF11)/SAI_FS_B(AF13)/ LTDC_B6(AF14)/LTDC_CLK(AF15) | SDMMC_D5_1(5) |
| 44 | PC10 | I/O | - | PC10 | SDMMC_D2(5)/TIM9_CH2(AF2)/ SPI3_SCK(AF6)/I2S2_CK(AF6)/ USART3_TX(AF7)/USART6_TX(AF8)/ QSPI1_SIO1(AF9)/LTDC_B1(AF10)/ SWPMI_RX(AF11)/DVP_D8(AF13)/ LTDC_R2(AF14)/LTDC_HSYNC(AF15) | SDMMC_STS_2/ SDMMC_STS_3/ SDMMC_CMD_2 / SDMMC_CMD_3 |

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| 45 | PC11 | I/O | - | PC11 | SDMMC_D3(5)/TIM9_CH4(AF2)/ SPI3_MISO(AF6)/I2S2_SDI(AF6)/ USART3_RX(AF7)/USART6_RX(AF8)/ QSPI1_SCSXN(AF9)/DVP_D4(AF13)/ LTDC_B4(AF14)/LTDC_VSYNC(AF15) | SDMMC_STR_2/ SDMMC_STR_3 |
| 46 | PC12 | I/O | - | PC12 | SDMMC_SDCK/SDMMC_SLVCK/ TIM9_CH3(AF2)/SPI3_MOSI(AF6)/ I2S2_SDO(AF6)/USART3_CK(AF7)/ USART7_TX(AF8)/DVP_D9(AF13)/ LTDC_R6(AF14)/LTDC_DE(AF15) | SDMMC_SDCK_2/ SDMMC_SDCK_3/ SDMMC_SLVCK_2/ SDMMC_SLVCK_3 |
| 47 | PD2 | I/O | - | PD2 | SDMMC_STS/SDMMC_CMD/ TIM3_ETR(AF2)/USART7_RX(AF8)/ LTDC_B7(AF9)/DVP_D11(AF13)/ LTDC_B2(AF14)/LTDC_R5(AF15) | SDMMC_D2_2(5)/ SDMMC_D2_3(5) |
| 48 | PD3 | I/O | - | PD3 | SDMMC_STR/TIM11_CH1(AF2)/ DFSDM_CKOUT(AF3)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART2_CTS(AF7)/ USART6_CK(AF8)/TIM3_CH1(AF9)/ DVP_D5(AF13)/LTDC_G7(AF14)/ LTDC_R6(AF15) | SDMMC_D3_2(5)/ SDMMC_D3_3(5) |
| 49 | PB3 | I/O | - | PB3 | TIM2_CH2(AF1)/CC1(AF4)/ SPI1_SCK(AF5)/SPI3_SCK(AF6)/ I2S2_CK(AF6)/SDIO_D2(AF9)/ USART8_RX(AF11)/DVP_D5(AF13)/ TIM12_ETR(AF14) | |
| 50 | PB4 | I/O | - | PB4 | TIM3_CH1(AF2)/CC2(AF4)/ SPI1_MISO(AF5)/ SPI3_MISO(AF6)/I2S2_SDI(AF6)/ SPI2_NSS(AF7)/I2S1_WS(AF7)/ SDIO_D3(AF9)/TIM4_ETR(AF10)/ USART8_TX(AF11)/ USART7_CK(AF14) | |
| 51 | PB5 | I/O | FT | PB5 | TIM10_ETR(AF0)/TIM3_CH2(AF2)/ LTDC_B5(AF3)/I2C1_SMBA(AF4)/ SPI1_MOSI(AF5)/I2C4_SMBA(AF6)/ | |

| Pin No. H416RDU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Default alternate function(2) | Remapping function(3) |
|---|---|---|---|---|---|---|
| | | | | | SPI3_MOSI(AF7)/I2S2_SDO(AF7)/ SPI2_MCK(AF8)/CAN2_RX(AF9)/ DVP_D10(AF13)/USART7_RX(AF14) | |
| 52 | PB6 | I/O | FT | PB6 | TIM10_CH1(AF0)/FSMC_A5(AF1)/ TIM4_CH1(AF2)/CAN1_RX(AF3)/ I2C1_SCL(AF4)/SPI3_MCK(AF5)/ I2C4_SCL(AF6)/USART1_TX(AF7)/ CAN2_TX(AF9)/QSPI1_SCSN(AF10)/ DVP_D5(AF13)/USART7_TX(AF14) | |
| 53 | PB7 | I/O | FT | PB7 | TIM10_CH2(AF0)/TIM4_CH2(AF2)/ CAN1_TX(AF3)/I2C1_SDA(AF4)/ I2C4_SDA(AF6)/USART1_RX(AF7)/ USART8_CK(AF10)/ DVP_VSYNC(AF13) | |
| 54 | PB8 | I/O/A | FT | PB8 | SWCLK/USBHS_DP/TIM10_CH3(AF1)/ TIM4_CH3(AF2)/I2C1_SCL(AF4)/ PIOC_IO0(AF5)/I2C4_SCL(AF6)/ USART6_RX(AF8)/CAN1_RX(AF9)/ SDIO_D4(AF10)/DVP_D6(AF13)/ LTDC_B6(AF14) | |
| 55 | PB9 | I/O/A | - | PB9 | SWIO/SWDIO/USBHS_DM/ TIM10_CH4(AF1)/TIM4_CH4(AF2)/ I2C1_SDA(AF4)/SPI2_NSS(AF5)/ I2S1_WS(AF5)/I2C4_SDA(AF6)/ PIOC_IO1(AF7)/USART6_TX(AF8)/ CAN1_TX(AF9)/SDIO_D5(AF10)/ I2C4_SMBA(AF11)/DVP_D7(AF13)/ LTDC_B7(AF14) | |
| 56 | SSTXB(4) | USB3.0 | - | SSTXB | | |
| 57 | SSTXA(4) | USB3.0 | - | SSTXA | | |
| 58 | $V_{DD12A}$ | P | - | $V_{DD12A}$ | | |
| 59 | SSRXB(4) | USB3.0 | - | SSRXB | | |
| 60 | SSRXA(4) | USB3.0 | - | SSRXA | | |

*Note 1: Explanation of table abbreviations:*

*I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output; A = analog signal input or output; P = power supply; FT = tolerant 5V.*

*Note 2: The I/O pins are connected to the on-board peripherals/modules through a multiplexer that allows only one peripheral's multiplexing function (AF) to be connected to the I/O pins at a time. The multiplexer utilizes up to*

*16 multiplexing function inputs (AF0 to AF15), which can be configured through the GPIOx_AFLR and GPIOx_AFHR registers: after reset, the multiplexer selects for multiplexing function 0, i.e. (AF0). For more detailed information, please refer to the Multiplexing Function I/O section and the Debug Setup section of the CH32H417RM manual.*

*Note 3: The value after the remapping function underline indicates the configuration value of the corresponding bit in the AFIO_PCFR1 register. For example, SDMMC_STR_1 indicates that the corresponding bit of the register is configured as 01b.*

*Note 4: USB3.0 pin signals support positive and negative identification and exchange, PCB alignment should refer to the USB specification for impedance matching to avoid over-hole. SSRXA/SSRXB default connection to each other TXP/TXN, support cross-connect TXN/TXP, SSTXA/SSTXB default connection to each other RXP/RXN, support cross-connect RXN/RXP.*

*Note 5: When using 1-wire or 4-wire mode, the GPIO pins corresponding to unused data lines cannot be repurposed for output. They may be used for input multiplexing or as general-purpose GPIO outputs.*

Table 2-1-3 CH32H415 Pin definitions

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| 0 | $V_{SS}$ | P | - | $V_{SS}$ | |
| 1 | PE3 | I/O | - | PE3 | TIM8_CH1(AF0)/TIM4_CH1(AF2)/ TIM12_CH1(AF3)/PIOC_IO0(AF5)/ SAI_SD_B(AF6)/USART5_TX(AF11)/ DVP_D3(AF13) |
| 2 | PE4 | I/O | - | PE4 | TIM8_CH2(AF0)/ TIM4_CH2(AF2)/TIM12_CH2(AF3)/ PIOC_IO1(AF4)/SPI4_NSS(AF5)/ SAI_FS_A(AF6)/DVP_D4(AF13)/ LTDC_B0(AF14) |
| 3 | PE5 | I/O | - | PE5 | TIM8_CH3(AF0)/ TIM4_CH3(AF2)/TIM12_CH3(AF3)/ TIM9_CH3(AF4)/SPI4_MISO(AF5)/ SAI_SCK_A(AF6)/DVP_D6(AF13)/ LTDC_G0(AF14) |
| 4 | PE6 | I/O | - | PE6 | TIM8_CH4(AF0)/ TIM1_BKIN2(AF1)/TIM4_CH4(AF2)/ TIM12_CH4(AF3)/TIM9_CH4(AF4)/ SPI4_MOSI(AF5)/SAI_SD_A(AF6)/ USART8_CK(AF8)/CMP_OUT(AF11)/ DVP_D7(AF13)/LTDC_G1(AF14) |
| 5 | $V_{DDK}$ | P | - | $V_{DDK}$ | |
| 6 | $V_{DD33}$ | P | - | $V_{DD33}$ | Main $V_{DD33}$ |
| 7 | XI | I/A | - | XI | |
| 8 | XO | O/A | - | XO | |
| 9 | PC0 | I/O/A | - | PC0 | ADC_IN10/HSADC_IN0/ TIM8_BKIN(AF0)/DFSDM_CKIN0(AF3)/ PIOC_IO1(AF5)/SAI_MCLK_A(AF7)/ I2C2_SCL(AF9)/QSPI2_SIO3(AF10)/ LTDC_G2(AF11)/LTDC_R5(AF14)/ |
| 10 | PC1 | I/O/A | - | PC1 | ADC_IN11/HSADC_IN1/ TIM8_CH1N(AF0)/TIM5_CH1(AF2)/ DFSDM_DATIN0(AF3)/SPI2_MOSI(AF5)/ I2S1_SDO(AF5)/SAI_SD_A(AF7)/ PIOC_IO0(AF7)/I2C2_SDA(AF9)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | QSPI2_SCSXN(AF10)/ SDIO_CK(AF11)/LTDC_G5(AF14)/ |
| 11 | PC2 | I/O/A | - | PC2 | ADC_IN12/HSADC_IN2/OPA3_P0/ TIM8_CH2N(AF0)/TIM5_CH2(AF2)/ DFSDM_CKIN1(AF3)/SPI2_MISO(AF5)/ I2S1_SDI(AF5)/DFSDM_CKOUT(AF6)/ SAI_SCK_A(AF7)/PIOC_IO1(AF8)/ I2C2_SMBA(AF9)/QSPI2_SIOX0(AF10) |
| 12 | PC3 | I/O/A | - | PC3 | ADC_IN13/HSADC_IN3/ OPA3_N0/TIM8_CH3N(AF0)/ TIM5_CH3(AF2)/DFSDM_DATIN1(AF3)/ SPI2_MOSI(AF5)/I2S1_SDO(AF5)/ SAI_FS_A(AF7)/QSPI2_SIOX1(AF10) |
| 13 | $V_{DD33A}$ | P | - | $V_{DD33A}$ | |
| 14 | PA0 | I/O/A | - | PA0 | ADC_IN0/OPA3_OUT0/ TIM2_CH1_ETR(AF1)/TIM5_CH1(AF2)/ TIM8_ETR(AF3)/QSPI2_SIOX2(AF4)/ IO2W_IO0(AF5)/TIM9_CH1(AF6)/ USART2_CTS(AF7)/USART6_TX(AF8)/ SDIO_CMD(AF9)/LTDC_R0(AF14)/ |
| 15 | PA1 | I/O/A | - | PA1 | ADC_IN1/TIM2_CH2(AF1)/ TIM5_CH2(AF2)/QSPI2_SIOX3(AF4)/ TIM9_CH2(AF6)/USART2_RTS(AF7)/ USART6_RX(AF8)/QSPI1_SIO3(AF9)/ LTDC_R2(AF14) |
| 16 | PA2 | I/O/A | - | PA2 | ADC_IN2/OPA3_P1/TIM2_CH3(AF1)/ TIM5_CH3(AF2)/USART6_CK(AF3)/ TIM9_CH3(AF4)/USART2_TX(AF7)/ LTDC_R1(AF14) |
| 17 | PA3 | I/O/A | - | PA3 | ADC_IN3/OPA3_N1/TIM2_CH4(AF1)/ TIM5_CH4(AF2)/TIM9_CH4(AF4)/ USART2_RX(AF7)/TIM10_CH3(AF8)/ LTDC_B2(AF9)/LTDC_B5(AF14) |
| 18 | PA4 | I/O/A | - | PA4 | ADC_IN4/DAC1_OUT/OPA3_OUT1/ TIM5_ETR(AF2)/TIM9_ETR(AF4)/ SPI1_NSS(AF5)/SPI3_NSS(AF6)/ I2S2_WS(AF6)/USART2_CK(AF7)/ TIM10_CH4(AF9)/DVP_HSYNC(AF13)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | LTDC_VSYNC(AF14) |
| 19 | PA5 | I/O/A | - | PA5 | ADC_IN5/DAC2_OUT/OPA1_OUT1/ TIM2_CH1_ETR(AF1)/TIM1_BKIN2(AF2)/ TIM8_CH1N(AF3)/SPI1_SCK(AF5)/ TIM10_ETR(AF9)/DVP_VSYNC(AF11)/ LTDC_R4(AF14) |
| 20 | PA6 | I/O/A | - | PA6 | ADC_IN6/OPA1_P1/TIM1_BKIN(AF1)/ TIM3_CH1(AF2)/TIM8_BKIN(AF3)/ SPI1_MISO(AF5)/TIM10_CH1(AF9)/ CMP_OUT(AF10)/LTDC_HSYNC(AF11)/ DVP_PCLK(AF13)/LTDC_G2(AF14) |
| 21 | PA7 | I/O/A | - | PA7 | ADC_IN7/OPA1_N1/TIM1_CH1N(AF1)/ TIM3_CH2(AF2)/TIM8_CH1N(AF3)/ SPI1_MOSI(AF5)/TIM10_CH2(AF9)/ LTDC_VSYNC(AF14)/ |
| 22 | PC4 | I/O/A | - | PC4 | ADC_IN14/OPA1_OUT0/CMP_N1/ CAN3_RX(AF6)/I3C_SCL(AF7)/ LTDC_R7(AF14) |
| 23 | PB0 | I/O/A | - | PB0 | ADC_IN8/OPA1_P0/CMP_P0/MCO(AF0)/ TIM1_CH2N(AF1)/TIM3_CH3(AF2)/ TIM8_CH2N(AF3)/TIM5_CH4(AF4)/ DFSDM_CKOUT(AF6)/USART6_CTS(AF8) / LTDC_R3(AF9)/TIM12_ETR(AF13)/ LTDC_G1(AF14) |
| 24 | PB1 | I/O/A | - | PB1 | ADC_IN9/OPA1_N0/CMP_N0/ TIM1_CH3N(AF1)/TIM3_CH4(AF2)/ TIM8_CH3N(AF3)/TIM12_CH1(AF5)/ DFSDM_DATIN1(AF6)/LTDC_R6(AF9)/ LTDC_G0(AF14) |
| 25 | PE11 | I/O | - | PE11 | TIM1_CH2(AF1)/SPI4_NSS(AF5)/ QSPI2_SCSN(AF7)/SDIO_D3(AF8)/ LTDC_G3(AF14) |
| 26 | PE12 | I/O | - | PE12 | TIM1_CH3N(AF1)/SPI4_SCK(AF5)/ QSPI2_SIO0(AF7)/SDIO_D4(AF8)/ CMP_OUT(AF13)/LTDC_B4(AF14)/ |
| 27 | PE13 | I/O | - | PE13 | TIM1_CH3(AF1)/ TIM12_CH2(AF2)/SPI4_MISO(AF5)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | QSPI2_SIO1(AF7)/SDIO_D5(AF8)/ LTDC_DE(AF14)/ |
| 28 | PE14 | I/O | - | PE14 | TIM1_CH4(AF1)/TIM12_CH3(AF2)/ I3C_SCL(AF3)/SPI4_MOSI(AF5)/ QSPI2_SIO2(AF7)/SDIO_D6(AF8)/ LTDC_CLK(AF13) |
| 29 | PE15(3) | I/O | - | PE15 | TIM1_BKIN(AF1)/TIM12_CH4(AF2)/ I3C_SDA(AF3)/QSPI2_SIO3(AF7)/ SDIO_D7(AF8)/USART5_CK(AF11)/ CMP_OUT(AF13)/LTDC_R7(AF14)/ |
| | PB10(3) | I/O | - | PB10 | TIM2_CH3(AF1)/TIM9_CH2(AF2)/ LPTIM2_CH1(AF3)/I2C2_SCL(AF4)/ SPI2_SCK(AF5)/I2S1_CK(AF5)/ USART3_TX(AF7)/SDIO_CMD(AF8)/ USART6_CK(AF9)/QSPI2_SCSXN(AF11)/ LTDC_G4(AF14) |
| 30 | PB11 | I/O | - | PB11 | TIM2_CH4(AF1)/LPTIM2_ETR(AF3)/ I2C2_SDA(AF4)/USART3_RX(AF7)/ SDIO_CK(AF8)/TIM9_CH4(AF9)/ QSPI2_SIOX0(AF11)/LTDC_G5(AF14) |
| 31 | $V_{DD33}$ | P | - | $V_{DD33}$ | |
| 32 | PB12 | I/O | - | PB12 | TIM1_BKIN(AF1)/TIM8_BKIN(AF2)/ I2C2_SMBA(AF4)/SPI2_NSS(AF5)/ I2S1_WS(AF5)/DFSDM_DATIN1(AF6)/ USART3_CK(AF7)/TIM9_CH3(AF8)/ CAN2_RX(AF9)/LTDC_VSYNC(AF10)/ QSPI2_SIOX1(AF11)/ CMP_OUT(AF13)/USART7_RX(AF14)/ DVP_PCLK(AF15) |
| 33 | PB13 | I/O | - | PB13 | TIM1_CH1N(AF1)/TIM8_BKIN2(AF2)/ LPTIM2_OC(AF3)/TIM9_ETR(AF4)/ SPI2_SCK(AF5)/I2S1_CK(AF5)/ DFSDM_CKIN1(AF6)/ USART3_CTS(AF7)/DVP_HSYNC(AF8)/ CAN2_TX(AF9)/QSPI2_SIOX0(AF11)/ DVP_D2(AF13)/USART7_TX(AF14)/ |
| 34 | PB14 | I/O | - | PB14 | TIM1_CH2N(AF1)/TIM9_CH1(AF2)/ TIM8_CH2N(AF3)/USART1_TX(AF4)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | SPI2_MISO(AF5)/I2S1_SDI(AF5)/ LTDC_G0(AF6)/USART3_RTS(AF7)/ USART6_RTS(AF8)/SDIO_D0(AF9)/ QSPI2_SIOX1(AF11)/USART7_CK(AF13)/ LTDC_CLK(AF14)/DVP_VSYNC(AF15) |
| 35 | PB15 | I/O | FT | PB15 | TIM1_CH3N(AF1)/TIM9_CH2(AF2)/ TIM8_CH3N(AF3)/USART1_RX(AF4)/ SPI2_MOSI(AF5)/I2S1_SDO(AF5)/ USART6_CTS(AF8)/SDIO_D1(AF9)/ LTDC_G7(AF14) |
| 36 | PC6 | I/O | - | PC6 | TIM3_CH1(AF2)/TIM8_CH1(AF3)/ SPI2_MCK(AF5)/USART4_TX(AF7)/ SDIO_D6(AF9)/SWPMI_IO(AF11)/ DVP_D0(AF13)/LTDC_HSYNC(AF14) |
| 37 | PC7 | I/O | - | PC7 | TIM3_CH2(AF2)/TIM8_CH2(AF3)/ SPI3_MCK(AF6)/USART4_RX(AF7)/ SDIO_D7(AF9)/SWPMI_TX(AF11)/ DVP_D1(AF13)/LTDC_G6(AF14) |
| 38 | PC8 | I/O | - | PC8 | TIM3_CH3(AF2)/TIM8_CH3(AF3)/ TIM9_ETR(AF6)/USART4_CK(AF7)/ USART7_RTS(AF8)/SWPMI_RX(AF11)/ DVP_D2(AF13)/LTDC_G4(AF14) |
| 39 | PC9 | I/O | - | PC9 | TIM3_CH4(AF2)/TIM8_CH4(AF3)/ I2C3_SDA(AF4)/SPI3_MISO(AF5)/ I2S2_SDI(AF5)/TIM9_CH1(AF6)/ USART7_CTS(AF8)/QSPI1_SIO0(AF9)/ LTDC_G3(AF10)/SWPMI_SUP(AF11)/ DVP_D3(AF13)/LTDC_B2(AF14)/ SAI_MCLK_B(AF15) |
| 40 | PA9 | I/O/A | FT | PA9 | OTG_VBUS/TIM1_CH2(AF1)/ I2C3_SMBA(AF4)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART1_TX(AF7)/ DVP_D0(AF13)/LTDC_R5(AF14) |
| 41 | PA10 | I/O/A | FT | PA10 | OTG_ID/TIM1_CH3(AF1)/ USART6_CK(AF6)/USART1_RX(AF7)/ LTDC_B4(AF12)/DVP_D1(AF13)/ LTDC_B1(AF14) |
| 42 | PA11 | I/O/A | FT | PA11 | OTG_DM/TIM1_CH4(AF1)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | USART3_CK(AF4)/SPI2_NSS(AF5)/ I2S1_WS(AF5)/USART6_RX(AF6)/ USART1_CTS(AF7)/CAN1_RX(AF9)/ LTDC_R4(AF14) |
| 43 | PA12 | I/O/A | FT | PA12 | OTG_DP/TIM1_ETR(AF1)/ USART3_RTS(AF4)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART6_TX(AF6)/ USART1_RTS(AF7)/CAN1_TX(AF9)/ TIM1_BKIN2(AF12)/LTDC_R5(AF14) |
| 44 | PA13 | I/O | - | PA13 | SPI3_MOSI(AF1)/I2S2_SDO(AF1)/ USART3_TX(AF4)/CAN_RX(AF5)/ I2C3_SDA(AF7)/LTDC_B2(AF8)/ SAI_SD_B(AF13) |
| 45 | PA14 | I/O | - | PA14 | SPI3_SCK(AF1)/I2S2_CK(AF1)/ USART3_RX(AF4)/CAN_TX(AF5)/ I2C3_SCL(AF7)/USART8_CK(AF11)/ SAI_SCK_B(AF13)/LTDC_B6(AF14)/ LTDC_R0(AF15) |
| 46 | PA15 | I/O | - | PA15 | TIM2_CH1_ETR(AF1)/USART3_CTS(AF4)/ SPI1_NSS(AF5)/SPI3_NSS(AF6)/ I2S2_WS(AF6)/I2C3_SMBA(AF7)/ USART6_RTS(AF8)/LTDC_R3(AF9)/ LTDC_B4(AF10)/USART8_TX(AF11)/ SAI_FS_B(AF13)/LTDC_B6(AF14)/ LTDC_CLK(AF15) |
| 47 | PC10 | I/O | - | PC10 | TIM9_CH2(AF2)/SPI3_SCK(AF6)/ I2S2_CK(AF6)/USART3_TX(AF7)/ USART6_TX(AF8)/QSPI1_SIO1(AF9)/ LTDC_B1(AF10)/SWPMI_RX(AF11)/ DVP_D8(AF13)/LTDC_R2(AF14)/ LTDC_HSYNC(AF15) |
| 48 | PC11 | I/O | - | PC11 | TIM9_CH4(AF2)/SPI3_MISO(AF6)/ I2S2_SDI(AF6)/USART3_RX(AF7)/ USART6_RX(AF8)/QSPI1_SCSXN(AF9)/ DVP_D4(AF13)/LTDC_B4(AF14)/ LTDC_VSYNC(AF15) |
| 49 | PC12 | I/O | - | PC12 | TIM9_CH3(AF2)/SPI3_MOSI(AF6)/ I2S2_SDO(AF6)/USART3_CK(AF7)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | USART7_TX(AF8)/DVP_D9(AF13)/ LTDC_R6(AF14)/LTDC_DE(AF15) |
| 50 | PD3 | I/O | - | PD3 | TIM11_CH1(AF2)/ DFSDM_CKOUT(AF3)/SPI2_SCK(AF5)/ I2S1_CK(AF5)/USART2_CTS(AF7)/ USART6_CK(AF8)/TIM3_CH1(AF9)/ DVP_D5(AF13)/LTDC_G7(AF14)/ LTDC_R6(AF15) |
| 51 | PF3 | I/O | - | PF3 | CAN3_TX(AF2)/SPI1_MISO(AF5)/ USART4_RX(AF7)/QSPI1_SIOX2(AF9)/ DVP_D9(AF11)/DVP_VSYNC(AF13)/ LTDC_B0(AF14)/LTDC_G5(AF15) |
| 52 | PF4 | I/O | - | PF4 | LPTIM1_ETR(AF1)/CAN3_RX(AF2)/ SPI1_NSS(AF5)/USART4_TX(AF7)/ LTDC_G3(AF9)/DVP_D8(AF11)/ DVP_D2(AF13)/LTDC_B2(AF14)/ LTDC_G6(AF15) |
| 53 | PF5 | I/O | - | PF5 | LPTIM1_CH2(AF1)/USART5_RX(AF4)/ SPI1_SCK(AF5)/QSPI1_SIOX3(AF9)/ DVP_D3(AF13)/LTDC_B3(AF14)/ LTDC_G7(AF15) |
| 54 | PE0 | I/O | - | PE0 | LPTIM1_CH1(AF1)/USART5_TX(AF4)/ USART4_RTS(AF7)/LTDC_B4(AF9)/ DVP_D0(AF11)/TIM11_CH1(AF13)/ LTDC_B1(AF14)/LTDC_B3(AF15) |
| 55 | PB3 | I/O | - | PB3 | TIM2_CH2(AF1)/CC1(AF4)/ SPI1_SCK(AF5)/SPI3_SCK(AF6)/ I2S2_CK(AF6)/SDIO_D2(AF9)/ USART8_RX(AF11)/DVP_D5(AF13)/ TIM12_ETR(AF14) |
| 56 | PB4 | I/O | - | PB4 | TIM3_CH1(AF2)/CC2(AF4)/ SPI1_MISO(AF5)/SPI3_MISO(AF6)/ I2S2_SDI(AF6)/SPI2_NSS(AF7)/ I2S1_WS(AF7)/SDIO_D3(AF9)/ TIM4_ETR(AF10)/USART8_TX(AF11)/ USART7_CK(AF14) |
| 57 | PB6 | I/O | FT | PB6 | TIM10_CH1(AF0)/TIM4_CH1(AF2)/ CAN1_RX(AF3)/I2C1_SCL(AF4)/ |

| Pin No. H415REU6 | Pin name | Pin type(1) | I/O characteristic(1) | Main function (After reset) | Remapping function(3) |
|---|---|---|---|---|---|
| | | | | | SPI3_MCK(AF5)/I2C4_SCL(AF6)/ USART1_TX(AF7)/CAN2_TX(AF9)/ QSPI1_SCSN(AF10)/DVP_D5(AF13)/ USART7_TX(AF14) |
| 58 | PB7 | I/O | FT | PB7 | TIM10_CH2(AF0)/TIM4_CH2(AF2)/ CAN1_TX(AF3)/I2C1_SDA(AF4)/ I2C4_SDA(AF6)/USART1_RX(AF7)/ USART8_CK(AF10)/DVP_VSYNC(AF13) |
| 59 | PB8 | I/O/A | - | PB8 | SWCLK/USBHS_DP/TIM10_CH3(AF1)/ TIM4_CH3(AF2)/I2C1_SCL(AF4)/ PIOC_IO0(AF5)/I2C4_SCL(AF6)/ USART6_RX(AF8)/CAN1_RX(AF9)/ SDIO_D4(AF10)/DVP_D6(AF13)/ LTDC_B6(AF14) |
| 60 | PB9 | I/O/A | - | PB9 | SWIO/SWDIO/USBHS_DM/ TIM10_CH4(AF1)/TIM4_CH4(AF2)/ I2C1_SDA(AF4)/SPI2_NSS(AF5)/ I2S1_WS(AF5)/I2C4_SDA(AF6)/ PIOC_IO1(AF7)/USART6_TX(AF8)/ CAN1_TX(AF9)/SDIO_D5(AF10)/ I2C4_SMBA(AF11)/DVP_D7(AF13)/ LTDC_B7(AF14) |

*Note 1: Explanation of table abbreviations:*

*I = TTL/CMOS level Schmitt input; O = CMOS level tri-state output; A = analog signal input or output;*

*P = power supply; FT = tolerant 5V; USB3.0 = USB3.0 signal; ETH = Ethernet signal; SDP = SerDes PHY signal.*

*Note 2: The I/O pins are connected to the on-board peripherals/modules through a multiplexer that allows only one peripheral's multiplexing function (AF) to be connected to the I/O pins at a time. The multiplexer utilizes up to 16 multiplexing function inputs (AF0 to AF15), which can be configured through the GPIOx_AFLR and GPIOx_AFHR registers: after reset, the multiplexer selects for multiplexing function 0, i.e. (AF0). For more detailed information, please refer to the Multiplexing Function I/O section and the Debug Setup section of the CH32H417RM manual.*

*Note 3: For the CH32H415REU6 chip, the PB10 and PE15 pins are short-connected inside the chip, and the configuration of both IOs is prohibited as output functions.*

## 2.3 Pin Alternate Function

*Note that the pin function descriptions in the following table are for all functions and do not relate to specific models. There are differences in peripheral resources between different models, please check whether this function is available according to the product model resource table before checking.*

*Note: When pins are configured as multiplexed inputs through the multiplexer, there is a priority level for the optional pins of the same peripheral (The optional pins in the same line in each of the following tables are listed in descending order of priority). When a low-priority pin is selected as a multiplexed input for a peripheral, a high-priority pin of the same peripheral must not be configured as a multiplexed function of that peripheral at the same time. Example: PE9 (AF1) and PA8 (AF1) are both optional pins for the TIM1_CH1 function, and the PE9 pin has a higher priority. If PA8 pin is used as TIM1_CH1, PE9 pin should be avoided to be configured as AF1.*

Table 2-2-1 ADC Pin functions

| ADC function | Default pin |
|---|---|
| ADC_IN0 | PA0 |
| ADC_IN1 | PA1 |
| ADC_IN2 | PA2 |
| ADC_IN3 | PA3 |
| ADC_IN4 | PA4 |
| ADC_IN5 | PA5 |
| ADC_IN6 | PA6 |
| ADC_IN7 | PA7 |
| ADC_IN8 | PB0 |
| ADC_IN9 | PB1 |
| ADC_IN10 | PC0 |
| ADC_IN11 | PC1 |
| ADC_IN12 | PC2 |
| ADC_IN13 | PC3 |
| ADC_IN14 | PC4 |
| ADC_IN15 | PC5 |
| ADC_IN16 | Temperature sensor |
| ADC_IN17 | Internal reference voltage $V_{REFINT}$ |

Table 2-2-2 HSADC Pin functions

| HSADC function | Default pin |
|---|---|
| HSADC_IN0 | PC0 |
| HSADC_IN1 | PC1 |
| HSADC_IN2 | PC2 |

| | |
|---|---|
| HSADC_IN3 | PC3 |
| HSADC_IN4 | PF8 |
| HSADC_IN5 | PF9 |
| HSADC_IN6 | PF10 |

Table 2-2-3 DAC Pin functions

| DAC1 function | Default pin |
|---|---|
| DAC1_OUT | PA4 |
| DAC2 function | Default pin |
| DAC2_OUT | PA5 |

Table 2-2-4 TIM Pin functions

| TIM1 function | Optional pins |
|---|---|
| TIM1_ETR | PE7(AF1), PA12(AF1) |
| TIM1_CH1 | PE9(AF1), PA8(AF1) |
| TIM1_CH2 | PE11(AF1), PA9(AF1) |
| TIM1_CH3 | PE13(AF1), PA10(AF1) |
| TIM1_CH4 | PE14(AF1), PA11(AF1) |
| TIM1_CH1N | PE8(AF1), PA7(AF1), PB13(AF1) |
| TIM1_CH2N | PE10(AF1), PB0(AF1), PB14(AF1) |
| TIM1_CH3N | PE12(AF1), PB1(AF1), PB15(AF1) |
| TIM1_BKIN | PE15(AF1), PA6(AF1), PB12(AF1) |
| TIM1_BKIN2 | PE6(AF1), PA5(AF2), PA12(AF12) |
| TIM8 function | Optional pins |
| TIM8_ETR | PA0(AF3), PF2(AF3) |
| TIM8_CH1 | PC6(AF3), PE3(AF0) |
| TIM8_CH2 | PC7(AF3), PE4(AF0) |
| TIM8_CH3 | PC8(AF3), PE5(AF0) |
| TIM8_CH4 | PC9(AF3), PE6(AF0) |
| TIM8_CH1N | PA7(AF3), PA5(AF3), PC1(AF0) |
| TIM8_CH2N | PB0(AF3), PB14(AF3), PC2(AF0) |
| TIM8_CH3N | PB1(AF3), PB15(AF3), PC3(AF0) |
| TIM8_BKIN | PA6(AF3), PB12(AF2), PC0(AF0) |
| TIM8_BKIN2 | PA8(AF3) PB13(AF2) |
| TIM2 function | Optional pins |
| TIM2_CH1_ETR | PA0(AF1), PA5(AF1), PA15(AF1) |
| TIM2_CH2 | PA1(AF1) PB3(AF1) |
| TIM2_CH3 | PA2(AF1), PB10(AF1) |

| | |
|---|---|
| TIM2_CH4 | PA3(AF1), PB11(AF1) |
| TIM3 function | Optional pins |
| TIM3_ETR | PD2(AF2) |
| TIM3_CH1 | PA6(AF2), PB4(AF2), PC6(AF2), PD3(AF9) |
| TIM3_CH2 | PA7(AF2), PB5(AF2), PC7(AF2), PD4(AF9) |
| TIM3_CH3 | PB0(AF2), PC8(AF2), PD5(AF9) |
| TIM3_CH4 | PB1(AF2), PC9(AF2), PD6(AF9) |
| TIM4 function | Optional pins |
| TIM4_ETR | PB4(AF10) |
| TIM4_CH1 | PB6(AF2), PD12(AF2), PE3(AF2) |
| TIM4_CH2 | PB7(AF2), PD13(AF2), PE4(AF2) |
| TIM4_CH3 | PB8(AF2), PD14(AF2), PE5(AF2) |
| TIM4_CH4 | PB9(AF2), PD15(AF2), PE6(AF2) |
| TIM5 function | Optional pins |
| TIM5_ETR | PA4(AF2), PD11(AF6) |
| TIM5_CH1 | PA0(AF2), PD12(AF6), PC1(AF2) |
| TIM5_CH2 | PA1(AF2), PD13(AF6), PC2(AF2) |
| TIM5_CH3 | PA2(AF2), PD14(AF6), PC3(AF2) |
| TIM5_CH4 | PA3(AF2), PD15(AF6), PB0(AF4) |
| TIM9 function | Optional pins |
| TIM9_ETR | PB13(AF4), PA4(AF4), PC8(AF6) |
| TIM9_CH1 | PB14(AF2), PA0(AF6), PC9(AF6) |
| TIM9_CH2 | PB15(AF2), PA1(AF6), PC10(AF2), PB10(AF2) |
| TIM9_CH3 | PE5(AF4), PA2(AF4), PC12(AF2), PB12(AF8) |
| TIM9_CH4 | PE6(AF4), PA3(AF4), PC11(AF2), PB11(AF9) |
| TIM10 function | Optional pins |
| TIM10_ETR | PF10(AF8), PA5(AF9), PB5(AF0) |
| TIM10_CH1 | PF8(AF9), PA6(AF9), PB6(AF0) |
| TIM10_CH2 | PF9(AF9), PA7(AF9), PB7(AF0) |
| TIM10_CH3 | PF6(AF9), PA3(AF8), PB8(AF1) |
| TIM10_CH4 | PF7(AF9), PA4(AF9), PB9(AF1) |
| TIM11 function | Optional pins |
| TIM11_ETR | PB2(AF13), PD5(AF13) |
| TIM11_CH1 | PD3(AF2), PF6(AF13), PE0(AF13) |
| TIM11_CH2 | PD4(AF2), PF7(AF13), PE1(AF13) |
| TIM11_CH3 | PD5(AF2), PF8(AF13), PD7(AF13) |
| TIM11_CH4 | PD6(AF2), PF9(AF13) |

| TIM12 function | Optional pins |
|---|---|
| TIM12_ETR | PB0(AF13), PB3(AF14) |
| TIM12_CH1 | PB1(AF5), PE3(AF3) |
| TIM12_CH2 | PB2(AF5), PE4(AF3), PE13(AF2) |
| TIM12_CH3 | PF12(AF13), PE5(AF3), PE14(AF2) |
| TIM12_CH4 | PF13(AF13), PE6(AF3), PE15(AF2) |

Table 2-2-5 LPTIM Pin functions

| LPTIM1 function | Optional pins |
|---|---|
| LPTIM1_ETR | PF4(AF1), PD11(AF1) |
| LPTIM1_CH1 | PE0(AF1), PD12(AF1) |
| LPTIM1_CH2 | PF5(AF1), PD14(AF1) |
| LPTIM1_OC | PE1(AF1), PD13(AF1) |
| LPTIM2 function | Optional pins |
| LPTIM2_ETR | PB11(AF3), PD10(AF4) |
| LPTIM2_CH1 | PB10(AF3), PD12(AF3) |
| LPTIM2_CH2 | PD11(AF3), PB12(AF13) |
| LPTIM2_OC | PB13(AF3) |

Table 2-2-6 I2C Pin functions

| I2C1 function | Optional pins |
|---|---|
| I2C1_SCL | PB6(AF4), PB8(AF4) |
| I2C1_SDA | PB7(AF4) PB9(AF4) |
| I2C1_SMBA | PB5(AF4) |
| I2C2 function | Optional pins |
| I2C2_SCL | PC0(AF9), PB10(AF4) |
| I2C2_SDA | PC1(AF9), PB11(AF4) |
| I2C2_SMBA | PC2(AF9) PB12(AF4) |
| I2C3 function | Optional pins |
| I2C3_SCL | PA8(AF4), PA14(AF7) |
| I2C3_SDA | PC9(AF4), PA13(AF7) |
| I2C3_SMBA | PA9(AF4), PA15(AF7) |
| I2C4 function | Optional pins |
| I2C4_SCL | PD12(AF4), PF12(AF2), PB6(AF6), PB8(AF6) |
| I2C4_SDA | PD13(AF4), PF13(AF2), PB7(AF6), PB9(AF6) |
| I2C4_SMBA | PD11(AF4), PF11(AF2), PB5(AF6), PB9(AF11) |

Table 2-2-7 I3C Pin functions

| I3C function | Optional pins |
|---|---|
| I3C_SCL | PE14(AF3), PC4(AF7), PD9(AF5), PF6(AF5) |
| I3C_SDA | PE15(AF3), PC5(AF7), PD10(AF5), PF7(AF5) |

Table 2-2-8 SPI and I2S Pin functions

| SPI1 function | Optional pins |
|---|---|
| SPI1_NSS | PA4(AF5), PA15(AF5), PF4(AF5), PF6(AF3) |
| SPI1_SCK | PA5(AF5), PB3(AF5), PF5(AF5), PF7(AF3) |
| SPI1_MOSI | PA7(AF5), PB5(AF5), PD7(AF5), PF8(AF3) |
| SPI1_MISO | PA6(AF5), PB4(AF5), PF3(AF5), PF9(AF3) |
| SPI2/I2S1 function | Optional pins |
| SPI2_MCK | PC6(AF5), PB5(AF8) |
| SPI2_NSS/I2S1_WS | PB12(AF5), PB9(AF5), PA11(AF5)、PB4(AF7) |
| SPI2_SCK/I2S1_CK | PB13(AF5), PB10(AF5), PA9(AF5), PA12(AF5), PD3(AF5) |
| SPI2_MOSI/I2S1_SDO | PB15(AF5), PC1(AF5), PC3(AF5) |
| SPI2_MISO | PB14(AF5), PC2(AF5) |
| SPI3/I2S2 function | Optional pins |
| SPI3_MCK | PC7(AF6), PB6(AF5) |
| SPI3_NSS/I2S2_WS | PA4(AF6), PA15(AF6) |
| SPI3_SCK/I2S2_CK | PB3(AF6), PC10(AF6), PA14(AF1) |
| SPI3_MOSI/I2S2_SDO | PB2(AF7), PB5(AF7), PC12(AF6), PD6(AF5), PA13(AF1) |
| SPI3_MISO | PB4(AF6), PC11(AF6), PC9(AF5) |
| SPI4 function | Optional pins |
| SPI4_NSS | PE4(AF5), PE11(AF5) |
| SPI4_SCK | PE2(AF5), PE12(AF5) |
| SPI4_MOSI | PE6(AF5), PE14(AF5) |
| SPI4_MISO | PE5(AF5), PE13(AF5) |

Table 2-2-9 USART Pin functions

| USART1 function | Optional pins |
|---|---|
| USART1_CK | PA8(AF7)、PD11(AF14) |
| USART1_RX | PA10(AF7)、PB7(AF7)、PB15(AF4)、PD12(AF14) |
| USART1_TX | PA9(AF7)、PB6(AF7), PB14(AF4)、PD13(AF14) |
| USART1_RTS | PA12(AF7), PD14(AF14) |
| USART1_CTS | PA11(AF7), PD15(AF14) |
| USART2 function | Optional pins |
| USART2_CK | PA4(AF7), PD7(AF7) |

| | |
|---|---|
| USART2_RX | PA3(AF7), PD6(AF7) |
| USART2_TX | PA2(AF7), PD5(AF7) |
| USART2_RTS | PA1(AF7), PD4(AF7) |
| USART2_CTS | PA0(AF7), PD3(AF7) |
| USART3 function | Optional pins |
| USART3_CK | PB12(AF7), PC12(AF7), PD10(AF7), PA11(AF4) |
| USART3_RX | PB11(AF7), PC11(AF7), PD9(AF7), PA14(AF4) |
| USART3_TX | PB10(AF7), PC10(AF7), PD8(AF7), PA13(AF4) |
| USART3_RTS | PB14(AF7), PD12(AF7), PA12(AF4) |
| USART3_CTS | PB13(AF7), PD11(AF7), PA15(AF4) |
| USART4 function | Optional pins |
| USART4_CK | PF1(AF7), PC8(AF7) |
| USART4_RX | PF3(AF7), PC7(AF7) |
| USART4_TX | PF4(AF7), PC6(AF7) |
| USART4_RTS | PF2(AF7), PE0(AF7) |
| USART4_CTS | PF0(AF7), PE1(AF7) |
| USART5 function | Optional pins |
| USART5_CK | PE15(AF11), PD6(AF11) |
| USART5_RX | PE2(AF4) PF5(AF4) |
| USART5_TX | PE3(AF11), PE0(AF4) |
| USART5_RTS | PD7(AF4) |
| USART5_CTS | PE1(AF4) |
| USART6 function | Optional pins |
| USART6_CK | PA2(AF3), PA10(AF6), PB10(AF9), PE2(AF8), PD3(AF8) |
| USART6_RX | PA1(AF8), PA11(AF6), PB8(AF8), PC11(AF8), PD0(AF8) |
| USART6_TX | PA0(AF8), PA12(AF6), PB9(AF8), PC10(AF8), PD1(AF8) |
| USART6_RTS | PA15(AF8), PB14(AF8) |
| USART6_CTS | PB0(AF8), PB15(AF8) |
| USART7 function | Optional pins |
| USART7_CK | PB4(AF14), PB14(AF13), PD4(AF8) |
| USART7_RX | PB5(AF14) PB12(AF14), PD2(AF8) |
| USART7_TX | PB6(AF14), PB13(AF14), PC12(AF8) |
| USART7_RTS | PC8(AF8) |
| USART7_CTS | PC9(AF8) |
| USART8 function | Optional pins |
| USART8_CK | PA14(AF11), PB7(AF10), PE6(AF8), PF10(AF7) |
| USART8_RX | PA8(AF11), PB3(AF11), PE7(AF7), PF6(AF7) |

| | |
|---|---|
| USART8_TX | PA15(AF11), PB4(AF11), PE8(AF7) PF7(AF7) |
| USART8_RTS | PE9(AF11), PF8(AF7) |
| USART8_CTS | PE10(AF11), PF9(AF7) |

Table 2-2-10 Debug Pin Functions

| Debug pin function | Default pin |
|---|---|
| SWCLK | PB8 |
| SWDIO/SWIO | PB9 |

Table 2-2-11 SDIO Pin Functions

| SDIO function | Optional pins |
|---|---|
| SDIO_CK | PB11(AF8), PC1(AF11) |
| SDIO_CMD | PB10(AF8), PA0(AF9) |
| SDIO_D0 | PE8(AF8), PB14(AF9) |
| SDIO_D1 | PE9(AF8), PB15(AF9s) |
| SDIO_D2 | PE10(AF8), PB3(AF9) |
| SDIO_D3 | PE11(AF8), PB4(AF9) |
| SDIO_D4 | PE12(AF8), PB8(AF10) |
| SDIO_D5 | PE13(AF8), PB9(AF10) |
| SDIO_D6 | PE14(AF8), PC6(AF9) |
| SDIO_D7 | PE15(AF8), PC7(AF9) |

Table 2-2-12 SDMMC Pin Functions

| SDMMC function | SDMMC_RM=00 Default map pin | SDMMC_RM=01 Remap pin | SDMMC_RM=1x Remap pin |
|---|---|---|---|
| SDMMC_STS/SDMMC_CMD | PD2 | PD12 | PC10 |
| SDMMC_SDCK/SDMMC_SLVCK | PC12 | PD11 | PC12 |
| SDMMC_STR | PD3 | PD10 | PC11 |
| SDMMC_D0 | PC8 | PB13 | PD0 |
| SDMMC_D1 | PC9 | PC9 | PD1 |
| SDMMC_D2 | PC10 | PB10 | PD2 |
| SDMMC_D3 | PC11 | PB11 | PD3 |
| SDMMC_D4 | PA14 | PA14 | PD4 |
| SDMMC_D5 | PA15 | PA15 | PD5 |
| SDMMC_D6 | PC6 | PC6 | PD6 |
| SDMMC_D7 | PC7 | PC7 | PD7 |

*Note: When using SDMMC in 1-wire or 4-wire mode, the GPIO pins corresponding to unused data lines cannot be repurposed for output. They may be used for input multiplexing or as general-purpose GPIO outputs.*

Table 2-2-13 CAN Pin Functions

| CAN1 function | Optional pins |
|---|---|
| CAN1_RX | PA11(AF9), PB6(AF3), PB8(AF9), PD0(AF9), PA13(AF5) |
| CAN1_TX | PA12(AF9), PB7(AF3), PB9(AF9), PD1(AF9), PA14(AF5) |
| CAN2 function | Optional pins |
| CAN2_RX | PB12(AF9), PB5(AF9) |
| CAN2_TX | PB13(AF9), PB6(AF9) |
| CAN3 function | Optional pins |
| CAN3_RX | PD12(AF5), PF6(AF2), PF4(AF2), PC4(AF6) |
| CAN3_TX | PD13(AF5), PF7(AF2), PF3(AF2), PC5(AF6) |

Table 2-2-14 FSMC Pin Functions

| FSMC function | Optional pins |
|---|---|
| FSMC_NE1 | PD7(AF12) |
| FSMC_NE2 | PF3(AF12) |
| FSMC_NE3 | PF4(AF12) |
| FSMC_NE4 | PE0(AF12) |
| FSMC_NADV | PB7(AF12), PF14(AF12) |
| FSMC_NBL0 | PC12(AF0) |
| FSMC_NBL1 | PC11(AF0) |
| FSMC_NBL2 | PC10(AF0) |
| FSMC_NBL3 | PA15(AF0) |
| FSMC_CLK | PD3(AF12) |
| FSMC_NOE | PD4(AF12) |
| FSMC_NWE | PD5(AF12) |
| FSMC_NWAIT | PD6(AF12) |
| FSMC_NCE2 | PF3(AF12) |
| FSMC_INT2 | PF1(AF12) |
| FSMC_A0 | PF5(AF12) |
| FSMC_A1 | PB3(AF12) |
| FSMC_A2 | PB4(AF12) |
| FSMC_A3 | PB8(AF12) |
| FSMC_A4 | PB9(AF12) |
| FSMC_A5 | PC13(AF12), PB6(AF1) |
| FSMC_A6 | PA10(AF10) |
| FSMC_A7 | PA11(AF10) |
| FSMC_A8 | PA12(AF10) |
| FSMC_A9 | PA13(AF10) |

| | |
|---|---|
| FSMC_A10 | PB10(AF12) |
| FSMC_A11 | PB11(AF12) |
| FSMC_A12 | PB12(AF12) |
| FSMC_A13 | PB13(AF12) |
| FSMC_A14 | PB14(AF12) |
| FSMC_A15 | PB15(AF12) |
| FSMC_A16 | PD11(AF12) |
| FSMC_A17 | PD12(AF12) |
| FSMC_A18 | PD13(AF12) |
| FSMC_A19 | PE3(AF12), PB10(AF6) |
| FSMC_A20 | PE4(AF12), PB11(AF2) |
| FSMC_A21 | PE5(AF12), PB12(AF3) |
| FSMC_A22 | PE6(AF12), PB13(AF15) |
| FSMC_A23 | PE2(AF12), PB14(AF0) |
| FSMC_A24 | PE1(AF12) |
| FSMC_A25 | PD2(AF11) |
| FSMC_D0 | PD14(AF12) |
| FSMC_D1 | PD15(AF12) |
| FSMC_D2 | PD0(AF12) |
| FSMC_D3 | PD1(AF12) |
| FSMC_D4 | PE7(AF12), PC0(AF4) |
| FSMC_D5 | PE8(AF12), PC1(AF4) |
| FSMC_D6 | PE9(AF12), PC2(AF4) |
| FSMC_D7 | PE10(AF12), PC3(AF4) |
| FSMC_D8 | PE11(AF12), PC6(AF4) |
| FSMC_D9 | PE12(AF12), PC7(AF4) |
| FSMC_D10 | PE13(AF12) |
| FSMC_D11 | PE14(AF12) |
| FSMC_D12 | PE15(AF12) |
| FSMC_D13 | PD8(AF12), PC8(AF4) |
| FSMC_D14 | PD9(AF12), PC9(AF7) |
| FSMC_D15 | PD10(AF12) |
| FSMC_D16 | PC14(AF12), PC3(AF11) |
| FSMC_D17 | PC15(AF12), PB5(AF11) |
| FSMC_D18 | PF6(AF12) |
| FSMC_D19 | PF7(AF12) |
| FSMC_D20 | PF8(AF12) |

| | |
|---|---|
| FSMC_D21 | PF9(AF12) |
| FSMC_D22 | PF10(AF12) |
| FSMC_D23 | PA0(AF12) |
| FSMC_D24 | PA1(AF12) |
| FSMC_D25 | PA2(AF12) |
| FSMC_D26 | PA3(AF12) |
| FSMC_D27 | PA4(AF12) |
| FSMC_D28 | PA5(AF12) |
| FSMC_D29 | PB0(AF12) |
| FSMC_D30 | PB1(AF12) |
| FSMC_D31 | PB2(AF12) |

Table 2-2-15 SDRAM Pin Functions

| SDRAM function | Optional pins |
|---|---|
| SDRAM_CLK | PF2(AF12), PE2(AF9), PF14(AF1) |
| SDRAM_CS_N0 | PC2(AF12), PC4(AF12), PD6(AF3), PE3(AF9) |
| SDRAM_CS_N1 | PF0(AF4), PB6(AF12), PD7(AF3), PE4(AF9) |
| SDRAM_CKE0 | PC5(AF12), PC3(AF12), PB8(AF3), PF3(AF4), PB8(AF3) |
| SDRAM_CKE1 | PB5(AF12), PC14(AF9), PF4(AF4), PB9(AF3) |
| SDRAM_RAS_N | PF11(AF12), PC15(AF9), PF3(AF3), PC10(AF1), PE5(AF9) |
| SDRAM_CAS_N | PF12(AF12), PC0(AF15), PC0(AF15) |
| SDRAM_WE_N | PC0(AF12), PA7(AF12), PC1(AF15) |
| SDRAM_DQM0 | PC12(AF0), PC2(AF15) |
| SDRAM_DQM1 | PC11(AF0), PE3(AF1), PC3(AF15) |
| SDRAM_DQM2 | PC10(AF0), PA6(AF6), PA0(AF15), PC11(AF1), PE6(AF7) |
| SDRAM_DQM3 | PA15(AF0), PA8(AF6), PB0(AF7) |
| SDRAM_BA0 | PB14(AF12), PB1(AF7) |
| SDRAM_BA1 | PB15(AF12), PE10(AF15), PA13(AF3) |
| SDRAM_A0 | PF5(AF12), PE11(AF15), PA14(AF3) |
| SDRAM_A1 | PB3(AF12), PE12(AF15), PA15(AF12) |
| SDRAM_A2 | PB4(AF12), PE13(AF15) |
| SDRAM_A3 | PB8(AF12), PE0(AF0), PE14(AF15) |
| SDRAM_A4 | PB9(AF12), PE1(AF0), PE15(AF15) |
| SDRAM_A5 | PB6(AF11), PC13(AF12), PB10(AF0) |
| SDRAM_A6 | PA10(AF10), PB11(AF0) |
| SDRAM_A7 | PA11(AF10), PB12(AF0) |
| SDRAM_A8 | PA12(AF10), PB13(AF0) |

| | |
|---|---|
| SDRAM_A9 | PA13(AF10), PD9(AF0), PB14(AF0) |
| SDRAM_A10 | PB10(AF12), PD10(AF0) |
| SDRAM_A11 | PB11(AF12), PD11(AF0) |
| SDRAM_A12 | PB12(AF12), PD12(AF0) |
| SDRAM_D0 | PD14(AF12), PD13(AF0) |
| SDRAM_D1 | PD15(AF12), PD14(AF0) |
| SDRAM_D2 | PD0(AF12), PD15(AF0) |
| SDRAM_D3 | PD1(AF12), PF0(AF2) |
| SDRAM_D4 | PE7(AF12), PF1(AF2) |
| SDRAM_D5 | PE8(AF12), PF2(AF2) |
| SDRAM_D6 | PE9(AF12), PC6(AF0) |
| SDRAM_D7 | PE10(AF12), PC7(AF0) |
| SDRAM_D8 | PE11(AF12), PC8(AF0) |
| SDRAM_D9 | PE12(AF12), PC9(AF0) |
| SDRAM_D10 | PE13(AF12), PA9(AF0), PD0(AF1) |
| SDRAM_D11 | PE14(AF12), PA10(AF0), PD1(AF1) |
| SDRAM_D12 | PE15(AF12), PA11(AF0), PD2(AF1) |
| SDRAM_D13 | PD8(AF12), PA12(AF0), PD3(AF1) |
| SDRAM_D14 | PD9(AF12), PA13(AF0), PD4(AF1) |
| SDRAM_D15 | PD10(AF12), PA14(AF0), PD5(AF1) |
| SDRAM_D16 | PC14(AF12), PC3(AF11) |
| SDRAM_D17 | PC15(AF12), PB5(AF11), PE10(AF3) |
| SDRAM_D18 | PF6(AF12), PE11(AF3) |
| SDRAM_D19 | PF7(AF12), PE12(AF3) |
| SDRAM_D20 | PF8(AF12), PA9(AF8) |
| SDRAM_D21 | PF9(AF12), PA10(AF8) |
| SDRAM_D22 | PF10(AF12), PA11(AF8) |
| SDRAM_D23 | PA0(AF12), PA12(AF8) |
| SDRAM_D24 | PA1(AF12), PC10(AF3) |
| SDRAM_D25 | PA2(AF12), PC11(AF3) |
| SDRAM_D26 | PA3(AF12), PC12(AF3) |
| SDRAM_D27 | PA4(AF12), PE5(AF10) |
| SDRAM_D28 | PA5(AF12), PE6(AF10) |
| SDRAM_D29 | PB0(AF12), PF5(AF3) |
| SDRAM_D30 | PB1(AF12), PE0(AF3) |
| SDRAM_D31 | PB2(AF12), PE1(AF3) |

Table 2-2-16 UHSIF Pin Functions

| UHSIF function | UHSIF_PORT_RM=00<br>Default mapping pin | UHSIF_PORT_RM=01<br>Remapping pin | UHSIF_PORT_RM=1x<br>Remapping pin |
|---|---|---|---|
| UHSIF_PORT0 | PF12 | PF12 | PC1 |
| UHSIF_PORT1 | PF13 | PF13 | PC2 |
| UHSIF_PORT2 | PE7 | PE7 | PC3 |
| UHSIF_PORT3 | PE8 | PC1 | PB0 |
| UHSIF_PORT4 | PE9 | PC2 | PB1 |
| UHSIF_PORT5 | PE10 | PC3 | PE10 |
| UHSIF_PORT6 | PE11 | PB0 | PE11 |
| UHSIF_PORT7 | PE12 | PB1 | PE12 |
| UHSIF_PORT8 | PE13 | | |
| UHSIF_PORT9 | PE14 | | |
| UHSIF_PORT10 | PE15 | | |
| UHSIF_PORT11 | PB10 | | |
| UHSIF_PORT12 | PB11 | | |
| UHSIF_PORT13 | PB12 | | |
| UHSIF_PORT14 | PB13 | | |
| UHSIF_PORT15 | PB14 | | |
| UHSIF_PORT16 | PD10 | | |
| UHSIF_PORT17 | PD11 | | |
| UHSIF_PORT18 | PD12 | | |
| UHSIF_PORT19 | PD13 | | |
| UHSIF_PORT20 | PD14 | | |
| UHSIF_PORT21 | PD15 | | |
| UHSIF_PORT22 | PF0 | | |
| UHSIF_PORT23 | PF1 | | |
| UHSIF_PORT24 | PF2 | | |
| UHSIF_PORT25 | PC6 | | |
| UHSIF_PORT26 | PC7 | | |
| UHSIF_PORT27 | PC8 | | |
| UHSIF_PORT28 | PC9 | | |
| UHSIF_PORT29 | PA13 | | |
| UHSIF_PORT30 | PA14 | | |
| UHSIF_PORT31 | PA15 | | |
| UHSIF_PORT32 | PC10 | | |
| UHSIF_PORT33 | PC11 | | |
| UHSIF_PORT34 | PC12 | | |
| UHSIF_PORT35 | PD0 | | |

| | | | | |
|---|---|---|---|---|
| UHSIF_PORT36 | PD1 | | | |
| UHSIF_PORT37 | PD2 | | | |
| UHSIF_PORT38 | PD3 | | | |
| UHSIF_PORT39 | PD4 | | | |
| UHSIF_PORT40 | PD5 | | | |
| UHSIF_PORT41 | PD6 | | | |
| UHSIF_PORT42 | PD7 | | | |
| UHSIF_PORT43 | PF3 | | | |
| UHSIF_PORT44 | PF4 | | | |
| UHSIF_PORT45 | PF5 | | | |
| UHSIF_PORT46 | PE0 | | | |
| UHSIF_PORT47 | PE1 | | | |
| UHSIF function | UHSIF_CLK_RM=00<br>Default mapping | UHSIF_CLK_RM=01<br>Remapping | UHSIF_CLK_RM=10<br>Remapping | UHSIF_CLK_RM=11<br>Remapping |
| UHSIF_CLK | PF11 | PC0 | PF14 | PD9 |

*Note: UHSIF_PORT_RM = 01 applies to chips packaged in 56/68-pin configurations; UHSIF_PORT_RM = 1x applies to chips packaged in 88-pin configurations.*

Table 2-2-17 USBPD Pin Functions

| USBPD function | Optional pin |
|---|---|
| CC1 | PB3(AF4) |
| CC2 | PB4(AF4) |

Table 2-2-18 USBFS Pin Functions

| USBFS function | Optional pin |
|---|---|
| OTG_DP | PA12 |
| OTG_DM | PA11 |
| OTG_VBUS | PA9 |
| OTG_ID | PA10 |

Table 2-2-19 USBHS Pin Functions

| USBHS function | Optional pin |
|---|---|
| USBHS_DP | PB8 |
| USBHS_DM | PB9 |

Table 2-2-20 SerDes Pin Functions

| SerDes function | Default pin |
|---|---|
| SERDES_RXP | PE3 |
| SERDES_RXN | PE4 |
| SERDES_TXP | PE5 |

| | |
|---|---|
| SERDES_TXN | PE6 |

Table 2-2-21 OPA Pin Functions

| OPA1 function | Optional pins |
|---|---|
| OPA1_P | PB0/OPA1_P0, PA6/OPA1_P1 |
| OPA1_N | PB1/OPA1_N0, PA7/OPA1_N1 |
| OPA1_OUT | PC4/OPA1_OUT0, PA5/OPA1_OUT1 |
| OPA2 function | Optional pins |
| OPA2_P | PE9/OPA2_P0, PF11/OPA2_P1 |
| OPA2_N | PE8/OPA2_N0, PF12/OPA2_N1 |
| OPA2_OUT | PE7/OPA2_OUT0, PB1/OPA2_OUT1 |
| OPA3 function | Optional pins |
| OPA3_P | PC2/OPA3_P0, PA2/OPA3_P1 |
| OPA3_N | PC3/OPA3_N0, PA3/OPA3_N1 |
| OPA3_OUT | PA0/OPA3_OUT0, PA4/OPA3_OUT1 |

Table 2-2-22 CMP Pin Functions

| CMP function | Optional pins |
|---|---|
| CMP_P | PB0/CMP_P0, PB2/CMP_P1, OPA1_OUT/CMP_P2 |
| CMP_N | PB1/CMP_N0, PC4/CMP_N1, DAC1_OUT/CMP_N2 |
| CMP function | Optional pins (MODE[3:0] = 0000b) |
| CMP_OUT | PC5(AF13), PE12(AF13), PA6(AF10), PA8(AF12), PB12(AF13), PE6(AF11), PE15(AF13) |

*Note: Refer to the Operational Amplifier (OPA) and Comparator (CMP) sections of the CH32H417RM manual for more information on bits MODE[3:0].*

Table 2-2-23 DVP Pin Functions

| DVP function | Optional pins |
|---|---|
| DVP_HSYNC | PA4(AF13), PB13(AF8) |
| DVP_VSYNC | PB7(AF13), PF3(AF13), PA5(AF11), PB14(AF15) |
| DVP_PCLK | PA6(AF13), PF13(AF11), PB12(AF15) |
| DVP_D0 | PC6(AF13), PA9(AF13), PE0(AF11) |
| DVP_D1 | PC7(AF13), PA10(AF13), PE1(AF11) |
| DVP_D2 | PC8(AF13), PE2(AF13), PF4(AF13), PB13(AF13) |
| DVP_D3 | PC9(AF13), PE3(AF13), PF5(AF13) |
| DVP_D4 | PC11(AF13), PE4(AF13), PD12(AF13) |
| DVP_D5 | PB6(AF13), PD3(AF13), PB3(AF13), PF14(AF11), PD13(AF13) |
| DVP_D6 | PB8(AF13), PE5(AF13), PD14(AF13) |

| | |
|---|---|
| DVP_D7 | PB9(AF13), PE6(AF13), PD15(AF13) |
| DVP_D8 | PC10(AF13), PF4(AF11) |
| DVP_D9 | PC12(AF13) PF3(AF11) |
| DVP_D10 | PD6(AF13), PB5(AF13) |
| DVP_D11 | PD2(AF13), PF10(AF13), PF0(AF12) |

Table 2-2-24 Ethernet Pin Functions

| Ethernet function | Optional pins |
|---|---|
| RGMII_RXC | PA15(AF3) |
| RGMII_RXDV | PA14(AF12) |
| RGMII_RD0 | PC9(AF12) |
| RGMII_RD1 | PC8(AF12) |
| RGMII_RD2 | PC7(AF12) |
| RGMII_RD3 | PC6(AF12) |
| RGMII_GTXC | PD15(AF10) |
| RGMII_TXEN | PD14(AF10) |
| RGMII_TXD0 | PD13(AF10) |
| RGMII_TXD1 | PD12(AF10) |
| RGMII_TXD2 | PD11(AF10) |
| RGMII_TXD3 | PD10(AF10) |
| ETH_PHY_LED0 | PF0(AF10) |
| ETH_PHY_LED1 | PF1(AF10) |
| ETH_PHY_LED2 | PF2(AF10) |
| ETH_PHY_LED3 | PB13(AF10) |
| ETH_PHY_LED4 | PB14(AF10) |
| ETH_MDC | PC0(AF1) |
| ETH_MDIO | PC1(AF1) |
| ETH_PPS | PC2(AF1) |

Table 2-2-25 QSPI Pin Functions

| QSPI1 function | Optional pins |
|---|---|
| QSPI1_SCK | PB2(AF9) |
| QSPI1_SCSN | PB6(AF10) |
| QSPI1_SIO0 | PF8(AF10), PD11(AF9), PC9(AF9) |
| QSPI1_SIO1 | PF9(AF10), PD12(AF9), PC10(AF9) |
| QSPI1_SIO2 | PF7(AF10), PD14(AF9) |
| QSPI1_SIO3 | PF6(AF10), PD13(AF9), PA1(AF9) |
| QSPI1_SCSXN | PC11(AF9) |

| | |
|---|---|
| QSPI1_SIOX0 | PE7(AF10) |
| QSPI1_SIOX1 | PE8(AF10) |
| QSPI1_SIOX2 | PE9(AF10), PF3(AF9) |
| QSPI1_SIOX3 | PE10(AF10), PF5AF9) |
| QSPI2 function | Optional pins |
| QSPI2_SCK | PF6(AF4), PE10(AF7), PF0(AF5) |
| QSPI2_SCSN | PF7(AF4), PE11(AF7), PF1(AF5) |
| QSPI2_SIO0 | PF8(AF4), PE12(AF7), PF2(AF5) |
| QSPI2_SIO1 | PF9(AF4), PE13(AF7) |
| QSPI2_SIO2 | PF10(AF4), PE14(AF7) |
| QSPI2_SIO3 | PC0(AF10), PE15(AF7) |
| QSPI2_SCSXN | PC1(AF10), PB10(AF11) |
| QSPI2_SIOX0 | PC2(AF10), PB11(AF11) |
| QSPI2_SIOX1 | PC3(AF10), PB12(AF11) |
| QSPI2_SIOX2 | PA0(AF4), PB13(AF11) |
| QSPI2_SIOX3 | PA1(AF4), PB14(AF11) |

Table 2-2-26 SWPMI Pin Functions

| SWPMI function | Optional pins (Non-1-wire mode) | Optional pins (1-wire mode) |
|---|---|---|
| SWP_RX | PC8(AF11), PC10(AF11) | PC6(AF11) |
| SWP_TX | PC7(AF11) | PC6(AF11) |
| SWP_SUP | PC9(AF11) | - |

Table 2-2-27 SAI Pin Functions

| SAI function | Optional pins |
|---|---|
| SAI_FS_A | PE4(AF6), PC3(AF7) |
| SAI_SCK_A | PE5(AF6), PC2(AF7) |
| SAI_SD_A | PE6(AF6), PC1(AF6), PB2(AF6), PD6(AF6) |
| SAI_MCLK_A | PE2(AF6), PG7PF1(AF6), PC0(AF7) |
| SAI_FS_B | PF9(AF6), PA15(AF13) |
| SAI_SCK_B | PF8(AF6), PA14(AF13) |
| SAI_SD_B | PF6(AF6), PE3(AF6), PA13(AF13) |
| SAI_MCLK_B | PF7(AF6), PC9(AF15) |

Table 2-2-28 LTDC Pin Functions

| LTDC function | Optional pins |
|---|---|
| LTDC_CLK | PF1(AF14), PB14(AF14), PE14(AF14), PA15(AF15) |

| | |
|---|---|
| LTDC_HSYNC | PC6(AF14), PC10(AF15), PA6(AF11) |
| LTDC_VSYNC | PA7(AF14), PA4(AF14), PC11(AF15), PB12(AF10) |
| LTDC_DE | PC5(AF14), PE13(AF14), PF10(AF14), PC12(AF15) |
| LTDC_R0 | PE1(AF14), PA0(AF14), PA14(AF15) |
| LTDC_R1 | PF0(AF11), PA2(AF14) |
| LTDC_R2 | PD13(AF3), PA1(AF14), PC10(AF14) |
| LTDC_R3 | PD12(AF11), PA15(AF9), PB0(AF9), PD0(AF15) |
| LTDC_R4 | PD11(AF11), PA5(AF14), PA11(AF14), PD1(AF15) |
| LTDC_R5 | PA9(AF14), PC0(AF14), PA12(AF14), PD2(AF15) |
| LTDC_R6 | PA8(AF14), PC12(AF14), PB1(AF9), PE2(AF14), PD3(AF15) |
| LTDC_R7 | PC4(AF14), PF0(AF14), PE15(AF14), PD4(AF15) |
| LTDC_G0 | PE5(AF14), PB1(AF14), PB14(AF6) |
| LTDC_G1 | PE6(AF14), PB0(AF14) |
| LTDC_G2 | PA6(AF14), PC0(AF11), PD5(AF15), PD15(AF7) |
| LTDC_G3 | PC9(AF10), PF4(AF9), PE11(AF14), PD6(AF15) |
| LTDC_G4 | PC8(AF14), PB10(AF14), PD7(AF15) |
| LTDC_G5 | PC1(AF14), PB11(AF14), PF3(AF15) |
| LTDC_G6 | PC7(AF14), PF4(AF15) |
| LTDC_G7 | PD3(AF14), PB15(AF14), PF2(AF14), PF5(AF15) |
| LTDC_B0 | PE4(AF14), PF3(AF14), PF1(AF8) |
| LTDC_B1 | PE0(AF14), PA10(AF14), PC10(AF10), PD0(AF14), PD14(AF8) |
| LTDC_B2 | PD6(AF14), PA3(AF9), PC9(AF14) PD2(AF14), PF4(AF14), PA13(AF8) |
| LTDC_B3 | PD7(AF14), PA8(AF13), PD10(AF14), PF5(AF14), PE0(AF15) |
| LTDC_B4 | PD4(AF14), PA10(AF12), PC11(AF14), PE12(AF14), PE0(AF9), PE1(AF15) |
| LTDC_B5 | PD5(AF14), PA3(AF14), PB5(AF3), PF14(AF15) |
| LTDC_B6 | PA14(AF14), PA15(AF14), PB8(AF14) |
| LTDC_B7 | PD2(AF9), PD8(AF14), PB9(AF14) |

Table 2-2-29 DFSDM Pin Functions

| DFSDM function | Optional pins |
|---|---|
| DFSDM_DATIN0 | PC1(AF3) |
| DFSDM_CKIN0 | PC0(AF3) |
| DFSDM_DATIN1 | PC3(AF3), PB1(AF6), PD6(AF4), PB12(AF6) |
| DFSDM_CKIN1 | PC2(AF3), PB2(AF4), PD7(AF6), PB13(AF6) |
| DFSDM_CKOUT | PE9(AF3), PB0(AF6), PC2(AF6), PD10(AF3), PD3(AF3) |

Table 2-2-30 MCO Pin Functions

| MCO function | Optional pins |
|---|---|
| MCO | PB0(AF0) |

Table 2-2-31 PIOC Pin Functions

| PIOC function | Optional pins |
|---|---|
| PIOC_IO0 | PE3(AF5), PB8(AF5), PF12(AF3), PC1(AF7), PA0(AF5) |
| PIOC_IO1 | PE4(AF4), PB9(AF7), PF13(AF5), PC2(AF8), PF14(AF5), PC0(AF5) |

# Chapter 3 Electrical Characteristics

## 3.1 Test Conditions

All voltages are referenced to $V_{SS}$ unless otherwise noted and labeled.

All minimum and maximum values will be guaranteed under worst case ambient temperature, supply voltage and clock frequency conditions.

CH32H417 typical values are based on a room temperature of 25°C, supplying $V_{DD33}$ = $V_{DD33A}$ = 3.3V, $V_{DDIO}$ = 3.3V, generating $V_{IO18}$ = 1.8V or 3.3V, $V_{DD12A}$ = 1.2V, and $V_{DDK}$ = 1.2V for design guidance.

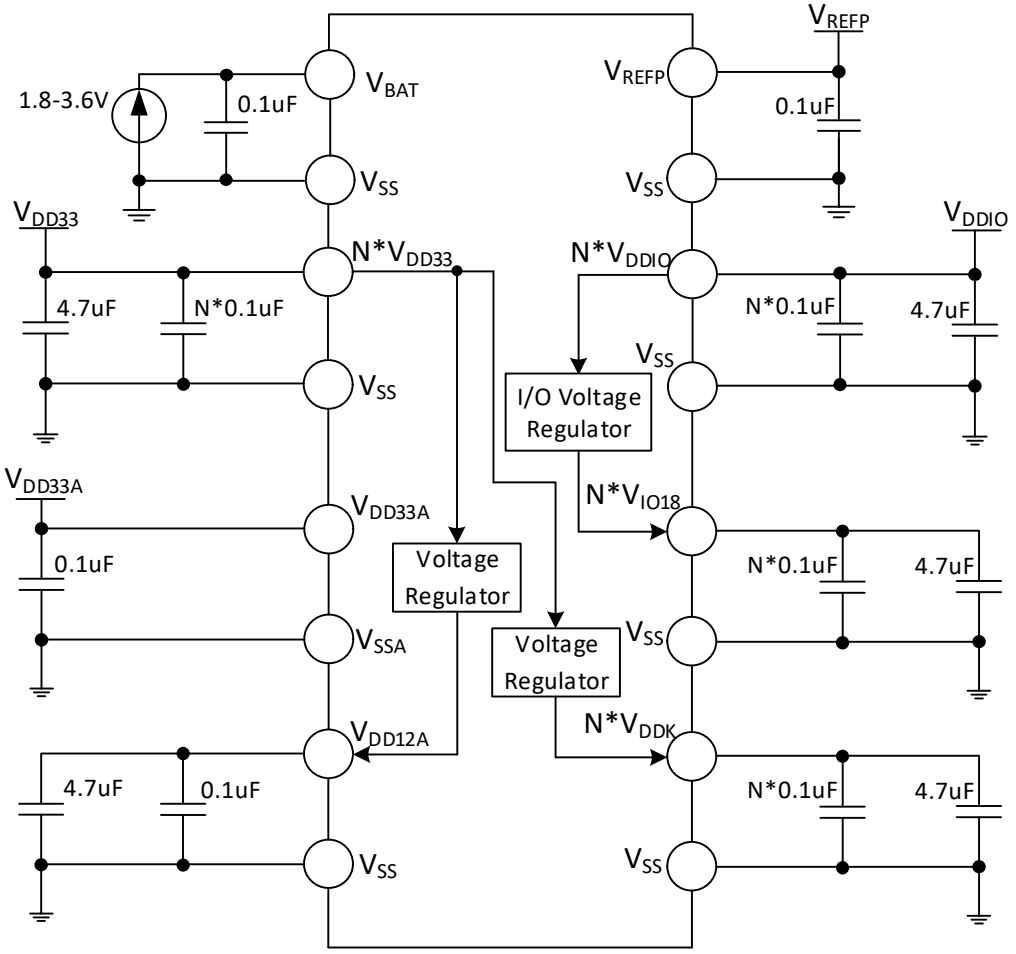
CH32H416 typical values are based on an environment used for design guidance at room temperature 25°C, supply $V_{DD33}$ = $V_{DD33A}$ = 3.3V, producing $V_{DD12A}$ = 1.2V, $V_{DDK}$ = 1.2V.

CH32H415 typical values are based on a room temperature of 25°C, supply $V_{DD33}$ = $V_{DD33A}$ = 3.3V, and generate $V_{DDK}$ = 1.2V for design guidance.

For data obtained through comprehensive evaluation, design simulation or process characterization, no testing is performed on the production line. Minimum and maximum values are statistically obtained after sample testing on the basis of a comprehensive evaluation. Characterization parameters are guaranteed by comprehensive evaluation or design unless specifically stated as measured values.

Power supply scheme:

Figure 3-1-1 CH32H417 Conventional power supply typical circuit




*Note: For CH32H417 chip, $V_{DD33}$, $V_{DDIO}$, $V_{IO18}$ and $V_{DDK}$ may have N (N>1) pins in some chip packages, and the power supply pins with the same name must be shorted.*

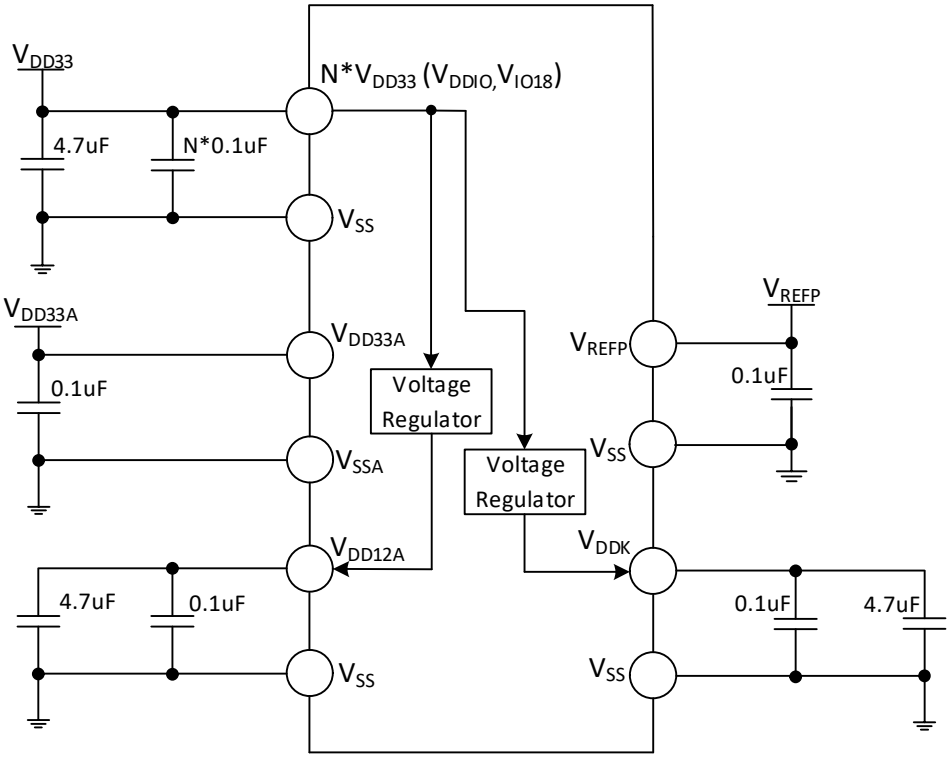
*The main $V_{DD33}$ pin (adjacent to the Ethernet signal pin) is connected to an external 0.1uF shunt decoupling capacitor of 4.7uF capacity, and the remaining $V_{DD33}$ pins are connected to an external decoupling capacitor of 0.1uF capacity only.*

*The main $V_{DDIO}$ pin (adjacent to $V_{IO18}$) is connected with 0.1uF external decoupling capacitor in parallel with 4.7uF capacity, and the remaining $V_{DDIO}$ pins only need to be connected with 0.1uF external decoupling capacitor.*

*The main $V_{IO18}$ pin (adjacent to $V_{DDIO}$) is connected to a 0.1uF shunt 4.7uF capacity decoupling capacitor externally, and the remaining $V_{IO18}$ pins only need to be connected to a 0.1uF capacity decoupling capacitor externally.*

*The main $V_{DDK}$ pin (adjacent to $V_{DD33}$) is connected with a 0.1uF shunt decoupling capacitor of 4.7uF capacity, and the remaining $V_{DDK}$ pins are connected with an external decoupling capacitor of 0.1uF capacity only.*

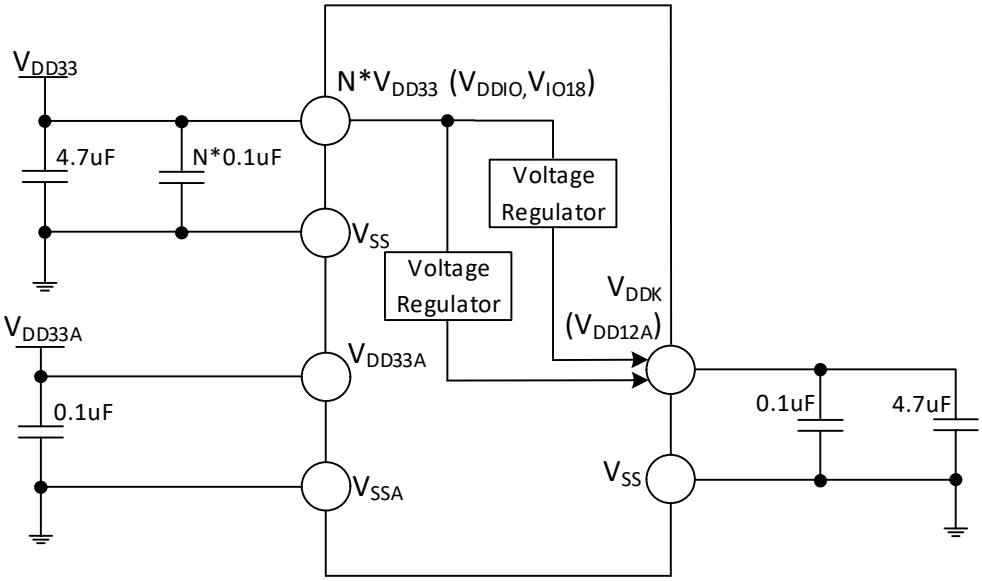
Figure 3-1-2 CH32H416 Conventional power supply typical circuit




*Note: For the CH32H416RDU6 chip, $V_{DD33}$ has 2 pins, and the power supply pin of the same name must be shorted.*

*The main $V_{DD33}$ pin (adjacent to the $V_{DDK}$ pin) is connected externally to a 0.1uF shunt decoupling capacitor of 4.7uF capacity, and the remaining $V_{DD33}$ pins are only connected externally to a 0.1uF capacity decoupling capacitor.*

Figure 3-1-3 CH32H415 Conventional power supply typical circuit




*Note: For the CH32H415REU6 chip, VDD33 has 2 pins, and the power supply pin of the same name must be shorted.*

*The main VDD33 pin (adjacent to the VDDK pin) is connected externally to a 0.1uF shunt decoupling capacitor*

*of 4.7uF capacity, and the remaining VDD33 pins are only connected externally to a 0.1uF capacity decoupling capacitor.*

## 3.2 Absolute Maximum Ratings

Critical or exceeding the absolute maximum value may cause the chip to operate improperly or even be damaged.

Table 3-1 Absolute maximum ratings

| Symbol | Description | Min. | Max. | Unit |
|---|---|---|---|---|
| $T_A$ | Ambient temperature during operation | -40 | 85 | ℃ |
| $T_S$ | Ambient temperature during storage | -40 | 125 | ℃ |
| $V_{DD33}$ | External mains supply voltage (including $V_{DD33A}$ and $V_{DD33}$) | -0.3 | 4.0 | V |
| $V_{DDIO}$ | Power supply voltage of some conventional I/O pins | -0.3 | 4.0 | V |
| $V_{IO18}$ | Power supply voltage of some high-speed I/O pins | -0.3 | 4.0 | V |
| $V_{DD12A}$ | USB 3.0 module power supply voltage | -0.3 | 1.5 | V |
| $V_{DDK}$ | Power supply decoupling terminal of core circuit | -0.3 | 1.5 | V |
| $V_{REFP}$ | Positive reference voltage of ADC, HSADC and DAC modules | -0.3 | $V_{DD33A}$+0.3 | V |
| $V_{IN}$ | Input voltage on FT (tolerant 5V) pin. | -0.3 | 5.5 | V |
| | Input voltage on USB 2.0 and Ethernet PHY pins | -0.3 | $V_{DD33}$+0.3 | V |
| | Input voltage on some high-speed I/O pins (powered by VIO18) | -0.3 | $V_{IO18}$+0.3 | V |
| | Input voltage on USB 3.0 pin | -0.3 | $V_{DD12A}$+0.3 | V |
| | Input voltage on other pins (supplied by $V_{DDIO}$) | -0.3 | $V_{DDIO}$+0.3 | V |
| $\|\Delta V_{DD33\_x}\|$ | Voltage difference between each $V_{DD33}$ of the main power supply pin | | 20 | mV |
| $\|\Delta V_{DDIO\_x}\|$ | Voltage difference between different $V_{DDIO}$ supply pins | | 20 | mV |
| $\|\Delta V_{IO18\_x}\|$ | Voltage difference between different $V_{IO18}$ supply pins | | 20 | mV |
| $\|\Delta V_{SS\_x}\|$ | Voltage difference between each $V_{SS}$ of the common ground pin | | 20 | mV |
| $V_{ESDIO(HBM)}$ | ESD electrostatic discharge voltage (HBM) for Common I/O Pins | 4K | | V |
| $I_{VDD33}$ | Total current of all $V_{DD33}$/$V_{DD33A}$ main supply pins | | 400 | mA |
| $I_{VIO}$ | Total current of all $V_{DDIO}$/$V_{IO18}$ supply pins | | 200 | mA |
| $I_{VSS}$ | Total current of all $V_{SS}$ common ground pins | | 600 | mA |
| $I_{IO}$ | Sink current on arbitrary I/O and control pins | | 25 | mA |
| | Source current on arbitrary I/O and control pins | | -25 | |

## 3.3 Electrical Characteristics

### 3.3.1 Operating Conditions

Table 3-2 General operating conditions

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{CORE1}$ | Core RISC-V5F frequency | LDO_VDDK = 011 (Default) | | | 400(4) | MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | LDO_VDDK = 101 | | | 480(5) | MHz |
| $F_{HCLK}$ Or $F_{CORE0}$ | Internal system bus frequency or core RISC-V3F frequency | LDO_VDDK = 011 (Default) | | | 150 | MHz |
| | | LDO_VDDK = 101 | | | 180(5) | MHz |
| $V_{DD33}$ | Standard working voltage | USB or ETH not used | 2.4 | 3.3 | 3.6 | V |
| | | Use USB or ETH or SerDes | 3.2 | 3.3 | 3.45 | V |
| $V_{DD33A}$ | Analog part working voltage | ADCs, HSADCs and DACs not used, $V_{DD33A}$ cannot be lower than $V_{DDIO}$ | 1.8 | 3.3 | 3.6 | V |
| | | Use the ADC, $V_{DD33A}$ cannot be lower than $V_{DDIO}$ and $V_{REFP}$ cannot be higher than $V_{DD33A}$ | 2.4 | 3.3 | 3.6 | V |
| | | Use the HSADC, $V_{DD33A}$ cannot be lower than $V_{DDIO}$ and $V_{REFP}$ cannot be higher than $V_{DD33A}$ | 3.0 | 3.3 | 3.6 | V |
| | | Use OPA, OPA output cannot be higher than $V_{DDIO}$ | 1.8 | 3.3 | 3.6 | V |
| | | Use DAC, DAC output cannot be higher than $V_{DDIO}$ | 2.4 | 3.3 | 3.6 | V |
| $V_{DD12A}$(1) | Working voltage of USB 3.0 module | | 1.18 | 1.2 | 1.28 | V |
| $V_{DDK}$(1) | Core operating voltage | | 1.17 | 1.2 | 1.27 | V |
| $V_{DDIO}$ | Working voltage of some conventional I/O pins | $V_{DDIO}$ cannot be higher than $V_{DD33}$ | 1.8 | 3.3 | 3.6 | V |
| $V_{IO18}$ | Working voltage of some high-speed I/O pins | $V_{IO18}$ cannot be higher than $V_{DDIO}$ | 1.1 | | 3.6 | V |
| $R_{HSEXO\_ext}$ | Pull-down resistor externally connected to XO pin (used to configure the default output voltage of $V_{IO18}$ during initial power-up) | $V_{IO18}$ default output 2.5V | 220 | 300 | 400 | kΩ |
| | | $V_{IO18}$ default output 1.8V | 1200 | Floating | | kΩ |
| | | $V_{IO18}$ default output 1.2V | 60 | 82 | 110 | kΩ |
| $V_{BAT}$ | Working voltage of backup unit | | 1.8 | | 3.6 | V |
| $V_{REFP}$(2) | Positive reference voltage of ADC, HSADC and DAC modules | $V_{REFP}$ cannot be higher than $V_{DD33A}$ | 2.4 | 3.3 | 3.6 | V |
| $T_A$ | Ambient temperature at work | | -40 | | 85 | ℃ |
| $T_J$ | Junction temperature | | -40 | | 105 | ℃ |

*Note:*

*1. $V_{DD12A}$ and $V_{DDK}$ current is large, consider the PCB alignment voltage drop loss, if the external power supply is recommended 1.2V plus 20 to 60mV.*

*2. $V_{REFP}$ external capacitance to be as close as possible, otherwise affect the ADC performance.*

*3. For CH32V417 chip, voltage relationship: $V_{DD33} \geq V_{DD33A} \geq V_{DDIO} \geq V_{IO18}$; and $V_{DD33A} \geq V_{REFP}$.*

*For CH32V416 chip, voltage relationship: $V_{DD33} = V_{DD33A}$; and $V_{DD33A} \geq V_{REFP}$.*

*For CH32V415 chip, voltage relationship: $V_{DD33} = V_{DD33A}$.*

*4. Measured at room temperature is not less than 480MHz. Temperature and process fluctuations are not taken into account, and 480MHz is prohibited to be used in official projects.*

*5. Only for commercial grade application: $T_A \leq 70℃$ and good heat dissipation.*

Table 3-3 Power-on and power-down conditions

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{VDD33}$ | $V_{DD33}$ rising rate | | 0 | ∞ | us/V |
| | $V_{DD33}$ falling rate | | 20 | ∞ | us/V |
| $t_{VDD33A}$ | $V_{DD33A}$ rising rate | $V_{DD33}$ power-on | 0 | 10000 | us/V |
| | $V_{DD33A}$ falling rate | | 20 | ∞ | us/V |

### 3.3.2 Built-in Reset and Power Control Block Characteristics

Table 3-4 Reset and voltage monitor

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{PVD}$(1) | Level selection of programmable voltage detector(2) | PLS[2:0] = 000 (Rising edge) | | 2.54 | | V |
| | | PLS[2:0] = 000 (Falling edge) | | 2.44 | | V |
| | | PLS[2:0] = 001 (Rising edge) | | 2.60 | | V |
| | | PLS[2:0] = 001 (Falling edge) | | 2.49 | | V |
| | | PLS[2:0] = 010 (Rising edge) | | 2.70 | | V |
| | | PLS[2:0] = 010 (Falling edge) | | 2.59 | | V |
| | | PLS[2:0] = 011 (Rising edge) | | 2.80 | | V |
| | | PLS[2:0] = 011 (Falling edge) | | 2.69 | | V |
| | | PLS[2:0] = 100 (Rising edge) | | 2.90 | | V |
| | | PLS[2:0] = 100 (Falling edge) | | 2.79 | | V |
| | | PLS[2:0] = 101 (Rising edge) | | 3.00 | | V |
| | | PLS[2:0] = 101 (Falling edge) | | 2.89 | | V |
| | | PLS[2:0] = 110 (Rising edge) | | 3.10 | | V |
| | | PLS[2:0] = 110 (Falling edge) | | 2.99 | | V |
| | | PLS[2:0] = 111 (Rising edge) | | 3.20 | | V |
| | | PLS[2:0] = 111 (Falling edge) | | 3.09 | | V |
| $V_{PVDhyst}$ | PVD hysteresis | | | 0.11 | | V |
| $V_{POR/PDR}$ | Power-on/power-down reset threshold | Rising edge | | 2.35 | | V |
| | | Falling edge | | 2.33 | | V |
| $V_{PDRhyst}$ | PDR hysteresis | | | 20 | | mV |

*Note: 1. Normal temperature test value.*

### 3.3.3 Embedded Reference Voltage

Table 3-5 Embedded reference voltage

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{REFINT}$ | Built-in reference voltage | $T_A$ = -40℃ ~ | 1.17 | 1.21 | 1.24 | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | 85℃ | | | | |

### 3.3.4 Supply Current Characteristics

Current consumption is a comprehensive index of a variety of parameters and factors. These parameters and factors include operating voltage, ambient temperature, I/O pin load, software configuration of the product, the operating frequency, flip rate of the I/O pin, the location of the program in memory and the executed code, etc. The current consumption measurement method is as follows:

Figure 3-2-1 CH32H417 Current consumption measurement

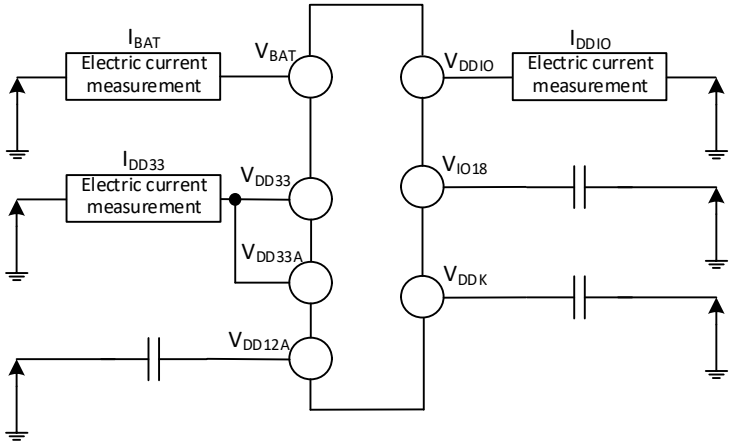



Figure 3-2-2 CH32H416 Current consumption measurement

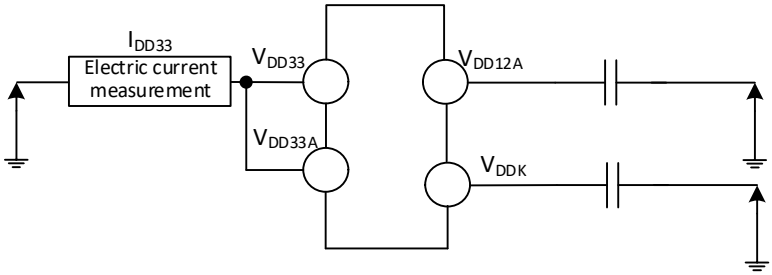
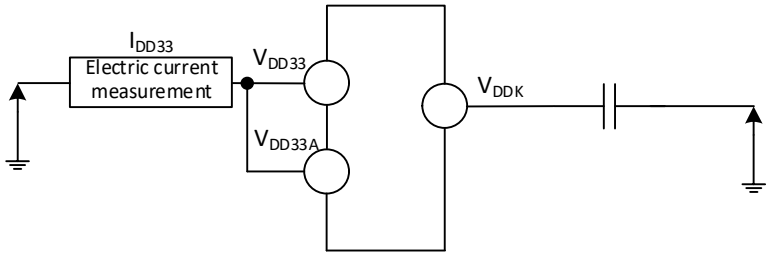



Figure 3-2-3 CH32H415 Current consumption measurement




The CH32H417 is at the following conditions:

Tested at room temperature $V_{DD33}$ = $V_{DD33A}$ = 3.3V, $V_{DDIO}$ = 3.3V, VIO18 = 1.8V: All I/O ports configured with pull-down inputs, HSI = 25MHz (calibrated), and $F_{HCLK}$ = $F_{V3F}$. Enable or disable all peripheral clocks for power consumption.

The CH32H416 is in the following conditions:

Tested at room temperature $V_{DD33}$ = $V_{DD33A}$ = 3.3V: All I/O ports configured with pull-down inputs, HSI = 25MHz (calibrated), and $F_{HCLK}$ = $F_{V3F}$. Enable or disable all peripheral clocks for power consumption.

The CH32H415 is in the following conditions:
Tested at room temperature $V_{DD33}$ = $V_{DD33A}$ = 3.3V: All I/O ports configured with pull-down inputs, HSI = 25MHz (calibrated), $F_{HCLK}$ = $F_{V3F}$. Enable or disable all peripheral clocks for power consumption.

*Note: The pins that are not encapsulated out of the small package model or the pins that have been encapsulated out but not used, it is recommended to configure them as pull-up inputs or pull-down inputs, or else the current index may be affected, please refer to the EVT low-power routines for specific operations.*

Table 3-6-1 Typical current consumption in run mode with data processing code running from SRAM (RISC-V5F)

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | Clock | $F_{V5F}$ | $F_{HCLK}$ | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$(1) | Supply current in Run mode | Run in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency. | 480MHz | 120MHz | 135.5 | 101.1 | mA |
| | | | 400MHz | 100MHz | 101.6 | 73.6 | |
| | | | 384MHz | 96MHz | 96.6 | 68.7 | |
| | | | 288MHz | 144MHz | 95.4 | 57.4 | |
| | | | 25MHz | 25MHz | 14.0 | 8.3 | |
| | | | 500kHz | 500kHz | 10.0 | 8.2 | |
| | | External clock | 480MHz | 120MHz | 136.7 | 101.9 | |
| | | | 400MHz | 100MHz | 102.2 | 74.2 | |
| | | | 384MHz | 96MHz | 97.4 | 69.6 | |
| | | | 288MHz | 144MHz | 96.0 | 58.0 | |
| | | | 25MHz | 25MHz | 14.7 | 8.9 | |
| | | | 500kHz | 500kHz | 10.7 | 8.8 | |

*Note: The above are measured parameters.*

Table 3-6-2 Typical current consumption in run mode with data processing code running from SRAM (RISC-V3F)

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | Clock | $F_{V3F}$ | $F_{HCLK}$ | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$(1) | Supply current in Run mode | Run in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency. | 144MHz | 144MHz | 77.1 | 33.2 | mA |
| | | | 96MHz | 96MHz | 59.2 | 33.2 | |
| | | | 25MHz | 25MHz | 15.4 | 8.6 | |
| | | | 500kHz | 500kHz | 9.9 | 8.4 | |
| | | External clock | 144MHz | 144MHz | 77.5 | 33.7 | |
| | | | 96MHz | 96MHz | 60.0 | 33.7 | |
| | | | 25MHz | 25MHz | 14.4 | 9.7 | |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| | | | 500kHz | 500kHz | 10.7 | 8.6 | |

*Note: The above are measured parameters.*

Table 3-6-3 Typical current consumption in run mode with data processing code running from SRAM (RISC-V5F + RISC-V3F)

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | Clock | $F_{V5F}$ | $F_{V3F}$ | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$ (1) | Supply current in Run mode | Run in high-speed internal RC oscillator (HSI), HB prescaler is used to reduce the frequency. | 480MHz | 120MHz | 143.4 | 110.8 | mA |
| | | | 400MHz | 100MHz | 115.5 | 87.8 | |
| | | | 384MHz | 96MHz | 106.6 | 78.8 | |
| | | | 288MHz | 144MHz | 124.2 | 86.5 | |
| | | | 25MHz | 25MHz | 16.9 | 10.9 | |
| | | | 500kHz | 500kHz | 10.0 | 8.8 | |
| | | External clock | 480MHz | 120MHz | 144.0 | 111.2 | |
| | | | 400MHz | 100MHz | 115.9 | 88.3 | |
| | | | 384MHz | 96MHz | 107.5 | 79.6 | |
| | | | 288MHz | 144MHz | 125.5 | 87.9 | |
| | | | 25MHz | 25MHz | 17.6 | 11.7 | |
| | | | 500kHz | 500kHz | 10.8 | 9.2 | |

*Note: The above are measured parameters.*

Table 3-7 Typical current consumption in sleep mode with data processing code running from SRAM (RISC-V5F + RISC-V3F)

| Symbol | Parameter | Condition | | | Typ. | | Unit |
|---|---|---|---|---|---|---|---|
| | | Clock | $F_{V5F}$ | $F_{V3F}$ | Enable all peripherals | Disable all peripherals | |
| $I_{DD}$(1) | Supply current in sleep mode (when peripherals are powered and clock is held) | Run on a high-speed internal RC oscillator (HSI) using HB prescaling for frequency reduction | 480MHz | 120MHz | 60.1 | 25.7 | mA |
| | | | 400MHz | 100MHz | 45.7 | 18.2 | |
| | | | 384MHz | 96MHz | 48.0 | 22.2 | |
| | | | 288MHz | 144MHz | 58.8 | 22.8 | |
| | | | 25MHz | 25MHz | 10.6 | 5.2 | |
| | | | 500kHz | 500kHz | 9.9 | 5.2 | |
| | | External clock | 480MHz | 120MHz | 60.8 | 26.4 | |
| | | | 400MHz | 100MHz | 46.3 | 19.0 | |
| | | | 384MHz | 96MHz | 48.8 | 22.8 | |
| | | | 288MHz | 144MHz | 60.1 | 23.5 | |
| | | | 25MHz | 25MHz | 11.4 | 6.0 | |
| | | | 500kHz | 500kHz | 10.6 | 5.9 | |

*Note: The above are measured parameters.*

Table 3-8 Typical current consumption in stop mode (RISC-V5F + RISC-V3F)

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| $I_{DD}$ | Supply current in stop mode | The voltage regulator is in the running mode, and the low-speed and high-speed internal RC oscillators and external oscillators are in the off state (no independent watchdog). | 2.41 | mA |
| | | The voltage regulator is in the low power consumption mode, the low-speed and high-speed internal RC oscillators and external oscillators are in the off state (PVD is off without independent watchdog), and the RAM enters the low power consumption mode. | 1.38 | mA |
| $I_{DD\_VBAT}$ | Supply current for backup area (Remove $V_{DD33}$, $V_{DD33A}$, and $V_{DDIO}$ and use only $V_{BAT}$ supply) | Low-speed external oscillator and RTC are turned on. | 3.5 | uA |

*Note: The above are measured parameters.*

### 3.3.5 External Clock Source Characteristics

Table 3-9 From external high-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSE\_ext}$ | External clock frequency | | 5 | 25 | 32 | MHz |
| $V_{HSEH}$(1) | XI input pin high voltage | | 0.8*$V_{DDIO}$ | | $V_{DDIO}$ | V |
| $V_{HSEL}$(1) | XI input pin low voltage | | 0 | | 0.2*$V_{DDIO}$ | V |
| $C_{in(HSE)}$ | XI input capacitance | | | 5 | | pF |
| $DuCy_{(HSE)}$ | Duty cycle | | | 50 | | % |
| $I_L$ | XI input leakage current | | | | ±1 | uA |

*Note 1: Failure to meet this condition may cause a level recognition error.*

Figure 3-3 High frequency clock circuit for external clock source

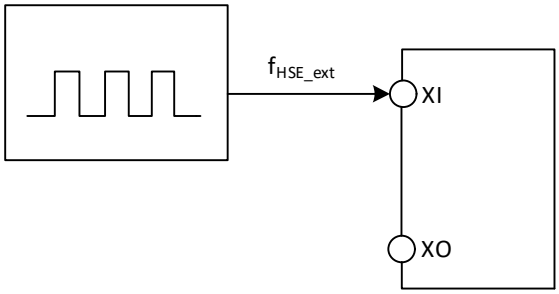


Table 3-10 From external low-speed clock

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSE\_ext}$ | User external clock frequency | | | 32.768 | | kHz |
| $V_{LSEH}$ | OSC32_IN input pin high level voltage | | 0.8*$V_{DD33}$ | | $V_{DD33}$ | V |
| $V_{LSEL}$ | OSC32_IN input pin low voltage | | 0 | | 0.2*$V_{DD33}$ | V |
| $C_{in\ (LSE)}$ | OSC32_IN input capacitance | | | 5 | | pF |
| $DuCy_{LSE}$ | Duty Cycle | | | 50 | | % |
| $I_L$ | OSC32_IN input leakage current | | | | ±1 | uA |

*Note 1: Failure to meet this condition may cause a level recognition error.*

Figure 3-4 Low frequency clock circuit for external clock source

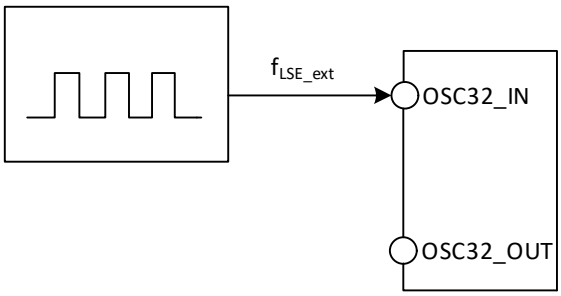



Table 3-11 High-Speed external clocks generated using one crystal/ceramic resonator

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{XI}$ | Resonator frequency | | 5 | 25 | 32 | MHz |
| $R_F$ | Feedback resistance (No need for external) | | | 250 | | kΩ |
| $C_{LOAD}$ | Suggested load capacitance with corresponding crystal serial impedance $R_S$ | $R_S$ = 60Ω(1) | | 20 | | pF |
| $I_{HSE}$ | HSE drive current | 20p load | | 0.8 | | mA |
| $g_m$ | Oscillator transconductance | Startup | | 26 | | mA/V |
| $t_{SU(HSE)}$ | Startup time | $V_{DD33}$ stabilization, 25M crystal | | 1.5(2) | | ms |

*Note: 1. 25M crystal ESR is recommended not to exceed 60Ω, below 25M can be relaxed appropriately.*

*2. Start-up time refers to the time difference from when HSEON is turned on to when HSERDY is set.*

*3. 3. When using Ethernet, the crystal oscillator must be 25MHz.*

Circuit reference design and requirements:

The load capacitance of the crystal is based on the crystal manufacturer's recommendation, usually $C_{L1}$=$C_{L2}$.

Figure 3-5 Typical circuit for external 25M crystal

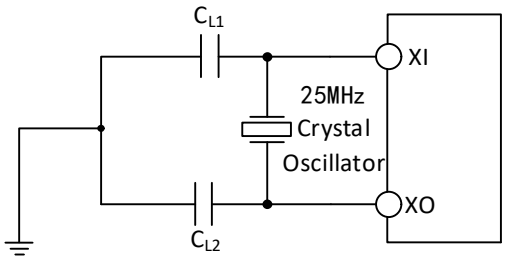


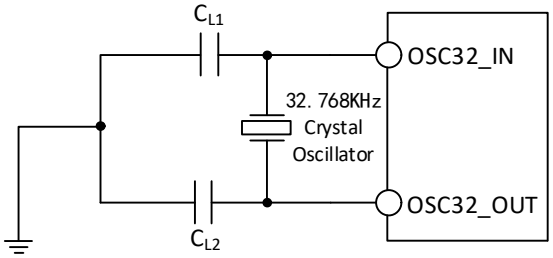

Table 3-12 Low-speed external clocks generated using a crystal/ceramic resonator ($f_{LSE}$=32.768KHz)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSE}$ | Resonator frequency | | | 32.768 | | kHz |
| $R_F$ | Feedback resistance | | | 5 | | MΩ |
| C | Suggested load capacitance with corresponding crystal serial impedance $R_S$ | $R_S$ < 70kΩ | | | 15 | pF |
| $i_2$ | LSE drive current | | | 0.35 | | uA |
| $g_m$ | Oscillator transconductance | Startup | | 30 | | uA/V |
| $t_{SU\ (LSE)}$ | Startup time | $V_{DD33}$ stabilization | | 800 | | mS |

Circuit reference design and requirements:

The load capacitance of the crystal is based on the crystal manufacturer's recommendation, usually $C_{L1}$=$C_{L2}$, optional about 12pF.

Figure 3-6 Typical Circuit for External 32.768K Crystal




*Note: The load capacitance $C_L$ is calculated by the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where $C_{stray}$ is the capacitance of the pins and the capacitance associated with the PCB board or PCB, and its typical value is between 2pF and 7pF.*

### 3.3.6 Internal Clock Source Characteristics

Table 3-13 Internal High-Speed (HSI) RC Oscillator Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{HSI}$ | Frequency (after calibration) | | | 25 | | MHz |
| $DuCy_{HSI}$ | Duty cycle | | 45 | 50 | 55 | % |
| $ACC_{HSI}$ | Accuracy of HSI oscillator (after calibration) | $T_A$ = 0℃~70℃ | -1.6 | | 1.6 | % |
| | | $T_A$ = -40℃~85℃ | -2.2 | | 2.2 | % |
| $t_{SU(HSI)}$ | HSI oscillator startup | | | 10 | | us |

| | | | | | | |
|---|---|---|---|---|---|---|
| | stabilization time | | | | | |

Table 3-14 Internal Low-Speed (LSI) RC Oscillator Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{LSI}$ | Frequency | | 25 | 40 | 60 | kHz |
| $DuCy_{LSI}$ | Duty Cycle | | 45 | 50 | 55 | % |
| $t_{SU(LSI)}$(1) | LSI oscillator startup stabilization time | | | 230 | | us |
| $I_{DD(LSI)}$ | LSI oscillator power consumption | | | 0.6 | | uA |

*Note: 1. Register RCC_CTLR LSION is set to 1. Wait for LSIRDY to be set to 1.*

### 3.3.7 PLL Characteristics

Table 3-15 PLL Characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{PLL\_IN}$ | PLL input clock | | 5 | 25 | 32 | MHz |
| | PLL input clock duty cycle | | 40 | | 60 | % |
| $F_{PLL\_OUT}$ | PLL multiplier output clock | | 100 | | 600 | MHz |
| $t_{LOCK}$ | PLL lock time | | | 40 | 90 | us |

### 3.3.8 Wakeup Time from Low-power Mode

Table 3-16 Wakeup time from low-power mode

| Symbol | Parameter | Condition | Typ. | Unit |
|---|---|---|---|---|
| $t_{wusleep}$ | Wakeup from Sleep mode | Use HSI RC clock wakeup | 0.3 | us |
| $t_{wustop}$ | Wakeup from Stop mode (Regulator in ON mode) | HSI RC clock wakeup | 4 | us |
| | Wakeup from Standby mode (Regulator in low-power mode) | Regulator wake-up time from low-power mode + HSI RC clock wake-up | 35 | us |

*Note: The above are measured parameters.*

### 3.3.9 Memory Characteristics

Table 3-17 Flash memory characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{prog\_page}$ | Page (256 bytes) programming time | | | 1.5 | 3 | ms |
| $t_{erase\_sec}$ | Sector erase time | DBMODE = 0, single 4K bytes | | 3 | 10 | ms |
| | | DBMODE = 1, single 8K bytes | | | | |
| $t_{erase\_32k}$ | Block erase time | DBMODE = 0, single 32K bytes | | 3 | 10 | ms |
| | | DBMODE = 1, single 64K bytes | | | | |

Table 3-18 Flash memory endurance and data retention

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $N_{END}$ | Endurance | $T_A$ = 25℃ | 50K | | | Times |
| $t_{RET}$ | Data retention period | | 20 | | | Years |

### 3.3.10 I/O Port Characteristics

Table 3-19 General-purpose I/O static characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Standard I/O pin, input high voltage | V*_IO_HSLV = 0 | 0.45*V*+0.41 | | V*+0.3 | V |
| | | V*_IO_HSLV = 0, and V* = 3.3V | 1.9 | | 3.6 | V |
| | | V*_IO_HSLV = 1, exclude PC13~PC15 | 0.7*V* | | V*+0.3 | V |
| | FT I/O pin, input high voltage | V*_IO_HSLV = 0 | 0.45*V*+0.41 | | 5.5 | V |
| | | V*_IO_HSLV = 0, And V* = 3.3V | 1.9 | | 5.5 | V |
| | | V*_IO_HSLV = 1 | 0.7*V* | | 5.5 | V |
| $V_{IL}$ | Standard I/O pin, input low level voltage | V*_IO_HSLV = 0 | -0.3 | | 0.29*V*-0.07 | V |
| | | V*_IO_HSLV = 0, and V* = 3.3V | -0.3 | | 0.9 | V |
| | | V*_IO_HSLV = 1, exclude PC13~PC15 | -0.3 | | 0.3*V* | V |
| | FT I/O pin, input low level voltage | V*_IO_HSLV = 0 | -0.3 | | 0.29*V*-0.07 | V |
| | | V*_IO_HSLV = 0, and V* = 3.3V | -0.3 | | 0.9 | V |
| | | V*_IO_HSLV = 1 | -0.3 | | 0.3*V* | V |
| $V_{hys}$ | Standard I/O pin Schmitt trigger voltage hysteresis | | | 240 | | mV |
| | FT I/O Schmitt trigger voltage hysteresis | | | 220 | | mV |
| $I_{lkg}$ | Input leakage current | Standard I/O port | | | 1 | uA |
| | | FT I/O port | | | 3 | uA |
| $R_{PU}$ | Pull up equivalent resistance | | 30 | 40 | 55 | kΩ |
| $R_{PD}$ | Pull down equivalent resistance | | 30 | 40 | 55 | kΩ |
| $C_{IO}$ | I/O pin capacitance | | | 5 | | pF |

*Note: For the CH32H417 chip, the I/O pins are powered by $V_{DDIO}$, $V_{IO18}$, $V_{DD33}$, or $V_{BAT}$; V* in the above table can be denoted as $V_{DDIO}$, $V_{IO18}$, $V_{DD33}$, or $V_{BAT}$ according to the specific pin; the bit V*_IO_HSLV in the above table can be denoted as VDD33_IO_HSLV, VDDO_ IO_HSLV or VIO18_IO_HSLV.*

Output Drive Current Characteristics

The GPIOs (General-purpose Input/Output Ports) can absorb or output up to ±8mA of current and absorb or output ±20mA of current (not strictly up to $V_{OL}/V_{OH}$). In user applications, the total current driven by all IO pins must not exceed the absolute maximum ratings given in section 3.2:

Table 3-20-1 Output voltage characteristics (excluding FT I/O pin and PC13~PC15 pin)

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level, 8 pins sink current | $I_{IO}$ = 8mA<br>2.7V≤V*≤3.6V,V*_IO_HSLV=0<br>1.6V≤V*≤2.7V,V*_IO_HSLV=1 | | 0.25 | V |
| $V_{OH}$ | Output high level, 8 pins output current. | | V*-0.25 | | |
| $V_{OL}$ | Output low level, 8 pins sink current | $I_{IO}$ = 20mA<br>2.7V≤V*≤3.6V,V*_IO_HSLV=0 | | 0.6 | V |
| $V_{OH}$ | Output high level, 8 pins output current. | | V*-0.6 | | |
| $V_{OL}$ | Output low level, 8 pins sink current | $I_{IO}$ = 8mA<br>1.6V≤V*≤2.7V,V*_IO_HSLV=0 | | 0.4 | V |
| $V_{OH}$ | Output high level, 8 pins output current. | | V*-0.4 | | |

*Note: 1. If multiple I/O pins are driven at the same time in the above conditions, the sum of the currents must not exceed the absolute maximum ratings given in section 3.2 of the table. In addition, when multiple I/O pins are driven at the same time, the current at the power/ground point is high, which can lead to a voltage drop so that the voltage of the internal I/O does not reach the power supply voltage in the table, thus causing the drive current to be less than the nominal value.*

*2. V* in the above table can be expressed as $V_{DDIO}$, $V_{IO18}$ or $V_{DD33}$ according to specific pins; bit V*_IO_HSLV in the above table can be expressed as VDD33_IO_HSLV, VDDIO_IO_HSLV or VIO18_IO_HSLV according to specific pins.*

Table 3-20-2 Output voltage characteristics (for FT I/O pins)

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level, 8 pins sink current | $I_{IO}$ = 8mA<br>2.7V≤V*≤3.6V, V*_IO_HSLV = 0<br>1.6V≤V*≤2.7V, V*_IO_HSLV = 1 | | 0.4 | V |
| $V_{OH}$ | Output high level, 8 pins output current | | V*-0.4 | | |
| $V_{OL}$ | Output low level, 8 pins sink current | $I_{IO}$ = 20mA,<br>2.7V≤V*≤3.6V, V*_IO_HSLV = 0 | | 1.0 | V |
| $V_{OH}$ | Output high level, 8 pins output current | | V*-1.0 | | |
| $V_{OL}$ | Output low level, 8 pins sink current | $I_{IO}$ = 5mA,<br>1.6V≤V*≤2.7V, V*_IO_HSLV = 0 | | 0.4 | V |
| $V_{OH}$ | Output high level, 8 pins output current | | V*-0.4 | | |

*Note: 1. V* in the above table can be expressed as $V_{DDIO}$, $V_{IO18}$ or $V_{DD33}$ according to specific pins; bit V*_IO_HSLV in the above table can be expressed as VDD33_IO_HSLV, VDDIO_IO_HSLV or VIO18_IO_HSLV according to specific pins.*

Table 3-20-3 Output voltage characteristics (for PC13~PC15 pins)

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{OL}$ | Output low level, 3 pins sink current | $I_{IO}$ = 8mA<br>2.7V≤ $V_{DD33}/V_{BAT}$ ≤3.6V | | 0.25 | V |
| $V_{OH}$ | Output high level, 3 pins output current | $I_{IO}$ = 3mA<br>2.7V≤ $V_{DD33}/V_{BAT}$ ≤3.6V | $V_{DD33/BAT}$-0.4 | | |
| $V_{OL}$ | Output low level, 3 pins sink current | $I_{IO}$ = 4mA<br>1.8V≤ $V_{DD33}/V_{BAT}$ ≤3.6V | | 0.25 | V |
| $V_{OH}$ | Output high level, 3 pins output current | $I_{IO}$ = 1.5mA<br>1.8V≤ $V_{DD33}/V_{BAT}$ ≤3.6V | $V_{DD33/BAT}$-0.4 | | |

*Note: For the CH32H417 chip, pins PC13 to PC15 are powered by $V_{DD33}$ or $V_{BAT}$ depending on the situation.*

Table 3-21-1 Input-output AC characteristics (VDD33/VDDIO/VIO18_IO_HSLV = 0, exclude FT I/O pin and PC13~PC15 pin)

| MODEy[1:0] Configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 00 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V∗ = 2.7-3.6V | | 40 | MHz |
| | | | CL=50pF, V∗ = 1.6-2.7V | | 18 | MHz |
| | | | CL=30pF, V∗ = 2.7-3.6V | | 50 | MHz |
| | | | CL=30pF, V∗ = 1.6-2.7V | | 22 | MHz |
| | | | CL=10pF, V∗ = 2.7-3.6V | | 70 | MHz |
| | | | CL=10pF, V∗ = 1.6-2.7V | | 28 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V∗ = 2.7-3.6V | | 8 | ns |
| | | | CL=50pF, V∗ = 1.6-2.7V | | 15 | ns |
| | | | CL=30pF, V∗ = 2.7-3.6V | | 6 | ns |
| | | | CL=30pF, V∗ = 1.6-2.7V | | 12 | ns |
| | | | CL=10pF, V∗ = 2.7-3.6V | | 4 | ns |
| | | | CL=10pF, V∗ = 1.6-2.7V | | 8 | ns |
| 01 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V∗ = 2.7-3.6V | | 75 | MHz |
| | | | CL=50pF, V∗ = 1.6-2.7V | | 35 | MHz |
| | | | CL=30pF, V∗ = 2.7-3.6V | | 100 | MHz |
| | | | CL=30pF, V∗ = 1.6-2.7V | | 40 | MHz |
| | | | CL=10pF, V∗ = 2.7-3.6V | | 180 | MHz |
| | | | CL=10pF, V∗ = 1.6-2.7V | | 50 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V∗ = 2.7-3.6V | | 4.4 | ns |
| | | | CL=50pF, V∗ = 1.6-2.7V | | 8.5 | ns |
| | | | CL=30pF, V∗ = 2.7-3.6V | | 3.2 | ns |
| | | | CL=30pF, V∗ = 1.6-2.7V | | 6 | ns |
| | | | CL=10pF, V∗ = 2.7-3.6V | | 1.7 | ns |
| | | | CL=10pF, V∗ = 1.6-2.7V | | 3.5 | ns |
| 10 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V∗ = 2.7-3.6V | | 75 | MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | CL=50pF, V* = 1.6-2.7V | | 40 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 110 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 50 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 200 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 65 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 4.3 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 8.2 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 3 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 5.6 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 1.5 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 3 | ns |
| 11 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 75 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 40 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 120 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 55 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 200 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 70 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 4.2 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 8 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 2.8 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 5.4 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 1.5 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 2.8 | ns |

*Note: 1. All of the above are guaranteed as design parameters.*

*2. In the above table, V* can be expressed as $V_{DDIO}$, $V_{IO18}$ or $V_{DD33}$ depending on the specific pin.*

Table 3-21-2 Input-output AC characteristics (VDD33/VDDIO/VIO18_IO_HSLV = 1, exclude FT I/O pin and PC13~PC15 pin)

| MODEx[1:0] Configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 00 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 75 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 35 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 95 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 45 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 130 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 55 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 4.3 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 8.3 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 3.3 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 6.4 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 2.2 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 4.2 | ns |
| 01 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 110 | MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | CL=50pF, V* = 1.6-2.7V | | 60 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 175 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 90 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 230 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 140 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 2.8 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 5.3 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 1.8 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 3.6 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 0.9 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 1.9 | ns |
| 10 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 120 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 64 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 170 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 95 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 240 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 160 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 2.7 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 5.2 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 1.7 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 3.4 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 0.8 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 1.7 | ns |
| 11 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 120 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 65 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 170 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 100 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 250 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 180 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 2.7 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 5.1 | ns |
| | | | CL=30pF V* = 2.7-3.6V | | 1.7 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 3.4 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 0.8 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 1.6 | ns |

*Note: 1. All of the above are guaranteed as design parameters.*

*2. In the above table, V* can be expressed as $V_{DDIO}$, $V_{IO18}$ or $V_{DD33}$ depending on the specific pin.*

Table 3-21-3 Input-output AC characteristics (VDD33/VDDIO/VIO18_IO_HSLV = 0, for FT I/O pin)

| MODEx[1:0] Configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 00 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 30 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 14 | MHz |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | CL=30pF, V* = 2.7-3.6V | | 35 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 20 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 43 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 23 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 10 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 22 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 7.6 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 14 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 5 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 9 | ns |
| 01 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 32 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 16 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 45 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 25 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 90 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 50 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 8 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 15 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 5.5 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 10.5 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 3 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 5.5 | ns |
| 10 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 35 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 18 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 50 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 28 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 100 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 55 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 8 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 15 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 5.5 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 11 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 3 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 5.5 | ns |
| 11 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 37 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 20 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 55 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 30 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 110 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 60 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high | CL=50pF, V* = 2.7-3.6V | | 8 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 15 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 5.5 | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | to low level | CL=30pF, V* = 1.6-2.7V | | 10 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 2.5 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 5.5 | ns |

*Note: 1. All of the above are guaranteed as design parameters.*

*2. In the above table, V* can be expressed as $V_{DDIO}$, $V_{IO18}$ or $V_{DD33}$ depending on the specific pin.*

Table 3-21-4 Input-output AC characteristics (VDD33/VDDIO/VIO18_IO_HSLV = 1, for FT I/O pin)

| MODEx[1:0] Configuration | Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| 00 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 45 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 25 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 50 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 35 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 55 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 42 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 6.5 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 12 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 4.6 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 8.6 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 3 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 5.3 | ns |
| 01 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 50 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 25 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 75 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 36 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 130 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 70 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 5.5 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 10.5 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 3.7 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 7.2 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 2 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 3.8 | ns |
| 10 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 55 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 28 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 80 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 40 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 135 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 75 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 5.5 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 10.5 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 3.7 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 7.1 | ns |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | | CL=10pF, V* = 2.7-3.6V | | 2 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 3.8 | ns |
| 11 | $F_{max(IO)out}$ | Maximum frequency | CL=50pF, V* = 2.7-3.6V | | 60 | MHz |
| | | | CL=50pF, V* = 1.6-2.7V | | 30 | MHz |
| | | | CL=30pF, V* = 2.7-3.6V | | 85 | MHz |
| | | | CL=30pF, V* = 1.6-2.7V | | 45 | MHz |
| | | | CL=10pF, V* = 2.7-3.6V | | 140 | MHz |
| | | | CL=10pF, V* = 1.6-2.7V | | 80 | MHz |
| | $t_r/t_{f(IO)out}$ | Output the rising time from low to high level, the falling time from high to low level | CL=50pF, V* = 2.7-3.6V | | 5.5 | ns |
| | | | CL=50pF, V* = 1.6-2.7V | | 10.5 | ns |
| | | | CL=30pF, V* = 2.7-3.6V | | 3.7 | ns |
| | | | CL=30pF, V* = 1.6-2.7V | | 7.1 | ns |
| | | | CL=10pF, V* = 2.7-3.6V | | 2 | ns |
| | | | CL=10pF, V* = 1.6-2.7V | | 3.8 | ns |

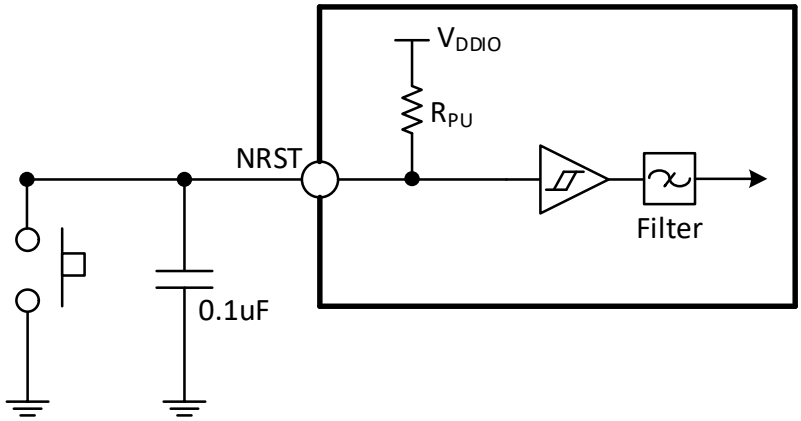
*Note: 1. All of the above are guaranteed as design parameters.*

*2. In the above table, V* can be expressed as $V_{DDIO}$, $V_{IO18}$ or $V_{DD33}$ depending on the specific pin.*

### 3.3.11 NRST Pin Characteristics

Circuit reference design and requirements:

Figure 3-7 Typical circuit of external reset pin




*Note: The capacitors shown are optional and can be used to filter out key jitter.*

Table 3-22 External reset pin characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL(NRST)}$ | NRST input low voltage | | -0.3 | | $0.29*V_{DDIO}$-0.07 | V |
| $V_{IH(NRST)}$ | NRST input high voltage | | $0.45*V_{DDIO}$+0.41 | | $V_{DDIO}$+0.3 | V |
| $V_{hys(NRST)}$ | NRST Schmitt trigger voltage hysteresis | | 150 | | | mV |
| $R_{PU}$(1) | Pull-up equivalent resistance | | 30 | 40 | 55 | kΩ |
| $V_{F(NRST)}$ | NRST input can be filtered for pulse width | | | | 100 | ns |
| $V_{NF(NRST)}$ | NRST input cannot be filtered pulse width | | 300 | | | ns |

*Note: The pull-up resistor is a real resistor in series with a switchable PMOS implementation. The resistance of this PMOS/NMOS switch is very small (about 10%).*

### 3.3.12 TIM Characteristics

Table 3-23-1 TIM1/8/2/3/4/5/6/7 and LPTIM1/2 characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer reference clock | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 150MHz | 6.7 | | ns |
| $F_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}$/2 | MHz |
| | | $f_{TIMxCLK}$ = 150MHz | 0 | 75 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 16 | Bit |
| $t_{COUNTER}$ | 16-bit counter clock cycle when the internal clock is selected | | 1 | 65536 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 150MHz | 0.0067 | 437 | us |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | 65535 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 150MHz | | 28.6 | s |

Table 3-23-2 TIM9/10/11/12 characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{res(TIM)}$ | Timer reference clock | | 1 | | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 150MHz | 6.7 | | ns |
| $F_{EXT}$ | Timer external clock frequency on CH1 to CH4 | | 0 | $f_{TIMxCLK}$/2 | MHz |
| | | $f_{TIMxCLK}$ = 150MHz | 0 | 75 | MHz |
| $R_{esTIM}$ | Timer resolution | | | 32 | Bit |
| $t_{COUNTER}$ | 32-bit counter clock cycle when the internal clock is selected | | 1 | $2^{32}$ | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 150MHz | 0.0067 | $2^{32}$/150 | us |
| $t_{MAX\_COUNT}$ | Maximum possible count | | | $2^{32}$-1 | $t_{TIMxCLK}$ |
| | | $f_{TIMxCLK}$ = 150MHz | | $(2^{32}-1)*2^{32}/150$ | us |

### 3.3.13 I2C Interface Characteristics

Figure 3-8 I2C bus timing diagram

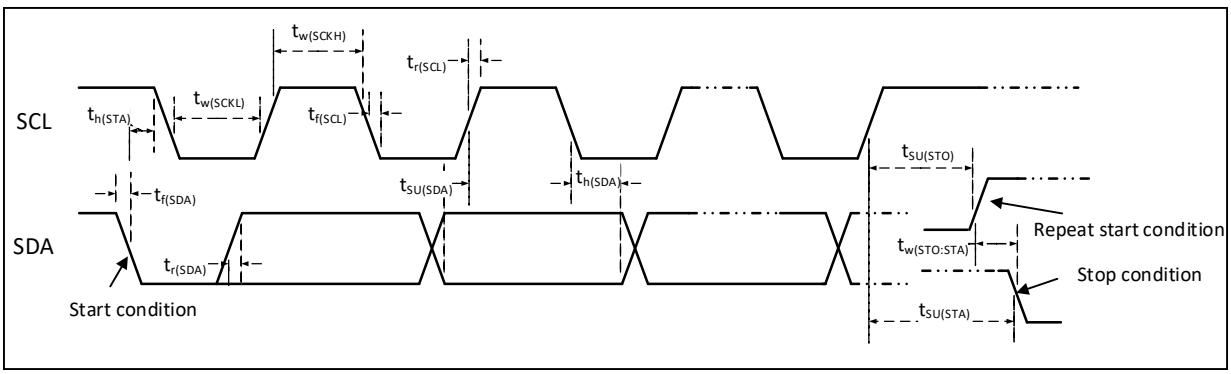


Table 3-24 I2C interface characteristics

| Symbol | Parameter | Standard I2C | | Fast I2C | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{w(SCKL)}$ | SCL clock low level time | 4.7 | | 1.2 | | us |
| $t_{w(SCKH)}$ | SCL clock high level time | 4.0 | | 0.6 | | us |
| $t_{SU(SDA)}$ | SDA data setup time | 250 | | 100 | | ns |
| $t_{h(SDA)}$ | SDA data hold time | 0 | | 0 | 900 | ns |
| $t_{r(SDA)}/t_{r(SCL)}$ | SDA and SCL rise time | | 1000 | 20 | | ns |
| $t_{f(SDA)}/t_{f(SCL)}$ | SDA and SCL fall time | | 300 | | | ns |
| $t_{h(STA)}$ | Start condition hold time | 4.0 | | 0.6 | | us |
| $t_{SU(STA)}$ | Repeated start condition setup time | 4.7 | | 0.6 | | us |
| $t_{SU(STO)}$ | Stop condition setup time | 4.0 | | 0.6 | | us |
| $t_{w(STO:STA)}$ | Time from stop condition to start condition (bus free) | 4.7 | | 1.2 | | us |
| $C_b$ | Capacitive load for each bus | | 400, | | 400 | pF |

### 3.3.14 I3C Interface Characteristics

Table 3-25 I3C interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $t_{r(SDA)\_OD}$(1) | SDA rise time in open-drain mode | $1.71<V_{IO18}<3.6V$ | 100 | | ns |
| $t_{r(SDA)\_PP}$(1) | SDA rise time in push-pull mode | $1.71<V_{IO18}<3.6V$ | 5.1 | | ns |

*Note: 1. $t_{r(SDA)\_OD}$ and $t_{r(SDA)\_PP}$ are guaranteed as design parameters and can be configured through register R32_I3C_TIMINGR0. Other timing parameters can be referred to the MIPI protocol.*

### 3.3.15 SPI Interface Characteristics

Figure 3-9 SPI timing diagram in Master mode

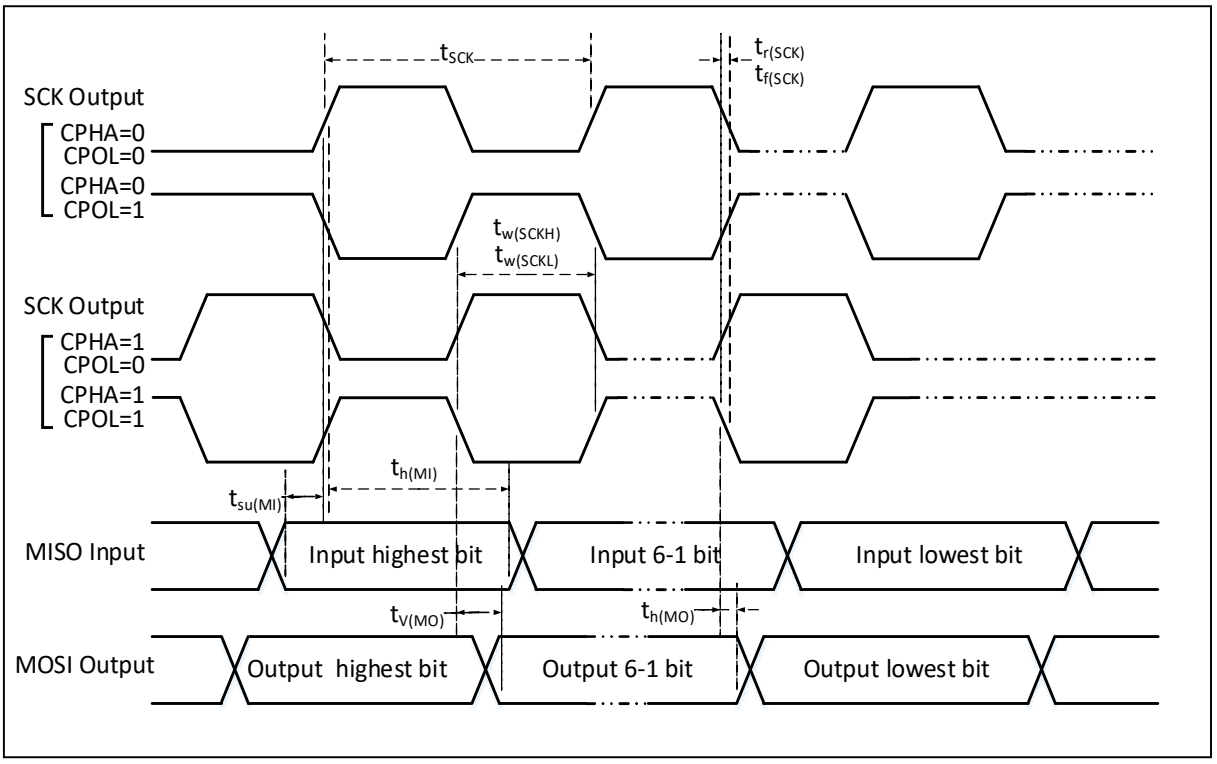



Figure 3-10 SPI timing diagram in Slave mode (CPHA=0)

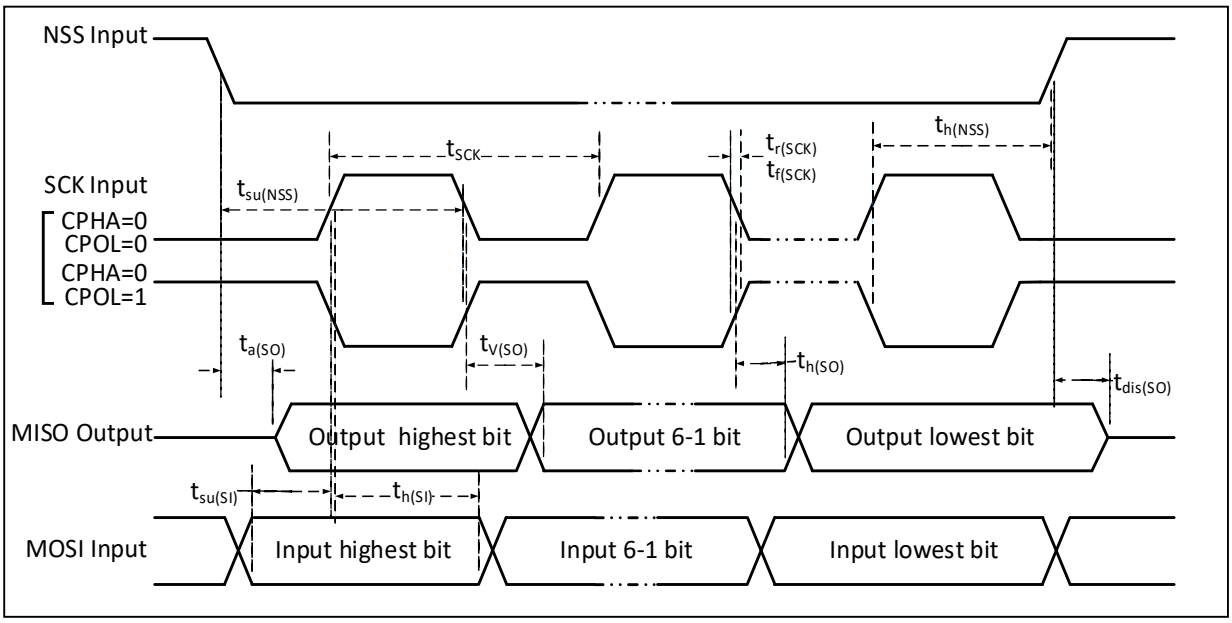


Figure 3-11 SPI timing diagram in Slave mode (CPHA=1)

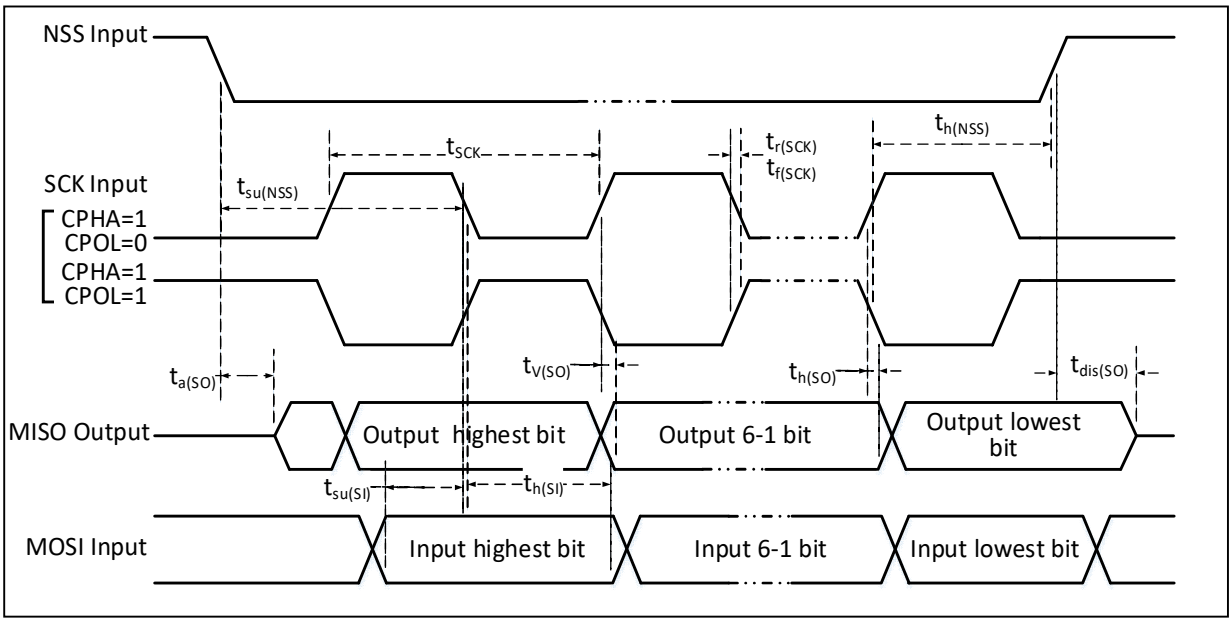



Table 3-26 SPI interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}/t_{SCK}$ | SPI clock frequency | Master mode | | 75 | MHz |
| | | Slave mode | | 75 | MHz |
| $t_{r(SCK)}/t_{f(SCK)}$ | SPI clock rise and fall time | Load capacitance: C = 30pF | | 20 | ns |
| $t_{SU(NSS)}$ | NSS setup time | Slave mode | $2*t_{HCLK}$ | | ns |
| $t_{h(NSS)}$ | NSS hold time | Slave mode | $2*t_{HCLK}$ | | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high-level and low-level time | Master mode, $f_{HCLK}$ = 36MHz, prescaler factor =4 | 40 | 60 | ns |
| $T_{su(MI)}$ | Data input setup time | Master mode | 5 | | ns |
| $t_{su(SI)}$ | | Slave mode | 5 | | ns |
| $t_{h(MI)}$ | Data input hold time | Master mode | 5 | | ns |
| $t_{h(SI)}$ | | Slave mode | 4 | | ns |
| $t_{a(SO)}$ | Data output access time | Slave mode, $f_{HCLK}$ = 20MHz | 0 | $1*t_{HCLK}$ | ns |
| $t_{dis(SO)}$ | Data output disable time | Slave mode | 0 | 10 | ns |
| $t_{V(SO)}$ | Data output valid time | Slave mode (After enabling edge) | | 25 | ns |
| $t_{V(MO)}$ | | Master mode (After enabling edge) | | 5 | ns |
| $t_{h(SO)}$ | Data output hold time | Slave mode (After enabling edge) | 15 | | ns |
| $t_{h(MO)}$ | | Master mode (After enabling edge) | 0 | | ns |

## 3.3.16 QSPI Interface Characteristics

Table 3-27 QSPI interface I/O characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{SCK}/t_{SCK}$ | QSPI clock frequency | | | 75 | MHz |

| | | | | | |
|---|---|---|---|---|---|
| $t_{r(SCK)}/t_{f(SCK)}$ | QSPI clock rise and fall time | Load capacitance: C = 30pF | | 20 | ns |
| $t_{w(SCKH)}/t_{w(SCKL)}$ | SCK high-level and low-level time | $f_{HCLK}$ = 36MHz, prescaler factor = 4 | 40 | 60 | ns |
| $t_{SU(SIO*)}$ | Data input setup time | | 5 | | ns |
| $t_{h(SIO*)}$ | Data input hold time | | 5 | | ns |
| $t_{V(SIO*)}$ | Data output valid time | | | 5 | ns |
| $t_{h(SIO*)}$ | Data output hold time | | 0 | | ns |

### 3.3.17 I2S Interface Characteristics

Figure 3-12 I2S Bus master mode timing diagram

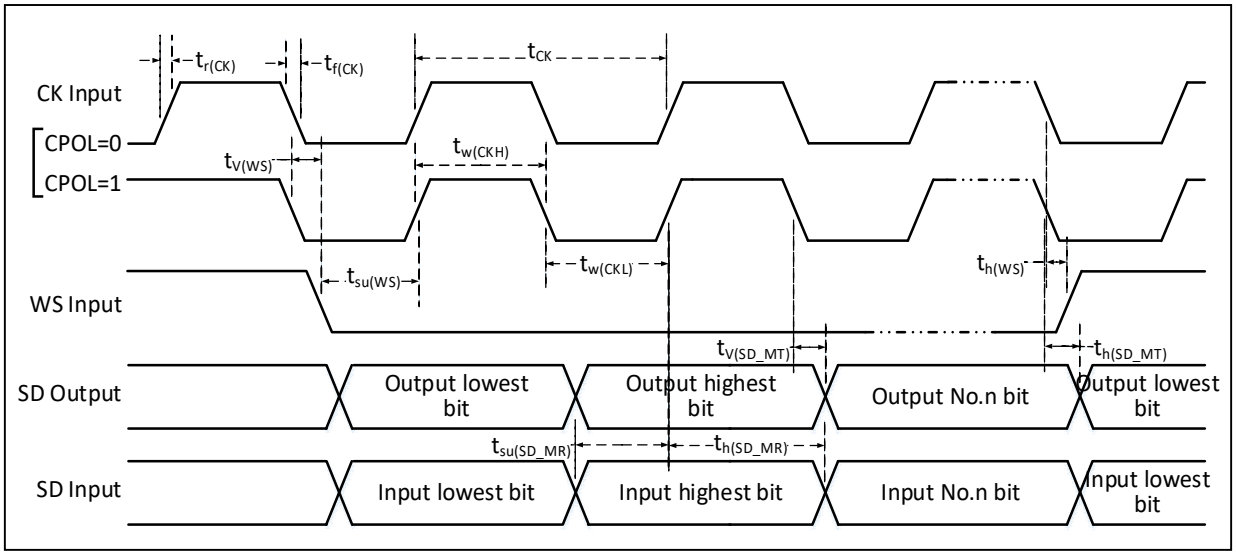



Figure 3-13 I2S Bus slave mode timing diagram

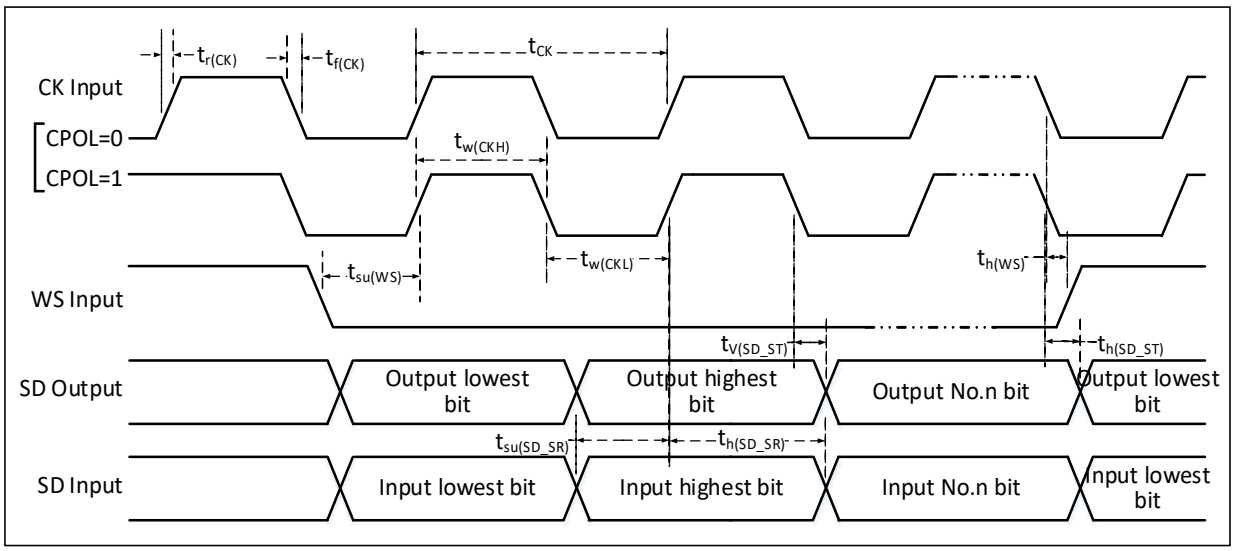



Table 3-28 I2S interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|

| | | | | | |
|---|---|---|---|---|---|
| $f_{CK}/t_{CK}$ | I2S clock frequency | Master mode | | 8 | MHz |
| | | Slave mode | | 8 | MHz |
| $t_{r(CK)}/t_{f(CK)}$ | I2S clock rise and fall time | Load capacitance: C = 30pF | | 20 | ns |
| $t_{V(WS)}$ | WS valid time | Master mode | | 5 | ns |
| $t_{SU(WS)}$ | WS setup time | Slave mode | 10 | | ns |
| $t_{h(WS)}$ | WS hold time | Master mode | 0 | | ns |
| | | Slave mode | 0 | | ns |
| $t_{w(CKH)}/t_{w(CKL)}$ | SCK high level and low level time | Master mode, $f_{HCLK}$ = 36MHz prescaler factor = 4 | 40 | 60 | % |
| $t_{SU(SD\_MR)}$ $t_{SU(SD\_SR)}$ | Data input setup time | Master mode | 8 | | ns |
| | | Slave mode | 8 | | ns |
| $t_{h(SD\_MR)}$ $t_{h(SD\_SR)}$ | Data input hold time | Master mode | 5 | | ns |
| | | Slave mode | 4 | | ns |
| $t_{h(SD\_MT)}$ | Data output hold time | Slave mode (After enabling edge) | | 5 | ns |
| $t_{h(SD\_ST)}$ | | Master mode (After enabling edge) | | 5 | ns |
| $t_{V(SD\_MT)}$ | Data output valid time | Slave mode (After enabling edge) | | 5 | ns |
| $t_{v(SD\_ST)}$ | | Master mode (After enabling edge) | | 4 | ns |

### 3.3.18 USB PD Interface Characteristics

Table 3-29-1 PD interface I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{Rise}$ | Rising time | The amplitude is between 10% and 90%, and the minimum value is the time under no-load condition. | 300 | 430 | | ns |
| $t_{Fall}$ | Falling time | The amplitude is between 10% and 90%, and the minimum value is the time under no-load condition. | 300 | 430 | | ns |
| $V_{Swing}$ | Output voltage swing (peak-to-peak) | | 1.04 | 1.12 | 1.20 | V |

Table 3-29-2 Type-C I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIL}$(1) | CC pin input low level voltage | USBPD_CC_HVT=0, FT I/O input | 0 | | 0.8 | V |
| | | USBPD_CC_HVT=1, high threshold detection input | 0 | | 2.0 | |
| $V_{CCIH}$(1) | CC pin input high voltage | USBPD_CC_HVT=0, FT I/O input | 2.0 | | $V_*$(2) | V |
| | | USBPD_CC_HVT=1, high threshold detection input | 2.45 | | $V_*$(2) | |
| $V_{CChys}$ | Hysteresis voltage | USBPD_CC_HVT=0, FT I/O input | 90 | | | mV |
| | | USBPD_CC_HVT=1, high threshold | | 120 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | | detection input | | | | |
| $I_{pu}$ | Pull-up current | Pin < V*(2)-0.6V | | 80 | | uA |
| | | | | 180 | | uA |
| | | | | 330 | | uA |
| Rd | Built-in Rd pull-down resistor on CC pin (for CC1R/CC2R) | $V_{IO33}$ ≥ 1.6V or external pull-up 330uA | | 5.1 | | kΩ |

*Note: 1. $V_{CCIL}$ and $V_{CCIH}$ corresponding to USBPD_CC_HVT =1 are guaranteed as design parameters.*

*2. For CH32H417 chips, V* is $V_{DDIO}$; for CH32H416 and CH32H415 chips, V* is $V_{DD33}$.*

### 3.3.19 USB 2.0 Interface Characteristics

Table 3-30 USB 2.0 interface I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33}$ | USB 2.0 operating voltage | | 3.2 | | 3.45 | V |
| $V_{SE}$ | Single ended receiver threshold | $V_{DD33}$ = 3.3V | 1.2 | | 1.9 | V |
| $V_{OL}$ | Static output low level | | | | 0.3 | V |
| $V_{OH}$ | Static output high level | | 2.8 | | 3.6 | V |
| $V_{HSOI}$ | High-speed idle level | | -10 | | 10 | mV |
| $V_{HSOH}$ | High-speed data high level | | 360 | | 440 | mV |
| $V_{HSOL}$ | High-speed data low level | | -10 | | 10 | mV |
| $R_{USBPU}$ | USB pin pull-up resistor | | 1.3 | 1.5 | 1.8 | kΩ |
| $R_{USBPD}$ | USB pin pull-down resistor | | 13 | 15 | 18 | kΩ |
| $V_{BC\_REF}$ | BC CMP reference voltage | | | 0.4 | | V |
| $V_{BC\_SRC}$ | BC protocol output voltage | | | 0.6 | | V |

### 3.3.20 USB 3.2 Gen1 Interface Characteristics

The CH32H417 complies with the features of the USB 3.2 Gen1 specification, for more information please refer to the relevant protocol specification.

### 3.3.21 SerDes Interface Characteristics

Table 3-31 SerDes interface I/O characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33}$ | SerDes operating voltage | | 3.2 | | 3.45 | V |
| $T_{SERDRAT}$ | Transmission data rate | Category 6 differential Ethernet cable, 5 m | 0.5 | | 1.5 | Gb/s |
| | | Category 6 differential Ethernet cable, 100 m | | 0.5 | | |
| $V_{TX-DIFF-PP}$ | Differential transmission peak-to-peak voltage amplitude | TX_OUTPUT_SWING[1:0] = 00 | 1.35 | 1.5 | 1.65 | V |
| | | TX_OUTPUT_SWING[1:0] = 01 | 1.62 | 1.8 | 1.98 | |
| | | TX_OUTPUT_SWING[1:0] = 10 | 1.89 | 2.1 | 2.31 | |
| | | TX_OUTPUT_SWING[1:0] = 11 | 2.16 | 2.4 | 2.64 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{TX-DE}$ | Pre-emphasis amplitude | TX_DE_EMPHASIS[1:0] = 00 | | 0 | | dB |
| | | TX_DE_EMPHASIS[1:0] = 01 | | 3 | | |
| | | TX_DE_EMPHASIS[1:0] = 10 | | 6 | | |
| | | TX_DE_EMPHASIS[1:0] = 11 | | 9 | | |
| $R_{TX}$ | Differential output impedance | | | 100 | | Ω |
| $V_{RX-DIFF-PP}$ | Differential reception peak-to-peak voltage amplitude | | 0.15 | 0.3 | | V |
| $R_{RX}$ | Differential input impedance | | | 100 | | Ω |
| $V_{RX-VCM}$ | Receiving common-mode voltage | | | 0.5* $V_{DD33}$ | | V |
| $C_{AC-COUPLING}$ | AC coupling capacitance | | 75 | 100 | 200 | nF |

*Note: 1. The data transmission rate is dependent on both the cable and analog parameters. Analog parameters can be configured via register R32_SYS_CFGR. For detailed information, refer to the CH32H417RM manual and the EVT example program on the official website.*

*2. For the maximum data transmission rate, it is recommended to reserve an appropriate margin based on actual measured values.*

### 3.3.22 SDIO Interface Characteristics

Table 3-32 SDIO interface I/O characteristics

| Symbol | Parameter | Condition | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{CK}/t_{CK}$ | Clock frequency in data transmission mode | CL≤30pF | | | 100 | MHz |
| $t_{W(CKL)}$ | Clock low level time | CL≤30pF | | 3 | | ns |
| $t_{W(CKH)}$ | Clock high level time | CL≤30pF | | 3 | | |
| $t_{r(CK)}$ | Rising time | CL≤30pF | | | 2 | |
| $t_{f(CK)}$ | Falling time | CL≤30pF | | | 2 | |
| CMD/DAT input (Refer to CK) | | | | | | |
| $t_{ISU}$ | Input setup time | CL≤30pF | | 5 | | ns |
| $t_{IH}$ | Input holding time | CL≤30pF | | 1 | | |
| In high-speed mode, CMD/DAT output (refer to CK) | | | | | | |
| $t_{OV}$ | Output valid time | CL≤30pF | Master mode | | 3 | ns |
| | | | Slave mode | | 9 | |
| $t_{OH}$ | Output holding time | CL≤30pF | | 10 | | |
| In default mode, CMD/DAT output (refer to CK) | | | | | | |
| $t_{OVD}$ | Output valid default time | CL≤30pF | Master mode | | 4 | ns |
| | | | Slave mode | | 10 | |
| $t_{OHD}$ | Output holding default time | CL≤30pF | | 10 | | |

### 3.3.23 SDMMC Interface Characteristics

Figure 3-14 SD high-speed mode timing diagram

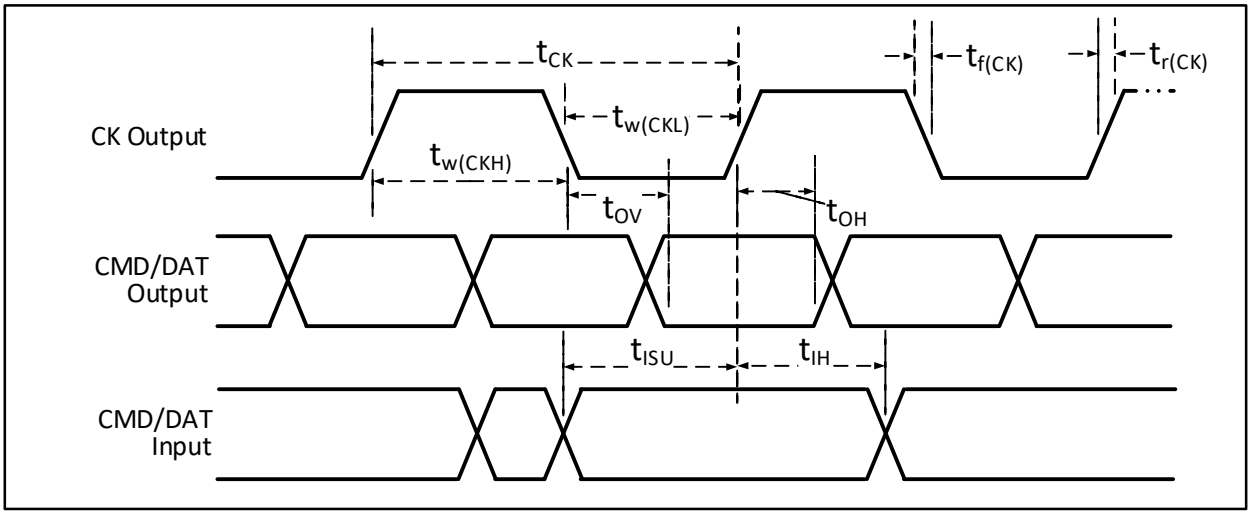



Figure 3-15 SD default mode timing diagram

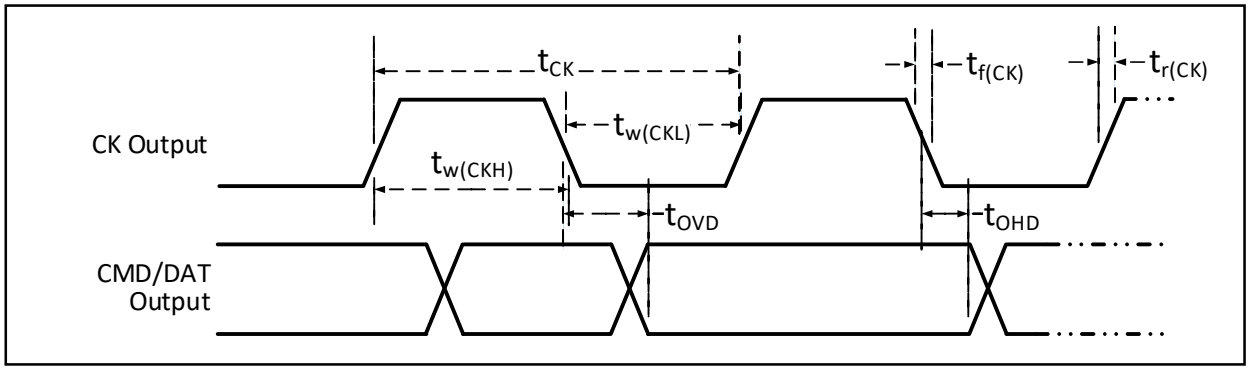



Table 3-33 SDMMC interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{CK}/t_{CK}$ | Clock frequency in data transmission mode | CL≤30pF | | 100 | MHz |
| | | CL≤10pF, $V_{DD18}$ = 1.8V (Single-edge) | | 200 | MHz |
| | | CL≤10pF, $V_{DD18}$ = 3.3V (Single-edge) | | 200 | MHz |
| | | CL≤10pF, $V_{DD18}$ = 1.8V (Single-edge) | | 150(1) | MHz |
| | | CL≤10pF, $V_{DD18}$ = 3.3V (Dual-edge) | | 180(1) | MHz |
| $t_{W(CKL)}$ | Clock low level time | CL≤10pF | 2.2 | | ns |
| $t_{W(CKH)}$ | Clock high level time | CL≤10pF | 2.2 | | |
| $t_{r(CK)}$ | Rising time | CL≤10pF | | 1.2 | |
| $t_{f(CK)}$ | Falling time | CL≤10pF | | 1.2 | |
| CMD/DAT input (Refer to CK) | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| $t_{ISU}$ | Input setup time | CL≤10pF | | 0.5 | | ns |
| $t_{IH}$ | Input holding time | CL≤10pF | | 0.5 | | |
| In high-speed mode, CMD/DAT output (refer to CK) | | | | | | |
| $t_{OV}$ | Output valid time | CL≤10pF | Master mode | | 1.2 | ns |
| | | | Slave mode | | 6 | |
| $t_{OH}$ | Output holding time | CL≤10pF | | 4.5 | | |
| In default mode, CMD/DAT output (refer to CK). | | | | | | |
| $t_{OVD}$ | Output valid default time | CL≤10pF | Master mode | | 1.2 | ns |
| | | | Slave mode | | 6 | |
| $t_{OHD}$ | Output holding default time | CL≤10pF | | 4.5 | | |

*Note: 1. These maximum clock frequencies are significantly influenced by the performance of the opposite end and PCB design; when $V_{DD18}$ = 1.8V, bidirectional communication with an EMMC card has been measured to reach 175MHz.*

*2. At higher clock frequency, if the recommended timing adjustment register value can't communicate stably, users need to initiate the bus sampling tuning sequence to find a better sampling point.*

### 3.3.24 UHSIF Interface Characteristics

Table 3-34 UHSIF interface characteristics

| Symbol | Parameter | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{CK}/t_{CK}$ | Clock frequency in data transmission mode | CL≤10pF, $V_{DD18}$ = 1.8V | | 125 | MHz |
| $t_C$ | Clock cycle | | 8 | | ns |
| $t_{IS}$ | Input signal rise time to CLK | | 0.5 | | ns |
| $t_{IH}$ | Input signal hold time to CLK | | 1.5 | | ns |
| $t_{OD}$ | Output signal delay to CLK | | 6.2 | 8 | ns |

### 3.3.25 FSMC Characteristics

Figure 3-16-1 Asynchronous bus multiplexing PSRAM/NOR read operation waveform

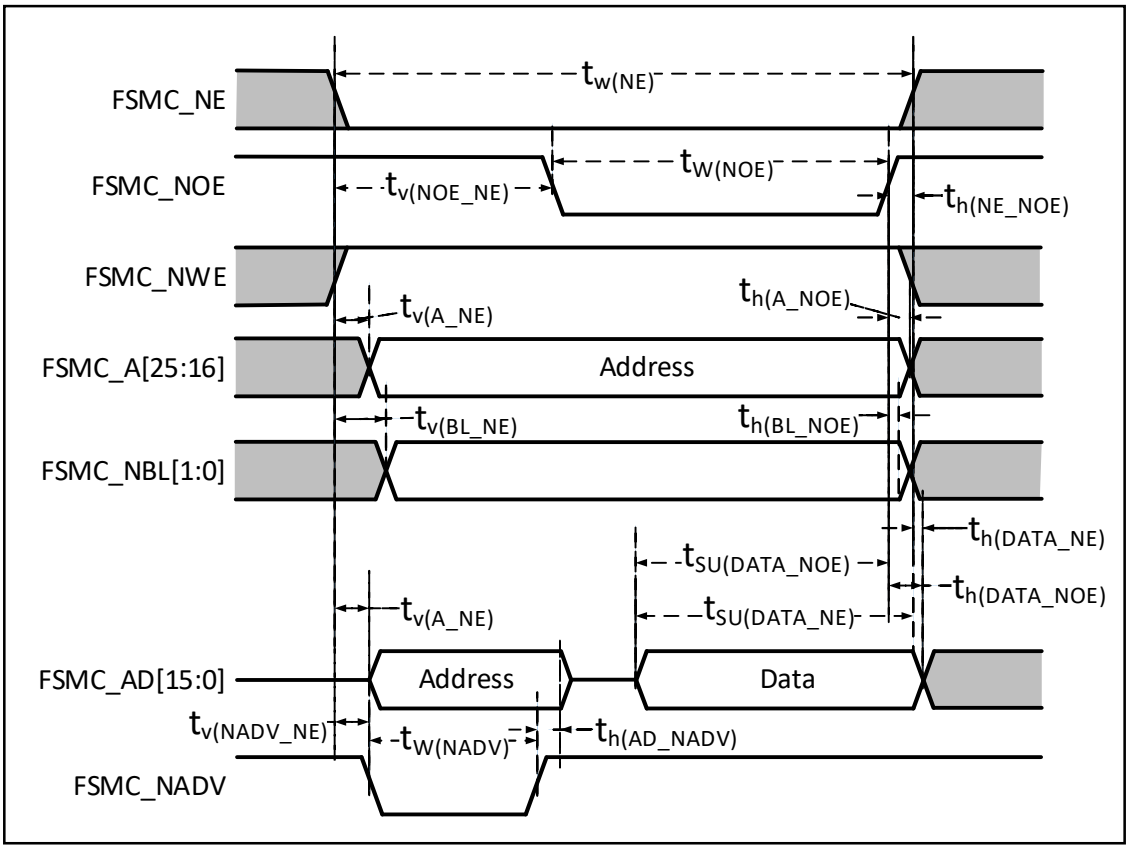


Figure 3-16-2 Asynchronous bus non-multiplexing PSRAM/NOR read operation waveform

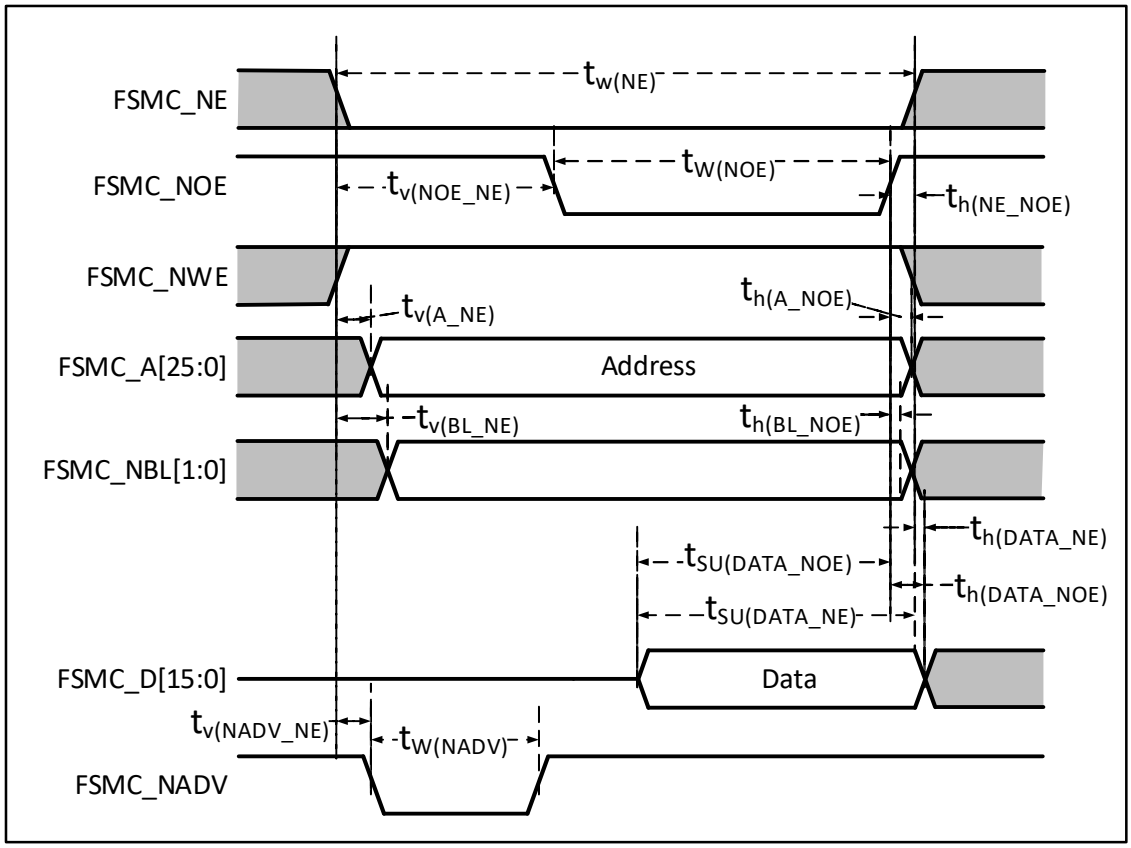



Table 3-35 Timing of PSRAM/NOR read operations for asynchronous bus multiplexing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(NE)}$ | FSMC_NE low level time | 7*$t_{HCLK}$ | | ns |
| $t_{V(NOE\_NE)}$ | FSMC_NE low to FSMC_NOE low | 0 | | |
| $t_{W(NOE)}$ | FSMC_NOE low time | 4*$t_{HCLK}$ | | |
| $t_{h(NE\_NOE)}$ | FSMC_NOE high to FSMC_NE high hold time | 0 | | |
| $t_{V(A\_NE)}$ | FSMC_NE low to FSMC_A valid | 0 | 5 | |
| $t_{V(NADV\_NE)}$ | FSMC_NE low to FSMC_NADV low | 0 | 5 | |
| $t_{W(NADV)}$ | FSMC_NADV low time | $t_{HCLK}$ | | |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | 2*$t_{HCLK}$ | | |
| $t_{h(A\_NOE)}$ | Address hold time after FSMC_NOE high | 0 | | |
| $t_{h(BL\_NOE)}$ | FSMC_BL hold time after FSMC_NOE high | 0 | | |
| $t_{V(BL\_NE)}$ | FSMC_NE low to FSMC_BL valid | 0 | 5 | |
| $t_{SU(DATA\_NE)}$ | Data to FSMC_NE high build time | 3*$t_{HCLK}$ | | |
| $t_{SU(DATA\_NOE)}$ | Data to FSMC_NOE high build time | 3*$t_{HCLK}$ | | |
| $t_{h(DATA\_NE)}$ | Data hold time after FSMC_NE high | 0 | | |
| $t_{h(DATA\_NOE)}$ | Data hold time after FSMC_NOE high | 0 | | |

Figure 3-17-1 Asynchronous bus multiplexing PSRAM/NOR write operation waveform

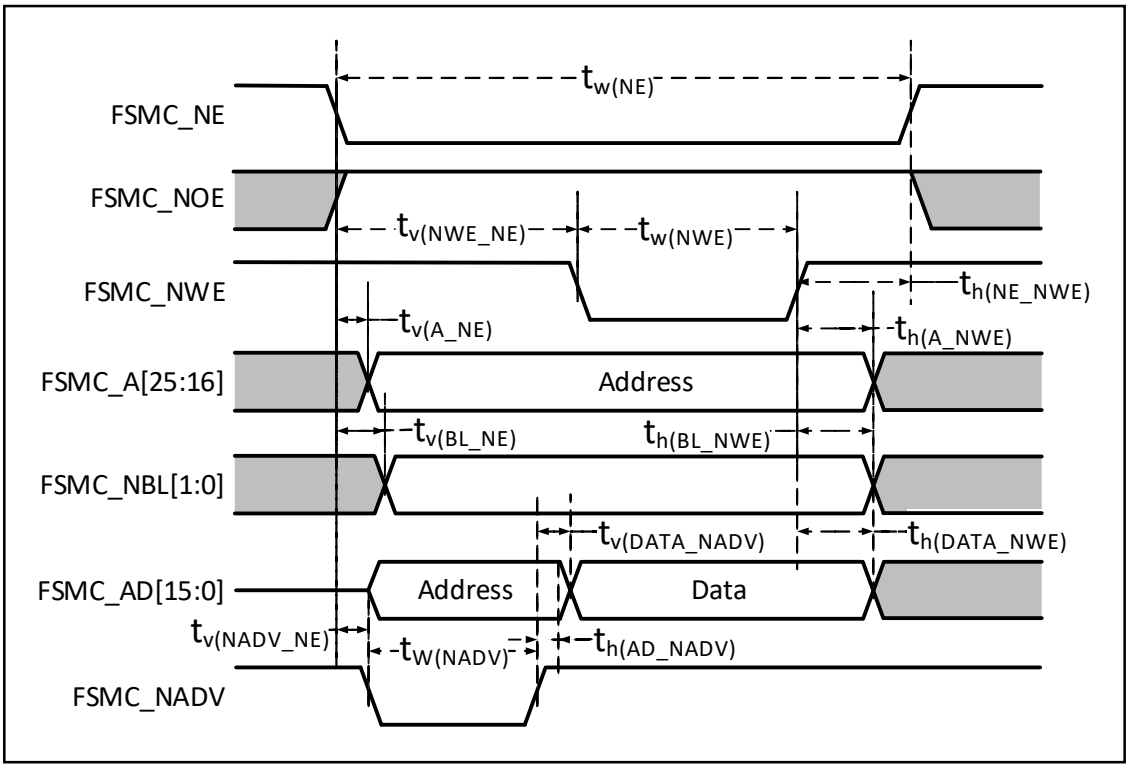



Figure 3-17-2 Asynchronous bus non-multiplexing PSRAM/NOR write operation waveform

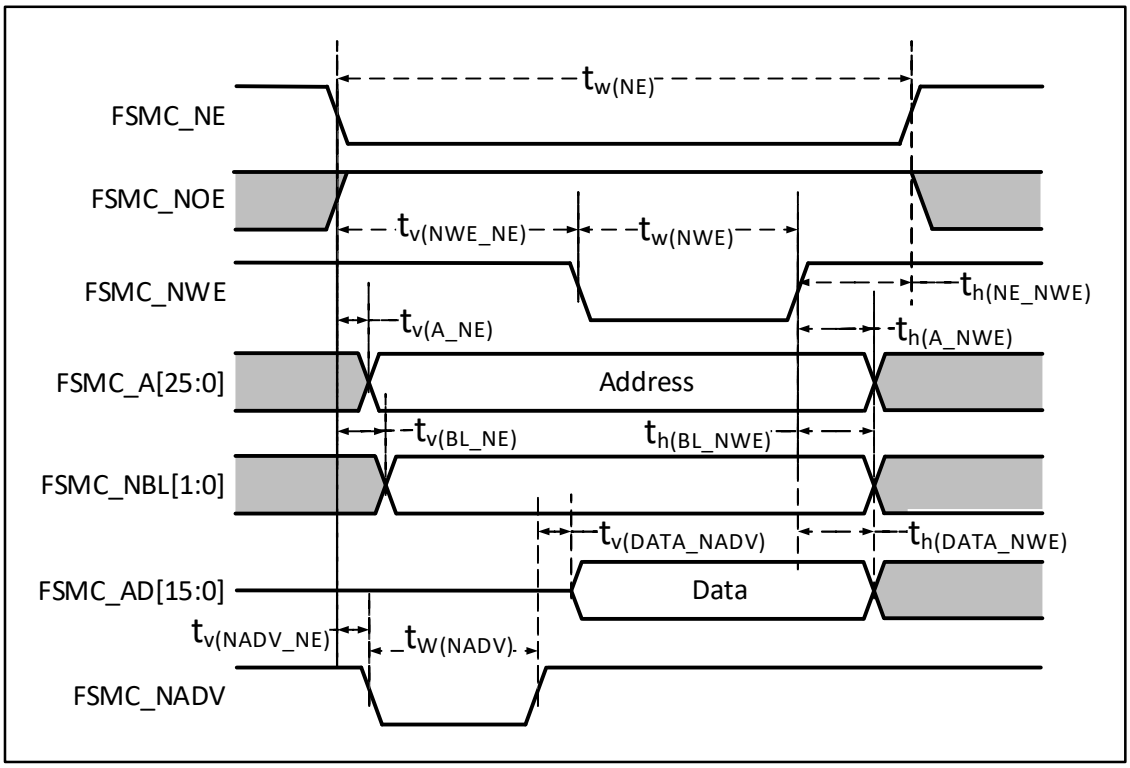



Table 3-36 Timing of PSRAM/NOR write operations for asynchronous bus multiplexing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|

| | | | | |
|---|---|---|---|---|
| $t_{W(NE)}$ | FSMC_NE low level time | $5*t_{HCLK}$ | | ns |
| $t_{V(NEW\_NE)}$ | FSMC_NE low to FSMC_NWE low | $3*t_{HCLK}$ | | |
| $t_{W(NWE)}$ | FSMC_NWE low time | $2*t_{HCLK}$ | | |
| $t_{h(NE\_NWE)}$ | FSMC_NWE high to FSMC_NE high hold time | $t_{HCLK}$ | | |
| $t_{V(A\_NE)}$ | FSMC_NE low to FSMC_A valid | 0 | 5 | |
| $t_{V(NADV\_NE)}$ | FSMC_NE low to FSMC_NADV low | 0 | 5 | |
| $t_{W(NADV)}$ | FSMC_NADV low time | $t_{HCLK}$ | | |
| $t_{h(AD\_NADV)}$ | FSMC_AD (address) valid hold time after FSMC_NADV high | $2*t_{HCLK}$ | | |
| $t_{h(A\_NWE)}$ | Address hold time after FSMC_NWE high | $t_{HCLK}$ | | |
| $t_{V(BL\_NE)}$ | FSMC_NE low to FSMC_BL valid | 0 | 5 | |
| $t_{h(BL\_NWE)}$ | FSMC_BL hold time after FSMC_NWE high | $t_{HCLK}$ | | |
| $t_{V(DATA\_NADV)}$ | FSMC_NADV high to data hold time | $2*t_{HCLK}$ | | |
| $t_{h(DATA\_NWE)}$ | Data hold time after FSMC_NWE high | $t_{HCLK}$ | | |

Figure 3-18 Synchronous bus multiplexing NOR/PSRAM read waveforms

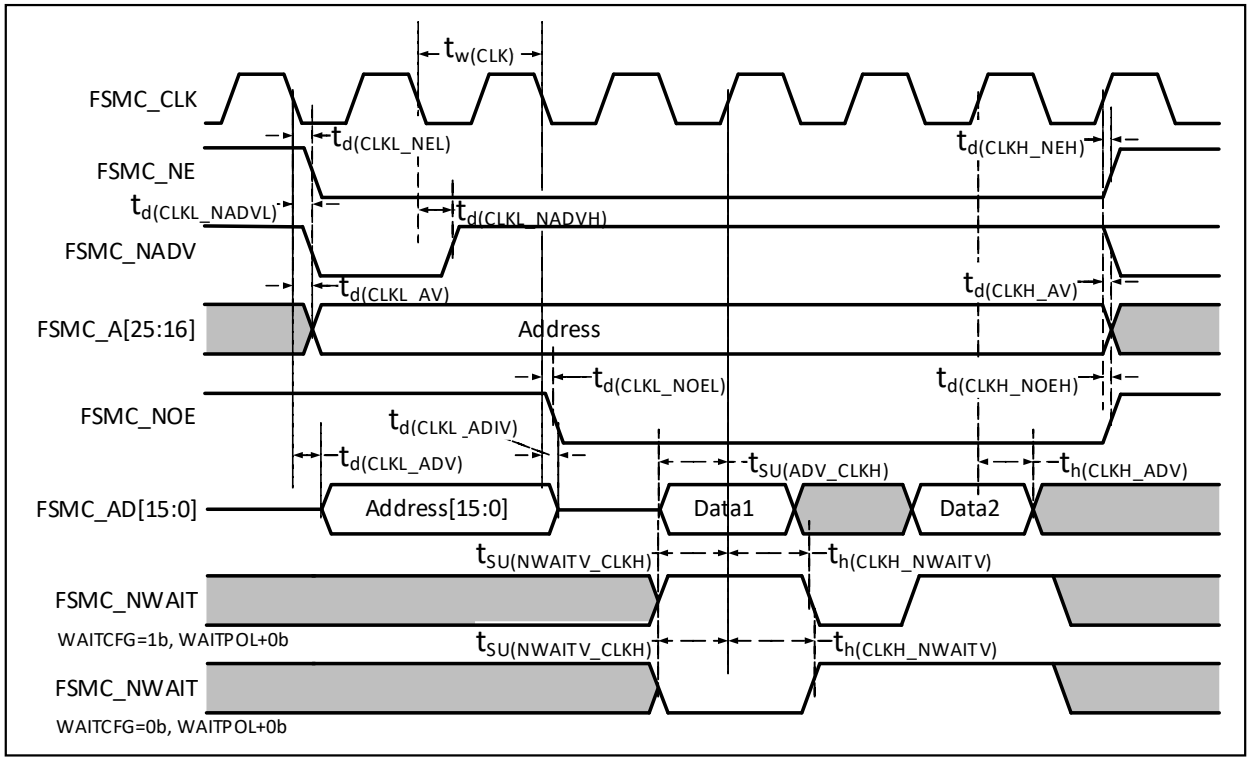



Table 3-37 Synchronous bus multiplexing NOR/PSRAM read timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(CLK)}$ | FSMC_CLK period | $2*t_{HCLK}$ | | ns |
| $t_{d(CLKL\_NEL)}$ | FSMC_CLK low to FSMC_NE low | 0 | 5 | |
| $t_{d(CLKH\_NEH)}$ | FSMC_CLK high to FSMC_NE high | $0.5*t_{HCLK}$ | $0.5*t_{HCLK}$ | |
| $t_{d(CLKL\_NADVL)}$ | FSMC_CLK low to FSMC_NADV low | 0 | 5 | |
| $t_{d(CLKL\_NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 0 | 5 | |
| $t_{d(CLKL\_AV)}$ | FSMC_CLK low to FSMC_Ax valid (x = 16…25) | 0 | 5 | |

| | | | | |
|---|---|---|---|---|
| $t_{d(CLKH\_AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16…25) | 0 | 5 | |
| $t_{d(CLKL\_NOEL)}$ | FSMC_CLK low to FSMC_NOE low | $2*t_{HCLK}$ | | |
| $t_{d(CLKH\_NOEH)}$ | FSMC_CLK high to FSMC_NOE high | $t_{HCLK}$ | | |
| $t_{d(CLKL\_ADV)}$ | FSMC_CLK low to FSMC_AD[15:0] valid | 0 | 5 | |
| $t_{d(CLKL\_ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | 5 | |
| $t_{SU(ADV\_CLKH)}$ | FSMC_AD[15:0] valid data before FSMC_CLK high | 8 | | |
| $t_{h(CLKH\_ADV)}$ | FSMC_AD[15:0] valid data after FSMC_CLK high | 8 | | |
| $t_{SU(NWAITV\_CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 6 | | |
| $t_{h(CLKH\_NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | | |

Figure 3-19 Synchronous bus multiplexing PSRAM write waveforms

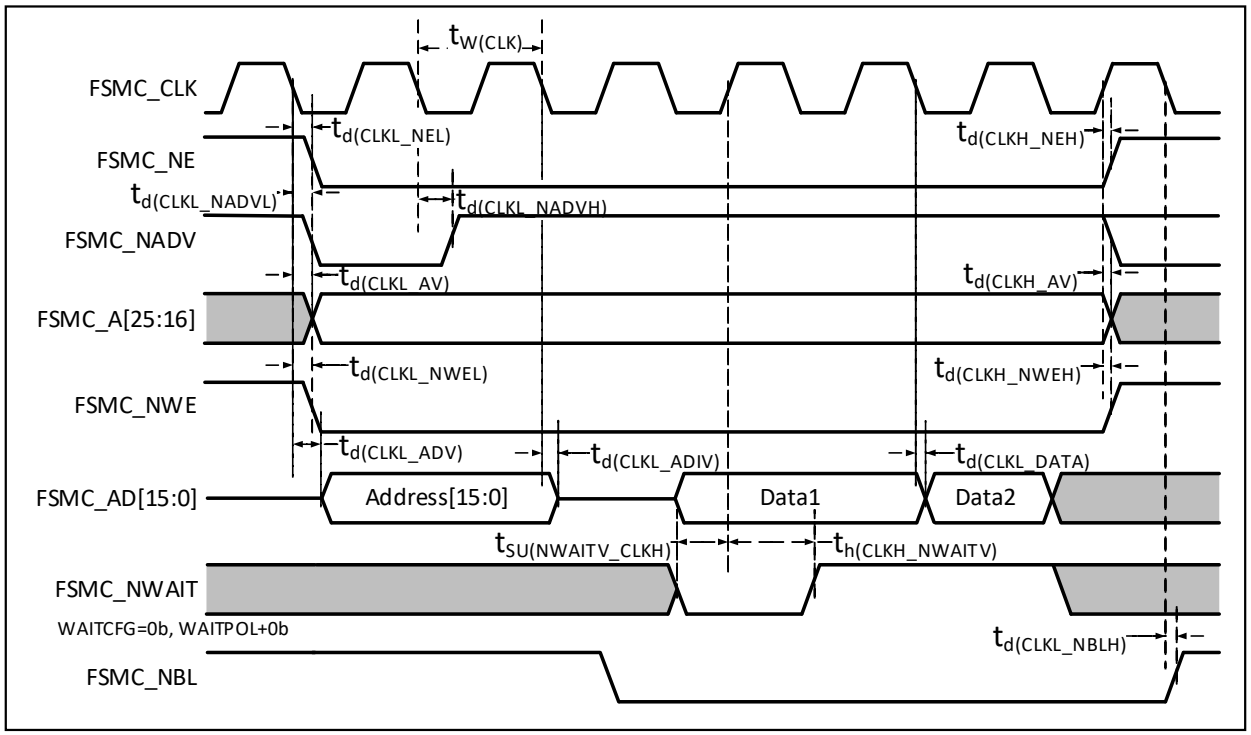



Table 3-38 Synchronous bus multiplexing PSRAM write timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(CLK)}$ | FSMC_CLK period | $2*t_{HCLK}$ | | ns |
| $t_{d(CLKL\_NEL)}$ | FSMC_CLK low to FSMC_NE low | 0 | 5 | |
| $t_{d(CLKH\_NEH)}$ | FSMC_CLK high to FSMC_NE high | $0.5*t_{HCLK}$ | $0.5*t_{HCLK}$ | |
| $t_{d(CLKL\_NADVL)}$ | FSMC_CLK low to FSMC_NADV low | 0 | 5 | |
| $t_{d(CLKL\_NADVH)}$ | FSMC_CLK low to FSMC_NADV high | 0 | 5 | |
| $t_{d(CLKL\_AV)}$ | FSMC_CLK low to FSMC_Ax valid (x = 16…25) | 0 | 5 | |
| $t_{d(CLKH\_AIV)}$ | FSMC_CLK high to FSMC_Ax invalid (x = 16…25) | 0 | 5 | |
| $t_{d(CLKL\_NWEL)}$ | FSMC_CLK low to FSMC_NWE low | 0 | | |
| $t_{d(CLKH\_NWEH)}$ | FSMC_CLK high to FSMC_NWE high | 0 | | |
| $t_{d(CLKL\_ADV)}$ | FSMC_CLK low to FSMC_AD[15:0] valid | 0 | 5 | |
| $t_{d(CLKL\_ADIV)}$ | FSMC_CLK low to FSMC_AD[15:0] invalid | 0 | 5 | |

| | | | | |
|---|---|---|---|---|
| $t_{d(CLKL\_DATA)}$ | FSMC_AD[15:0] valid after FSMC_CLK low | 2 | | |
| $t_{SU(NWAITV\_CLKH)}$ | FSMC_NWAIT valid before FSMC_CLK high | 6 | | |
| $t_{h(CLKH\_NWAITV)}$ | FSMC_NWAIT valid after FSMC_CLK high | 2 | | |
| $t_{d(CLKL\_NBLH)}$ | FSMC_CLK low to FSMC_NBL high | 2 | | |

NAND Controller Waveforms and Timing

Test conditions: NAND operation area, 16-bit data width selected, ECC calculation circuitry enabled, 512-byte page size, other timing configured to set registers FSMC_PCR2 = 0x0002005E, FSMC_PMEM2 = 0x01020301, FSMC_PATT2 = 0x01020301.

Figure 3-20 NAND controller read operation waveform

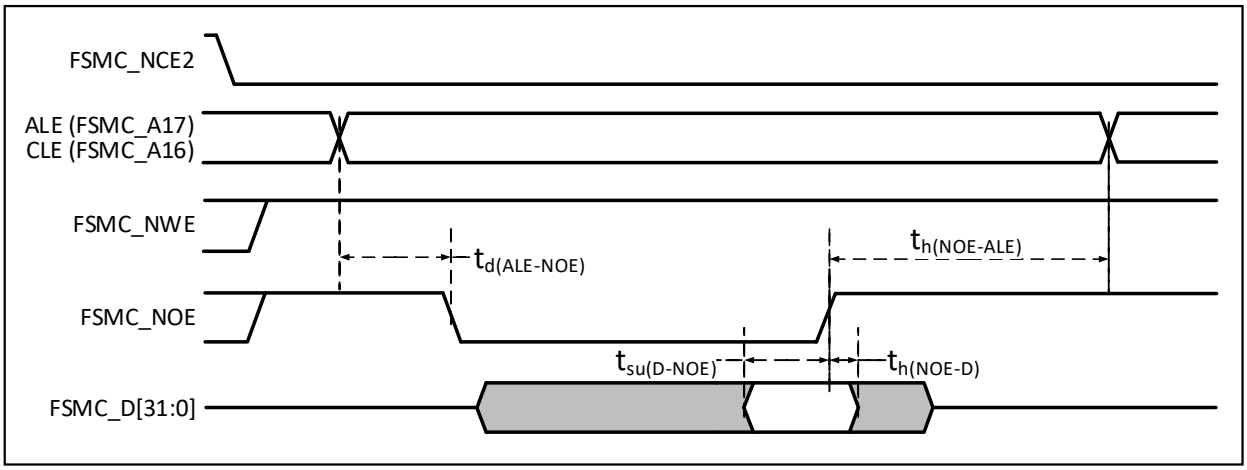



Figure 3-21 NAND controller write operation waveform

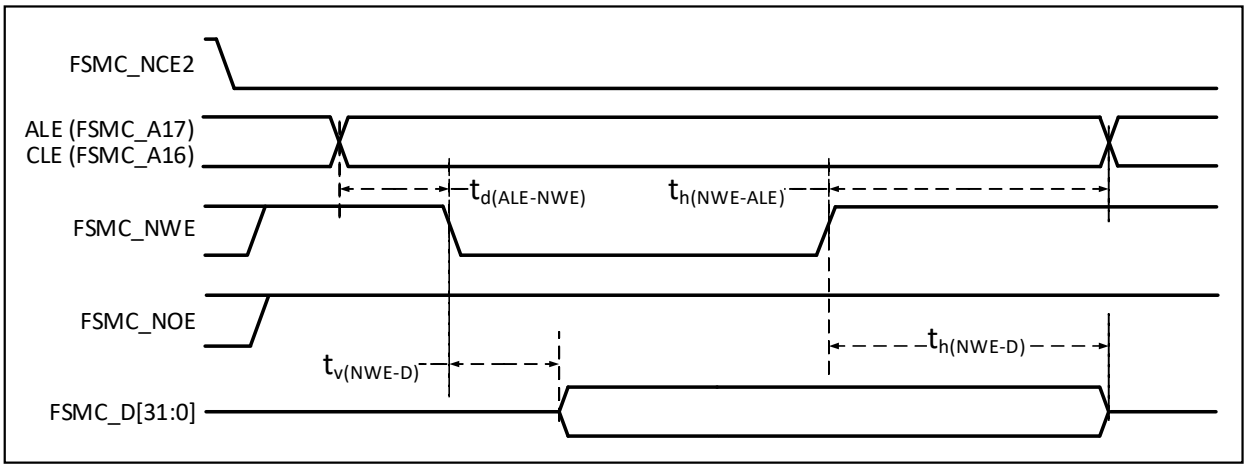


Figure 3-22 Waveforms of NAND controller read operations in general-purpose memory space

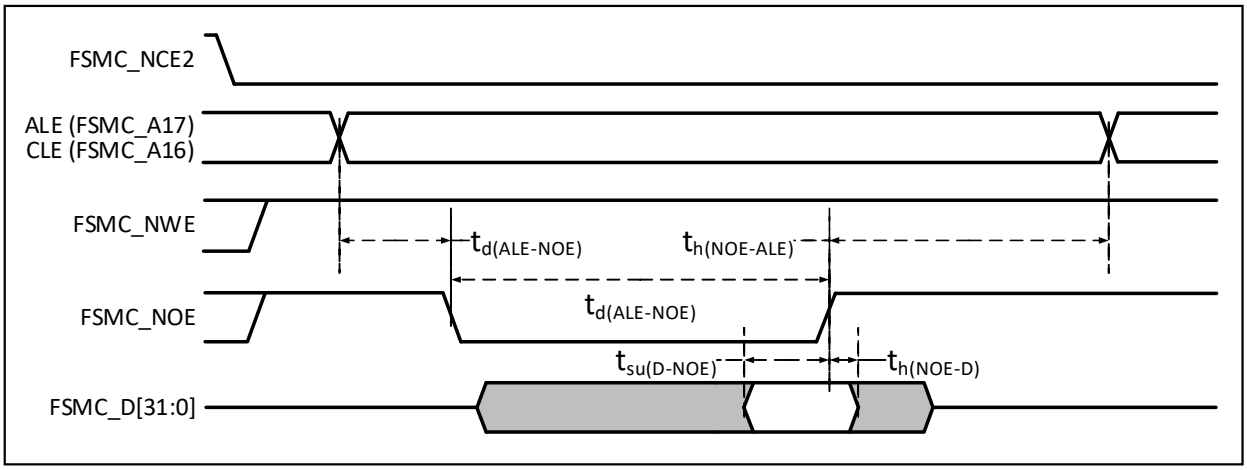



Figure 3-23 Waveforms of NAND controller write operations in general-purpose memory space

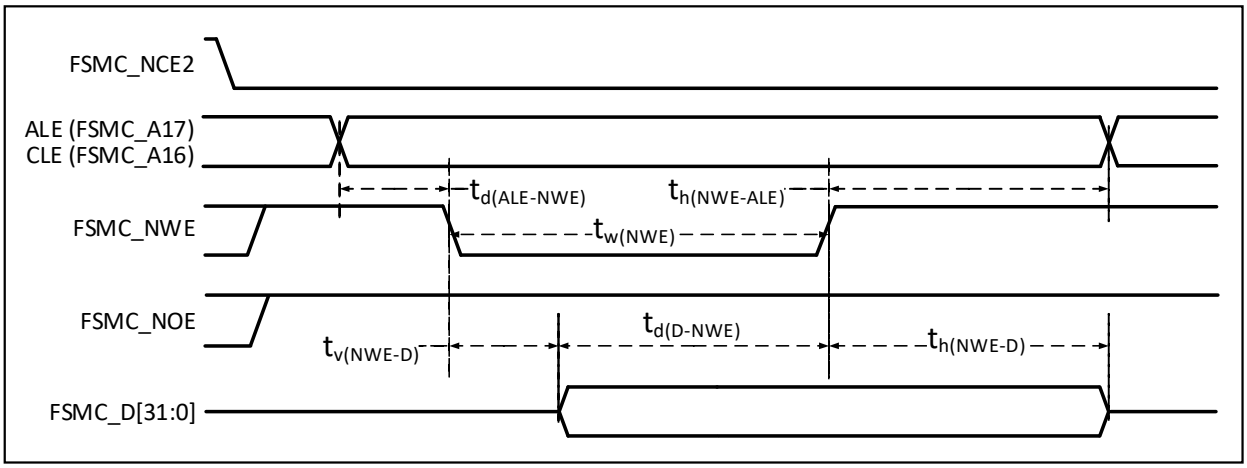



Table 3-39 Timing characteristics of NAND flash read and write cycles

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{d(D-NEW)}$ | FSMC_NWE high before to FSMC_D[31:0] data valid | $4*t_{HCLK}$ | | ns |
| $t_{w(NOE)}$ | FSMC_NOE low time | $4*t_{HCLK}$ | | |
| $t_{su(D-NOE)}$ | FSMC_NOE high before to FSMC_D[31:0] data valid | 20 | | |
| $t_{h(NOE-D)}$ | FSMC_NOE high followed by to FSMC_D[31:0] data valid | 15 | | |
| $t_{w(NWE)}$ | FSMC_NWE low time | $4*t_{HCLK}$ | | |
| $t_{v(NWE-D)}$ | FSMC_NWE low to FSMC_D[31:0] data valid | 0 | | |
| $t_{h(NWE-D)}$ | FSMC_NWE high to FSMC_D[31:0] data invalid | $2*t_{HCLK}$ | | |
| $t_{d(ALE-NWE)}$ | FSMC_NWE low before to FSMC_ALE valid | $2*t_{HCLK}$ | | |
| $t_{h(NWE-ALE)}$ | FSMC_NWE high to FSMC_ALE invalid | $2*t_{HCLK}$ | | |
| $t_{d(ALE-NOE)}$ | FSMC_NOE low before to FSMC_ALE valid | $2*t_{HCLK}$ | | |
| $t_{h(NOE-ALE)}$ | FSMC_NOE high to FSMC_ALE invalid | $4*t_{HCLK}$ | | |

### 3.3.26 SDRAM Characteristics

Figure 3-24 SDRAM read operation waveform (CL = 1)

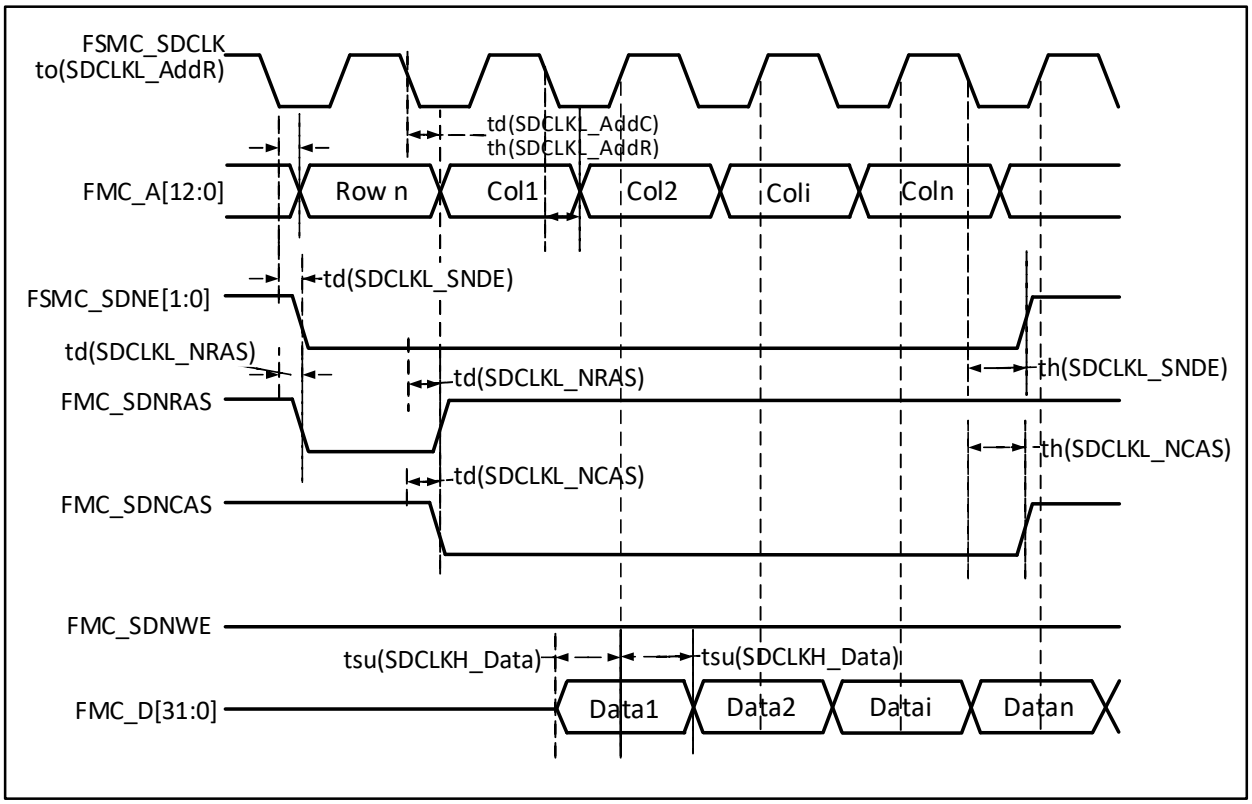



Table 3-40 SDRAM read operation timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | 9.5 | 10.5 | ns |
| $t_{SU(SDCLKH\_DATA)}$ | Data input setup time | 3.5 | | |
| $t_{h(SDCLKH\_DATA)}$ | Data input holding time | 1.5 | | |
| $t_{d(SDCLKL\_ADD)}$ | Address valid time | | 4 | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip selection valid time | | 1 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip selection holding time | 0 | | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS holding time | 0 | | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS holding time | 0 | | |

*Note: When reading SDRAM, the maximum value for FMC_SDCLK is set to 100MHz.*

Table 3-41 LPSDR SDRAM read operation timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | 9.5 | 10.5 | ns |
| $t_{SU(SDCLKH\_DATA)}$ | Data input setup time | 3.0 | | |
| $t_{h(SDCLKH\_DATA)}$ | Data input holding time | 1.5 | | |

| | | | | |
|---|---|---|---|---|
| $t_{d(SDCLKL\_ADD)}$ | Address valid time | | 3.5 | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip selection valid time | | 1 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip selection holding time | 0 | | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS holding time | 0 | | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS holding time | 0 | | |

*Note: When reading SDRAM, the maximum value for FMC_SDCLK is set to 100MHz.*

Figure 3-25 SDRAM write operation waveform

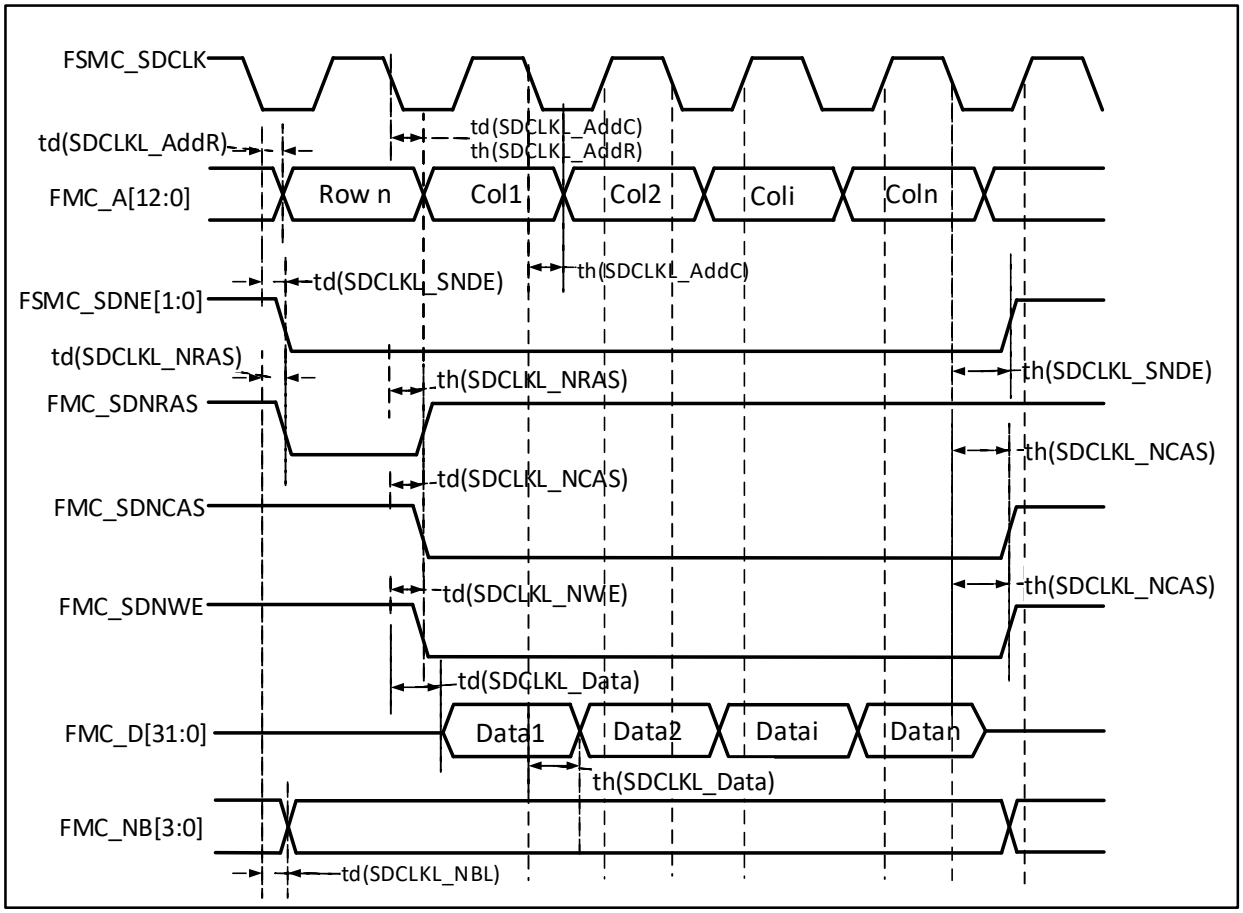



Table 3-42 SDRAM write operation timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | 9.5 | 10.5 | ns |
| $t_{SU(SDCLKL\_DATA)}$ | Data output valid time | | 2 | |
| $t_{h(SDCLKL\_DATA)}$ | Data output holding time | 0.5 | | |
| $t_{d(SDCLKL\_ADD)}$ | Address valid time | | 4 | |
| $t_{d(SDCLKL\_SDNWE)}$ | SDNWE valid time | | 1 | |
| $t_{h(SDCLKL\_SDNWE)}$ | SDNWE holding time | 0 | | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip selection valid time | | 1 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip selection holding time | 0 | | |

| | | | | |
|---|---|---|---|---|
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS holding time | 0 | | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS holding time | 0 | | |

*Note: When reading SDRAM, the maximum value for FMC_SDCLK is set to 100MHz.*

Table 3-43 LPSDR SDRAM write operation timing

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $t_{W(SDCLK)}$ | FMC_SDCLK period | 9.5 | 10.5 | ns |
| $t_{SU(SDCLKL\_DATA)}$ | Data output valid time | | 4 | |
| $t_{h(SDCLKL\_DATA)}$ | Data output holding time | 0 | | |
| $t_{d(SDCLKL\_ADD)}$ | Address valid time | | 3.5 | |
| $t_{d(SDCLKL\_SDNWE)}$ | SDNWE valid time | | 1 | |
| $t_{h(SDCLKL\_SDNWE)}$ | SDNWE holding time | 0 | | |
| $t_{d(SDCLKL\_SDNE)}$ | Chip selection valid time | | 1 | |
| $t_{h(SDCLKL\_SDNE)}$ | Chip selection holding time | 0 | | |
| $t_{d(SDCLKL\_SDNRAS)}$ | SDNRAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNRAS)}$ | SDNRAS holding time | 0 | | |
| $t_{d(SDCLKL\_SDNCAS)}$ | SDNCAS valid time | | 1 | |
| $t_{h(SDCLKL\_SDNCAS)}$ | SDNCAS holding time | 0 | | |

*Note: When reading SDRAM, the maximum value for FMC_SDCLK is set to 100MHz.*

### 3.3.27 DVP Interface Characteristics

Figure 3-26 DVP timing waveform

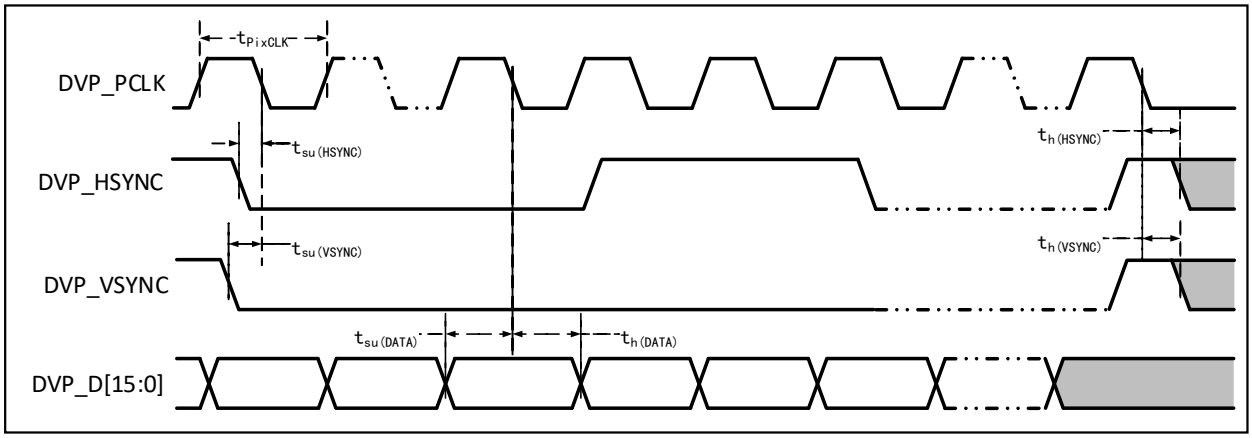



Table 3-44 DVP interface characteristics

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $f_{PixCLK}/t_{PixCLK}$ | Pixel clock input frequency | | 150 | MHz |
| $Duty_{(PixCLK)}$ | Duty cycle of pixel clock | 15 | | % |
| $t_{su(DATA)}$ | Data setup time | 2.5 | | ns |
| $t_{h(DATA)}$ | Data holding time | 1 | | ns |

| | | | | |
|---|---|---|---|---|
| $t_{su(HSYNC)}/t_{su(VSYNC)}$ | HSYNC/VSYNC signal input setup time | 2.5 | | ns |
| $t_{h(HSYNC)}/t_{h(VSYNC)}$ | HSYNC/VSYNC signal input holding time | 1 | | ns |

### 3.3.28 LTDC Interface Characteristics

Figure 3-27 LTDC horizontal sequence diagram

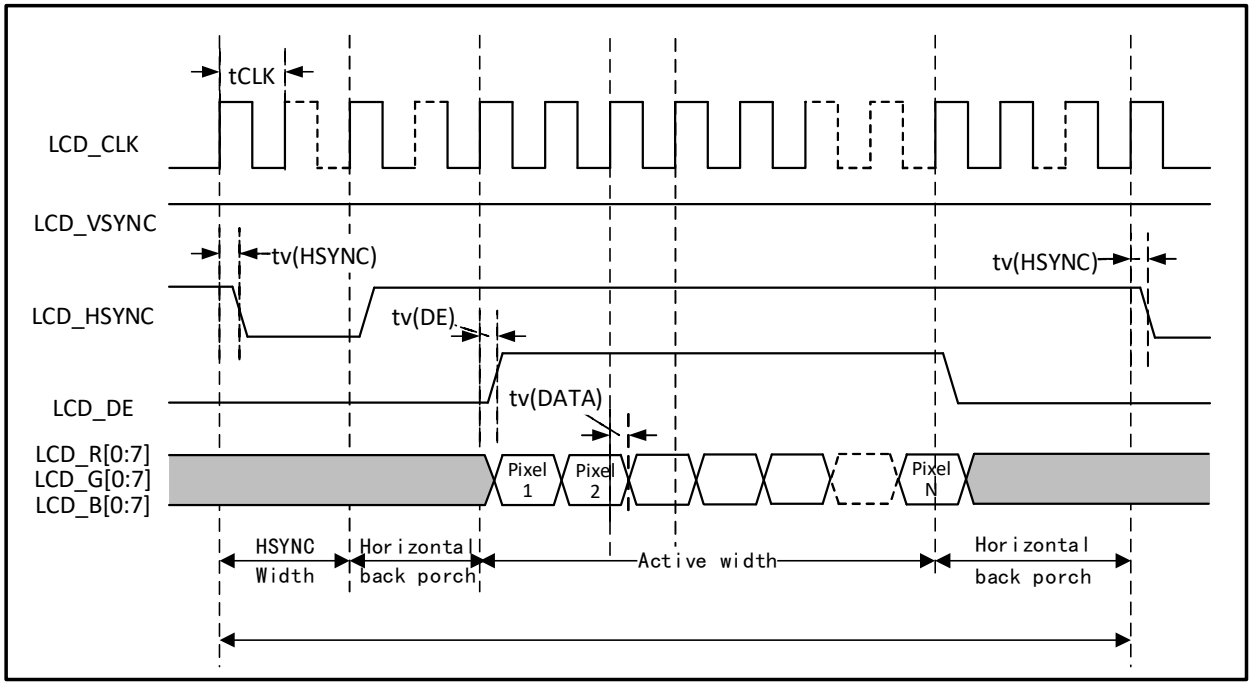



Figure 3-28 LTDC vertical sequence diagram

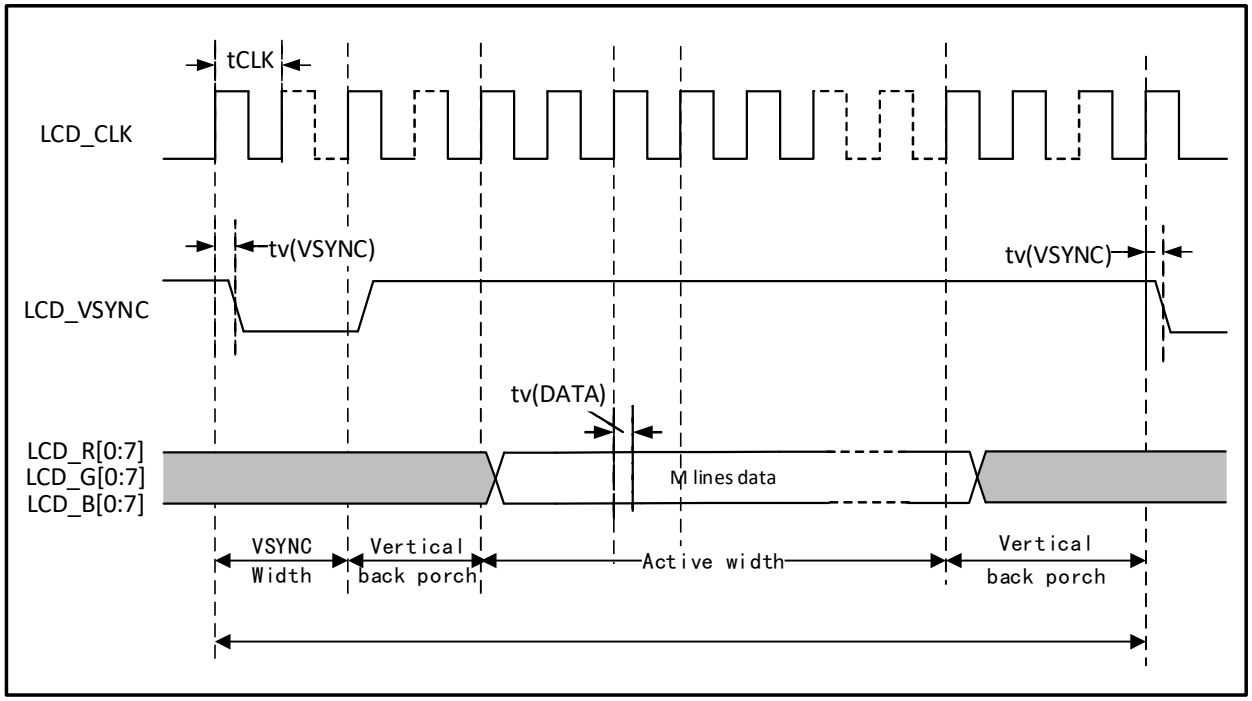


Table 3-45 LDTC interface characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $F_{CLK}$ | Clock output frequency | CL=30pF, $V_*$(1) = 2.7-3.6V | | | 120 | MHz |
| | | CL=10pF, $V_*$(1) = 2.7-3.6V | | | 200 | MHz |
| | | CL=30pF, $V_*$(1) = 1.6-2.7V | | | 55 | MHz |
| Duty (CLK) | Clock duty cycle | CL=30pF | 45 | | 55 | % |
| $t_{W\ (CKH)}$ | Clock high/low level duration | CL=30pF | $t_{CLK}$/2-0.7 | | $t_{CLK}$/2+0.7 | ns |
| $t_V$ | Data and control signal output active duration | CL=30pF | | | 0.7 | ns |
| $t_S$ | Data and control signal output hold time | CL=30pF | 0 | | | ns |

*Note: 1. In the table above, V* may be represented as $V_{DDIO}$, $V_{IO18}$, or $V_{DD33}$ depending on the specific pin.*

### 3.3.29 Gigabit Ethernet Interface Characteristics

Figure 3-29 ETH-SMI timing waveforms

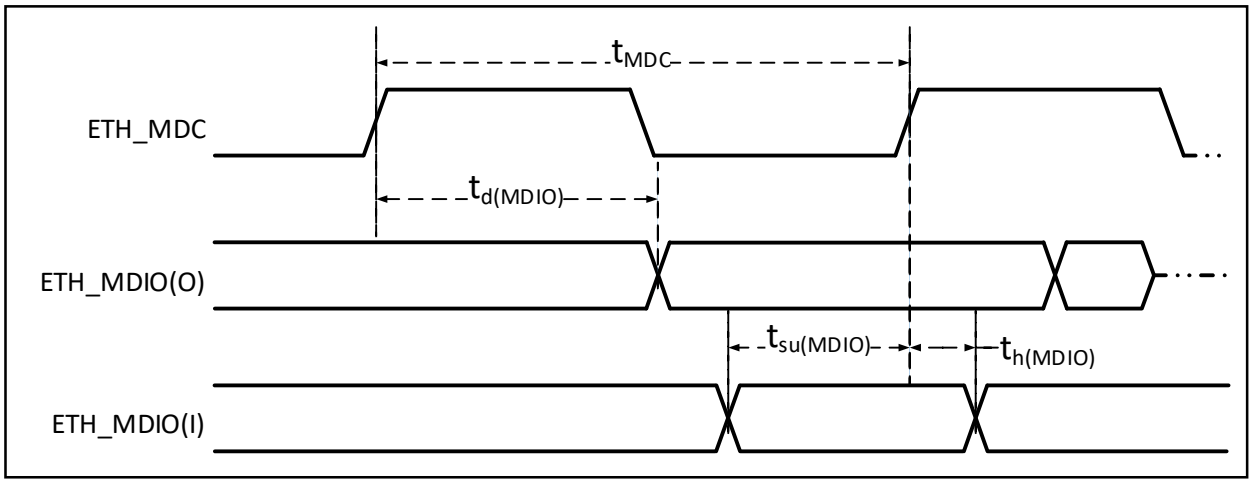



Table 3-46 SMI signaling characteristics for Ethernet MACs

| Symbol | Parameter & Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{MDC}$/$t_{MDC}$ | MDC clock frequency | | | 2.5 | MHz |
| $t_{d(MDIO)}$ | Valid time for MDIO write data | 0 | | 300 | ns |
| $t_{su(MDIO)}$ | Read data setup time | 10 | | | |
| $t_{h(MDIO)}$ | Read data holding time | 10 | | | |

Figure 3-30 ETH-RGMII signal timing waveforms

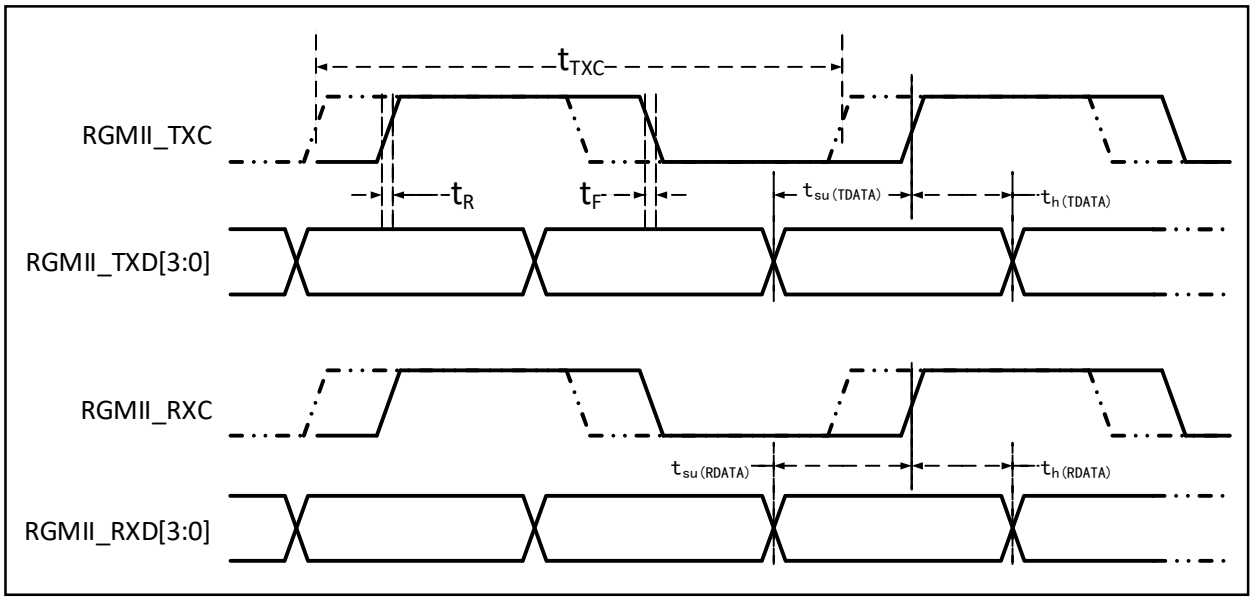



Table 3-47 RGMII signaling characteristics for Ethernet MACs

| Symbol | Parameter & Description | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $f_{TXC}/t_{TXC}$ | TXC/RXC clock frequency | 7.2 | 8 | 8.8 | ns |
| $t_R$ | TXC/RXC rising time | | | 2.0 | |
| $t_F$ | TXC/RXC falling time | | | 2.0 | |
| $t_{su(TDATA)}$ | Send data setup time | 1.2 | 2.0 | | |
| $t_{h(TDATA)}$ | Send data holding time | 1.2 | 2.0 | | |
| $t_{su(RDATA)}$ | Input data setup time | 1.2 | 2.0 | | |
| $t_{h(RDATA)}$ | Input data holding time | 1.2 | 2.0 | | |

### 3.3.30 12-bit ADC Characteristics

Table 3-48 ADC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Supply voltage | $f_S$ < 2MHz | 2.7 | | 3.6 | V |
| | | $f_S \geq$ 2MHz | 3 | | 3.6 | V |
| $V_{REFP}$(2) | Positive reference voltage | $V_{REFP} \leq V_{DD33A}$ | 2.4 | 3.3 | 3.6 | V |
| $I_{DD33A}$ | ADC supply current (excluding buffer) | ADC_LP = 0 | | 1.42 | | mA |
| | | ADC_LP = 1 | | 0.37 | | mA |
| $I_{BUF}$ | ADC buffer own current | ADC_LP = 0 | | 0.76 | | mA |
| | | ADC_LP = 1 | | 0.19 | | mA |
| $f_{ADC}$ | ADC clock frequency | | | 14 | 80 | MHz |
| $f_S$ | Sampling rate | | 0.06 | | 5 | MHz |
| $f_{TRIG}$ | External trigger frequency | $f_{ADC}$ = 14MHz | | | 875 | kHz |
| | | | | | 16 | $1/f_{ADC}$ |
| | | $f_{ADC}$ = 80MHz | | | 4.4 | MHz |
| | | | | | 18 | $1/f_{ADC}$ |

| | | | | | | |
|---|---|---|---|---|---|---|
| $V_{AIN}$ | Conversion voltage range | $V_{REFP} \geq V_{DDIO}$ | 0 | | $V_{DDIO}$ | V |
| | | $V_{REFP} < V_{DDIO}$ | 0 | | $V_{REFP}$ | V |
| $R_{AIN}$ | External input impedance | | | | 50 | kΩ |
| $R_{ADC}$ | Sampling switch resistance | | | 0.6 | 1.5 | kΩ |
| $C_{ADC}$ | Internal sampling and holding capacitance | | | 4.5 | | pF |
| $t_{CAL}$ | Calibration time | $f_{ADC}$ = 14MHz | 2 | | | us |
| $t_{Iat}$ | Injection-triggered conversion delay | $f_{ADC}$ = 14MHz | | | 0.143 | us |
| | | $f_{ADC}$ = 80MHz | | | 0.025 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_{Iatr}$ | Conventional trigger conversion delay | $f_{ADC}$ = 14MHz | | | 0.143 | us |
| | | $f_{ADC}$ = 80MHz | | | 0.025 | us |
| | | | | | 2 | $1/f_{ADC}$ |
| $t_s$ | Sampling time | $f_{ADC}$ = 14MHz | 0.107 | | 17.11 | us |
| | | | 1.5 | | 239.5 | $1/f_{ADC}$ |
| | | $f_{ADC}$ = 80MHz | 0.037 | | 2.49 | us |
| | | | 3.5 | | 239.5 | $1/f_{ADC}$ |
| $t_{STAB}$ | Power-on time | | | | 1 | us |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{ADC}$ = 14MHz | 1 | | 18 | us |
| | | | 14 | | 252 | $1/f_{ADC}$ |
| | | $f_{ADC}$ = 80MHz | 0.2 | | 3.15 | us |
| | | | 16 | | 252 | $1/f_{ADC}$ |

*Note: 1. All of the above are guaranteed by design parameters.*

*2. $V_{REFP}$ external capacitance should be as close as possible, otherwise it will affect the ADC performance.*

Formula: Maximum $R_{AIN}$

$$R_{AIN} < \frac{T_S}{f_{ADC} \times C_{ADC} \times \ln 2^{N+2}} - R_{ADC}$$

The above formula is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. where N=12 (indicating 12-bit resolution).

Table 3-49 Maximum $R_{AIN}$ when $f_{ADC}$ = 14MHz

| $T_S$(Period) | $t_S$(us) | 最大 $R_{AIN}$(kΩ) |
|---|---|---|
| 1.5 | 0.11 | 1.0 |
| 3.5 | 0.25 | 4.0 |
| 7.5 | 0.54 | 10.9 |
| 13.5 | 0.96 | 20.5 |
| 28.5 | 2.04 | 44.9 |
| 41.5 | 2.96 | 66.3 |

Table 3-50 ADC error ($f_{ADC}$ = 14MHz, ADC_LP = 1)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| EO | Offset error | $R_{AIN}$ < 10kΩ, $V_{DD33A}$ = 3.3V | | ±2 | ±5 | LSB |
| ED | Differential nonlinear error | | | ±1 | ±4 | |
| EL | Integral nonlinear error | | | ±2 | ±4 | |

*Note: The above are guaranteed design parameters.*

Table 3-51 ADC error ($f_{ADC}$ = 80MHz, ADC_LP = 0)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| EO | Offset error | $R_{AIN}$ < 2kΩ, $V_{DD33A}$ = 3.3V | | ±3 | ±7 | LSB |
| ED | Differential nonlinear error | | | ±2 | ±5 | |
| EL | Integral nonlinear error | | | ±3 | ±5 | |

*Note: The above are guaranteed design parameters.*

Cp indicates the parasitic capacitance on the PCB and pads (About 5pF), which may be related to the quality of the pads and PCB layout. Larger values of Cp will reduce the conversion accuracy and the solution is to reduce the $f_{ADC}$

Figure 3-31 ADC typical connection diagram

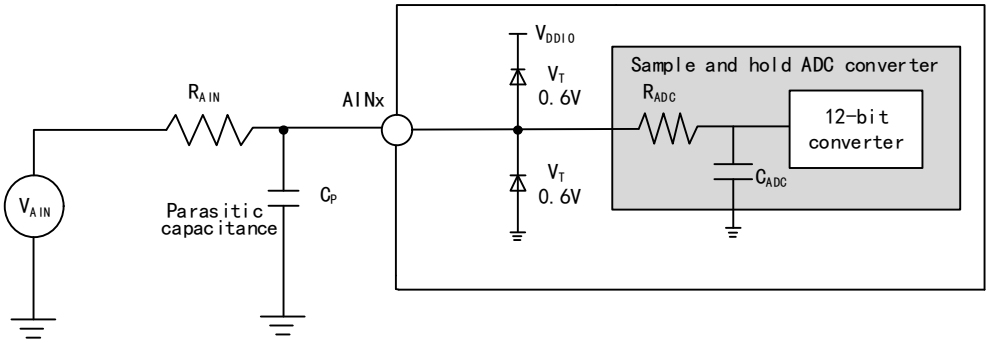
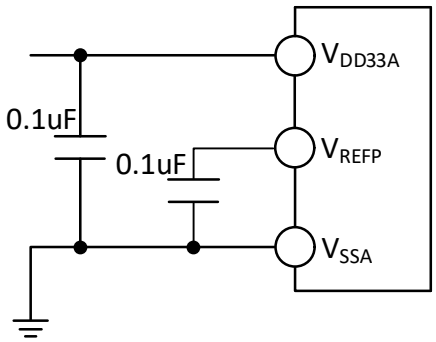



Figure 3-32 Analog power supply and decoupling circuit reference



### 3.3.31 10-bit HSADC Characteristics

Table 3-52 HSADC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Supply voltage | | 3.0 | 3.3 | 3.6 | V |
| $V_{REFP}$(2) | Positive reference voltage | $V_{REFP} \leq V_{DD33A}$ | 2.4 | 3.3 | 3.6 | V |
| $V_{DDIO}$ | I/O pin voltage when using HSADC | | $V_{REFP}$ | | | V |
| $I_{DDA}$ | Supply current | | | 1.1 | | mA |
| $I_{DDIO}$ | ADC I/O pin current | | | 1.8 | | mA |
| $f_{HSADC}$ | ADC clock frequency | | | 100 | | MHz |
| $f_S$ | Sampling rate | | | 20 | | MHz |
| $V_{AIN}$ | Conversion voltage range | $V_{REFP} \geq V_{DDIO}$ | 0 | | $V_{DDIO}$ | V |
| | | $V_{REFP} < V_{DDIO}$ | 0 | | $V_{REFP}$ | V |
| $R_{AIN}$ | External input impedance | | | | 0.4 | kΩ |
| $R_{HSADC}$ | Sampling switch resistance | | | 0.1 | 0.25 | kΩ |
| $C_{HSADC}$ | Internal sampling and holding capacitance | | | 1.1 | | pF |
| $t_{CAL}$ | Calibration time | | | 1 | | us |
| $t_s$ | Sampling time | $f_{HSADC}$ = 100MHz | | 10 | | ns |
| | | | | 1 | | $1/f_{HSADC}$ |
| $t_{STAB}$ | Power-on time | | | | 1 | us |
| $t_{CONV}$ | Total conversion time (including sampling time) | $f_{HSADC}$ = 100MHz | | 50 | | ns |
| | | | | 5 | | $1/f_{HSADC}$ |

*Note: 1. All of the above are guaranteed by design parameters.*

*2. $V_{REFP}$ external capacitance should be as close as possible, otherwise it will affect the HSADC performance.*

Formula: Maximum $R_{AIN}$

$$R_{AIN} < \frac{T_S}{f_{HSADC} \times C_{HSADC} \times \ln 2^{N+2}} - R_{HSADC}$$

The above formula is used to determine the maximum external impedance such that the error can be less than 1/4 LSB. where N=10 (indicating 10-bit resolution).

Table 3-53 HSADC error

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| EO | Offset error | $R_{AIN}$ < 0.4kΩ, $V_{DD33A}$ = 3.3V | | ±4 | ±9 | LSB |
| ED | Differential nonlinear error | | | ±2 | ±4 | |
| EL | Integral nonlinear error | | | ±3 | ±4 | |

*Note: The above are guaranteed design parameters.*

Cp indicates the parasitic capacitance on the PCB and pads (About 5pF), which may be related to the quality of the pads and PCB layout. Larger values of Cp will reduce the conversion accuracy and the solution is to reduce the $f_{ADC}$.

Figure 3-33 HSADC typical connection diagram

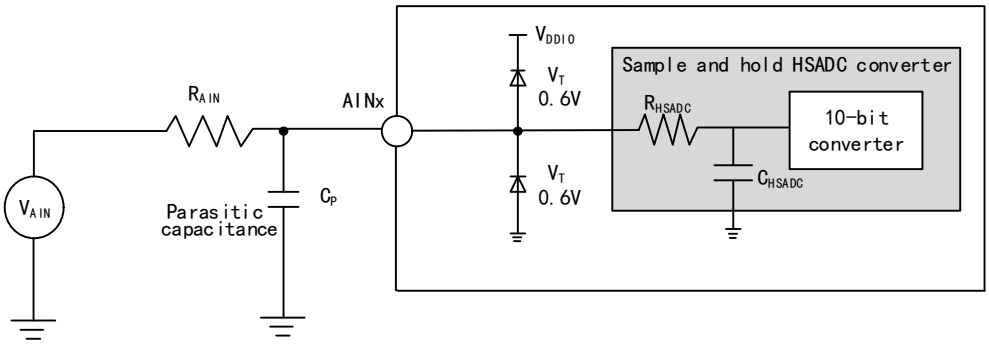
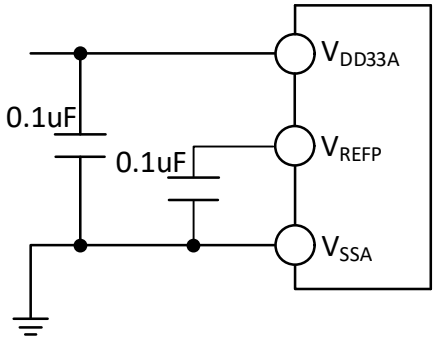



Figure 3-34 Analog power supply and decoupling circuit reference




### 3.3.32 DAC Characteristics

Table 3-54 DAC characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Supply voltage | | 2.4 | 3.3 | 3.6 | V |
| $V_{REFP}$ | Positive reference voltage | $V_{REFP} \leq V_{DD33A}$ | 2.4 | 3.3 | 3.6 | V |
| $R_L$(1) | Load resistance when the buffer is open | | 5 | | | kΩ |
| $C_L$(1) | Load capacitance when buffer is open | | | | 50 | pF |
| $V_{OUT\_MIN}$(1) | Buffer on, 12-bit DAC conversion | | 0 | | 8 | mV |
| $V_{OUT\_MAX}$(1) | | $V_{REFP}$ = 3.3V | 3.29 | | 3.3 | V |
| $V_{OUT\_MIN}$(1) | Buffer off, 12-bit DAC conversion | | 0 | | 3 | mV |
| $V_{OUT\_MAX}$(1) | | $V_{REFP}$ = 3.3V | 3.295 | | 3.3 | V |
| $I_{VREFP}$ | No load, input value 0x800 | | | 58 | | uA |
| | No load, when $V_{REFP}$ = 3.6V, the input value is 0xF1C. | | | 194 | | |
| | No load, when VREFP = 3.6V, the input value is 0x555 (worst) | | | 331 | | |
| $I_{DDA}$ | Buffer opened without load, input value 0x800 | | | 170 | | uA |
| | Buffer open without load, $V_{REFP}$ = 3.6V, input value 0xF1C | | | 150 | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| | Buffer open without load, $V_{REFP}$ = 3.6V, input value 0x555 (worst) | | | 170 | | |
| DNL | Differential nonlinear error | | | ±2 | | LSB |
| INL | Integral nonlinear error | After offset error and gain error correction | | ±4 | | LSB |
| Lose balance | Offset error | | | ±3 | ±12 | mV |
| | | $V_{REFP}$ = 3.6V | | | ±10 | LSB |
| Gain error | | DAC configured as 12-bit | | ±0.4 | | % |
| Amplifier gain(1) | Amplifier gain with open loop | 5kΩ load (max.) | 80 | 85 | | dB |
| $t_{SETTLING}$ | The maximum frequency of the correct DAC_OUT is obtained when the input code is a small change (from the value i to i+1 LSB) | $C_{LOAD}$ ≤ 50pF<br>$R_{LOAD}$ ≥ 5kΩ | | 3 | 4 | us |
| Update rate | When the input code changes slightly (from the value I to i+1LSB), the maximum frequency of the correct DAC_OUT is obtained. | $C_{LOAD}$ ≤ 50pF<br>$R_{LOAD}$ ≥ 5kΩ | | | 1 | MS/s |
| PSRR+(1) | Power supply rejection ratio (relative to $V_{DD33A}$) (static DC measurement) | Without $R_{LOAD}$, $C_{LOAD}$ ≤ 50pF | | -100 | -75 | dB |

*Note: 1. Design parameters are guaranteed;*

### 3.3.33 OPA Characteristics

Table 3-55-1 OPA characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Supply voltage | Recommended not less than 2V | 1.8 | 3.3 | 3.6 | V |
| $V_{CMIR}$ | Common-mode input voltage | | 0 | | $V_{DD33A}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | ±0.2 | ±0.8 | mV |
| $V_{IN\_OUT}$ | Voltage range for channel inputs and outputs | For PB0~PB1, PE8~PE9, PE11~PE12, PC2~PC3 pins | | | $V_{IO18}$ | V |
| | | Other OPA input/output channel pins | | | $V_{DDIO}$ | V |
| $I_{LOAD}$ | Drive current | $R_{LOAD}$ = 4kΩ | | | 900 | uA |
| $I_{LOAD\_PGA}$ | PGA mode drive current | | | | 500 | uA |
| $I_{DDOPAMP}$ | Current consumption | No load, static mode | | 200 | | uA |
| CMRR(1) | Common mode rejection ratio | @1kHz | | 96 | | dB |
| PSRR(1) | Power supply rejection ratio | @1kHz | | 82 | | dB |

| | | | | | | |
|---|---|---|---|---|---|---|
| $Av^{(1)}$ | Open loop voltage gain | $C_{LOAD}$ = 5pF | | 110 | | dB |
| $G_{BW}^{(1)}$ | Open loop gain | $C_{LOAD}$ = 5pF | | 16 | | MHz |
| $P_M^{(1)}$ | Unit gain bandwidth | $C_{LOAD}$ = 5pF | | 75 | | ° |
| $S_R^{(1)}$ | Phase margin | $C_{LOAD}$ = 5pF | | 7 | | V/us |
| $t_{WAKUP}^{(1)}$ | Setup time from shutdown to wake up, 0.1% | Input $V_{DD33A}$/2, $C_{LOAD}$ = 50pF, $R_{LOAD}$ = 4kΩ | | | 1 | us |
| $R_{LOAD}$ | Resistive load | | 4 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | 50 | pF |
| $V_{OHSAT}^{(2)}$ | High saturation output voltage | $R_{LOAD}$ = 4kΩ | $V_{DD33A}$ -160 | | | mV |
| | | $R_{LOAD}$ = 20kΩ | $V_{DD33A}$ -35 | | | mV |
| $V_{OLSAT}^{(2)}$ | Low saturation output voltage | $R_{LOAD}$ = 4kΩ | | | 3 | mV |
| | | $R_{LOAD}$ = 4KΩ, pull-up | | | 160 | mV |
| | | $R_{LOAD}$ = 20kΩ | | | 3 | mV |
| | | $R_{LOAD}$ = 20kΩ, pull-up | | | 35 | mV |
| PGA Gain$^{(1)}$ | PGADIFx = 0, in-phase PGA gain error | Gain = 8, $V_{CMIR}$ < ($V_{DD33A}$/7) | -1 | | 1 | % |
| | | Gain = 16, $V_{CMIR}$ < ($V_{DD33A}$/15) | -1 | | 1 | % |
| | | Gain = 32, $V_{CMIR}$ < ($V_{DD33A}$/31) | -1 | | 1 | % |
| | | Gain = 64, $V_{CMIR}$ < ($V_{DD33A}$/63) | -1.5 | | 1.5 | % |
| | PGADIFx = 1, in-phase PGA gain error | Gain = 8 | -2 | | 2 | % |
| | | Gain = 16 | -2 | | 2 | % |
| | | Gain = 32 | -2 | | 2 | % |
| | | Gain = 64 | -2.5 | | 2.5 | % |
| Delta R | Absolute change in resistance | | -15 | | 15 | % |
| $eN^{(1)}$ | Equivalent input voltage noise | $R_{LOAD}$ = 4kΩ@1kHz | | 100 | | nV/ sqrt(Hz) |
| | | $R_{LOAD}$ = 20kΩ@1kHz | | 60 | | |

*Note: 1. Design parameters are guaranteed;*

*2. Load current will limit saturated output voltage.*

Table 3-55-2 OPA characteristics (High-speed mode)

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Supply voltage | Recommended not less than 2V | 1.8 | 3.3 | 3.6 | V |
| $V_{CMIR}$ | Common-mode input voltage | | 0 | | $V_{DD33A}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | ±3 | ±12 | mV |
| $V_{IN\_OUT}$ | Voltage range for | For PB0~PB1, PE8~PE9, | | | $V_{IO18}$ | V |

| | | | | | | |
|---|---|---|---|---|---|---|
| | channel inputs and outputs | PE11~PE12, PC2~PC3 pins | | | | |
| | | Other OPA input/output channel pins | | | $V_{DDIO}$ | V |
| $I_{LOAD}$ | Drive current | $R_{LOAD}$ = 4kΩ | | | 900 | uA |
| $I_{LOAD\_PGA}$ | PGA mode drive current | | | | 500 | uA |
| $I_{DDOPAMP}$ | Current consumption | No load, static mode | | 450 | | uA |
| CMRR(1) | Common mode rejection ratio | @1kHz | | 96 | | dB |
| PSRR(1) | Power supply rejection ratio | @1kHz | | 82 | | dB |
| Av(1) | Open loop voltage gain | $C_{LOAD}$ = 5pF | | 110 | | dB |
| $G_{BW}$(1) | Open loop gain | $C_{LOAD}$ = 5pF | | 28 | | MHz |
| $P_M$(1) | Unit gain bandwidth | $C_{LOAD}$ = 5pF | | 80 | | ° |
| $S_R$(1) | Phase margin | $C_{LOAD}$ = 5pF | | 25 | | V/us |
| $t_{WAKUP}$(1) | Setup time from shutdown to wake up, 0.1% | Input $V_{DD33A}$/2, $C_{LOAD}$ = 50pF, $R_{LOAD}$ = 4kΩ | | | 1 | us |
| $R_{LOAD}$ | Resistive load | | 4 | | | kΩ |
| $C_{LOAD}$ | Capacitive load | | | | 50 | pF |
| $V_{OHSAT}$(2) | High saturation output voltage | $R_{LOAD}$ = 4kΩ | $V_{DD33A}$-160 | | | mV |
| | | $R_{LOAD}$ = 20kΩ | $V_{DD33A}$-35 | | | mV |
| $V_{OLSAT}$(2) | Low saturation output voltage | $R_{LOAD}$ = 4kΩ | | | 3 | mV |
| | | $R_{LOAD}$ = 4KΩ, pull up | | | 160 | mV |
| | | $R_{LOAD}$ = 20kΩ | | | 3 | mV |
| | | $R_{LOAD}$ = 20kΩ, pull up | | | 35 | mV |
| PGA Gain(1) | Internal in-phase PGA gain error | Gain = 8, $V_{CMIR}$ < ($V_{DD33A}$/7) | -1 | | 1 | % |
| | | Gain = 16, $V_{CMIR}$ < ($V_{DD33A}$/15) | -1 | | 1 | % |
| | | Gain = 32, $V_{CMIR}$ < ($V_{DD33A}$/31) | -1 | | 1 | % |
| | | Gain = 64, $V_{CMIR}$ < ($V_{DD33A}$/63) | -1.5 | | 1.5 | % |
| | Differential PGA gain error | Gain = 8 | -2 | | 2 | % |
| | | Gain = 16 | -2 | | 2 | % |
| | | Gain = 32 | -2 | | 2 | % |
| | | Gain = 64 | -2.5 | | 2.5 | % |
| Delta R | Absolute change in resistance | | -15 | | 15 | % |
| eN(1) | Equivalent input voltage noise | $R_{LOAD}$ = 4kΩ@1kHz | | 100 | | nV/ sqrt(Hz) |
| | | $R_{LOAD}$ = 20kΩ@1kHz | | 60 | | |

*Note: 1. Design parameters are guaranteed;*

*2. Load current will limit saturated output voltage.*

### 3.3.34 CMP Characteristics

Table 3-56 CMP characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DD33A}$ | Supply voltage | Recommended not less than 2V | 1.8 | 3.3 | 3.6 | V |
| $V_{CMIR}$ | Common mode input voltage | | 0 | | $V_{DD33A}$ | V |
| $V_{IOFFSET}$ | Input offset voltage | | | ±3 | ±12 | mV |
| $V_{IN\_OUT}$ | Voltage range for channel inputs and outputs | For PB0~PB1 pin | | | $V_{IO18}$ | V |
| | | Other CMP input and output channel pins | | | $V_{DDIO}$ | V |
| $I_{DDOPAMP}$ | Current consumption | | | 40 | | uA |
| $V_{hys}$(1) | Hysteresis voltage | HYPSEL = 00 | | 0 | | mV |
| | | HYPSEL = 01 | | 10 | | |
| | | HYPSEL = 10 | | 20 | | |
| | | HYPSEL = 11 | | 30 | | |
| $t_D$(1) | Comparator delay, $V_{INP}$ from ($V_{INN}$-100mV) to ($V_{INN}$+100mV) change | 0≤ $V_{INN}$ ≤$V_{DD33A}$ | | 20 | | ns |

*Note: 1. Design parameters are guaranteed;*

### 3.3.35 Temperature Sensor Characteristics

Table 3-57 TS characteristics

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $R_{TS}$ | Temperature sensor measuring range | | -40 | | 85 | ℃ |
| $A_{TSC}$ | Measurement errors in temperature sensors | | | ±12 | | ℃ |
| Avg_Slope | Average slope (negative temperature coefficient) | | 3.8 | 4.3 | 4.8 | mV/℃ |
| $V_{25}$ | Voltage at 25°C | | 1.34 | 1.40 | 1.46 | V |
| $T_{S\_temp}$ | ADC sampling time when reading temperature | $f_{ADC}$ = 14MHz | | | 17.1 | us |

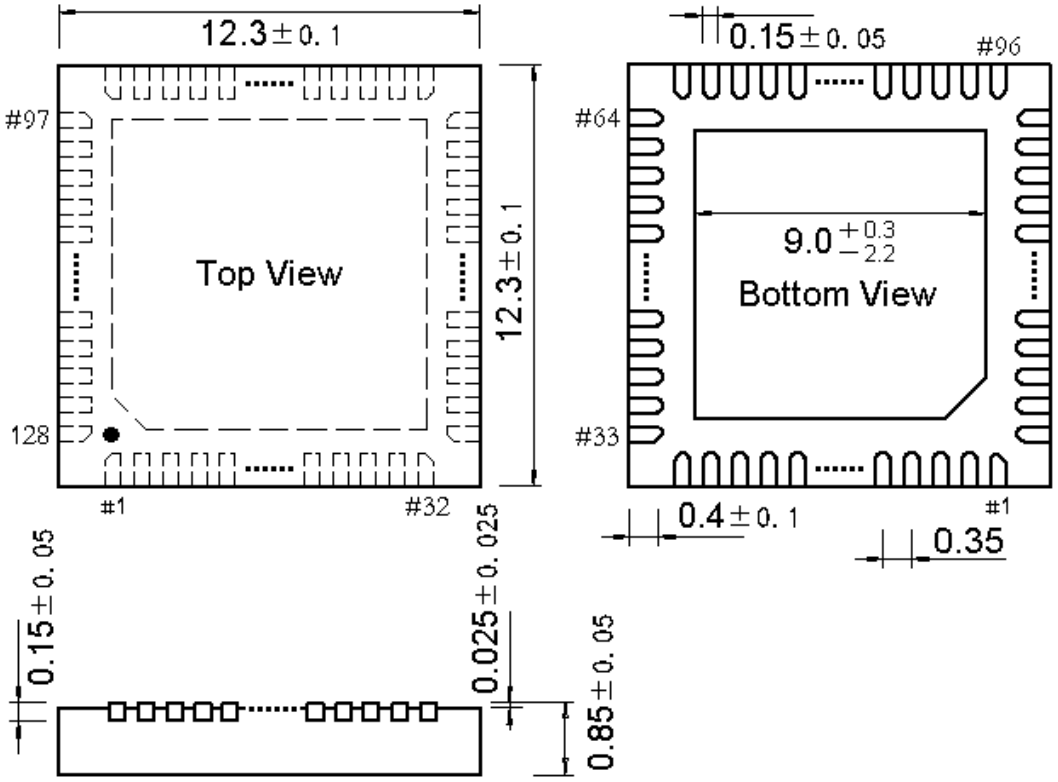
# Chapter 4 Package and Ordering Information

## Packages

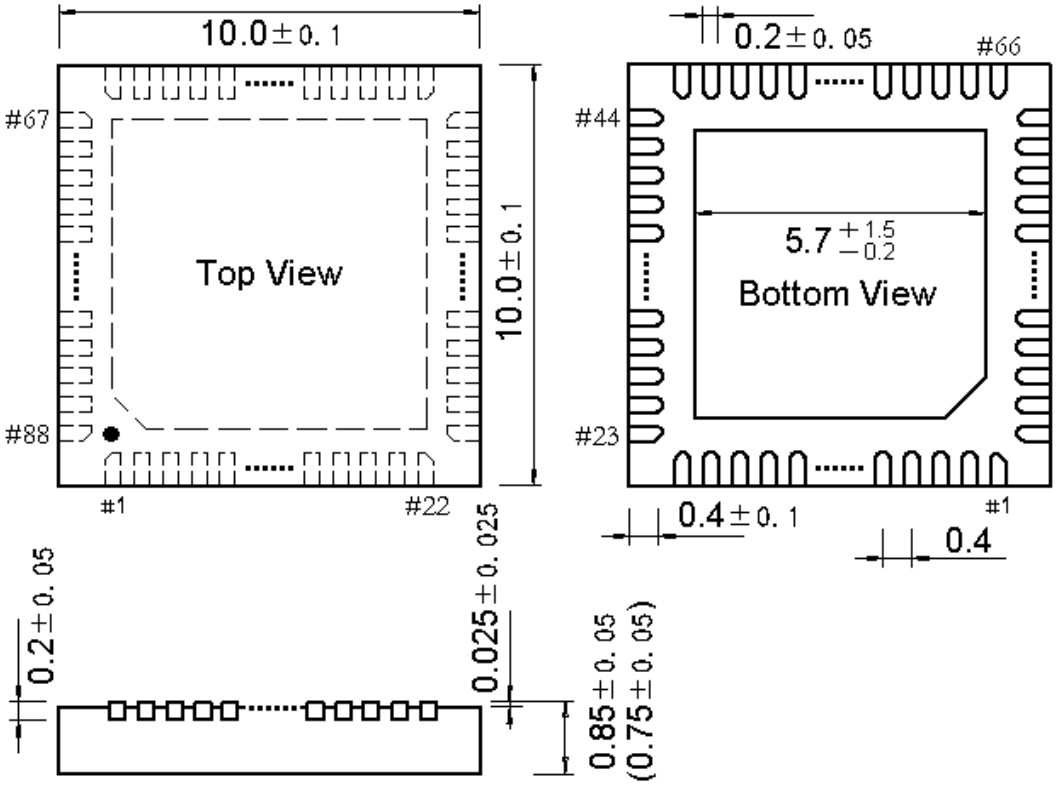
| Package Form | Body Size | Pin Pitch | | Package Description | Order Model |
|---|---|---|---|---|---|
| QFN128 | 12.3*12.3mm | 0.35mm | 13.8mil | Quad Flat No-Lead Package | CH32H417QEU6 |
| QFN88 | 10*10mm | 0.4mm | 15.7mil | Quad Flat No-Lead Package | CH32H417MEU6 |
| QFN68 | 8*8mm | 0.4mm | 15.7mil | Quad Flat No-Lead Package | CH32H417WEU6 |
| QFN60X6 | 6*6mm | 0.35mm | 13.8mil | Quad Flat No-Lead Package | CH32H416RDU6 |
| QFN60X6 | 6*6mm | 0.35mm | 13.8mil | Quad Flat No-Lead Package | CH32H415REU6 |

*Note: All dimensions are in millimeters. The pin center spacing values are nominal values, with no error. Other than that, the dimensional error is not greater than the greater of ±0.2mm or 10%.*

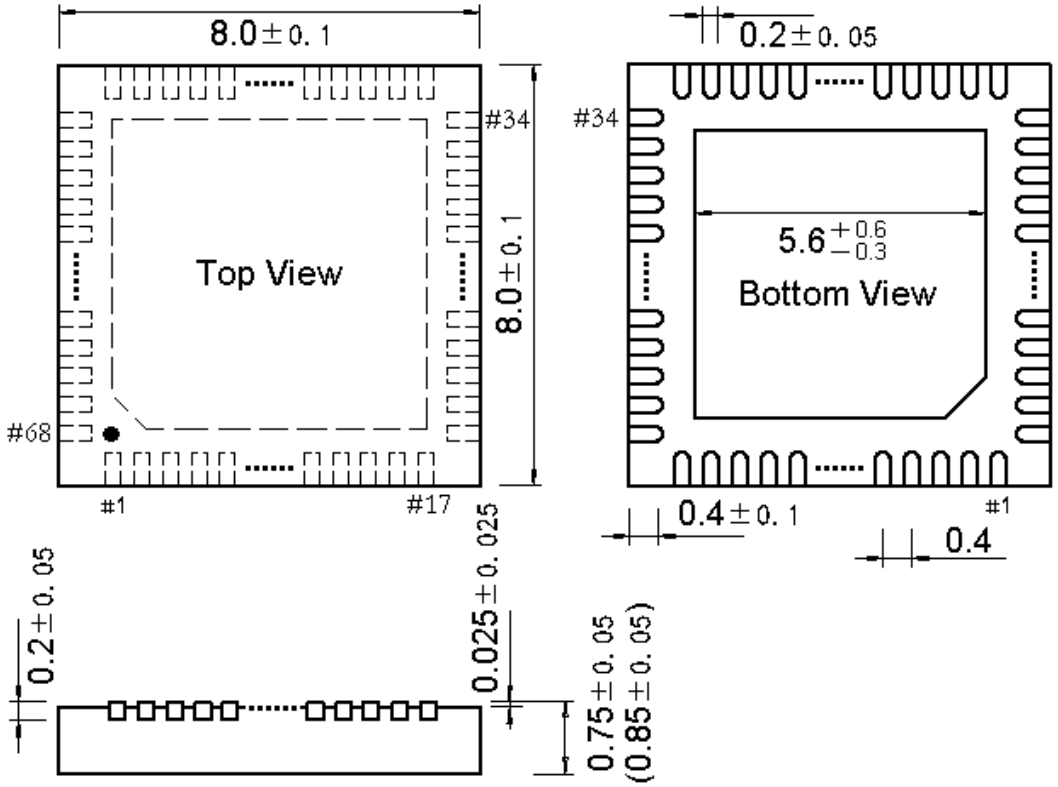
## 4.1 QFN128 package



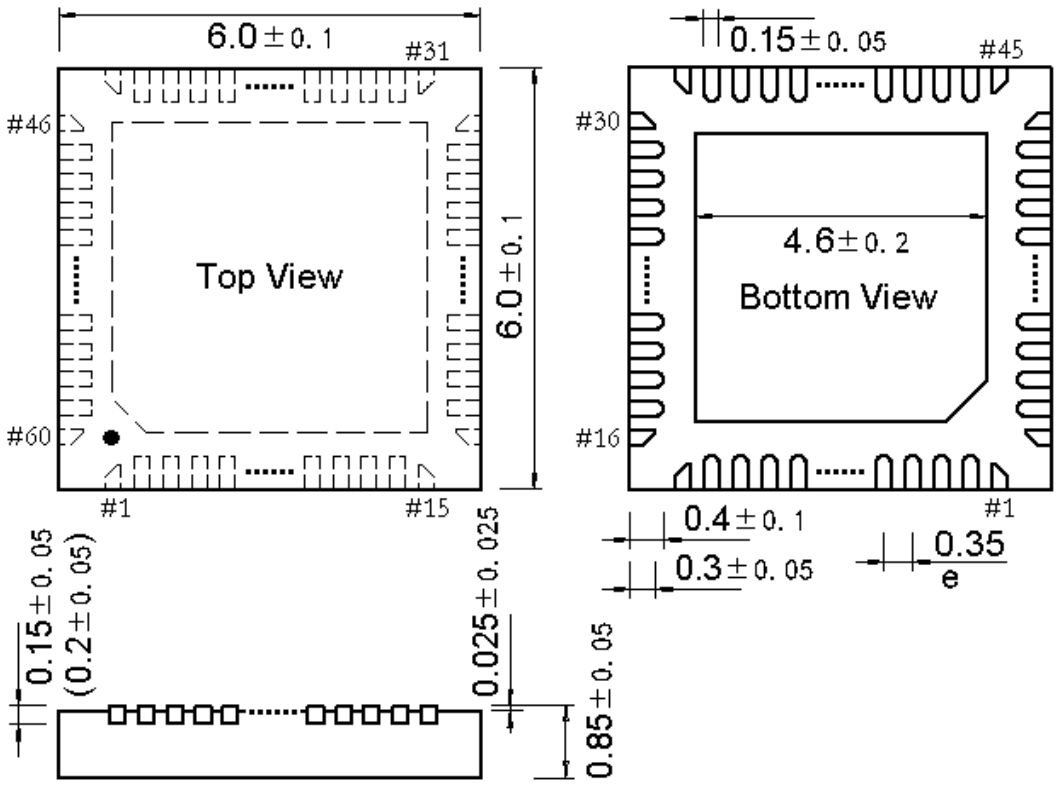
## 4.2 QFN88 package




## 4.3 QFN68 package



## 4.4 QFN60X6 package



# Series Product Naming Rules

Example: CH32 V 303 R 8 T 6

Product Series

F = Arm core, general-purpose MCU
V = QingKe RISC-V core, general-purpose MCU
L = QingKe RISC-V core, low-power MCU
X = QingKe RISC-V core, dedicated or special peripheral MCU
M = QingKe RISC-V core, Built-in gate drive motor MCU
H = QingKe RISC-V core, high-performance MCU

Product type (*)+Product sub-series (**)

| Product type | Product sub-series |
|---|---|
| 0 = Value version, main frequency <=48M | 06 = 64K Flash multi-function general-purpose type, OPA, dual-purpose, TKey<br>07 = Basic motor application type, OPA+CMP |
| 1 = Basic version, main frequency <=100M<br>2 = Enhanced version, main frequency <=200M<br>3 = Hardware floating point, medium and large capacity <480KB | 03 = Connected, USB<br>05 = Connected, USB HS, CAN<br>07 = Interconnected, USB HS, CAN, Ethernet, SDIO, FSMC<br>08 = Wireless, BLE5.x, CAN, USB, Ethernet<br>17 = Interconnected, USB HS, CAN, Ethernet (Built-in PHY), SDIO |
| 4 = Hardware floating point, large capacity >=480KB | 15 = Interconnected, USB HS, HSADC<br>15 = Interconnected, USB HS, HSADC, SDMMC<br>17 = Interconnected, USB SS, SerDes, HSADC, UHSIF, SDIO, DVP, SDMMC, Ethernet (Built-in PHY) |

Pin number

J = 8 pin D = 12 pin A = 16 pin F = 20 pin E = 24 pin
G = 28 pin K = 32 pin T = 36 pin C = 48 pin R = 60&64 pin
W = 68 pin M = 88 pin V = 100 pin Q = 128 pin Z = 144 pin

Flash memory capacity

4 = 16K Flash memory 6 = 32K Flash memory 7 = 48K Flash memory 8 = 64K Flash memory
B = 128K Flash memory C = 256K Flash memory D = 480K Flash memory E = 512K Flash memory

Package

T = LQFP U = QFN R = QSOP P = TSSOP M = SOP

| Temperature range | |
|---|---|
| 6 = -40℃~85℃ | 7 = -40℃~105℃ |
| 3 = -40℃~125℃ | D = -40℃~150℃ |