ARM®-based 32-bit Cortex®-M4F MCU, 256 to 512 KB Flash, sLib, QSPI, SDRAM, 17 timers, 2 ADCs, 23 communication interfaces (3x CAN or CANFD, OTGFS, EMAC)

Features

- **Core: ARM® 32-bit Cortex®-M4F CPU with FPU**
  - 192 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication and hardware division
  - Floating point unit (FPU)
  - DSP instructions
- **Memories**
  - 256 to 512 Kbytes of Flash memory
  - 26 Kbytes of boot memory used as a Bootloader or as a general instruction/data memory (one-time-configurable)
  - 4 Kbytes of OTP memory
  - sLib: configurable part of main Flash as a library area with code executable but secured, non-readable
  - 144 to 108 Kbytes of SRAM (configurable as 128 to 96 KB SRAM with party check)
  - External memory controller (XMC) with 16-bit data bus supporting SRAM, PSRAM, NOR and SDRAM memories
  - QSPI interface for external SPI Flash or SPI RAM extension, supporting address mapping
- **XMC as LCD parallel interface, 8080/6800 modes**
- **Power control (PWC)**
  - 2.4 to 3.6 V supply
  - Power-on reset (POR), low voltage reset (LVR), and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep and Standby modes (woke up via 6 WKUP pins)
  - V_{BAT} supply for LEXT, ERTC and 20x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal oscillator (HEXT)
  - 48 MHz internal factory-trimmed high speed clock (HICK) with ±1% accuracy at T_A= 25 °C and ±2.5% at T_A= -40 °C to +105 °C, with automatic clock calibration (ACC)
  - 32 kHz crystal oscillator (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 2x 12-bit 5.33 MSPS A/D converters, up to 16 external input channels; 12/10/8/6-bit resolution, hardware oversampling up to equivalent 16-bit resolution
  - Temperature sensor (V_{TS}), internal reference voltage (V_{INTRV}), V_{BAT} monitor (V_{BAT}/4)
  - 2x 12-bit D/A converters
- **DMA**
  - 2x 7-channel DMA controllers for flexible mapping
- **Up to 117 fast GPIOs**
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 17 timers (TMR)**
  - 2x 16-bit 8-channel advanced timers, including PWM outputs with dead-time generator and emergency brake
  - Up to 8x 16-bit + 2x 32-bit general-purpose timers, each with up to 4 IC/OC/PWM or pulse counter and incremental encoder input
  - 2x 16-bit basic timers
  - 2x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC with auto-wakeup, alarm, subsecond accuracy, and hardware calendar with calibration feature**
- **Up to 23 communication interfaces**
  - Up to 3x I^2C interfaces (SMBus/PMBus)
  - Up to 8x USART interfaces support master synchronization SPI and modem control, ISO7816 interface, LIN, IrDA, and RS485 driver enable, supporting TX/RX swap
  - Up to 4x SPI interfaces (40 Mbit/s), all with multiplexed half-duplex I^2S, and I^2S2/I^2S3 full-duplex mode
  - 1x separated full-duplex I^2S interface (I^2SF)
  - Up to 3x CAN interfaces, each with dedicated 1408 bytes of buffer (AT32F456/457 support CAN FD protocol)
  - SDIO interface

  - OTGFS full-speed controller with on-chip PHY, dedicated 1280 bytes of buffer, supporting crystal-less in device mode
  - 10/100M Ethernet MAC (EMAC) with dedicated DMA and 4 Kbytes of buffer, IEEE 1588 hardware support, MII/RMII available (for AT32F457 only)
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **AES hardware accelerator supporting 256/192/128-bit key**
- **True random number generator (TRNG)**
- **Debug mode**
  - Serial wire debug (SWD) and serial wire output (SWO)
- **Operating temperature: -40 to +105 °C**
- **Packages**
  - LQFP144 20 x 20 mm
  - LQFP100 14 x 14 mm
  - LQFP64 10 x 10 mm
  - LQFP48 7 x 7 mm
  - QFN48 6 x 6 mm

Table 1. AT32F455 device summary

Flash	Part number
512 Kbytes	AT32F455ZET7, AT32F455VET7, AT32F455RET7, AT32F455CET7, AT32F455CEU7
256 Kbytes	AT32F455ZCT7, AT32F455VCT7, AT32F455RCT7, AT32F455CCT7, AT32F455CCU7

Table 2. AT32F456 device summary

Flash	Part number
512 Kbytes	AT32F456ZET7, AT32F456VET7, AT32F456RET7, AT32F456CET7, AT32F456CEU7
256 Kbytes	AT32F456ZCT7, AT32F456VCT7, AT32F456RCT7, AT32F456CCT7, AT32F456CCU7

Table 3. AT32F457 device summary

Flash	Part number
512 Kbytes	AT32F457ZET7, AT32F457VET7, AT32F457RET7
256 Kbytes	AT32F457ZCT7, AT32F457VCT7, AT32F457RCT7

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1 Descriptions

The AT32F455/456/457 series are based on the high-performance ARM® Cortex®-M4F 32-bit RISC core operating at a frequency of up to 192 MHz. The Cortex®-M4F core features a Floating Point Unit (FPU) single precision supporting all ARM® single-precision data processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) that enhances application security.

The AT32F455/456/457 series incorporate high-speed embedded memories, including up to 512 Kbytes of Flash memory, 128+16 Kbytes of SRAM, and 26 Kbytes of boot memory that can be used as a Bootloader or as a general instruction/data memory (one-time-configurable) to achieve the maximum of 512+26 Kbytes, as well as 4 Kbytes of OTP data storage space. Any block of the embedded Flash memory can be protected by the “sLib” (security library), functioning as a security area with code-executable only. In addition, the AT32F455/456/457 device includes high-level memory extensions: one external memory controller (XMC) (including SDRAM interface) and one quad SPI memory interface (QSPI).

The AT32F455/456/457 series offer two 12-bit ADCs, two 12-bit DACs, ten general-purpose 16-bit timers (including two motor control PWM advanced timers), two general-purpose 32-bit timers, two basic timers, one low-power ERTC, one AES hardware accelerator, and one true random number generator (TRNG). They feature standard and advanced communication interfaces: up to three I^2Cs, four SPIs (multiplexed as I^2S), one full-duplex I^2SF interface, one SDIO, eight USARTs, three CAN or CANFD interfaces, one infrared transmitter, one OTGFS and one Ethernet MAC interface.

The AT32F455/456/457 series operate in the -40 °C to +105 °C temperature range, from a 2.4 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32F455/456/457 offer devices in different package types. They are fully pin-to-pin, software and functionally compatible throughout the AT32F455/456/457 series, except the configurations of peripherals which are not fully identical depending on the package types.

Table 4. AT32F455 features and peripheral counts

Part number		AT32F455xxU7		AT32F455xxT7							
		CC	CE	CC	CE	RC	RE	VC	VE	ZC	ZE
Frequency (MHz)		192									
Flash (KB)		256	512	256	512	256	512	256	512	256	512
SRAM (KB)		96+12	128+16	96+12	128+16	96+12	128+16	96+12	128+16	96+12	128+16
XMC		-		-		1(1)		1(2)		1	
SDRAM		-		-		-		1		1	
Timers	Advanced	2		2		2		2		2	
	32-bit general-purpose	2		2		2		2		2	
	16-bit general-purpose	8		8		8		8		8	
	Basic	2		2		2		2		2	
	SysTick	1		1		1		1		1	
	WDT	1		1		1		1		1	
	WWDT	1		1		1		1		1	
	ERTC	1		1		1		1		1	
Communication interfaces	I^2C	3		3		3		3		3	
	SPI(3)	4		4		4		4		4	
	I^2S(F)(3)	5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)	
	USART	7(4)		7(4)		8		8		8	
	SDIO	1		1		1		1		1	
	OTGFS	1		1		1		1		1	
	CAN2.0	3		3		3		3		3	
	IRTMR	1		1		1		1		1	
Analog	12-bit ADC numbers/ external channels	2									
		10		10		16		16		16	
	12-bit DAC	2									
TRNG		1									
AES		1									
GPIO		39		39		53		85		117	
Operating temperatures		-40 °C to +105 °C									
Packages		QFN48 6 x 6 mm		LQFP48 7 x 7 mm		LQFP64 10 x 10 mm		LQFP100 14 x 14 mm		LQFP144 20 x 20 mm	

(1) For LQFP64 package, XMC supports only 8-bit mode LCD panel.
(2) For LQFP100 package, XMC can be connected to non-multiplexed PSRAM and SRAM, directly or through external latch device. Refer to AN0068 for details. For this package, interrupt lines can not be used for no Port G.
(3) Half-duplex $I^2S1/4$ share the same pin with full-duplex $I^2S2/3$ and SPI. Also there is a separate full-duplex I^2SF5.
(4) For 48-pin packages, USART8 is not available.

Table 5. AT32F456 features and peripheral counts

Part number		AT32F456xxU7		AT32F456xxT7							
		CC	CE	CC	CE	RC	RE	VC	VE	ZC	ZE
Frequency (MHz)		192									
Flash (KB)		256	512	256	512	256	512	256	512	256	512
SRAM (KB)		96+12	128+16	96+12	128+16	96+12	128+16	96+12	128+16	96+12	128+16
XMC		-		-		1(1)		1(2)		1	
SDRAM		-		-		-		1		1	
Timers	Advanced	2		2		2		2		2	
	32-bit general-purpose	2		2		2		2		2	
	16-bit general-purpose	8		8		8		8		8	
	Basic	2		2		2		2		2	
	SysTick	1		1		1		1		1	
	WDT	1		1		1		1		1	
	WWDT	1		1		1		1		1	
	ERTC	1		1		1		1		1	
Communication interfaces	I^2C	3		3		3		3		3	
	SPI(3)	4		4		4		4		4	
	$I^2S(F)$(3)	5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)	
	USART	7(4)		7(4)		8		8		8	
	SDIO	1		1		1		1		1	
	OTGFS	1		1		1		1		1	
	CANFD	3		3		3		3		3	
	IRTMR	1		1		1		1		1	
Analog	12-bit ADC numbers/ external channels	2									
		10		10		16		16		16	
	12-bit DAC	2									
TRNG		1									
AES		1									
GPIO		39		39		53		85		117	
Operating temperatures		-40 °C to +105 °C									
Packages		QFN48 6 x 6 mm		LQFP48 7 x 7 mm		LQFP64 10 x 10 mm		LQFP100 14 x 14 mm		LQFP144 20 x 20 mm	

(1) For LQFP64 package, XMC supports only 8-bit mode LCD panel.
(2) For LQFP100 package, XMC can be connected to non-multiplexed PSRAM and SRAM, directly or through external latch device. Refer to AN0068 for details. For this package, interrupt lines can not be used for no Port G.
(3) Half-duplex $I^2S1/4$ shares the same pin with full-duplex $I^2S2/3$ and SPI. Also there is a separate full-duplex I^2SF5.
(4) For 48-pin packages, USART8 is not available.

Table 6. AT32F457 features and peripheral counts

Part number		AT32F457xxT7					
		RC	RE	VC	VE	ZC	ZE
Frequency (MHz)		192					
Flash (KB)		256	512	256	512	256	512
SRAM (KB)		96+12	128+16	96+12	128+16	96+12	128+16
XMC		1(1)		1(2)		1	
SDRAM		-		1		1	
Timers	Advanced	2		2		2	
	32-bit general-purpose	2		2		2	
	16-bit general-purpose	8		8		8	
	Basic	2		2		2	
	SysTick	1		1		1	
	WDT	1		1		1	
	WWDT	1		1		1	
	ERTC	1		1		1	
Communication interfaces	I^2C	3		3		3	
	SPI(3)	4		4		4	
	$I^2S(F)$(3)	5 (3x full-duplex)		5 (3x full-duplex)		5 (3x full-duplex)	
	USART	8		8		8	
	SDIO	1		1		1	
	OTGFS	1		1		1	
	CANFD	3		3		3	
	Ethernet MAC	1		1		1	
	IRTMR	1		1		1	
Analog	12-bit ADC numbers / external channels	2					
		16		16		16	
	12-bit DA	2					
TRNG		1					
AES		1					
GPIO		53		85		117	
Operating temperatures		-40 °C to +105 °C					
Packages		LQFP64 10 x 10 mm		LQFP100 14 x 14 mm		LQFP144 20 x 20 mm	

(1) For LQFP64 package, XMC supports only 8-bit mode LCD panel.
(2) For LQFP100 package, XMC can be connected to non-multiplexed PSRAM and SRAM, directly or through external latch device. Refer to AN0068 for details. For this package, interrupt lines can not be used for no Port G.
(3) Half-duplex $I^2S1/4$ shares the same pin with full-duplex $I^2S2/3$ and SPI. Also there is a separate full-duplex I^2SF5.

2 Functionality overview

2.1 ARM® Cortex®-M4F

The ARM® Cortex®-M4F processor is the latest generation of ARM® processor for embedded systems. It is a 32-bit RISC processor that features exceptional code efficiency, outstanding computational performance and advanced response to interrupts. The processor supports a set of DSP instructions that enable efficient signal processing and complex algorithm execution. Its single-precision FPU (floating point unit) speeds up floating point calculation while avoiding saturation.

2.2 Memory

2.2.1 Flash memory

Up to 512 Kbytes of embedded Flash is available for storing programs and data. Any part of the embedded Flash memory can be protected by “sLib” (security library), a security area that is code-executable only but non-readable. “sLib” is a mechanism designed to protect the intelligence of solution venders and facilitate the second-level development by customers.

There is another 26-Kbyte boot memory in which the bootloader is stored. If it is not needed, this boot memory can be used as a general instruction/data memory (one-time-configurable) instead. It can be used to achieve the maximum of 512+26 Kbytes of Flash memory.

The 4-Kbyte OTP (one-time programmable) memory is used for storing user data. The content in OTP can be programmed for one time only, but cannot be erased.

There is a User System Data block available for hardware configurations such as access/erase/write protection, watchdog self-enable and SRAM parity check. User System Data allows the independent configuration of Flash memory erase/write and access protection. There are two levels of memory access protection: low-level protection and high-level protection.

2.2.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suited to the applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.2.3 SRAM

The on-chip SRAM can be configured in two different configurations:

- Up to 144 KB SRAM without parity check (default setting)
- Up to 128 KB SRAM with parity check

It is accessible at CPU clock speed with zero wait state.

2.2.4 External memory controller (XMC)

The AT32F455/456/457 series embed an external memory controller (XMC). It has four Chip Select outputs supporting the following devices: SRAM, PSRAM, NOR memory and SDRAM.

Main features:

- 8-bit or 16-bit data bus width
- Read buffer for SDRAM controller
- Write buffer

The XMC can be configured to interface with many graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes.

2.2.5 Quad SPI memory interface (QSPI)

The AT32F455/456/457 series embed a quad SPI memory interface (QSPI). It is a specialized accessing interface to be connected with single, dual, quad SPI Flash memories or SPI RAM. It can operate in indirect mode (all operations are executed with registers), status polling mode or memory-mapped mode. Up to 256 Mbytes of external Flash memory or RAM can be mapped onto the device address space. Byte access, half-word access and word access types are all supported. It also supports XIP operation (execute in place operation). Operation code and frame format are programmable.

2.3 Interrupts

2.3.1 Nested vectored interrupt controller (NVIC)

The AT32F455/456/457 series embed a nested vectored interrupt controller that is able to manage 16 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of Cortex®-M4F. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.3.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly to NVIC, consists of 22 edge-detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connect up to 16 GPIOs.

2.4 Power control (PWC)

2.4.1 Power supply schemes

- V_{DD} = 2.4~3.6 V: power supply for GPIOs and the internal blocks such as voltage regulator (LDO), provided external via V_{DD} pin.
- V_{DDA} = 2.4~3.6 V: power supply for ADC and DAC, provided externally via V_{DDA} pin. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.
- V_{BAT} = 1.62~3.6 V: V_{BAT} pin can supply V_{BAT} domain from the external battery or super capacitor, or from V_{DD} without the external battery or super capacitor. V_{BAT} (through internal power switch) supplies for ERTC, external crystal 32 kHz (LEXT), and battery powered registers (BPR) when V_{DD} is not present.

2.4.2 Reset and power voltage monitoring (POR / LVR / PVM)

The AT32F455/456/457 series have an integrated power-on reset (POR) and low voltage reset (LVR) circuitry. The POR/LVR is always active and allows proper operation starting from 2.4 V. The device remains in reset mode when V_{DD} goes below a specified threshold (V_{LVR}), without the need for an external reset circuit.

These devices embed a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt is generated when V_{DD} drops below the V_{PVM} threshold or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.4.3 Voltage regulator (LDO)

The LDO has three operating modes: normal, low-power, and power down.

- Normal mode: used in Run/Sleep mode or in Deepsleep mode;
- Low-power mode: can be used in Deepsleep mode;
- Power-down mode: used in Standby mode. The regulator LDO output is in high impedance and the kernel circuitry is powered down, and the contents of the registers and SRAM are lost.

This LDO operates always in its normal mode after chip reset.

LDO output voltage is software configurable, including 1.3 V and 1.1 V in addition to default 1.2 V, so as to ensure the best trade-off between good performance and power consumption. For the corresponding maximum clock frequency of different LDO output voltage, refer to *Table 17*. For details about LDO voltage switch and system clock configuration, refer to *AT32F455/456/457 Series Reference Manual*.

2.4.4 Low-power modes

The AT32F455/456/457 series support three low-power modes:

- Sleep mode

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.
- Deepsleep mode

  Deepsleep mode achieves low-power consumption while keeping the content of SRAM and registers. All clocks in the LDO power domain are stopped, disabling the PLL, the HICK clock and the HEXT crystal. The LDO can also be set in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external lines, the PVM output, an ERTC alarm/wakeup/tamper/timestamp event, OTGFS or Ethernet MAC wakeup signal.
- Standby mode

  The Standby mode is used to acquire the lowest power consumption. The internal LDO is switched off so that the entire LDO power domain is powered down. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for ERTC and BPR registers and standby circuitry.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, an effective edge on the WKUPx pin, or an ERTC alarm/wakeup/tamper/timestamp occurs.

Note: The ERTC and the corresponding clock sources are not stopped by entering Deepsleep or Standby mode. WDT depends on the User System Data settings.

2.5 Boot modes

At startup, BOOT0 and BOOT1 pins are used to select one of three boot options:

- Boot from Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in the boot memory. It is used to reprogram the Flash memory through USART1, USART2, USART3, OTGFS1, I²C1, I²C2, I²C3, CAN1, CAN2, SPI1 or SPI2. Of them, OTGFS1 supports crystal-less mode. CAN1 and CAN2 must be used in conjunction with 4, 6, 8, 12, 14.7456, 16, 20, 24 or 25 MHz HEXT oscillator. *Table 7* provides the supporting part numbers and the pin configurations for bootloader.

Individual peripherals supported by bootloader can be enabled or disabled with the User System Data settings. All peripherals are enabled by default.

Table 7. Part numbers and pin configurations for bootloader

Peripherals	Part numbers	Pins
USART1	All	PA9: USART1_TX PA10: USART1_RX
USART2	AT32F455ZxT7, AT32F455VxT7 AT32F456ZxT7, AT32F456VxT7 AT32F457ZxT7, AT32F457VxT7	PD5: USART2_TX PD6: USART2_RX
	Others	PA2: USART2_TX PA3: USART2_RX
USART3	AT32F455ZxT7, AT32F455VxT7, AT32F455RxT7 AT32F456ZxT7, AT32F456VxT7, AT32F456RxT7 AT32F457ZxT7, AT32F457VxT7, AT32F457RxT7	PC10: USART3_TX PC11: USART3_RX or PB10: USART3_TX PB11: USART3_RX
	Others	PB10: USART3_TX PB11: USART3_RX
OTGFS1	All	PA11: OTGFS1_D- PA12: OTGFS1_D+
I²C1	All	PB6: I2C1_SCL PB7: I2C1_SDA
I²C2	All	PB10: I2C2_SCL PB3: I2C2_SDA
I²C3	All	PA8: I2C3_SCL PB4: I2C3_SDA
CAN1	AT32F455ZxT7, AT32F455VxT7 AT32F456ZxT7, AT32F456VxT7 AT32F457ZxT7, AT32F457VxT7	PD0: CAN1_RX PD1: CAN1_TX
	Others	PB8: CAN1_RX PB9: CAN1_TX

Peripherals	Part numbers	Pins
CAN2	All	PB5: CAN2_RX PB13: CAN2_TX
SPI1	All	PA4: SPI1_CS PA5: SPI1_SCK PA6: SPI1_MISO PA7: SPI1_MOSI
SPI2	AT32F455ZxT7, AT32F455VxT7, AT32F455RxT7 AT32F457ZxT7, AT32F457VxT7, AT32F457RxT7	PB12: SPI2_CS PC7: SPI2_SCK PC2: SPI2_MISO PC3: SPI2_MOSI

2.6 Clocks

The internal 48 MHz clock (HICK) divided by 6 (that is 8 MHz) is selected as the default CPU clock after any reset. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If a failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are available to allow the configuration of the AHB and the APB (APB1, APB2 and APB3) frequency. The maximum frequency of AHB, APB1 and APB2 domains is 192 MHz, and APB3 90 MHz.

In addition, the AT32F455/456/457 series embed an automatic clock calibration (ACC) block, which calibrates the internal 48 MHz HICK, assuring the most precise accuracy of the HICK in the full range of the operating temperatures.

2.7 General-purpose inputs / outputs (GPIOs)

Each of the GPIO pins is in analog mode at reset, by default. After reset, each of them can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), input (floating with or without pull-up or pull-down) or as multiplexed functions. Most of the GPIO pins are shared with digital or analog multiplexed functions. All GPIOs are high current-capable.

The GPIO’s configuration can be locked, if needed, in order to avoid false writing to the GPIO’s registers by following a specific sequence.

2.8 Direct Memory Access Controller (DMA)

AT32F455/456/457 series feature two general-purpose 7-channel DMA controllers DMA1 and DMA2 providing totally 14 channels. They are able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers. These DMA channels can be connected to peripherals with flexible mapping ability.

DMA controllers support circular buffer management, removing the need for user code intervention when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software, and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals: SPI/I²S, I²SF, I²C, USART, all timers (TMR), ADC, DAC, SDIO, QSPI and AES.

2.9 Timers (TMR)

The AT32F455/456/457 series include two advanced timers, up to ten general-purpose timers, two basic timers and one SysTick timer.

The table below compares the features of the advanced, general-purpose and basic timers.

Table 8. Timer feature comparison

Type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary output
Advanced	TMR1 TMR8	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	4
General-purpose	TMR2 TMR5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR3 TMR4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR9 TMR12	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	2	2
	TMR10 TMR11 TMR13 TMR14	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	1	1
Basic	TMR6 TMR7	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.9.1 Advanced timers (TMR1 and TMR8)

These two advanced timers (TMR1 and TMR8) can be seen as four-phase PWM multiplexed on 8 channels. They have complementary PWM outputs with programmable dead-time insertion. They can also be considered as complete general-purpose timers. Their four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-period mode output

If configured as standard 16-bit timers, they have the same features as those of the TMRx timer. If configured as a 16-bit PWM generator, it boasts full modulation capability (0 to 100%).

In debug mode, the advanced timer counter can be frozen, and the PWM outputs are disabled to turn off any power switch driven by these outputs.

Many features are identical with those of the general-purpose TMRs that have the same architecture. Thus, the advanced timer can work together with the general-purpose TMR timers via the link feature for synchronization or event chaining.

2.9.2 General-purpose timers (TMR2~5 and TMR9~14)

Up to ten synchronizable general-purpose timers are available in the AT32F455/456/457 series.

- **TMR2, TMR3, TMR4 and TMR5**

  TMR2 and TMR5 timers are based on a 32-bit auto-reload upcounter/downcounter and a 16-bit prescaler. TMR3 and TMR4 timers are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They can offer up to four independent channels on the large-size packages. Each channel can be used for input capture/output compare, PWM or one-period mode output.

  These general-purpose timers can work with the advanced timers via the link feature for synchronization or event chaining. In debug mode, counter can be frozen. Any of these general-purpose timers can be used to generate PWM output. Each timer has its individual DMA request mechanism. They are capable of handling incremental encoder signals and 1 to 3 digital outputs coming from hall-effect sensors.

- **TMR9 and TMR12**

  TMR9 and TMR12 are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They both feature two independent channels and two complementary channels for input capture/output compare, PWM, or one-period mode output. They can be synchronized with the full-featured general-purpose timers. They can also be used as simple time bases. In debug mode, counter can be frozen. These timers have their separate DMA request generation.

- **TMR10, TMR11, TMR13 and TMR14**

  These timers are based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. They all feature one independent channel and one complementary channel for input capture/output compare, PWM, or one-period mode output. They can be synchronized with the full-featured general-purpose timers. They can also be used as simple time bases. In debug mode, counter can be frozen. These timers have their separate DMA request generation.

2.9.3 Basic timers (TMR6 and TMR7)

Both timers are mainly used to generate DAC trigger signals, and they can also be used as generic 16-bit time base.

2.9.4 SysTick timer

This timer is dedicated to real-time operating systems, but it could also be used as a standard downcounter. Its features include:

- A 24-bit downcounter
- Auto-reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock sources (HCLK or HCLK/8)

2.10 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when an error occurs, or as a free running timer for application timeout management. It is self-enabled or not through the User System Data. The counter can be frozen in debug mode.

2.11 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when an error occurs. It is clocked by the main clock and works as an early warning interrupt feature. The counter can be frozen in debug mode.

2.12 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- 20x 32-bit battery powered registers (BPRs)

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- Support sub-seconds value in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.
- Programmable alarms and periodic interrupts wakeup from Deepsleep or Standby mode.
- Calibrate 1~32767 ERTC clock pulses during running, which can be used for ERTC synchronization with the main clock.
- Digital calibration circuit has 1 ppm resolution to compensate for the inaccuracy of quartz crystal.
- Anti-tamper detection pin has a programmable filter; MCU wakes up from Deepsleep or Standby mode when a tamper event is detected.
- Timestamp function can be used for storing calendar contents. It is triggered by an event on the timestamp pin or a tamper event. MCU wakes up from Deepsleep or Standby mode when a timestamp event is detected.
- Reference clock detection: the more accurate second clock source (50 or 60 Hz) can be used to improve calendar accuracy.

These two alarm registers are used to generate an alarm at a specific time whereas the calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours. Other 32-bit registers also feature programmable sub-second, second, minute, hour, week day and date.

A prescaler is used as a time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 80 bytes of user application data. Battery powered registers are not reset by a system or power reset, nor when the device is woken up from the Standby mode.

ERTC and BPR are powered through power switch. When V_{DD} exists, the switch selects V_{DD} as power supply, or V_{BAT} is used as supply source.

2.13 Communication interfaces

2.13.1 Serial peripheral interface (SPI)

Up to four SPIs are able to communicate at up to 40 Mbit/s in slave and master modes in full-duplex and half-duplex modes. The prescaler gives multiple master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD/MMC/SDHC card modes. All SPIs can be served by the DMA controllers.

The SPI interface can be configured in TI mode for communications in master and slave modes.

2.13.2 Half-duplex and full-duplex inter-integrated sound (I^2S / I^2SF)

Up to four standard I^2S interfaces (multiplexed with SPI) are available, which can be operated in master or slave mode in half-duplex mode. Of them, I^2S2 and I^2S3 also allows full-duplex communication mode. These interfaces can be configured to operate with 16/24/32-bit resolution, as input or output channels. Audio sampling frequencies ranging from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is configured in master mode, the master clock can be output at 256 times the sampling frequency. All I^2S interfaces can be served by the DMA controllers.

In addition, the AT32F455/456/457 series include a separate full-duplex I^2S interface (I^2SF), which can work half- or full-duplex in master or slave mode. It can be configured to operate with 16/24/32-bit resolution, as input or output channels. When I^2SF interface is configured in master mode, the master clock can be output at 256 times the sampling frequency.

The main input clock source of I^2SF interface can be system clock, PLL output clock, 48 MHz HICK or external input clock. More precise audio frequency can be achieved by setting the main input clock of I^2SF interface.

2.13.3 Universal synchronous / asynchronous receiver transmitter (USART)

The AT32F455/456/457 series embed eight universal synchronous/asynchronous receiver transmitters (USART1~8).

These eight interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, LIN Master/Slave capability, hardware management of the CTS and RTS signals, RS485 driver enable signal, Smart Card mode (ISO7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controllers.

These eight interfaces are able to communicate at a speed of up to 12 Mbit/s.

Table 9. USART feature comparison

USART feature	USART1/2/3/4/6	USART5/7/8
Modem with hardware flow control	Yes	RTS only
Continuous communication using DMA	Yes	Yes
Multiprocessor communication	Yes	Yes
Synchronous mode	Yes	Yes
Smart card mode	Yes	Yes
Single-wire half-duplex communication	Yes	Yes
IrDA SIR	Yes	Yes
LIN mode	Yes	Yes
TX/RX swap	Yes	Yes
RS-485 driver enable	Yes	Yes

2.13.4 Inter-integrated-circuit interface (I^2C)

Up to three I^2C bus interfaces can operate in multi-master and slave modes. They can support standard mode (max.100 kHz), fast mode (max. 400 kHz) and fast mode plus (max. 1 MHz). Some GPIOs can support ultra-high sink current of 20 mA.

They feature 7-bit/10-bit addressing mode and 7-bit dual addressing mode (as slave) and embed a hardware CRC generation/verification.

They can be served by DMA controllers and they support SMBus 2.0/PMBus.

2.13.5 Secure digital input / output interface (SDIO)

An SD/SDIO/MMC host interface is available, supporting MultiMediaCard System Specification Version 4.2 in three of different data bus width: 1-bit (default), 4-bit and 8-bit. The interface allows data transfer at up to 48 MHz in 8-bit mode, and is compliant with SD Memory Card Specifications Version 2.0.

The SDIO Card Specification Version 2.0 supports two of different data bus width: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time but several cards of MMC4.1 or previous versions.

Apart from SD/SDIO/MMC/eMMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

2.13.6 Controller area network (CAN)

There are up to three CAN interfaces that are compliant with the 2.0A and 2.0B (active) specifications with a bit rate up to 1 Mbit/s. In particular, the AT32F456/457 series support the CAN FD protocol V1.0. Each of them can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers, having two transmit buffers (one primary transmit buffer and one secondary transmit buffer with three stages), one receive buffer with six stages, and sixteen programmable receive filters. Each CAN also has dedicated 1408 bytes of buffer, which is not shared with any other CAN or peripherals.

To guarantee CAN transmission quality, the CAN protocol states that its clock source must come from the HEXT-based PLL clock.

2.13.7 Universal serial bus On-The-Go full-speed (OTGFS)

The AT32F455/456/457 series embed an OTG full-speed (12 Mb/s) device/host peripheral with integrated transceivers (PHY). It has software-configurable endpoint settings and supports suspend/resume. The OTGFS controller requires a dedicated 48 MHz clock. In host mode, this clock should be PLL clocked by HEXT crystal, and only in device mode, the 48 MHz HICK can be selected as the source of this clock directly.

OTGFS has the main features such as:

- Dedicated 1280 bytes of buffer (not shared with any other peripherals)
- 8 IN + 8 OUT endpoints (including endpoint 0, device mode)
- 16 channels (host mode)
- SOF and OE output
- In accordance with the USB 2.0 Specification, the supported transfer speeds are:
  - Host mode: full-speed and low-speed
  - Device mode: full-speed

2.13.8 Ethernet MAC interface (EMAC)

This peripheral is available only on AT32F457 series.

The AT32F457 series provide an IEEE-802.3-2002-compliant media access controller (MAC) for Ethernet LAN communications through an industry-standard media-independent interface (MII) or a reduced media-independent interface (RMII). The AT32F457 series requires an external physical interface device (PHY) to be connected to the physical LAN bus (twisted-pair, fiber, etc.). The PHY is connected to the AT32F457 EMAC port using as many as 17 signals (MII) or 9 signals (RMII).

The EMAC has the following features:

- Supports 10 and 100 Mbit/s rates
- Dedicated DMA controller enabling high-speed transfers between dedicated buffer and descriptors
- Supports tagged MAC frame (VLAN support)
- Half-duplex (CSMA/CD) and full-duplex operations
- Supports MAC control sublayer (control frames)
- 32-bit CRC generation and removal
- Multiple address filtering modes for physical and multicast address (multicast and group addresses)
- 32-bit status code for each transmitted or received frame
- Internal buffer for transmitted and received frames. The transmit buffer and the receive buffer are both 2 Kbytes, that is, 4 Kbytes in total
- Supports hardware PTP (precision time protocol) in line with IEEE 1588 with the timestamp comparator connected to the TMR2 trigger input
- Interrupt trigger when system time becomes greater than the target time

2.13.9 Infrared transmitter (IRTMR)

The AT32F455/456/457 series provide an infrared transmitter. The infrared transmitter solution is based on the internal connection between TMR10, USART1, or USART2 and TMR11. The TMR11 is used to provide carrier frequency, while TMR10, USART1 or USART2 provides the main signal to be sent. Infrared output signals are available on PB9 or PA13.

To generate infrared remote control signals, TMR10 channel 1 and TMR11 channel 1 must be correctly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

2.14 Advanced-encryption-standard (AES) hardware accelerator

The AT32F455/456/457 series embed an advanced-encryption-standard (AES) hardware accelerator that is compliant with the Federal Information Processing Standards (FIPS) publication 197 specifications issued by the American National Institute of Standards and Technology (NIST). It supports 256-bit, 192-bit or 128-bit key length. It provides several operating modes:

- Electronic codebook (ECB) mode
- Cipher block chaining (CBC) mode
- Counter (CTR) mode
- Galois counter mode (GCM) and Galois message authentication code (GMAC) mode based on GCM
- Counter with CBC-MAC (CCM) mode

The AES unit can be supported by DMA with two channels, one for incoming data, and one for outgoing data.

2.15 True random number generator (TRNG)

The AT32F455/456/457 series embed a true random number generator (TRNG) which is compliant with the American National Institute of Standards and Technology (NIST) SP800-90B specifications. The TRNG produces four 32-bit random numbers every operating cycle. It embeds a mechanism for health check during initial state, running state and under specific circumstances, and these health test results are indicated by error flag bits and interrupt signals.

2.16 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word using a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.17 Analog-to-digital converter (ADC)

Two 12-bit analog-to-digital converters (ADC) are embedded in AT32F455/456/457 series, with the main features below:

- Configurable 12-bit, 10-bit, 8-bit, 6-bit resolution with self-calibration
- 5.33 MSPS maximum conversion rate in 12-bit resolution. Conversion time can be shorten through the reduction of resolution
- Share up to 16 external channels, including 6 fast channels

- Three internal channels dedicated to internal temperature sensor (V_{TS}), internal reference voltage (V_{INTRV}) and V_{BAT} monitor ($V_{BAT}/4$)
- Channel-by-channel programmable sampling time
- 2 to 256 times hardware oversampling, maximum 16-bit resolution equivalent
- Trigger option for both regular and preempted conversions:
  - By software
  - By polarity-configurable hardware (internal timer event or GPIO input event)
- Conversion modes:
  - Single mode or sequential mode
  - In sequential mode, each trigger performs conversions on a selected group of channels
  - Repeated mode converts the selected channels continuously
  - Partition mode
- Support synchronous mode or shift mode between ADCs
- A voltage monitor feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds
- Both ADCs can be served by the DMA controllers

2.17.1 Temperature sensor (V_{TS})

The temperature sensor generates a voltage V_{TS} that varies linearly with temperature. The temperature sensor is internally connected to the ADC1_IN16 input channel, which is used to convert the sensor output voltage into a digital value.

The offset of this line varies from chip to chip due to process variation. The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.

2.17.2 Internal reference voltage (V_{INTRV})

The internal reference voltage (V_{INTRV}) provides a stable voltage source for ADC. The V_{INTRV} is internally connected to the ADC1_IN17 input channel.

2.17.3 V_{BAT} monitor ($V_{BAT}/4$)

This embedded hardware uses internal ADC1_IN18 channel to measure V_{BAT} voltage. As the V_{BAT} voltage may be higher than V_{REF+} or V_{DDA} to be outside the ADC input range, the V_{BAT} is internally connected to a divided-by-4 bridge. The converted value is 1/4 of the V_{BAT} voltage.

2.18 Digital-to-analog converter (DAC)

The two 12-bit buffered DACs can be used to convert two digital signals into two analog voltage signal outputs.

This DAC has the following features:

- Two DAC converters: one for each output channel
- 8-bit or 12-bit monotonic output
- Left- or right-aligned data in 12-bit mode
- Synchronized update capability
- Noise-wave generation
- Triangular-wave generation
- Dual DAC channel independent or simultaneous conversions
- DMA capability for each DAC channel
- External triggers for conversion
- Input voltage reference V_{REF+}

Multiple DAC trigger inputs are used in the AT32F455/456/457. DAC outputs can be triggered through the timer update outputs that are also connected to different DMA channels.

2.19 Serial wire debug (SWD)/Serial wire output (SWO)

The ARM® SWD interface is embedded in the AT32F455/456/457 series. It is a serial wire debug port that can be connected to the target for programming and debug purposes. In addition, the SWO feature is available for asynchronous tracing in debug mode.

3 Pin functional definitions

Figure 1. AT32F455/456/457 LQFP144 pinout

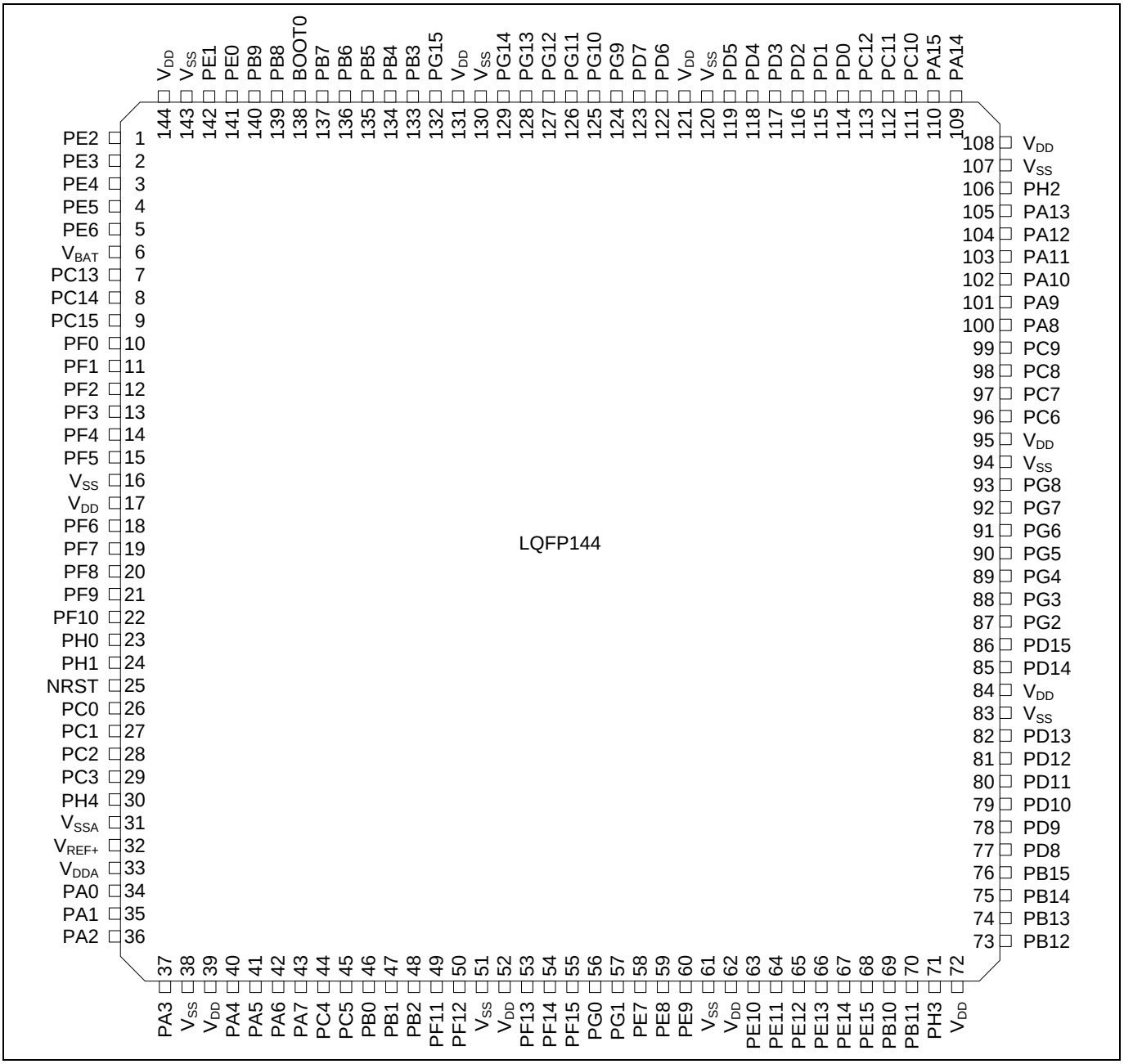


Figure 2. AT32F455/456/457 LQFP100 pinout

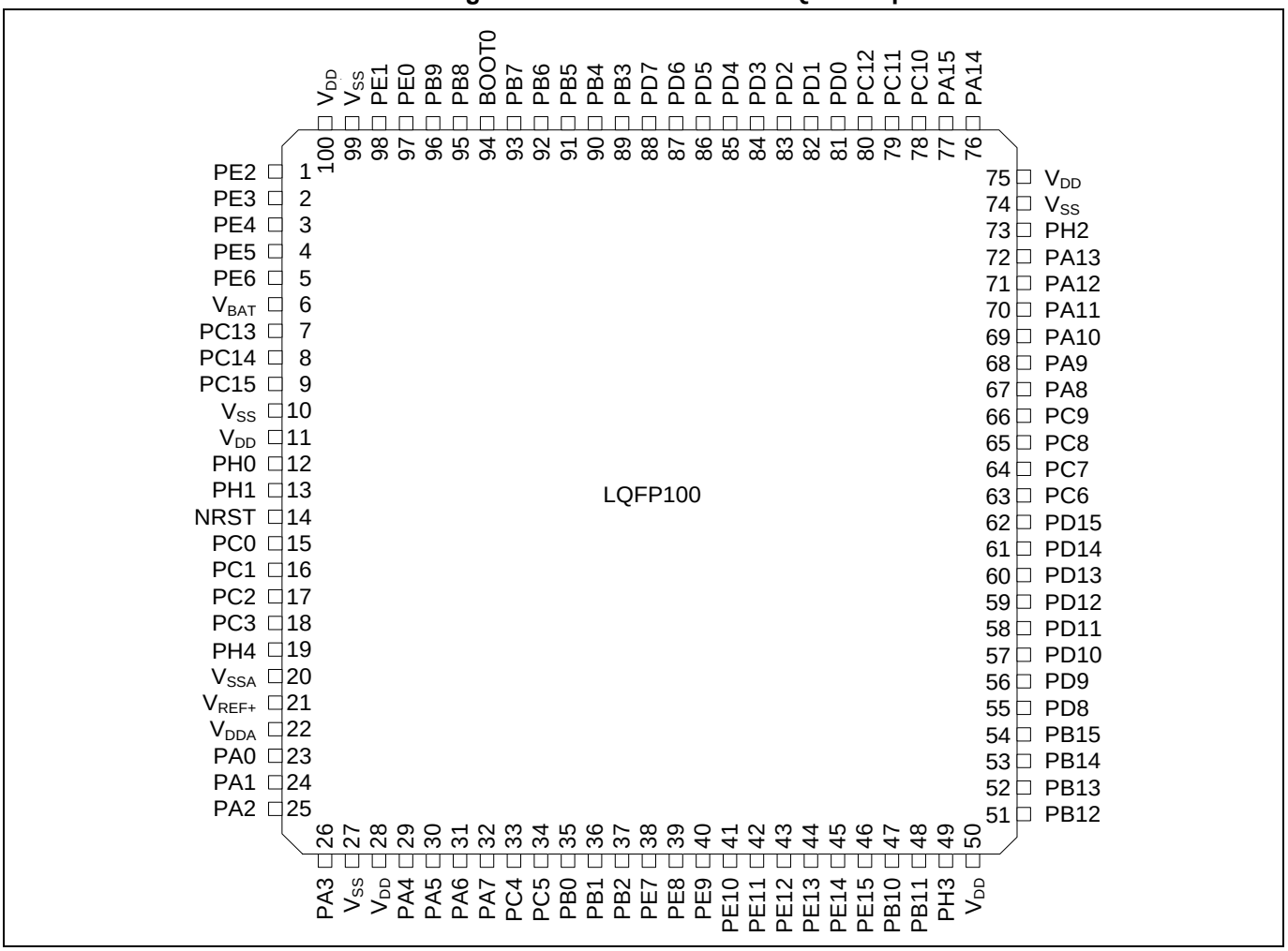


Figure 3. AT32F455/456/457 LQFP64 pinout

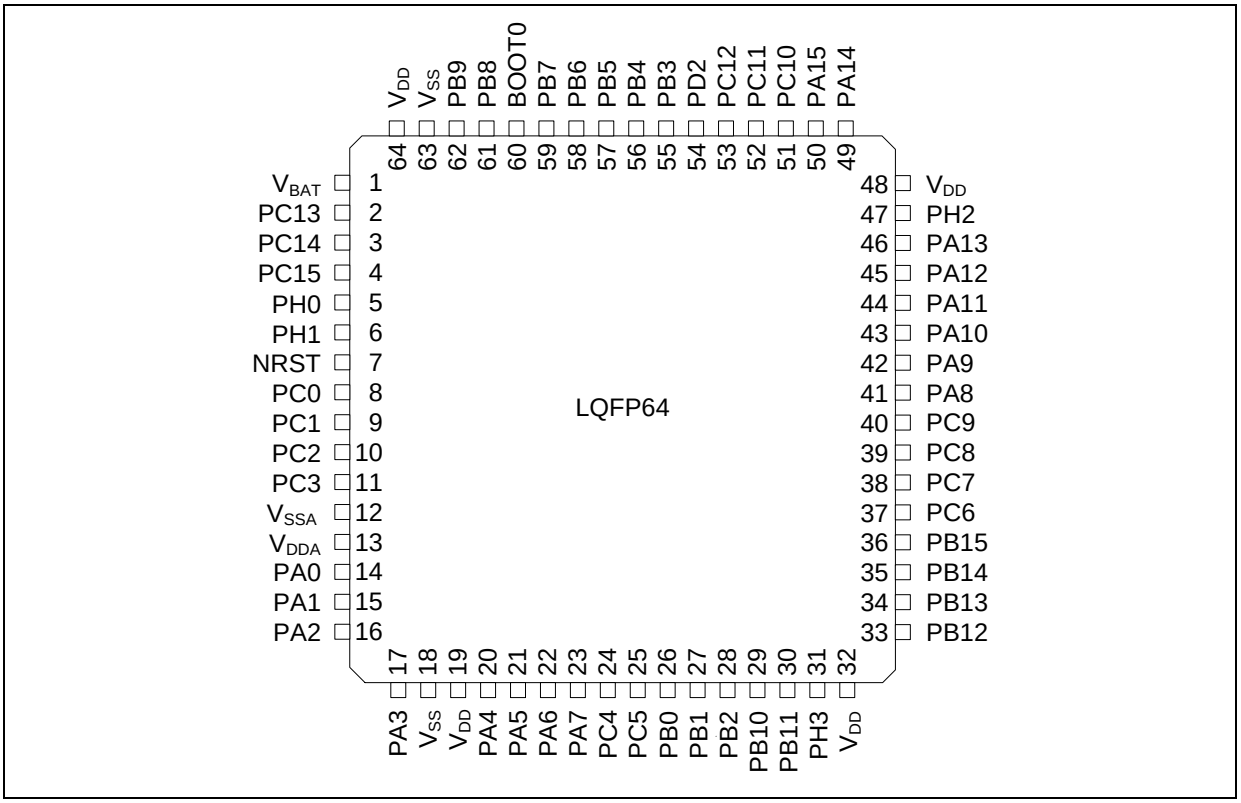


Figure 4. AT32F455/456 LQFP48 pinout

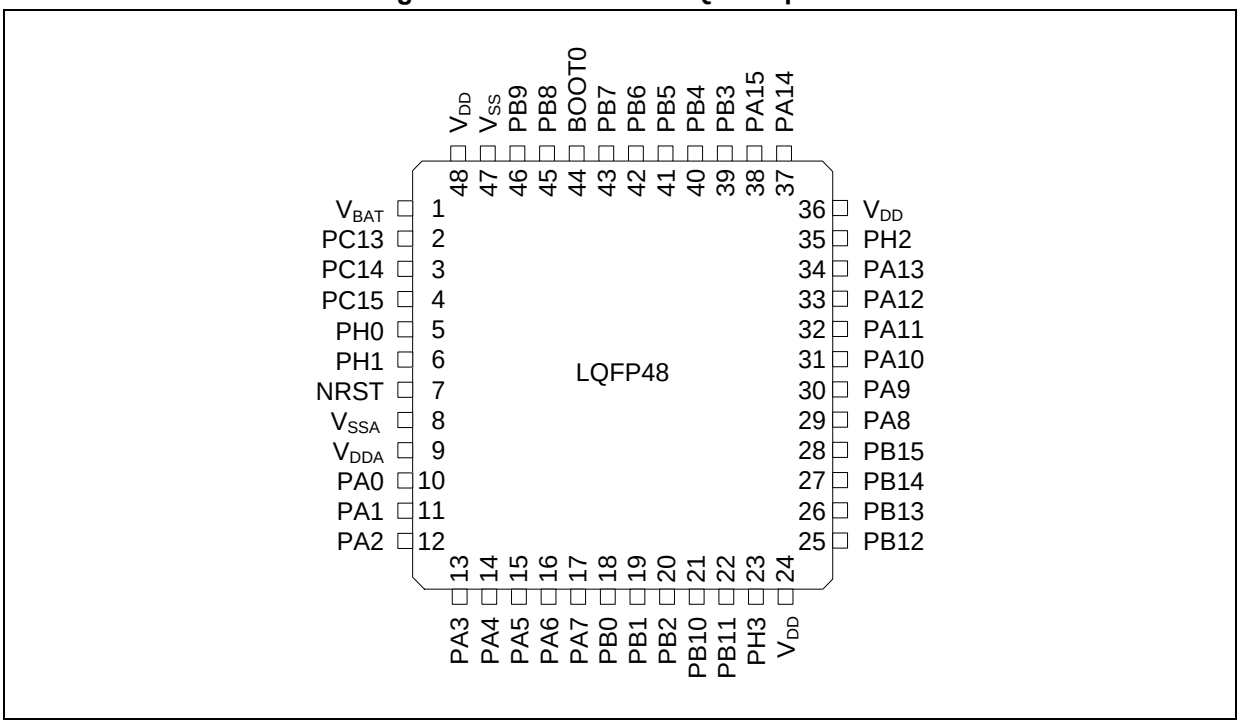
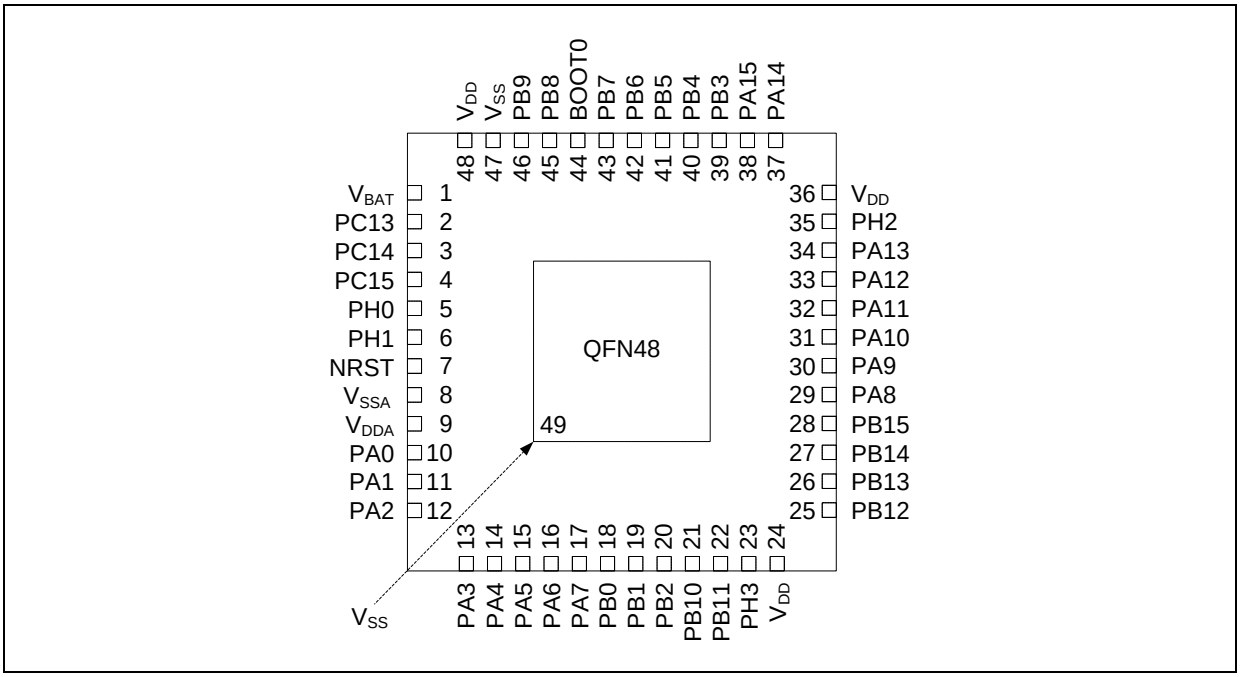


Figure 5. AT32F455/456 QFN48 pinout



The table below is the pin definition of the AT32F455/456/457 series. “-” represents that there is no such pinout on the related package. Unless descriptions in () under pin name, the functions during reset and after reset are the same as those of the actual pin name. Unless otherwise specified, all GPIOs are set as analog mode during reset and after reset. Pin multiplexed functions are selected through GPIOx_MUXx registers and the additional functions are directly selected/enabled through peripheral registers.

Table 10. AT32F455/456/457 series pin definitions

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
-	-	1	1	PE2	I/O	FT	TMR3_EXT / TMR9_BRK / SPI4_SCK / I2S4_CK / QSPI1_IO2 / XMC_SDNCAS / EMAC_MII_TXD3 / XMC_A23 / TMR14_CH1C	-
-	-	2	2	PE3	I/O	FT	TMR3_CH1 / TMR9_CH2C / TMR14_BRK / XMC_A19	-
-	-	3	3	PE4	I/O	FT	CLKOUT / TMR3_CH2 / TMR9_CH1C / SPI4_CS / I2S4_WS / XMC_A20	-
-	-	4	4	PE5	I/O	FT	TMR3_CH3 / TMR9_CH1 / SPI4_MISO / XMC_A21	-
-	-	5	5	PE6	I/O	FT	TMR3_CH4 / TMR9_CH2 / SPI4_MOSI / I2S4_SD / XMC_SDNRAS / XMC_A22	-
1	1	6	6	V_{BAT}	S	-	Battery power supply	
2	2	7	7	PC13(4)(5)	I/O	FT	TMR8_CH4C	ERTC_MUX1 / WKUP2
3	3	8	8	PC14(4)(5)	I/O	TC	-	LEXT_IN
4	4	9	9	PC15(4)(5)	I/O	TC	-	LEXT_OUT
-	-	-	10	PF0	I/O	FT	I2C2_SDA / XMC_A0	-
-	-	-	11	PF1	I/O	FT	I2C2_SCL / XMC_A1	-
-	-	-	12	PF2	I/O	FT	I2C2_SMBA / XMC_A2	-
-	-	-	13	PF3	I/O	FTa	XMC_A3	-
-	-	-	14	PF4	I/O	FTa	XMC_A4	-
-	-	-	15	PF5	I/O	FTa	CAN3_STB / XMC_A5	-
-	-	10	16	V_{SS}	S	-	Digital ground	
-	-	11	17	V_{DD}	S	-	Digital power supply	
-	-	-	18	PF6	I/O	FTa	TMR10_CH1 / USART7_RX / QSPI1_IO3 / CAN3_RX	-
-	-	-	19	PF7	I/O	FTa	TMR11_CH1 / USART7_TX / QSPI1_IO2 / CAN3_TX	-
-	-	-	20	PF8	I/O	FTa	USART8_RX / TMR13_CH1 / QSPI1_IO0	-
-	-	-	21	PF9	I/O	FTa	USART8_TX / TMR14_CH1 / QSPI1_IO1	-
-	-	-	22	PF10	I/O	FTa	TMR1_EXT / TMR5_CH4 / QSPI1_SCK	-
5	5	12	23	PH0	I/O	TC	TMR1_CH1 / I2C1_SDA	HEXT_IN
6	6	13	24	PH1	I/O	TC	TMR1_CH2C / I2C1_SCL / SPI2_CS / I2S2_WS	HEXT_OUT

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
7	7	14	25	NRST	I/O	R	Device reset input/internal reset output (active low)	
-	8	15	26	PC0	I/O	FTa	I2C3_SCL / I2C1_SCL / USART6_TX / USART7_TX / XMC_SDNWE	ADC12_IN10(6)
-	9	16	27	PC1	I/O	FTa	I2C3_SDA / SPI3_MOSI / I2S3_SD / I2C1_SDA / SPI2_MOSI / I2S2_SD / USART6_RX / USART7_RX / EMAC_MDC	ADC12_IN11(6)
-	10	17	28	PC2	I/O	FTa	SPI2_MISO / I2S2_SDEXT / USART8_TX / EMAC_MII_TXD2 / XMC_SDCS0 / XMC_NWE	ADC12_IN12(6)
-	11	18	29	PC3	I/O	FTa	SPI2_MOSI / I2S2_SD / USART8_RX / EMAC_MII_TX_CLK / XMC_SDCKE0 / XMC_A0	ADC12_IN13(6)
-	-	19	30	PH4	I/O	FT	SPI2_SCK / I2S2_CK / USART7_CK_RTS_DE	-
8	12	20	31	V_{SSA}	S	-	Analog ground	
-	-	21	32	V_{REF+}	S	-	Positive reference voltage	
9	13	22	33	V_{DDA}	S	-	Analog power supply	
10	14	23	34	PA0	I/O	FTa	TMR2_CH1 / TMR2_EXT / TMR5_CH1 / TMR8_EXT / I2C2_SCL / USART2_RX / USART2_CTS / USART4_TX / TMR9_CH2C / EMAC_MII_CRS	ADC12_IN0(6) / ERTC_MUX2 / WKUP1
11	15	24	35	PA1	I/O	FTa	TMR2_CH2 / TMR5_CH2 / TMR9_CH1C / I2C2_SDA / SPI4_MOSI / I2S4_SD / SPI3_CS / I2S3_WS / USART2_RTS_DE / USART4_RX / QSPI1_IO3 / EMAC_MII_RX_CLK / EMAC_RMII_REF_CLK / I2SF5_SD / I2C1_SMBA	ADC12_IN1(6)
12	16	25	36	PA2	I/O	FTa	TMR2_CH3 / TMR5_CH3 / TMR9_CH1 / I2SF5_CKIN / USART2_TX / CAN2_RX / QSPI1_CS / EMAC_MDIO / XMC_D4	ADC12_IN2 / WKUP4
13	17	26	37	PA3	I/O	FTa	TMR2_CH4 / TMR5_CH4 / TMR9_CH2 / I2S2_MCK / USART2_RX / CAN2_TX / EMAC_MII_COL / XMC_D5	ADC12_IN3
-	18	27	38	V_{SS}	S	-	Digital ground	
-	19	28	39	V_{DD}	S	-	Digital power supply	
14	20	29	40	PA4	I/O	FTa	I2C1_SCL / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART2_CK / USART6_TX / TMR14_CH1 / OTGFS1_OE / XMC_D6	ADC12_IN4 / DAC1_OUT
15	21	30	41	PA5	I/O	FTa	TMR2_CH1 / TMR2_EXT / TMR8_CH1C / SPI1_SCK / I2S1_CK / USART3_CK / USART3_RX / USART6_RX / TMR13_CH1C / XMC_D7	ADC12_IN5 / DAC2_OUT
16	22	31	42	PA6	I/O	FTa	TMR1_BRK / TMR3_CH1 / TMR8_BRK / SPI1_MISO / I2S2_MCK / USART3_CTS / USART3_RX / TMR13_CH1 / QSPI1_IO0 / SDIO1_CMD / QSPI1_IO2	ADC12_IN6

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
17	23	32	43	PA7	I/O	FTa	TMR1_CH1C / TMR3_CH2 / TMR8_CH1C / I2C3_SCL / SPI1_MOSI / I2S1_SD / USART3_TX / TMR14_CH1 / QSPI1_IO1 / EMAC_MII_RX_DV / EMAC_RMII_CRS_DV / XMC_SDNWE	ADC12_IN7
-	24	33	44	PC4	I/O	FTa	TMR9_CH1 / I2S1_MCK / USART3_TX / TMR13_CH1 / QSPI1_IO2 / EMAC_MII_RXD0 / EMAC_RMII_RXD0 / XMC_SDCS0 / XMC_NE4	ADC12_IN14
-	25	34	45	PC5	I/O	FTa	TMR1_CH4C / TMR9_CH2 / I2C1_SMBA / USART3_RX / TMR13_CH1C / QSPI1_IO3 / EMAC_MII_RXD1 / EMAC_RMII_RXD1 / XMC_SDCKE0 / XMC_NOE	ADC12_IN15 / WKUP5
18	26	35	46	PB0	I/O	FTa	TMR1_CH2C / TMR3_CH3 / TMR8_CH2C / SPI1_MISO / USART2_RX / SPI3_MOSI / I2S3_SD / USART3_CK / QSPI1_IO0 / EMAC_MII_RXD2 / SDIO1_D1 / I2SF5_CK	ADC12_IN8
19	27	36	47	PB1	I/O	FTa	TMR1_CH3C / TMR3_CH4 / TMR8_CH3C / SPI1_MOSI / I2S1_SD / SPI2_SCK / I2S2_CK / USART2_CK / USART3_RTS_DE / QSPI1_SCK / EMAC_MII_RXD3 / SDIO1_D2 / I2SF5_WS / TMR14_CH1	ADC12_IN9
20	28	37	48	PB2 / BOOT1 (PB2)	I/O	FT	TMR2_CH4 / TMR3_EXT / I2C3_SMBA / SPI3_MOSI / I2S3_SD / QSPI1_SCK / CAN3_STB / SDIO1_CK / TMR14_CH1C	Boot mode select 1
-	-	-	49	PF11	I/O	FT	TMR8_EXT / XMC_SDNRAS	-
-	-	-	50	PF12	I/O	FT	TMR8_BRK / XMC_A6	-
-	-	-	51	V_{SS}	S	-	Digital ground	
-	-	-	52	V_{DD}	S	-	Digital power supply	
-	-	-	53	PF13	I/O	FT	I2C3_SMBA / XMC_A7	-
-	-	-	54	PF14	I/O	FTf	I2C3_SCL / XMC_A8	-
-	-	-	55	PF15	I/O	FTf	I2C3_SDA / CAN1_STB / XMC_A9	-
-	-	-	56	PG0	I/O	FT	SPI1_MISO / CAN1_RX / XMC_A10	-
-	-	-	57	PG1	I/O	FT	SPI1_MOSI / I2S1_SD / CAN1_TX / XMC_A11	-
-	-	38	58	PE7	I/O	FT	TMR1_EXT / USART5_CK_RTS_DE / USART7_RX / XMC_A13 / XMC_D4	-
-	-	39	59	PE8	I/O	FT	TMR1_CH1C / USART4_TX / USART7_TX / XMC_A16 / XMC_D5	-
-	-	40	60	PE9	I/O	FT	TMR1_CH1 / USART4_RX / XMC_A17 / XMC_D6	-
-	-	-	61	V_{SS}	S	-	Digital ground	
-	-	-	62	V_{DD}	S	-	Digital power supply	
-	-	41	63	PE10	I/O	FT	TMR1_CH2C / USART5_TX / XMC_A18 / XMC_D7	-
-	-	42	64	PE11	I/O	FT	TMR1_CH2 / SPI4_CS / I2S4_WS / USART5_RX / XMC_D8	-

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
-	-	43	65	PE12	I/O	FT	TMR1_CH3C / SPI1_CS / I2S1_WS / SPI4_SCK / I2S4_CK / XMC_D9	-
-	-	44	66	PE13	I/O	FT	TMR1_CH3 / SPI1_SCK / I2S1_CK / SPI4_MISO / XMC_D10	-
-	-	45	67	PE14	I/O	FT	TMR1_CH4 / SPI1_MISO / SPI4_MOSI / I2S4_SD / XMC_D11	-
-	-	46	68	PE15	I/O	FT	TMR1_BRK / TMR1_CH4C / SPI1_MOSI / I2S1_SD / XMC_D12	-
21	29	47	69	PB10	I/O	FTf	TMR2_CH3 / I2C2_SCL / SPI2_SCK / I2S2_CK / I2S3_MCK / USART3_TX / QSPI1_CS / EMAC_MII_RX_ER / QSPI1_IO1 / SDIO1_D7 / XMC_NOE	-
22	30	48	70	PB11	I/O	FT	TMR2_CH4 / TMR5_CH4 / I2C2_SDA / I2SF5_CKIN / USART3_RX / TMR13_BRK / EMAC_MII_TX_EN / EMAC_RMII_TX_EN / QSPI1_IO0 / CAN2_STB / XMC_LB	-
23	31	49	71	PH3	I/O	FT	TMR2_CH2 / TMR5_CH2 / I2C2_SDA / USART4_TX / USART7_TX / QSPI1_IO1	-
24	32	50	72	V_{DD}	S	-	Digital power supply	
25	33	51	73	PB12	I/O	FT	TMR1_BRK / TMR5_CH1 / TMR12_BRK / I2C2_SMBA / SPI2_CS / I2S2_WS / SPI4_CS / I2S4_WS / SPI3_SCK / I2S3_CK / USART3_CK / CAN2_RX / EMAC_MII_TXD0 / EMAC_RMII_TXD0 / USART5_RX / I2SF5_WS / XMC_D13	-
26	34	52	74	PB13	I/O	FT	CLKOUT / TMR1_CH1C / TMR12_CH1C / I2C3_SMBA / SPI2_SCK / I2S2_CK / SPI4_SCK / I2S4_CK / I2C3_SCL / USART3_CTS / CAN2_TX / EMAC_MII_TXD1 / EMAC_RMII_TXD1 / USART5_TX / I2SF5_CK / XMC_UB	-
27	35	53	75	PB14	I/O	TC	TMR1_CH2C / TMR8_CH2C / I2C3_SDA / SPI2_MISO / I2S2_SDEXT / USART3_RTS_DE / TMR12_CH1 / SDIO1_D6 / XMC_D0	-
28	36	54	76	PB15	I/O	TC	ERTC_REFIN / TMR1_CH3C / TMR8_CH3C / I2C3_SCL / SPI2_MOSI / I2S2_SD / TMR12_CH2 / SDIO1_CK / TMR12_CH1C	WKUP7
-	-	55	77	PD8	I/O	FT	USART3_TX / TMR12_CH2C / EMAC_MII_RX_DV / EMAC_RMII_CRS_DV / XMC_D13	-
-	-	56	78	PD9	I/O	FT	USART3_RX / EMAC_MII_RXD0 / EMAC_RMII_RXD0 / XMC_D14	-
-	-	57	79	PD10	I/O	FT	USART3_CK / USART4_TX / EMAC_MII_RXD1 / EMAC_RMII_RXD1 / XMC_D15	-
-	-	58	80	PD11	I/O	FT	I2C2_SMBA / USART3_CTS / QSPI1_IO0 / EMAC_MII_RXD2 / XMC_A14 / XMC_SDBA0 / XMC_A16 / CAN3_STB	-

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
-	-	59	81	PD12	I/O	FTf	TMR4_CH1 / I2C2_SCL / USART3_RTS_DE / USART8_CK_RTS_DE / QSPI1_IO1 / EMAC_MII_RXD3 / XMC_A15 / XMC_SDBA1 / XMC_A17 / CAN3_RX	-
-	-	60	82	PD13	I/O	FTf	TMR4_CH2 / I2C2_SDA / USART8_TX / QSPI1_IO3 / XMC_SDCLK / XMC_A18 / CAN3_TX	-
-	-	-	83	V_{SS}	S	-	Digital ground	
-	-	-	84	V_{DD}	S	-	Digital power supply	
-	-	61	85	PD14	I/O	FTf	TMR4_CH3 / I2C3_SCL / USART8_RX / XMC_D0	-
-	-	62	86	PD15	I/O	FTf	TMR4_CH4 / I2C3_SDA / USART7_CK_RTS_DE / XMC_D1	-
-	-	-	87	PG2	I/O	FT	XMC_A12	-
-	-	-	88	PG3	I/O	FT	XMC_A13	-
-	-	-	89	PG4	I/O	FT	XMC_A14 / XMC_SDBA0	-
-	-	-	90	PG5	I/O	FT	XMC_A15 / XMC_SDBA1	-
-	-	-	91	PG6	I/O	FT	QSPI1_CS	-
-	-	-	92	PG7	I/O	FT	USART6_CK	-
-	-	-	93	PG8	I/O	FT	USART6_RTS_DE / EMAC_PPS_OUT / XMC_SDCLK	-
-	-	-	94	V_{SS}	S	-	Digital ground	
-	-	-	95	V_{DD}	S	-	Digital power supply	
-	37	63	96	PC6	I/O	FT	TMR1_CH1 / TMR3_CH1 / TMR8_CH1 / I2C1_SCL / I2S2_MCK / USART6_TX / USART7_TX / XMC_A0 / SDIO1_D6 / XMC_D1	-
-	38	64	97	PC7	I/O	FT	TMR1_CH2 / TMR3_CH2 / TMR8_CH2 / I2C1_SDA / SPI2_SCK / I2S2_CK / I2S3_MCK / USART6_RX / USART7_RX / XMC_A1 / SDIO1_D7 / XMC_NADV	-
-	39	65	98	PC8	I/O	FT	TMR1_CH3 / TMR3_CH3 / TMR8_CH3 / I2S4_MCK / I2SF5_MCK / USART8_TX / USART6_CK / QSPI1_IO2 / XMC_A2 / SDIO1_D0	-
-	40	66	99	PC9	I/O	FT	CLKOUT / TMR1_CH4 / TMR3_CH4 / TMR8_CH4 / I2C3_SDA / I2SF5_CKIN / USART8_RX / I2C1_SDA / QSPI1_IO0 / OTGFS1_OE / XMC_A3 / SDIO1_D1	-
29	41	67	100	PA8	I/O	FT	CLKOUT / TMR1_CH1 / TMR9_BRK / I2C3_SCL / USART1_CK / USART2_TX / USART7_RX / CAN3_RX / OTGFS1_SOF / SDIO1_D1 / XMC_A4	-
30	42	68	101	PA9	I/O	FT	CLKOUT / TMR1_CH2 / I2C3_SMBA / SPI2_SCK / I2S2_CK / USART1_TX / I2C1_SCL / TMR14_BRK / OTGFS1_VBUS / SDIO1_D2	-

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
31	43	69	102	PA10	I/O	FT	ERTC_REFIN / TMR1_CH3 / SPI2_MOSI / I2S2_SD / I2S4_MCK / USART1_RX / I2C1_SDA / OTGFS1_ID / I2SF5_MCK / I2SF5_SD	-
32	44	70	103	PA11	I/O	TC	TMR1_CH4 / I2C2_SCL / SPI2_CS / I2S2_WS / SPI4_MISO / USART1_CTS / USART6_TX / CAN1_RX / USART4_RX / I2C1_SMBA	OTGFS1_D-
33	45	71	104	PA12	I/O	TC	TMR1_EXT / I2C2_SDA / SPI2_MISO / I2SF5_SDEXT / USART1_RTS_DE / USART6_RX / CAN1_TX / USART4_TX	OTGFS1_D+
34	46	72	105	PA13 (SWDIO)(7)	I/O	FT	PA13 / IR_OUT / I2C1_SDA / SPI3_MISO / OTGFS1_OE	-
35	47	73	106	PH2	I/O	FT	TMR2_CH1 / TMR5_CH1 / I2C2_SCL / USART4_RX / USART7_RX / QSPI1_IO0	-
-	-	74	107	V_{SS}	S	-	Digital ground	
36	48	75	108	V_{DD}	S	-	Digital power supply	
37	49	76	109	PA14 (SWCLK)(7)	I/O	FT	PA14 / I2C1_SMBA / SPI3_MOSI / I2S3_SD / USART2_TX	-
38	50	77	110	PA15	I/O	FT	TMR2_CH1 / TMR2_EXT / SPI1_CS / I2S1_WS / SPI3_CS / I2S3_WS / USART1_TX / USART2_RX / USART7_TX / CAN3_TX / QSPI1_IO2 / XMC_NE2 / USART4_RTS_DE	-
-	51	78	111	PC10	I/O	FT	TMR5_CH2 / SPI3_SCK / I2S3_CK / USART3_TX / USART4_TX / QSPI1_IO1 / SDIO1_D2	-
-	52	79	112	PC11	I/O	FT	TMR5_CH3 / SPI3_MISO / I2S3_SDEXT / USART3_RX / USART4_RX / QSPI1_CS / SDIO1_D3 / XMC_D2	-
-	53	80	113	PC12	I/O	FT	TMR11_CH1 / I2C2_SDA / SPI3_MOSI / I2S3_SD / USART3_CK / USART4_CK / USART5_TX / SDIO1_CK / XMC_D3	-
-	-	81	114	PD0	I/O	FT	TMR8_CH4C / SPI4_MISO / SPI3_MOSI / I2S3_SD / SPI2_CS / I2S2_WS / USART4_RX / CAN1_RX / XMC_A5 / XMC_D2	-
-	-	82	115	PD1	I/O	FT	TMR8_CH4 / SPI2_SCK / I2S2_CK / SPI2_CS / I2S2_WS / USART4_TX / CAN1_TX / XMC_A6 / XMC_D3	-
-	54	83	116	PD2	I/O	FT	TMR3_EXT / USART3_RTS_DE / USART5_RX / XMC_A7 / SDIO1_CMD / XMC_NWE	-
-	-	84	117	PD3	I/O	FT	SPI2_SCK / I2S2_CK / SPI2_MISO / USART2_CTS / QSPI1_SCK / XMC_A8 / XMC_CLK	-
-	-	85	118	PD4	I/O	FT	SPI2_MOSI / I2S2_SD / USART2_RTS_DE / XMC_A9 / XMC_NOE	-
-	-	86	119	PD5	I/O	FT	USART2_TX / XMC_A10 / XMC_NWE	-

Pin numbers				Pin names (function after reset)	Type[1]	GPIO level[2]	Multiplexed functions[3]	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
-	-	-	120	V_{SS}	S	-	Digital ground	
-	-	-	121	V_{DD}	S	-	Digital power supply	
-	-	87	122	PD6	I/O	FT	SPI3_MOSI / I2S3_SD / USART2_RX / XMC_A11 / XMC_NWAIT	-
-	-	88	123	PD7	I/O	FT	USART2_CK / XMC_A12 / XMC_NE1	-
-	-	-	124	PG9	I/O	FT	USART6_RX / QSPI1_IO2 / CAN3_TX / XMC_NE2	-
-	-	-	125	PG10	I/O	FT	CAN3_RX / XMC_NE3	-
-	-	-	126	PG11	I/O	FT	SPI4_SCK / I2S4_CK / CAN2_RX / EMAC_MII_TX_EN / EMAC_RMII_TX_EN	-
-	-	-	127	PG12	I/O	FT	SPI4_MISO / USART6_RTS_DE / CAN2_TX / XMC_NE4	-
-	-	-	128	PG13	I/O	FT	SPI4_MOSI / I2S4_SD / USART6_CTS / EMAC_MII_TXD0 / EMAC_RMII_TXD0 / CAN2_STB / XMC_A24	-
-	-	-	129	PG14	I/O	FT	SPI4_CS / I2S4_WS / USART6_TX / QSPI1_IO3 / EMAC_MII_TXD1 / EMAC_RMII_TXD1 / XMC_A25	-
-	-	-	130	V_{SS}	S	-	Digital ground	
-	-	-	131	V_{DD}	S	-	Digital power supply	
-	-	-	132	PG15	I/O	FT	USART6_CTS / XMC_SDNCAS	-
39	55	89	133	PB3 (SWO)[7]	I/O	FTf	PB3 / TMR2_CH2 / I2C2_SDA / SPI1_SCK / I2S1_CK / SPI3_SCK / I2S3_CK / USART1_RX / USART1_RTS_DE / USART7_RX / CAN3_RX / QSPI1_IO3 / USART5_TX	-
40	56	90	134	PB4	I/O	FT	TMR1_CH4C / TMR3_CH1 / TMR11_BRK / I2C3_SDA / SPI1_MISO / SPI3_MISO / I2S3_SDEXT / USART1_CTS / USART7_TX / CAN3_TX / QSPI1_SCK / SDIO1_D0 / USART5_RX	-
41	57	91	135	PB5	I/O	FT	TMR3_CH2 / TMR10_BRK / I2C1_SMBA / SPI1_MOSI / I2S1_SD / SPI3_MOSI / I2S3_SD / USART1_CK / USART5_RX / CAN2_RX / EMAC_PPS_OUT / QSPI1_IO0 / XMC_SDCKE1 / USART5_CK_RTS_DE / SDIO1_D3	WKUP6
42	58	92	136	PB6	I/O	FT	TMR4_CH1 / TMR10_CH1C / I2C1_SCL / I2S1_MCK / SPI4_CS / I2S4_WS / USART1_TX / USART5_TX / CAN2_TX / USART4_CK / QSPI1_CS / XMC_SDCS1 / I2SF5_WS / SDIO1_D0	-
43	59	93	137	PB7	I/O	FT	TMR4_CH2 / TMR8_BRK / I2C1_SDA / SPI4_SCK / I2S4_CK / USART1_RX / USART4_CTS / TMR11_CH1C / CAN1_STB / QSPI1_IO1 / XMC_NADV / I2SF5_CK / SDIO1_D0	-
44	60	94	138	BOOT0	I	B	Boot mode select 0	

Pin numbers				Pin names (function after reset)	Type(1)	GPIO level(2)	Multiplexed functions(3)	Additional functions
LQFP48 / QFN48	LQFP64	LQFP100	LQFP144					
45	61	95	139	PB8	I/O	FTf	TMR2_CH1 / TMR2_EXT / TMR4_CH3 / TMR10_CH1 / I2C1_SCL / SPI4_MISO / USART1_TX / USART5_RX / CAN1_RX / EMAC_MII_TXD3 / SDIO1_D4 / I2SF5_SDEXT / I2SF5_SD	-
46	62	96	140	PB9	I/O	FTf	IR_OUT / TMR2_CH2 / TMR4_CH4 / TMR11_CH1 / I2C1_SDA / SPI2_CS / I2S2_WS / SPI4_MOSI / I2S4_SD / I2C2_SDA / USART5_TX / CAN1_TX / QSPI1_CS / SDIO1_D5 / I2SF5_SD / I2S1_MCK	-
-	-	97	141	PE0	I/O	FT	TMR4_EXT / USART8_RX / TMR13_CH1 / XMC_LB / XMC_SDDQML	-
-	-	98	142	PE1	I/O	FT	TMR1_CH2C / USART8_TX / TMR14_CH1 / XMC_UB / XMC_SDDQMH	-
47	63	99	143	V_{SS}	S	-	Digital ground	
48	64	100	144	V_{DD}	S	-	Digital power supply	
-/49	-	-	-	EPAD (V_{SS})	S	-	Digital ground	

(1) I = input, O = output, S = power supply.

(2) TC = standard 3.3 V GPIO, FT = general 5 V-tolerant GPIO, FTa = 5 V-tolerant GPIO with analog function, FTf = 5 V-tolerant GPIO with 20 mA sink current capability, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor.

(3) Function availability depends on the selected product part number. Any of GPIOs has EVENTOUT feature.

(4) PC13, PC14 and PC15 are supplied through the power switch. Since the switch can only drive a limited amount of current (3 mA), the use of GPIOs PC13 to PC15 in output mode is limited not to be used as a current source (e.g. to drive an LED).

(5) Main function after the first battery-powered domain power-up. Later on, it depends on the contents of the battery-powered domain registers even after reset (because these registers are not reset by the main reset). For details on how to manage these I/Os, refer to the Battery-powered domain and BPR register description sections in the AT32F455/456/457 reference manual.

(6) PA0, PA1, PC0, PC1, PC2 and PC3 represent fast ADC channel, others slow ADC channels.

(7) After reset, PA13/PA14/PB3 are multiplexed as SWDIO/SWCLK/SWO. The internal pull-up resistor on SWDIO/SWO and the internal pull-down resistor on SWCLK are ON.

Table 11. XMC pin definitions

Pin name	XMC				LQFP100	LQFP64
	SRAM/PSRAM/ NOR	Multiplexed PSRAM/NOR	SDRAM(1)			
PF0	A0	-	-	A0	-	-
PF1	A1	-	-	A1	-	-
PF2	A2	-	-	A2	-	-
PF3	A3	-	-	A3	-	-
PF4	A4	-	-	A4	-	-
PF5	A5	-	-	A5	-	-
PF12	A6	-	-	A6	-	-
PF13	A7	-	-	A7	-	-
PF14	A8	-	-	A8	-	-
PF15	A9	-	-	A9	-	-
PG0	A10	-	-	A10	-	-
PG1	A11	-	-	A11	-	-
PG2	A12	-	-	A12	-	-
PG3	A13	-	-		-	-
PG4	A14	-	-	SDBA0	-	-
PG5	A15	-	-	SDBA1	-	-
PD11	A14 / A16	A16	SDBA0	-	Yes	-
PD12	A15 / A17	A17	SDBA1	-	Yes	-
PD13	A18	A18	SDCLK	-	Yes	-
PE3	A19	A19	-		Yes	-
PE4	A20	A20	-		Yes	-
PE5	A21	A21	-		Yes	-
PE6	A22	A22	SDNRAS		Yes	-
PE2	A23	A23	SDNCAS		Yes	-
PG13	A24	A24	-		-	-
PG14	A25	A25	-		-	-
PC3	A0	-	SDCKE0		Yes	Yes
PC6	A0 / D1	AD1	A0	-	Yes	Yes
PC7	A1	NADV	A1	-	Yes	Yes
PC8	A2	-	A2	-	Yes	Yes
PC9	A3	-	A3	-	Yes	Yes
PA8	A4	-	A4	-	Yes	Yes
PD0	A5 / D2	AD2	A5	D2	Yes	-
PD1	A6 / D3	AD3	A6	D3	Yes	-
PD2	A7 / NWE	NWE	A7	-	Yes	Yes
PD3	A8 / CLK	CLK	A8	-	Yes	-
PD4	A9 / NOE	NOE	A9	-	Yes	-

Pin name	XMC				LQFP100	LQFP64
	SRAM/PSRAM/ NOR	Multiplexed PSRAM/NOR	SDRAM(1)			
PD5	A10 / NWE	NWE	A10	-	Yes	-
PD6	A11 / NWAIT	NWAIT	A11	-	Yes	-
PD7	A12 / NE1	NE1	A12	-	Yes	-
PD14	D0	AD0	D0		Yes	-
PD15	D1	AD1	D1		Yes	-
PC11	D2	AD2	D2	-	Yes	Yes
PC12	D3	AD3	D3	-	Yes	Yes
PE7	D4 / A13	AD4	D4		Yes	-
PE8	D5 / A16	AD5	D5		Yes	-
PE9	D6 / A17	AD6	D6		Yes	-
PE10	D7 / A18	AD7	D7		Yes	-
PE11	D8	AD8	D8		Yes	-
PE12	D9	AD9	D9		Yes	-
PE13	D10	AD10	D10		Yes	-
PE14	D11	AD11	D11		Yes	-
PE15	D12	AD12	D12		Yes	-
PD8	D13	AD13	D13		Yes	-
PD9	D14	AD14	D14		Yes	-
PD10	D15	AD15	D15		Yes	-
PB14	D0	AD0	-		Yes	Yes
PC6	D1	AD1	-		Yes	Yes
PA2	D4	AD4	-		Yes	Yes
PA3	D5	AD5	-		Yes	Yes
PA4	D6	AD6	-		Yes	Yes
PA5	D7	AD7	-		Yes	Yes
PB12	D13	AD13	-		Yes	Yes
PD7	NE1	NE1	-		Yes	-
PG9	NE2	NE2	-		-	-
PA15	NE2	NE2	-		Yes	Yes
PG10	NE3	NE3	-		-	-
PG12	NE4	NE4	-		-	-
PC4	NE4	NE4	SDCS0		Yes	Yes
PB7	-	NADV	-		Yes	Yes
PB10	NOE	NOE	-		Yes	Yes
PC5	NOE	NOE	SDCKE0		Yes	Yes
PC2	NWE	NWE	SDCS0		Yes	Yes
PE0	LB	LB	SDDQML		Yes	-
PB11	LB	LB	-		Yes	Yes

Pin name	XMC			LQFP100	LQFP64
	SRAM/PSRAM/ NOR	Multiplexed PSRAM/NOR	SDRAM(1)		
PE1	UB	UB	SDDQMH	Yes	-
PB13	UB	UB	-	Yes	Yes
PG8	-	-	- SDCLK	-	-
PB5	-	-	SDCKE1	Yes	-
PB6	-	-	SDCS1	Yes	-
PF11	-	-	SDNRAS	-	-
PG15	-	-	SDNCAS	-	-
PC0	-	-	SDNWE	Yes	-
PA7	-	-	SDNWE	Yes	Yes

(1) Two sets of pin combination listed in “SDRAM” column are recommended to use for SDRAM address, block address, data and clock. Otherwise, maximum performance cannot be achieved even though they can work normally.

4 Electrical characteristics

4.1 Test conditions

4.1.1 Maximum and minimum values

The minimum and maximum values are obtained in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

4.1.2 Typical values

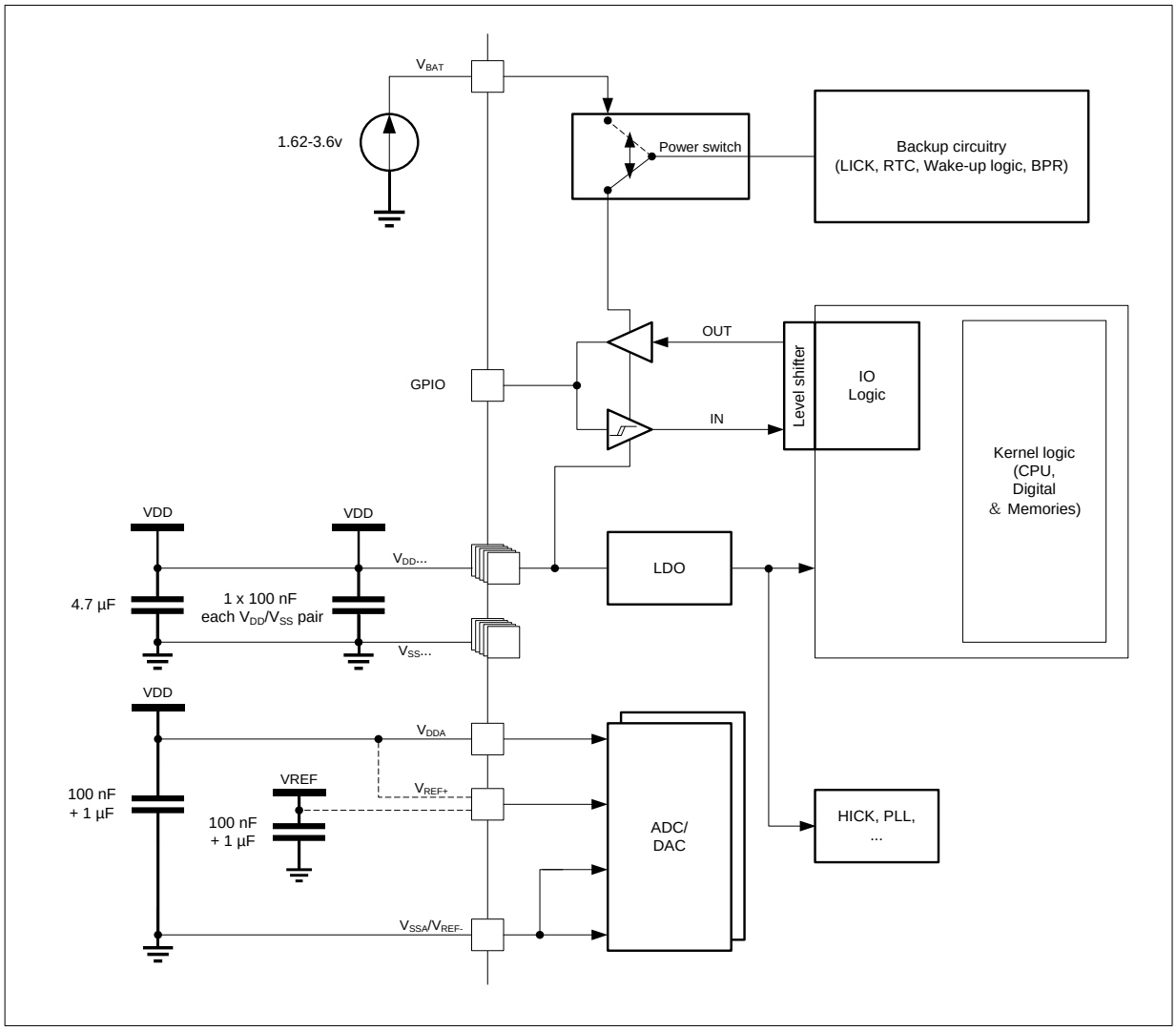
Typical values are based on T_A = 25 °C and V_{DD} = 3.3 V.

4.1.3 Typical curves

All typical curves are provided only as design guidelines and are not tested.

4.1.4 Power supply scheme

Figure 6. Power supply scheme



4.2 Absolute maximum values

4.2.1 Ratings

If stresses were out of the absolute maximum ratings listed in *Table 12*, *Table 13* and *Table 14*, it may cause permanent damage to the device. These are the maximum stresses only that the device could withstand, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

Table 12. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DDx}-V_{SS}	External main supply voltage	-0.3	4.0	V
V_{BAT}-V_{SS}	Battery power voltage	-0.3	4.0	
V_{IN}	Input voltage on TC GPIOs	V_{SS}-0.3	4.0	
	Input voltage on FT, FTf and FTa GPIOs	V_{SS}-0.3	6.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 13. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	150	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	150	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIO and control pin	-25	

Table 14. Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test is in accordance with the JS-001-2023/JS-002-2022 standard.

Table 15. ESD values

Symbol	Parameter	Conditions	Class	Min	Unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conform to JS-001-2023	2	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conform toJS-002-2022	III	±1000	

Static latch-up

Tests compliant with JESD78F latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 16. Static latch-up values

Symbol	Parameters	Conditions	Level/Class
LU	Static latch-up class	T_A = +105 °C, conform to JESD78F	II level A (±200 mA)

4.3 Specifications

4.3.1 General operating conditions

Table 17. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	LDO voltage	1.3 V	0	192	MHz
			1.2 V	0	160	
			1.1 V	0	108	
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-		0	f_{HCLK}	MHz
f_{PCLK3}	Internal APB3 clock frequency	-		0	90	MHz
V_{DD}	Digital operating voltage	-		2.4	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}		V_{DD}		V
V_{BAT}	Battery power operating voltage	-		1.62	3.6	V
P_D	Power dissipation: T_A = 105 °C	LQFP144 – 20 x 20 mm		-	298	mW
		LQFP100 – 14 x 14 mm		-	265	
		LQFP64 – 10 x 10 mm		-	248	
		LQFP48 – 7 x 7 mm		-	229	
		QFN48 – 6 x 6 mm		-	351	
T_A	Ambient temperature	-		-40	105	°C

4.3.2 Operating conditions at power-up / power-down

Table 18. Operating conditions at power-up / power-down

Symbol	Parameter	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	0	∞	ms/V
	V_{DD} fall time rate	20	∞	μs/V

4.3.3 Embedded reset and power control block characteristics

Table 19. Embedded reset characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}	Power-on reset threshold	1.73	2.06	2.4	V
V_{LVR}	Low voltage reset threshold	1.62(2)	1.88	2.16	V
$V_{LVRhyst}$	LVR hysteresis	-	180	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RESTTEMPO}$	-	830	-	μs

(1) Guaranteed by characterization results, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 7. Power-on reset and low voltage reset waveform

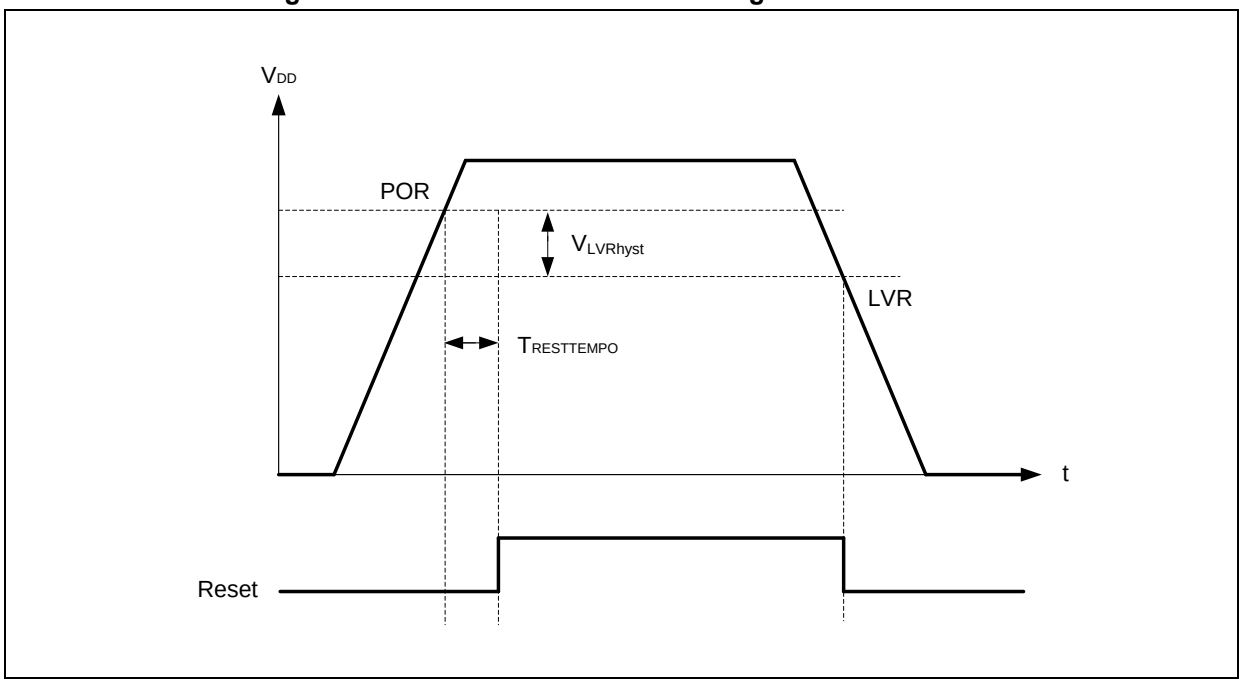


Table 20. Programmable voltage monitoring characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVM1}	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge	2.19	2.28	2.37	V
		Falling edge	2.09	2.18	2.27	V
V_{PVM2}	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge(1)	2.28	2.38	2.48	V
		Falling edge(1)	2.18	2.28	2.38	V
V_{PVM3}	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge(1)	2.38	2.48	2.58	V
		Falling edge(1)	2.28	2.38	2.48	V
V_{PVM4}	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge(1)	2.47	2.58	2.69	V
		Falling edge(1)	2.37	2.48	2.59	V
V_{PVM5}	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge(1)	2.57	2.68	2.79	V
		Falling edge(1)	2.47	2.58	2.69	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge(1)	2.66	2.78	2.9	V
		Falling edge(1)	2.56	2.68	2.8	V
V_{PVM7}	PVM threshold 7 (PVMSEL[2:0] = 111)	Rising edge	2.76	2.88	3	V
		Falling edge	2.66	2.78	2.9	V
V_{HYS_P}(1)	PVM hysteresis	-	-	100	-	mV
$I_{DD\ (PVM)}$(1)	PVM current dissipation	-	-	20	30	μA

(1) Guaranteed by characterization results, not tested in production.

4.3.4 Memory characteristics

Table 21. Flash memory characteristics(1)

Symbol	Parameter	Condition	Typ	Max	Unit
T_{PROG}	Programming time	-	60	65	μs
t_{SE}	Sector erase time	-	13.2	16	ms
t_{ME}	Mass erase time	-	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 22. Flash memory endurance and data retention(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	year

(1) Guaranteed by design, not tested in production.

4.3.5 Supply current characteristics

The current consumption, obtained by characterization results and not tested in production, is subject to several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin toggling rate, and executed binary code.

Typical and maximum current consumption

The device is placed under the following conditions:

- All GPIO pins are in analog mode
- Flash memory access time depends on the f_{HCLK} frequency (0 ~ 32 MHz: zero wait state; 33 ~ 64 MHz: one wait state; 65 ~ 96 MHz: two wait states; 97 ~ 128 MHz: three wait states; 129 ~ 160 MHz: four wait states; above 160 MHz: five wait states).
- Prefetch ON.
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{PCLK3} = f_{HCLK}/4$, $f_{ADCCLK} = f_{PCLK2}/4$.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition, and the maximum values are measured with V_{DD} = 3.6 V.

Table 23. Typical current consumption in Run mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Typ			Unit
					All peripherals enabled (AT32F455/456)	All peripherals enabled (AT32F457)	All peripherals disabled	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1)(2)	192 MHz	1.3	67.1	69.3	25.8	mA
			180 MHz	1.3	63.0	65.1	24.3	
			160 MHz	1.2	51.5	53.2	20.0	
			144 MHz	1.2	46.5	48.1	18.1	
			120 MHz	1.2	39.3	40.6	15.6	
			108 MHz	1.1	32.5	33.6	13.1	
			96 MHz	1.1	29.1	30.0	11.8	
			72 MHz	1.1	22.2	23.0	9.29	
			48 MHz	1.1	15.5	16.0	6.79	
			36 MHz	1.1	12.0	12.4	5.46	
			24 MHz	1.1	8.69	8.92	4.24	
			8 MHz	1.1	3.44	3.52	1.86	
			4 MHz	1.1	2.36	2.39	1.49	
			2 MHz	1.1	1.80	1.82	1.30	
			1 MHz	1.1	1.52	1.54	1.20	
		High speed internal crystal (HICK)(2)	192 MHz	1.3	66.7	68.9	25.4	mA
			180 MHz	1.3	62.6	64.6	23.9	
			160 MHz	1.2	51.1	52.8	19.6	
			144 MHz	1.2	46.2	47.7	17.8	
			120 MHz	1.2	38.9	40.2	15.2	
			108 MHz	1.1	32.1	33.1	12.6	
			96 MHz	1.1	28.6	29.5	11.3	
			72 MHz	1.1	21.9	22.6	8.81	
			48 MHz	1.1	15.0	15.5	6.34	
			36 MHz	1.1	11.5	11.9	4.97	
			24 MHz	1.1	8.17	8.36	3.78	
			8 MHz	1.1	2.92	2.99	1.40	
			4 MHz	1.1	1.82	1.86	1.02	
			2 MHz	1.1	1.28	1.32	0.83	
			1 MHz	1.1	1.02	1.05	0.74	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 24. Typical current consumption in Sleep mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Typ			Unit
					All peripherals enabled (AT32F455/456)	All peripherals enabled (AT32F457)	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1)(2)	192 MHz	1.3	54.4	56.6	12.6	mA
			180 MHz	1.3	51.1	53.1	11.8	
			160 MHz	1.2	41.7	43.4	9.82	
			144 MHz	1.2	37.7	39.2	8.95	
			120 MHz	1.2	32.0	33.2	7.95	
			108 MHz	1.1	26.4	27.5	6.70	
			96 MHz	1.1	23.6	24.6	6.08	
			72 MHz	1.1	18.2	18.9	5.02	
			48 MHz	1.1	12.8	13.3	3.94	
			36 MHz	1.1	9.99	10.4	3.32	
			24 MHz	1.1	7.31	7.54	2.81	
			8 MHz	1.1	2.96	3.04	1.37	
			4 MHz	1.1	2.10	2.14	1.23	
			2 MHz	1.1	1.66	1.69	1.15	
			1 MHz	1.1	1.45	1.47	1.12	
		High speed internal crystal (HICK)(2)	192 MHz	1.3	53.9	56.1	12.1	mA
			180 MHz	1.3	50.6	52.7	11.4	
			160 MHz	1.2	41.3	43.0	9.38	
			144 MHz	1.2	37.3	38.8	8.51	
			120 MHz	1.2	31.5	32.8	7.51	
			108 MHz	1.1	26.0	27.0	6.26	
			96 MHz	1.1	23.2	24.1	5.63	
			72 MHz	1.1	17.7	18.4	4.57	
			48 MHz	1.1	12.3	12.8	3.49	
			36 MHz	1.1	9.49	9.84	2.86	
			24 MHz	1.1	6.79	7.02	2.35	
			8 MHz	1.1	2.43	2.51	0.92	
			4 MHz	1.1	1.57	1.61	0.78	
			2 MHz	1.1	1.13	1.16	0.70	
			1 MHz	1.1	0.92	0.94	0.67	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 25. Maximum current consumption in Run mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High speed external crystal (HEXT)(1), all peripheral enabled (AT32F455/456)	192 MHz	1.3	69.8	71.7	mA
			180 MHz	1.3	65.6	67.5	
			160 MHz	1.2	53.5	55.0	
			144 MHz	1.2	48.5	50.0	
			120 MHz	1.2	41.1	42.6	
			108 MHz	1.1	33.9	35.1	
			96 MHz	1.1	30.4	31.6	
			72 MHz	1.1	23.6	24.8	
			48 MHz	1.1	16.8	18.0	
			36 MHz	1.1	13.3	14.5	
			24 MHz	1.1	9.97	11.2	
			8 MHz	1.1	4.80	6.02	
		High speed external crystal (HEXT)(1), all peripheral enabled (AT32F457)	192 MHz	1.3	72.0	73.9	mA
			180 MHz	1.3	67.7	69.6	
			160 MHz	1.2	55.2	56.7	
			144 MHz	1.2	50.0	51.5	
			120 MHz	1.2	42.4	43.9	
			108 MHz	1.1	35.0	36.2	
			96 MHz	1.1	31.4	32.5	
			72 MHz	1.1	24.3	25.5	
			48 MHz	1.1	17.3	18.5	
			36 MHz	1.1	13.7	14.9	
			24 MHz	1.1	10.2	11.4	
			8 MHz	1.1	4.87	6.09	
		High speed external crystal (HEXT)(1), all peripheral disabled	192 MHz	1.3	27.4	29.1	mA
			180 MHz	1.3	25.9	27.5	
			160 MHz	1.2	21.3	22.7	
			144 MHz	1.2	19.4	20.8	
			120 MHz	1.2	16.9	18.3	
			108 MHz	1.1	14.1	15.3	
			96 MHz	1.1	12.8	14.0	
			72 MHz	1.1	10.4	11.6	
			48 MHz	1.1	7.96	9.13	
			36 MHz	1.1	6.65	7.83	
			24 MHz	1.1	5.46	6.65	
			8 MHz	1.1	3.12	4.31	

(1) External clock is 8 MHz, and PLL is ON when f_{HCLK} > 8 MHz.

Table 26. Maximum current consumption in Sleep mode

Sym.	Parameter	Condition	f_{HCLK}	LDO voltage (V)	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High speed external crystal (HEXT)(1), all peripherals enabled (AT32F455/456)	192 MHz	1.3	57.1	58.9	mA
			180 MHz	1.3	53.7	55.5	
			160 MHz	1.2	43.7	45.2	
			144 MHz	1.2	39.6	41.1	
			120 MHz	1.2	33.8	35.3	
			108 MHz	1.1	27.9	29.1	
			96 MHz	1.1	25.0	26.2	
			72 MHz	1.1	19.6	20.8	
			48 MHz	1.1	14.1	15.4	
			36 MHz	1.1	11.3	12.6	
			24 MHz	1.1	8.64	9.88	
			8 MHz	1.1	4.36	5.58	
		High speed external crystal (HEXT)(1), all peripherals enabled (AT32F457)	192 MHz	1.3	59.3	61.2	mA
			180 MHz	1.3	55.8	57.6	
			160 MHz	1.2	45.5	46.9	
			144 MHz	1.2	41.2	42.7	
			120 MHz	1.2	35.1	36.5	
			108 MHz	1.1	28.9	30.1	
			96 MHz	1.1	26.0	27.2	
			72 MHz	1.1	20.3	21.5	
			48 MHz	1.1	14.6	15.8	
			36 MHz	1.1	11.7	12.9	
			24 MHz	1.1	8.88	10.1	
			8 MHz	1.1	4.43	5.67	
		High speed external crystal (HEXT)(1), all peripherals disabled	192 MHz	1.3	14.3	15.9	mA
			180 MHz	1.3	13.6	15.2	
			160 MHz	1.2	11.3	12.6	
			144 MHz	1.2	10.4	11.8	
			120 MHz	1.2	9.39	10.8	
			108 MHz	1.1	7.91	9.11	
			96 MHz	1.1	7.29	8.49	
			72 MHz	1.1	6.26	7.46	
			48 MHz	1.1	5.20	6.41	
			36 MHz	1.1	4.59	5.79	
			24 MHz	1.1	4.09	5.30	
			8 MHz	1.1	2.67	3.88	

(1) External clock is 8 MHz, and PLL is ON when f_{HCLK} > 8 MHz.

Table 27. Typical and maximum current consumptions in Deepsleep and Standby modes

Sym.	Parameter	Condition	Typ(1)		Max(2)			Unit
			V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode	LDO 1.2 V in normal mode, HICK and HEXT OFF, WDT OFF	372	376	450	2100	3600	µA
		LDO in extra low-power mode, HICK and HEXT OFF, WDT OFF	170	172	200	1050	1900	
	Supply current in Standby mode	LEXT and ERTC OFF	2.5	3.7	4.9	7.1	10.9	µA
		LEXT and ERTC ON	3.4	5.0	6.2	8.3	12.4	

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 8. Typical current consumption in Deepsleep mode with LDO 1.2 V in normal mode vs. temperature at different V_{DD}

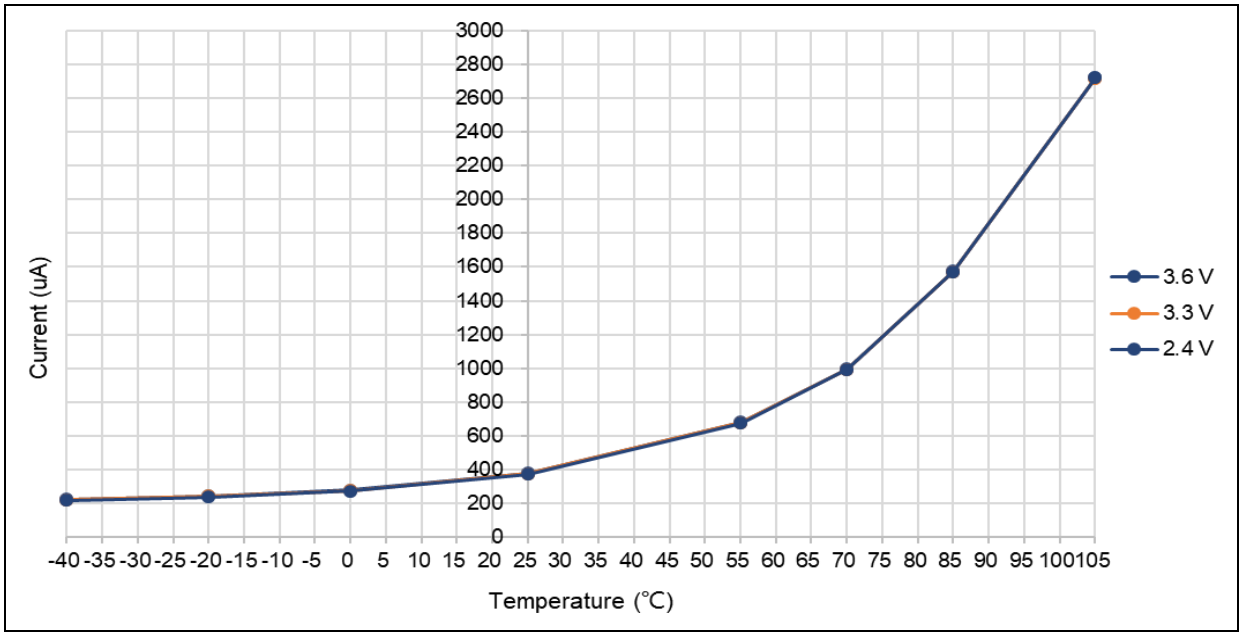


Figure 9. Typical current consumption in Deepsleep mode with LDO in extra low-power mode vs. temperature at different V_{DD}

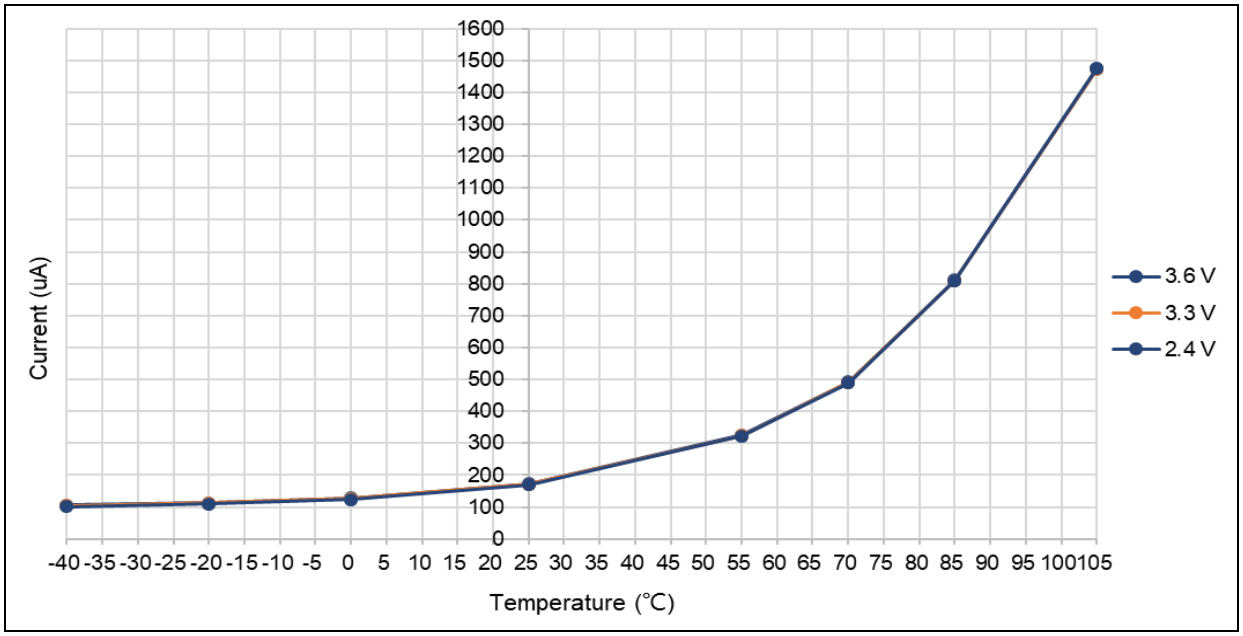


Figure 10. Typical current consumption in Standby mode vs. temperature at different V_{DD}

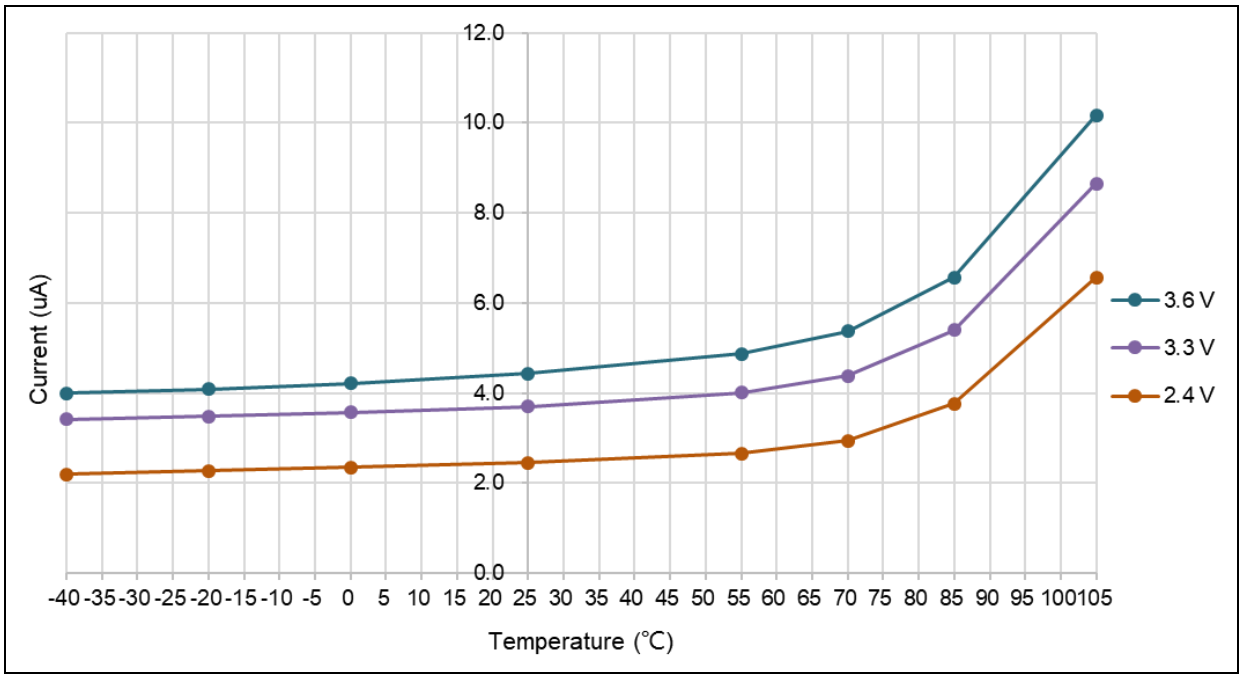
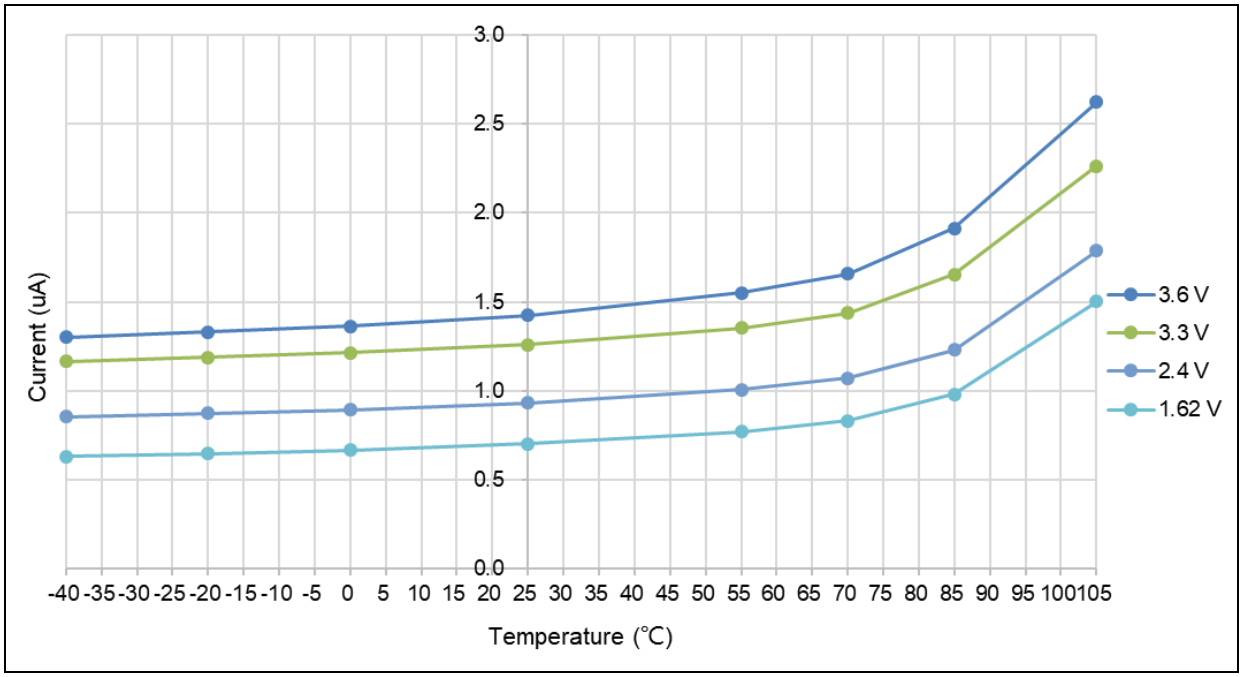


Table 28. Typical and maximum current consumptions on V_{BAT}

Symbol	Parameter	Condition	Typ(1)			Max(2)			Unit
			V_{BAT} = 1.62 V	V_{BAT} = 2.4 V	V_{BAT} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD_VBAT}	Supply power of V_{BAT}	LEXT and ERTC ON, $V_{DD} < V_{LVR}$	0.71	0.93	1.26	1.47	1.98	2.76	μA

(1) Typical values are measured at T_A = 25 °C.
(2) Guaranteed by characterization results, not tested in production.

Figure 11. Typical current consumption on V_{BAT} (LEXT and ERTC ON) vs. temperature at different V_{BAT}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIOs are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 29. Peripheral current consumption

Peripheral		LDO voltage (V)			Unit
		1.3	1.2	1.1	
AHB1	DMA1	4.01	3.65	3.32	μA/MHz
	DMA2	4.21	3.83	3.49	
	Flash	13.53	12.32	11.44	
	SRAM	2.23	2.06	1.88	
	GPIOA	0.66	0.58	0.54	
	GPIOB	0.61	0.54	0.49	
	GPIOC	0.55	0.49	0.45	
	GPIOD	0.55	0.49	0.45	
	GPIOE	0.61	0.55	0.50	
	GPIOF	0.54	0.47	0.43	
	GPIOG	0.58	0.52	0.47	
	GPIOH	0.56	0.50	0.46	
	XMC	7.81	7.12	6.49	
	CRC	0.43	0.38	0.36	
	EMAC EMAC_TX EMAC_RX EMAC_PTP	11.61	10.60	9.67	
AHB2	AES	5.25	4.81	4.39	μA/MHz
	TRNG	5.36	4.89	4.47	
	OTGFS1	15.57	14.27	13.28	
	SDIO1	8.60	7.83	7.15	
AHB3	XMC	7.81	7.12	6.49	μA/MHz
	QSPI1	13.72	12.48	11.37	
APB1	TMR2	9.96	9.13	8.36	μA/MHz
	TMR3	7.06	6.45	5.91	
	TMR4	7.55	6.90	6.30	
	TMR5	10.1	9.26	8.48	
	TMR6	0.47	0.42	0.39	
	TMR7	0.47	0.42	0.39	
	TMR12	5.93	5.43	4.97	
	TMR13	3.72	3.39	3.10	
	TMR14	3.78	3.45	3.16	
	WWDT	0.14	0.13	0.12	

Peripheral		LDO voltage (V)			Unit
		1.3	1.2	1.1	
APB1	SPI2/I²S2	3.74	3.42	3.14	μA/MHz
	SPI3/I²S3	4.60	4.20	3.85	
	USART2	3.23	2.94	2.68	
	USART3	3.21	2.92	2.66	
	USART4	3.23	2.94	2.69	
	USART5	3.24	2.95	2.68	
	I²C1	6.34	5.77	5.25	
	I²C2	6.26	5.70	5.19	
	I²C3	6.31	5.75	5.23	
	CAN1	3.84	3.51	3.28	
	CAN2	3.85	3.51	3.26	
	CAN3	3.84	3.51	3.26	
	PWC	0.99	0.91	0.83	
	DAC1/2	1.42	1.30	1.20	
	USART7	3.20	2.91	2.66	
	USART8	3.25	2.95	2.70	
APB2	TMR1	10.68	9.70	8.82	μA/MHz
	TMR8	10.58	9.62	8.75	
	USART1	3.25	2.94	2.69	
	USART6	3.26	2.96	2.70	
	ADC1	9.04	8.25	7.52	
	ADC2	8.93	8.13	7.41	
	SPI1/I²S1	3.20	2.92	2.68	
	SPI4/I²S4	3.19	2.91	2.66	
	SCFG	2.19	1.98	1.82	
	EXINT	2.20	1.99	1.82	
	TMR9	5.90	5.37	4.90	
	TMR10	3.62	3.30	3.01	
	TMR11	3.90	3.54	3.25	
	I²SF5	1.01	0.92	0.84	
	ACC	0.25	0.21	0.19	
	I²S2EXT	3.08	2.81	2.58	
	I²S3EXT	3.09	2.80	2.58	

4.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be generated with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

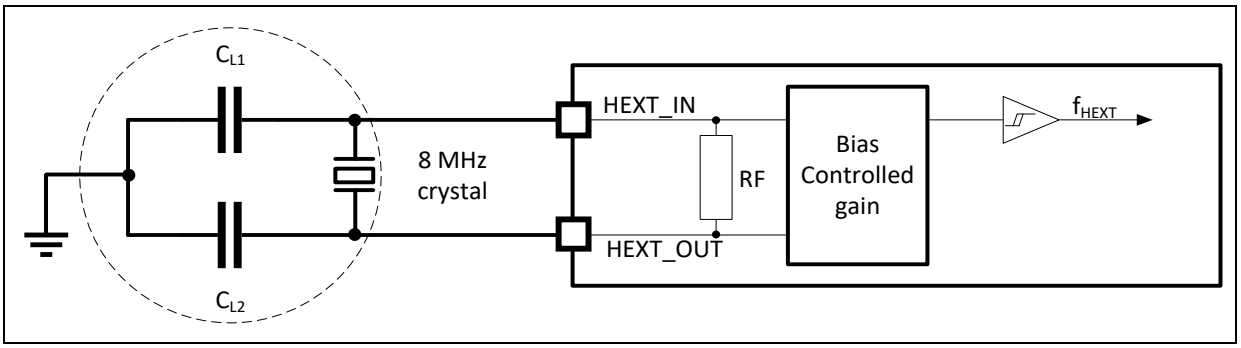
Table 30. HEXT 4 ~ 25 MHz crystal characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HEXT_IN}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	8 MHz, HEXTDRV = 0x2	-	2.3	-	ms
$I_{DD(HEXT)}$	Current consumption	8 MHz, HEXTDRV = 0x2	-	440	600	μA

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 33 pF range (typ.), designed for high-frequency applications, and selected to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be taken into account when selecting C_{L1} and C_{L2}. The load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 12. HEXT typical application with 8 MHz crystal



High-speed external clock generated from an external source

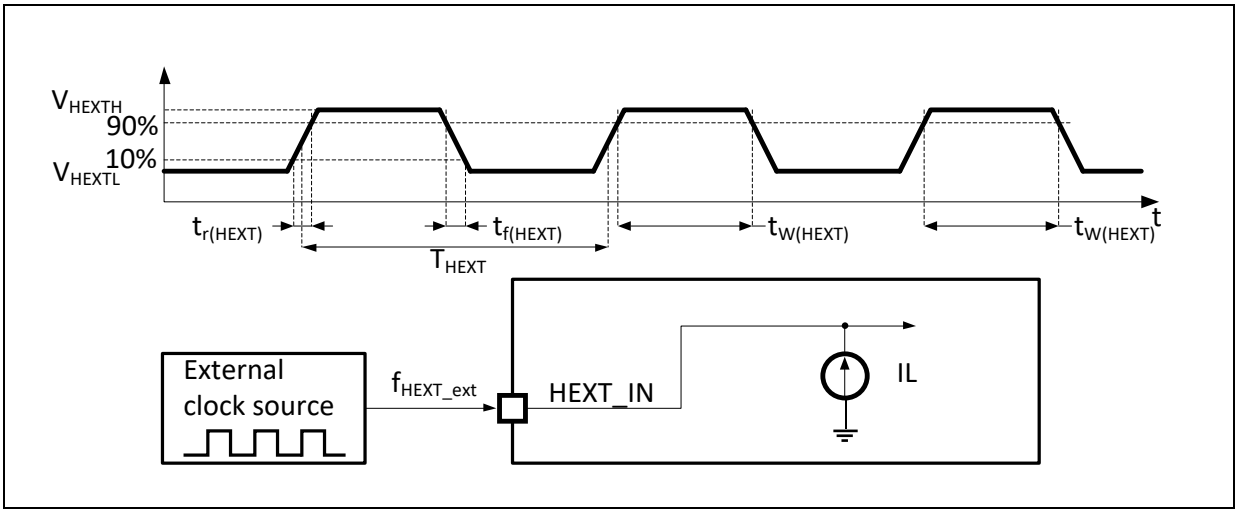
The characteristics given in the table below come from tests performed using a high-speed external clock source.

Table 31. HEXT external source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency (1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time (1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time (1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance (1)	-	-	5	-	pF
$Duty_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 13. High-speed external clock source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be generated with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

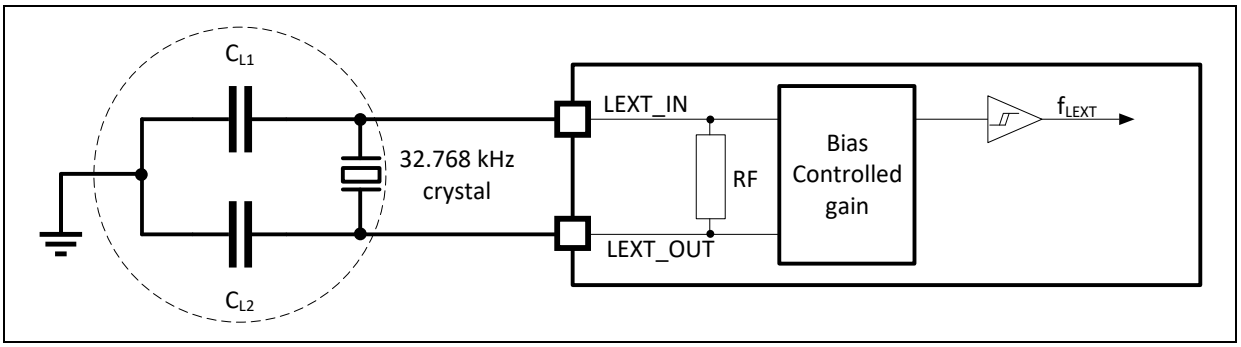
Table 32. LEXT 32.768 kHz crystal characteristics(1)(2)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	LEXTDRV = 0x3	-	90	-	ms

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range and select to meet the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance that is the series combination of C_{L1} and C_{L2}. The load capacitance C_L is based on the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 14. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT and it is also prohibited to add it.

Low-speed external clock generated from an external source

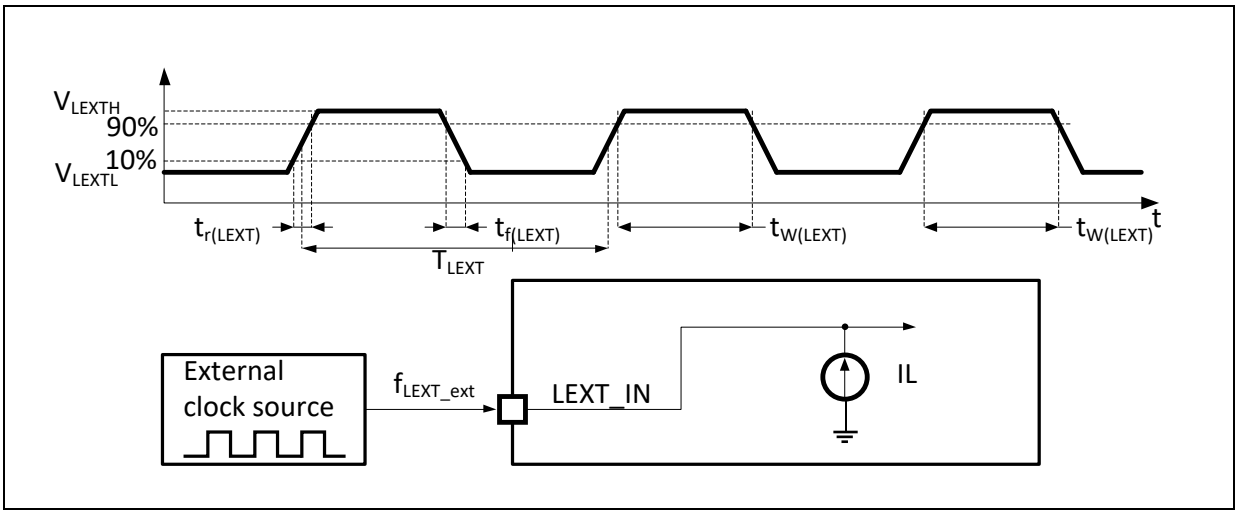
The characteristics given in the table below come from tests performed using a low-speed external clock source.

Table 33. Low-speed external source characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LEXT_ext}	User external clock source frequency(1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time (1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time (1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance (1)	-	-	5	-	pF
$Duty_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 15. Low-speed external clock source AC timing diagram



4.3.7 Internal clock source characteristics

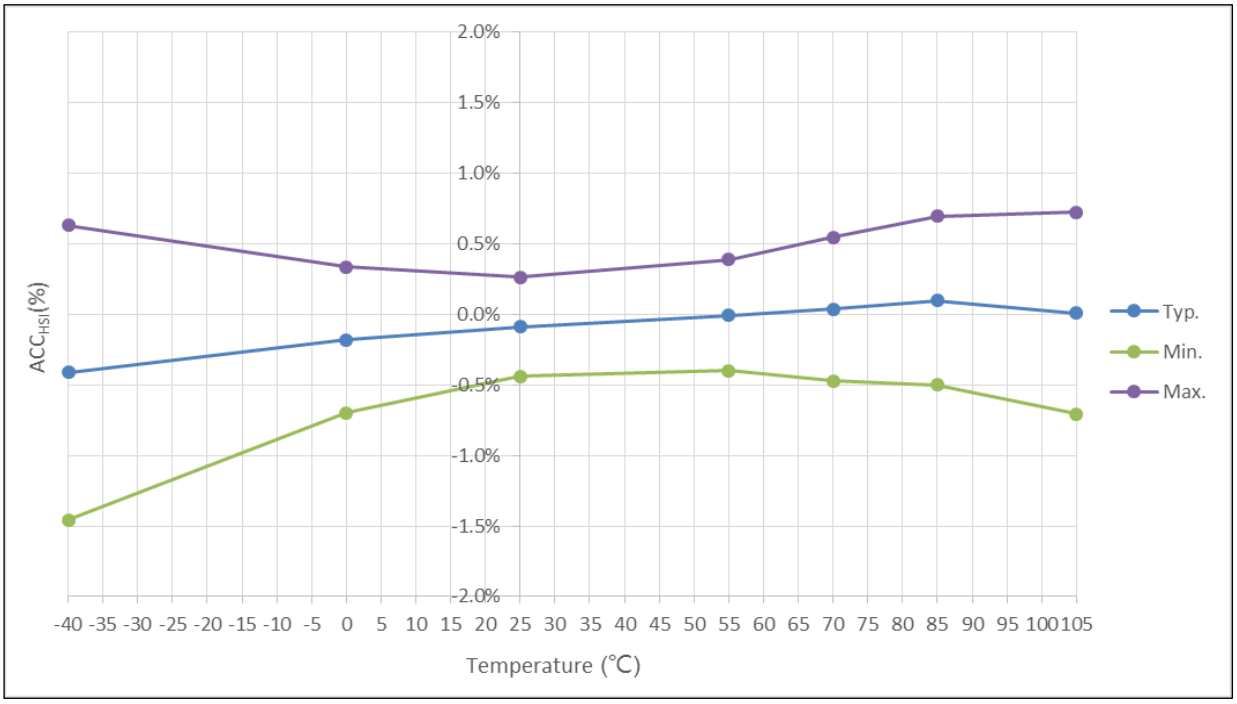
High-speed internal clock (HICK)

Table 34. HICK clock characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
f_{HICK}	Frequency	-		-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-		45	-	55	%
ACC_{HICK}	HICK clock accuracy	User-trimmed with the CRM_CTRL register(1)		-1	-	1	%
		ACC calibration(1)		-0.25	-	0.25	
		Factory-calibrated (2)	T_A = -40 ~ 105 °C	-2	-	1.5	
			T_A = -40 ~ 85 °C	-2	-	1.2	
			T_A = 0 ~ 70 °C	-1.5	-	1.2	
			T_A = 25 °C	-1	-	1	
$t_{SU(HICK)}$(2)	HICK startup time	-		-	1.8	2.0	µs
$I_{DD(HICK)}$(2)	HICK power consumption	-		-	220	240	µA

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 16. HICK clock frequency accuracy vs. temperature



Low-speed internal clock (LICK)

Table 35. LICK clock characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	25	35	45	kHz

(1) Guaranteed by characterization results, not tested in production.

4.3.8 PLL characteristics

Table 36. PLL characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
f_{PLL_IN}	PLL input clock(2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	24	-	192	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Use the appropriate multiplier factor to ensure that PLL input clock values are compatible with the range defined by f_{PLL_OUT}.

4.3.9 Wakeup time from low-power modes

The wakeup times given in the table below are measured on a wakeup phase with the HICK. The clock source used to wake up the device depends on the current operating mode:

- Sleep mode: The clock source is the clock that was configured before entering Sleep mode.
- Deepsleep or Standby mode: The clock source is the HICK.

Table 37. Low-power mode wakeup time

Symbol	Parameter	Condition	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	-	2.3	µs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode	LDO in normal mode	450	µs
		LDO in extra low-power mode	520	
$t_{WUSTDBY}$	Wakeup from Standby mode	-	800	µs

4.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional error occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 38. EMS characteristics

Sym.	Parameter	Condition	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforming to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional error. Both V_{DD} and V_{SS} have a 47 µF capacitor on their entries. Each V_{DD} and V_{SS} pair has a 0.1 µF bypass capacitor.	V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 192 MHz	4A (±4 kV)
		V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 160 MHz	
		V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 108 MHz	
		V_{DD} = 3.3 V, LQFP144, T_A = +25 °C, f_{HCLK} = 8 MHz	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore, it is recommended that the user applies EMC optimization and prequalification tests in relation with the EMC level.

4.3.11 GPIO port characteristics

General input/output characteristics

All GPIOs are CMOS and TTL compliant.

Table 39. GPIO static characteristics

Sym.	Parameter	Condition	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	-0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	TC GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT, FTa and FTf CPIO input high level voltage	-		-	5.5	
V_{hys}	Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input floating mode leakage current(2)	$V_{SS} \le V_{IN} \le V_{DD}$ TC GPIO	-	-	±1	µA
		$V_{SS} \le V_{IN} \le 5.5$ V FT, FTa and FTf GPIOs (PA11 and PA12 excluded)	-	-	±1	
		$V_{SS} \le V_{IN} \le 5.5$ V PA11 and PA12	-	-	±15	
R_{PU}	Weak pull-up equivalent resistor(3)	$V_{IN} = V_{SS}$	60	80	130	kΩ
R_{PD}	Weak pull-down equivalent resistor(3)(4)	$V_{IN} = V_{DD}$	60	70	130	kΩ
C_{IO}	GPIO pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
(2) Leakage could be higher than the max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up/pull-down resistors must be disabled for FT, FTf and FTa pins.
(4) The weak pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics take into account the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in Section *4.2.1*.

- The sum of the currents sourced by all GPIOs on V_{DD}, plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 13*).
- The sum of the currents sunk by all GPIOs on V_{SS}, plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot exceed the absolute maximum rating I_{VSS} (see *Table 13*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 40. Output voltage characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL port, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}	Output low level voltage	I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL port, I_{IO} = 5 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}	Output low level voltage	I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Maximum sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS port, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL port, I_{IO} = 12 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 12 mA	-	0.4	V
V_{OH}	Output high level voltage	2.4 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Ultra high sourcing/sinking strength(2)					
V_{OL}	Output low level voltage	I_{IO} = 25 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OL}	Output low level voltage	I_{IO} = 18 mA, 2.4 V ≤ V_{DD} < 2.7 V			

(1) Guaranteed by characterization results, not tested in production.
(2) When GPIO ultra high sinking strength is enabled, its V_{OH} is the same as that of maximum sourcing strength.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 41. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$(1)	Pulse width of external signals detected by EXINT controller	10	-	ns

(1) Guaranteed by design, not tested in production.

4.3.12 NRST pin characteristics

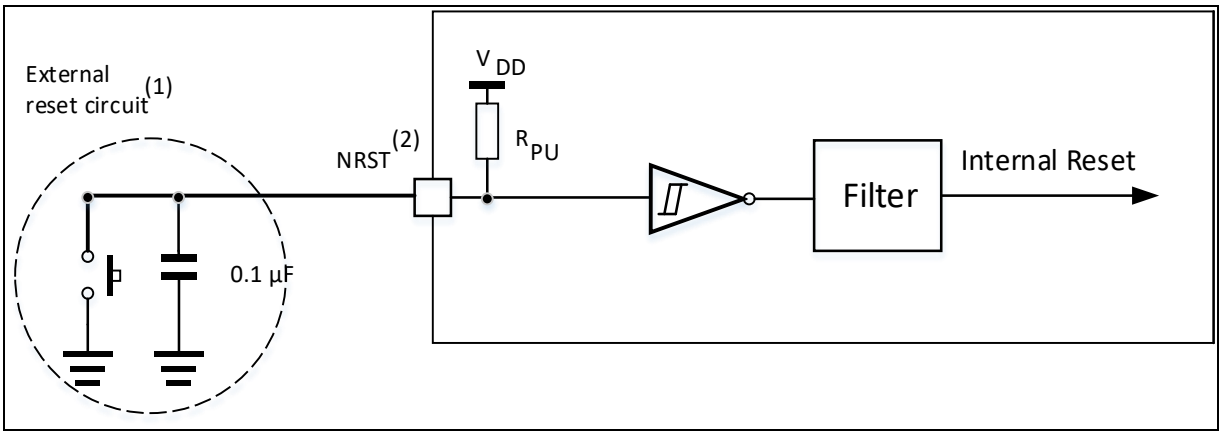
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 42. NRST pin characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	-	-0.3	-	0.72	V
$V_{IH(NRST)}$(1)	NRST input high level voltage	-	2	-	V_{DD} + 0.3	
$V_{hys(NRST)}$(1)	NRST Schmitt trigger voltage hysteresis	-	-	400	-	mV
R_{PU}(2)	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level inactive	-	-	-	40	µs
$t_{ILNV(NRST)}$(1)	NRST input low level active	-	80	-	-	µs

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production.

Figure 17. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) The user must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 42*. Otherwise, the reset will not be performed by the device.

4.3.13 XMC (including SDRAM) characteristics

Parameters listed in the table below are guaranteed by design, not tested in production.

Asynchronous waveforms and timings of SRAM/PSRAM/NOR

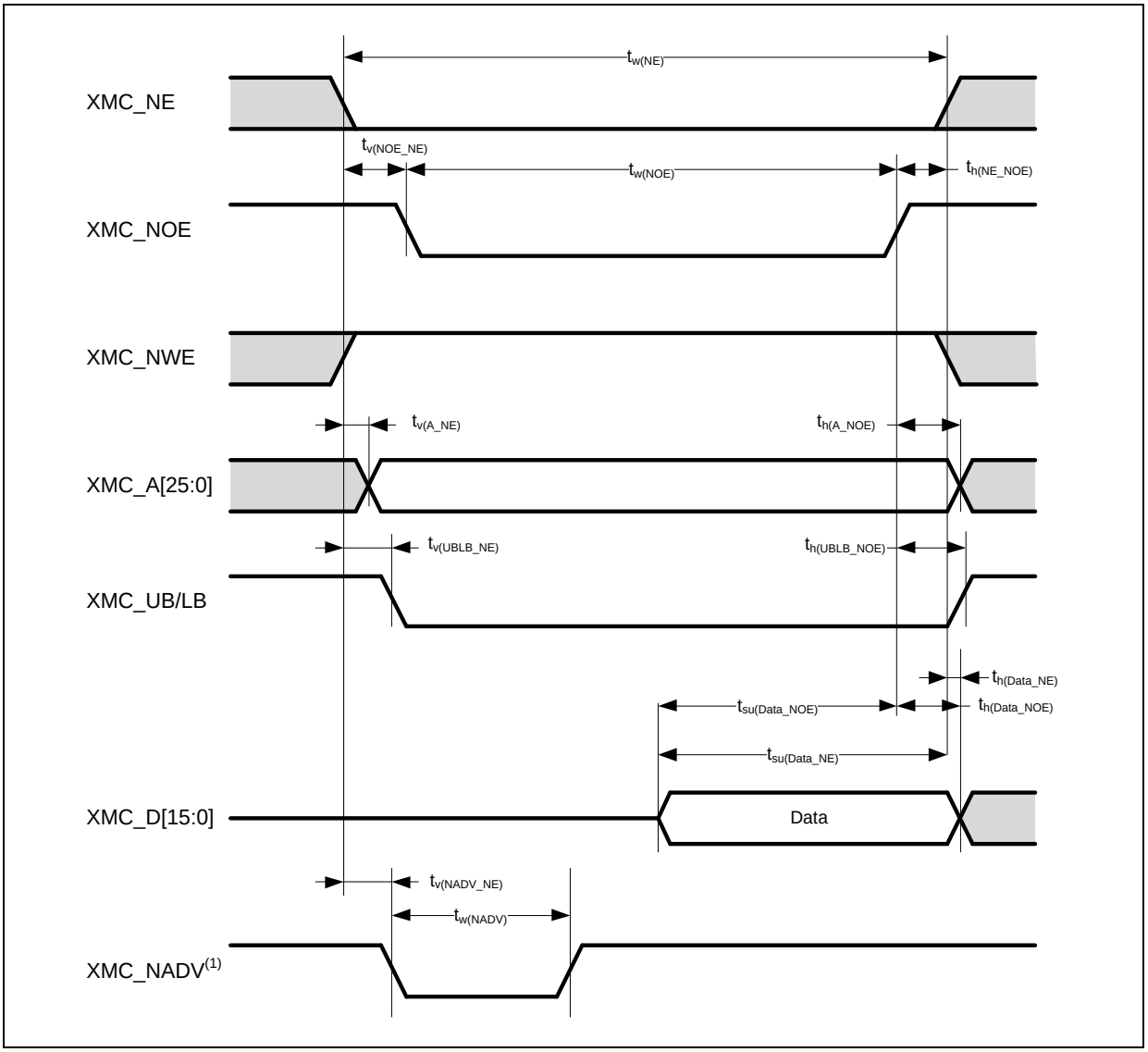
The results given in these tables are obtained with the following XMC configuration:

- AddressSetupTime = 0
- AddressHoldTime = 1
- DataSetupTime = 1

Table 43. Asynchronous non-multiplexed SRAM/PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$5t_{HCLK}$ - 1.5	$5t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	XMC_NE low to XMC_NOE low valid time	0.5	1.5	ns
$t_{w(NOE)}$	XMC_NOE low time	$5t_{HCLK}$ - 1.5	$5t_{HCLK}$ + 1.5	ns
$t_{h(NE\_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1.5	-	ns
$t_{v(A\_NE)}$	XMC_NE low to XMC_A valid time	-	7	ns
$t_{h(A\_NOE)}$	Address hold time after XMC_NOE high	2.5	-	ns
$t_{v(UBLB\_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	0	ns
$t_{h(UBLB\_NOE)}$	XMC_UB/LB hold time after XMC_NOE high	2.5	-	ns
$t_{su(Data\_NE)}$	Data to XMC_NE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{su(Data\_NOE)}$	Data to XMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NOE)}$	Data hold time after XMC_NOE high	0	-	ns
$t_{h(Data\_NE)}$	Data hold time after XMC_NE high	0	-	ns
$t_{v(NADV\_NE)}$	XMC_NE low to XMC_NADV low valid time	-	5	ns
$t_{w(NADV)}$	XMC_NADV low time	-	t_{HCLK} + 1.5	ns

Figure 18. Asynchronous non-multiplexed SRAM/PSRAM/NOR read waveforms

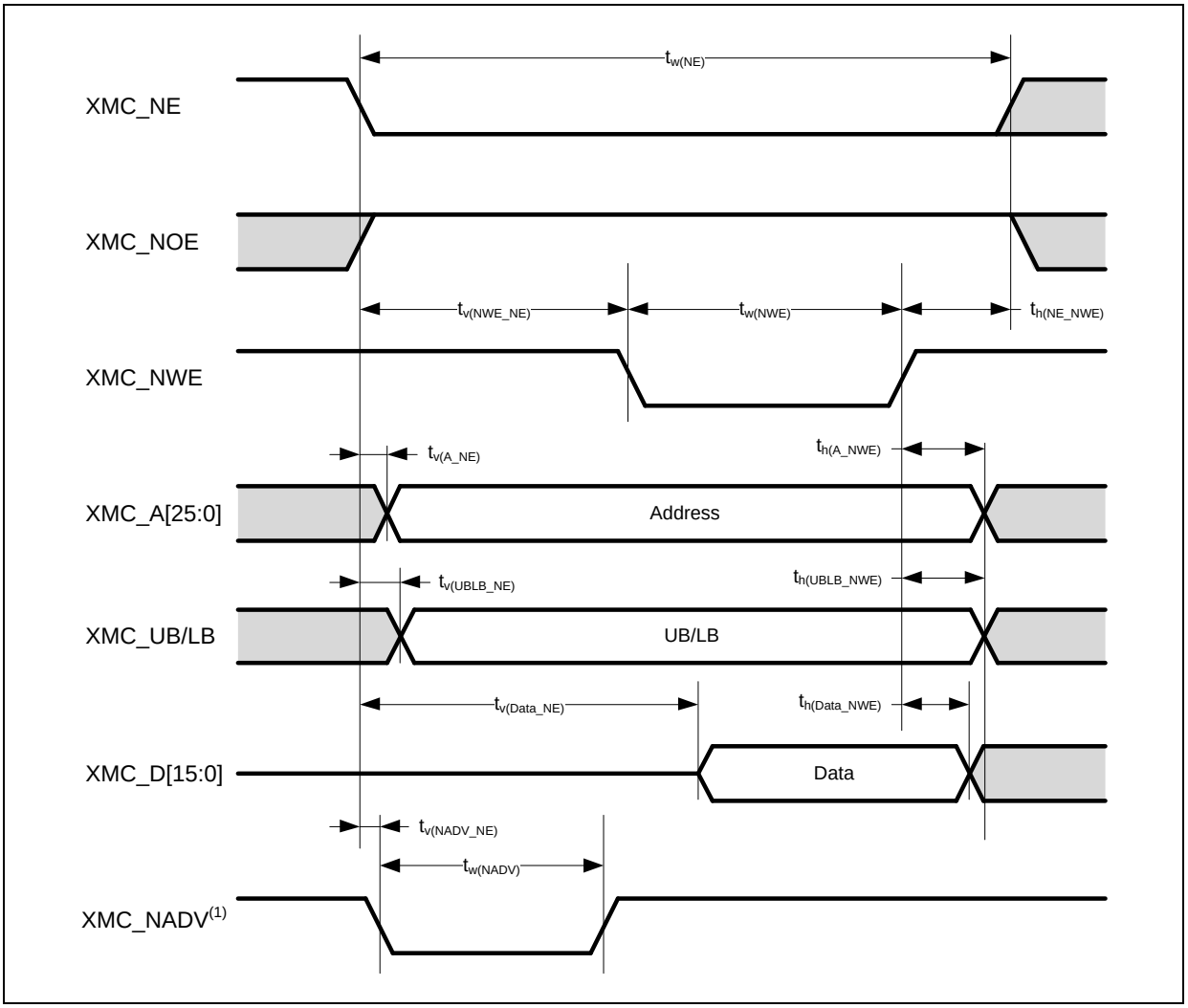


(1) Only available in mode 2/B, C and D. XMC_NADV is not used in mode 1.

Table 44. Asynchronous non-multiplexed SRAM/PSRAM/NOR write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$4t_{HCLK} – 1.5$	$4t_{HCLK} + 2$	ns
$t_{v(NWE\_NE)}$	XMC_NE low to XMC_NWE low valid time	t_{HCLK} - 0.5	t_{HCLK} + 1.5	ns
$t_{w(NWE)}$	XMC_NWE low time	$2t_{HCLK}$ - 0.5	$2t_{HCLK}$ + 1.5	ns
$t_{h(NE\_NWE)}$	XMC_NWE high to XMC_NE high hold time	t_{HCLK} - 0.5	-	ns
$t_{v(A\_NE)}$	XMC_NE low to XMC_A valid time	-	7.5	ns
$t_{h(A\_NWE)}$	Address hold time after XMC_NWE high	t_{HCLK} + 2	-	ns
$t_{v(UBLB\_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	1.5	ns
$t_{h(UBLB\_NWE)}$	XMC_UB/LB hold time after XMC_NWE high	t_{HCLK} - 0.5	-	ns
$t_{v(Data\_NE)}$	XMC_NE low to data valid time	-	t_{HCLK} + 7	ns
$t_{h(Data\_NWE)}$	Data hold time after XMC_NWE high	t_{HCLK} + 3	-	ns
$t_{v(NADV\_NE)}$	XMC_NE low to XMC_NADV low valid time	-	5.5	ns
$t_{w(NADV)}$	XMC_NADV low time	-	t_{HCLK} + 1.5	ns

Figure 19. Asynchronous non-multiplexed SRAM/PSRAM/NOR write waveforms



(1) Only available in mode 2/B, C and D. XMC_NADV is not used in mode 1.

Table 45. Asynchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$8t_{HCLK}$ - 2	$8t_{HCLK}$ + 2	ns
$t_{v(NOE\_NE)}$	XMC_NE low to XMC_NOE low valid time	$4t_{HCLK}$ - 0.5	$4t_{HCLK}$ + 1.5	ns
$t_{w(NOE)}$	XMC_NOE low time	$4t_{HCLK}$ - 1	$4t_{HCLK}$ + 2	ns
$t_{h(NE\_NOE)}$	XMC_NOE high to XMC_NE high hold time	-1	-	ns
$t_{v(A\_NE)}$	XMC_NE low to XMC_A valid time	-	7	ns
$t_{v(NADV\_NE)}$	XMC_NE low to XMC_NADV low valid time	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1.5	t_{HCLK} + 1.5	ns
$t_{h(AD\_NADV)}$	XMC_AD (address) valid hold time after XMC_NADV high	t_{HCLK} + 3	-	ns
$t_{h(A\_NOE)}$	Address hold time after XMC_NOE high	t_{HCLK} + 3	-	ns
$t_{h(UBLB\_NOE)}$	XMC_UB/LB hold time after XMC_NOE high	0	-	ns
$t_{v(UBLB\_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	0	ns
$t_{su(Data\_NE)}$	Data to XMC_NE high setup time	$2t_{HCLK}$ + 24	-	ns
$t_{su(Data\_NOE)}$	Data to XMC_NOE high setup time	$2t_{HCLK}$ + 25	-	ns
$t_{h(Data\_NE)}$	Data hold time after XMC_NE high	0	-	ns
$t_{h(Data\_NOE)}$	Data hold time after XMC_NOE high	0	-	ns

Figure 20. Asynchronous multiplexed PSRAM/NOR read waveforms

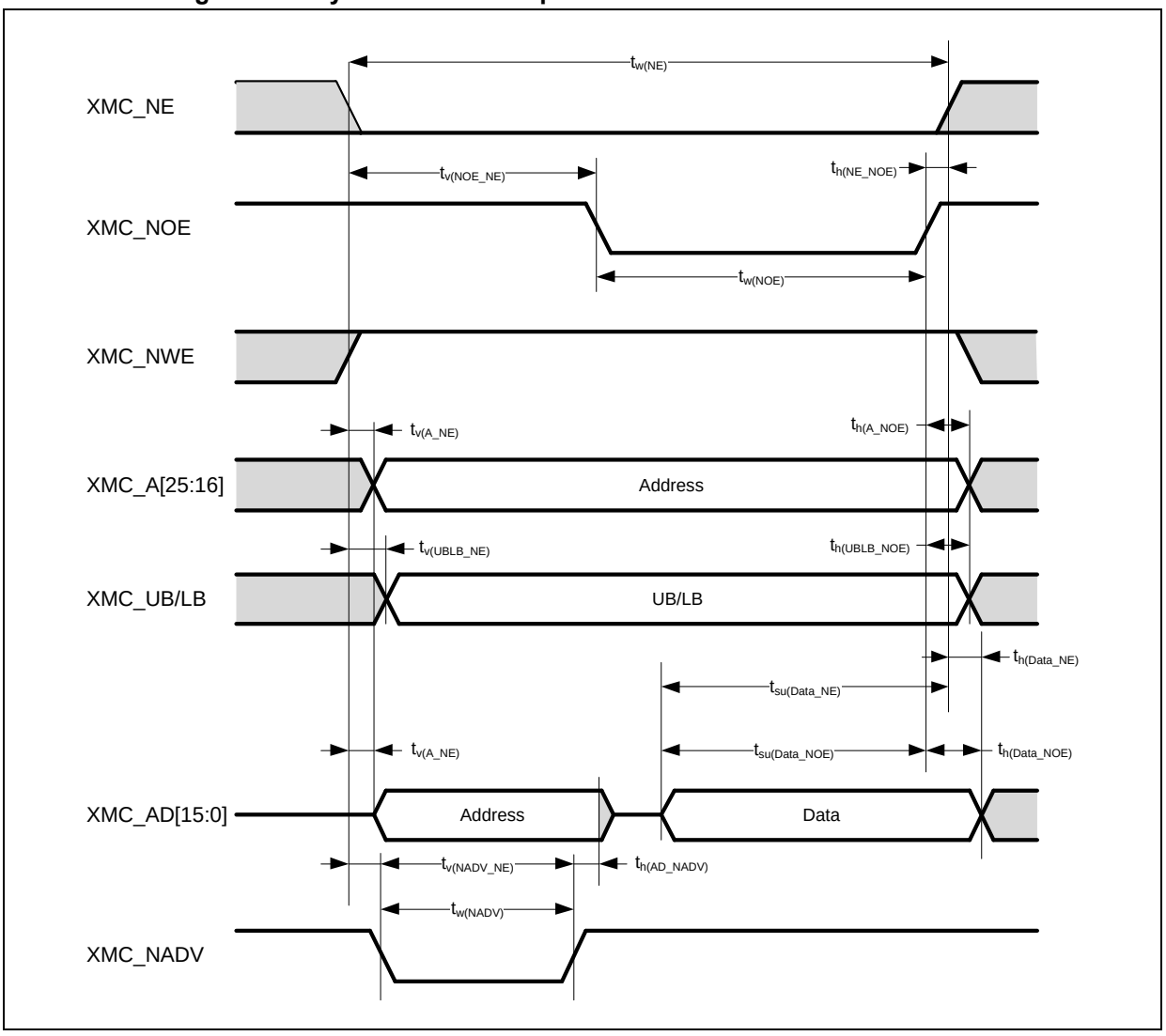
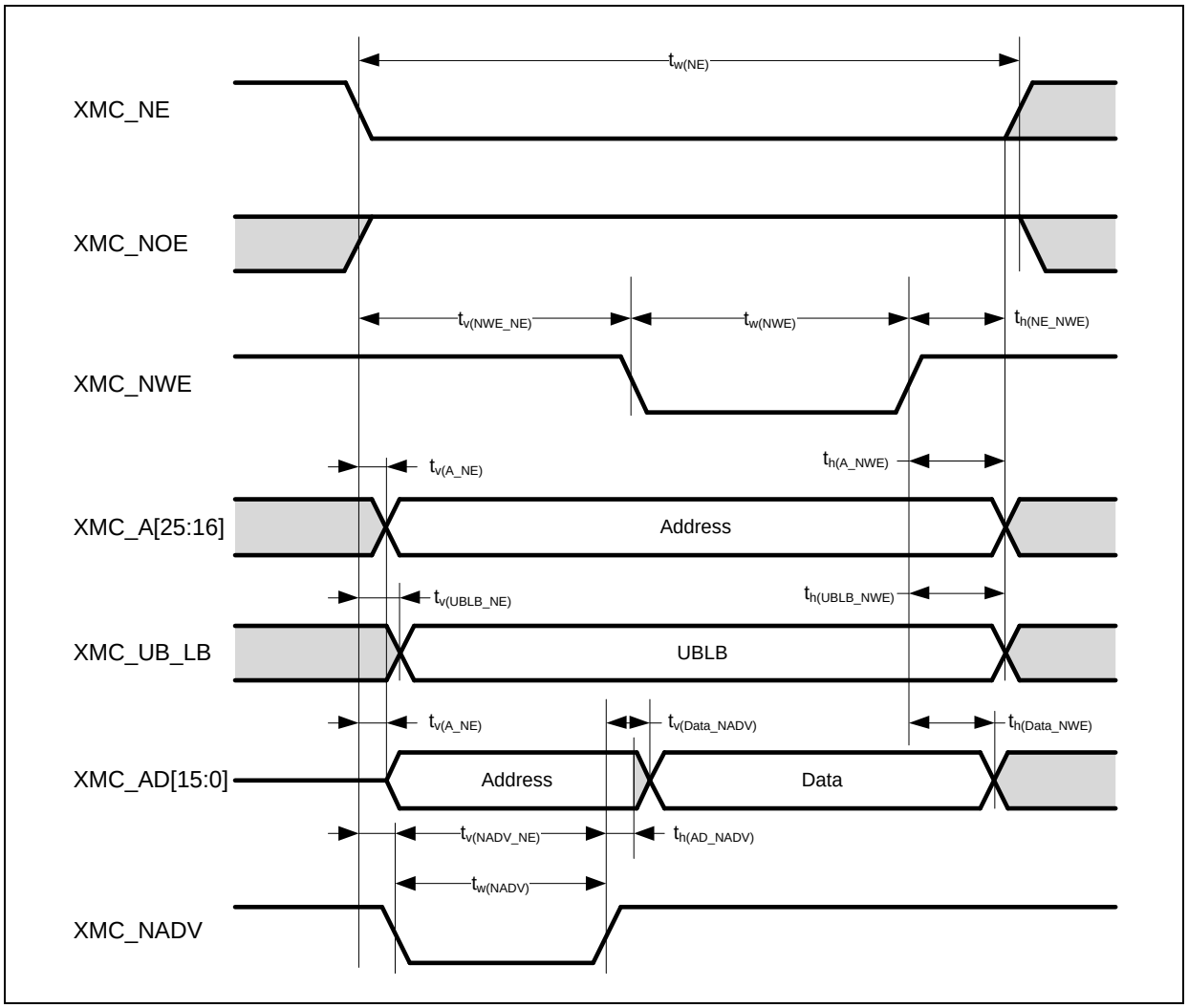


Table 46. Asynchronous multiplexed PSRAM/NOR write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(NE)}$	XMC_NE low time	$7t_{HCLK}$ - 1	$7t_{HCLK}$ + 2	ns
$t_{v(NWE\_NE)}$	XMC_NE low to XMC_NWE low valid time	t_{HCLK}	t_{HCLK} + 1	ns
$t_{w(NWE)}$	XMC_NWE low time	$5t_{HCLK}$ - 1	$5t_{HCLK}$ + 2	ns
$t_{h(NE\_NWE)}$	XMC_NWE high to XMC_NE high hold time	t_{HCLK} - 1	-	ns
$t_{v(A\_NE)}$	XMC_NE low to XMC_A valid time	-	7	ns
$t_{v(NADV\_NE)}$	XMC_NE low to XMC_NADV low valid time	3	5	ns
$t_{w(NADV)}$	XMC_NADV low time	t_{HCLK} - 1	t_{HCLK} + 1	ns
$t_{h(AD\_NADV)}$	XMC_AD (address) hold time after XMC_NADV high	t_{HCLK} - 3	-	ns
$t_{h(A\_NWE)}$	Address hold time after XMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{h(UBLB\_NWE)}$	XMC_UB/LB hold time after XMC_NWE high	t_{HCLK} - 1.5	-	ns
$t_{v(UBLB\_NE)}$	XMC_NE low to XMC_UB/LB valid time	-	1.6	ns
$t_{v(Data\_NADV)}$	XMC_NADV high to data valid time	-	$2t_{HCLK}$ + 1.5	ns
$t_{h(Data\_NWE)}$	Data hold time after XMC_NWE high	t_{HCLK} - 5	-	ns

Figure 21. Asynchronous multiplexed PSRAM/NOR write waveforms



Synchronous waveforms and timings of PSRAM/NOR

The results given in these tables are obtained with the following XMC configuration:

- BurstAccessMode = XMC_BurstAccessMode_Enable
- MemoryType = XMC_MemoryType_CRAM
- WriteBurst = XMC_WriteBurst_Enable
- CLKPrescale = 1 (1 memory cycle = 2 HCLK cycles) (note: CLKPrescale is the CLKPSC bit in the XMC_BK1TMGx register; refer to AT32F455/456/457 series reference manual)
- DataLatency = 1 for NOR; DataLatency = 0 for PSRAM (note: DataLatency is the DATLAT bit in the XMC_BK1TMGx register; refer to AT32F455/456/457 series reference manual)

Table 47. Synchronous non-multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKH-NOEL)}$	XMC_CLK high to XMC_NOE low	-	2	ns
$t_{d(CLKL-NOEH)}$	XMC_CLK low to XMC_NOE high	0.5	-	ns
$t_{su(DV-CLKH)}$	XMC_D valid data before XMC_CLK high	6.5	-	ns
$t_{h(CLKH-DV)}$	XMC_D valid data after XMC_CLK high	7	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	2	-	ns

Figure 22. Synchronous non-multiplexed PSRAM/NOR read waveforms

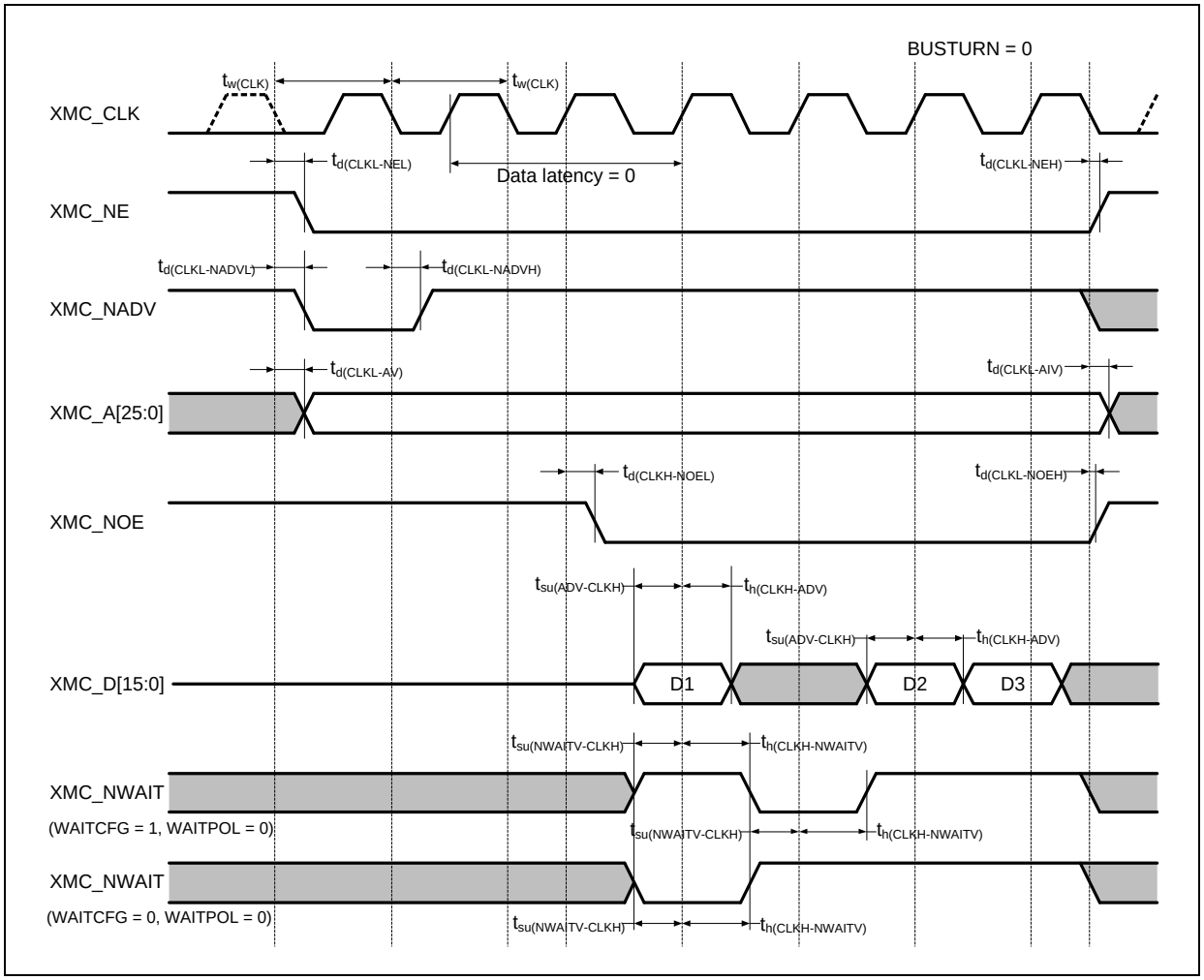


Table 48. Synchronous non-multiplexed PSRAM write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	XMC_CLK low to XMC_NWE high	0.5	-	ns
$t_{d(CLKL-Data)}$	XMC_D after XMC_CLK low	-	6	ns
$t_{d(CLKL-UBLBH)}$	XMC_CLK low to XMC_UB/LB high	1.5	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	7	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	2	-	ns

Figure 23. Synchronous non-multiplexed PSRAM write waveforms

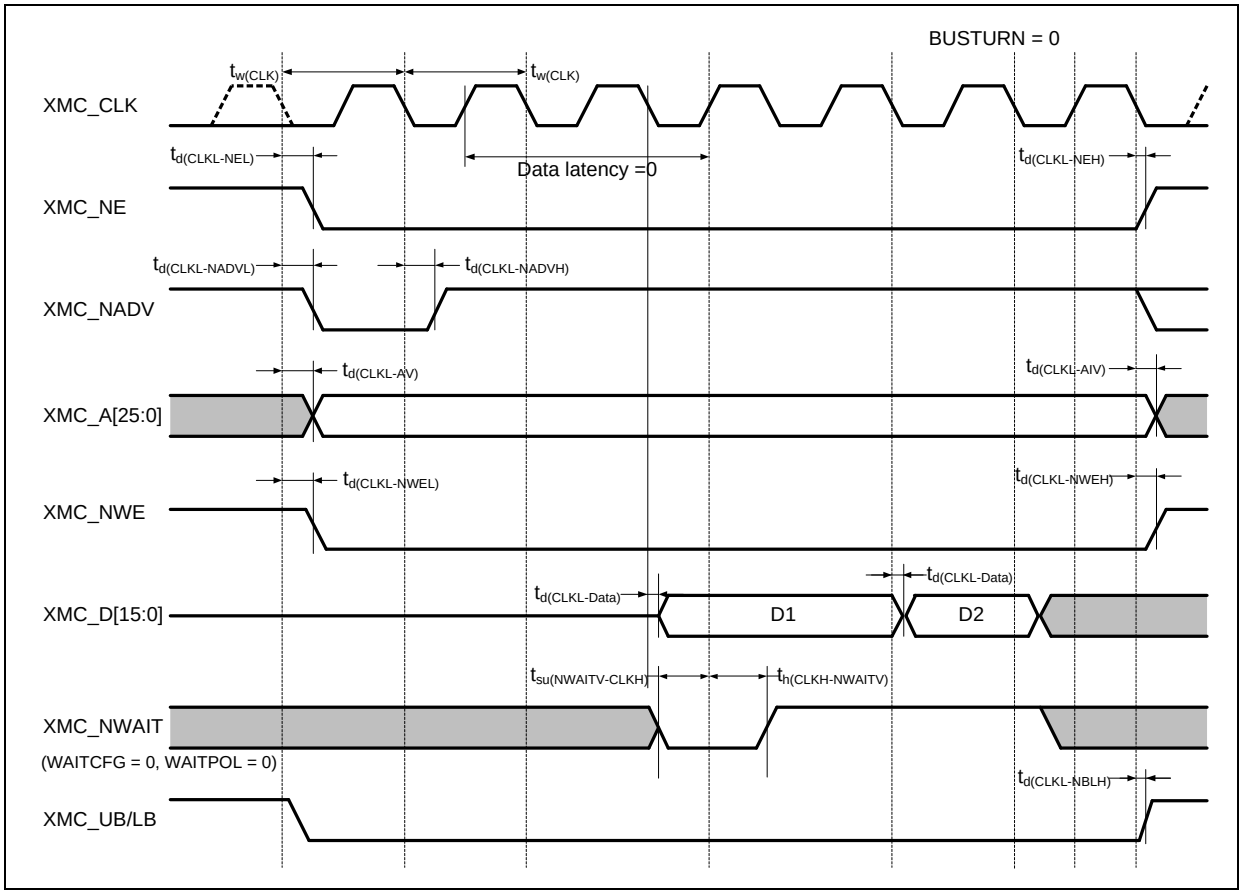


Table 49. Synchronous multiplexed PSRAM/NOR read timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKH-NOEL)}$	XMC_CLK high to XMC_NOE low	-	1	ns
$t_{d(CLKL-NOEH)}$	XMC_CLK low to XMC_NOE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD invalid	0	-	ns
$t_{su(ADV-CLKH)}$	XMC_AD valid before XMC_CLK high	6	-	ns
$t_{h(CLKH-ADV)}$	XMC_AD valid after XMC_CLK high	6	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	6	-	ns

Figure 24. Synchronous multiplexed PSRAM/NOR read waveforms

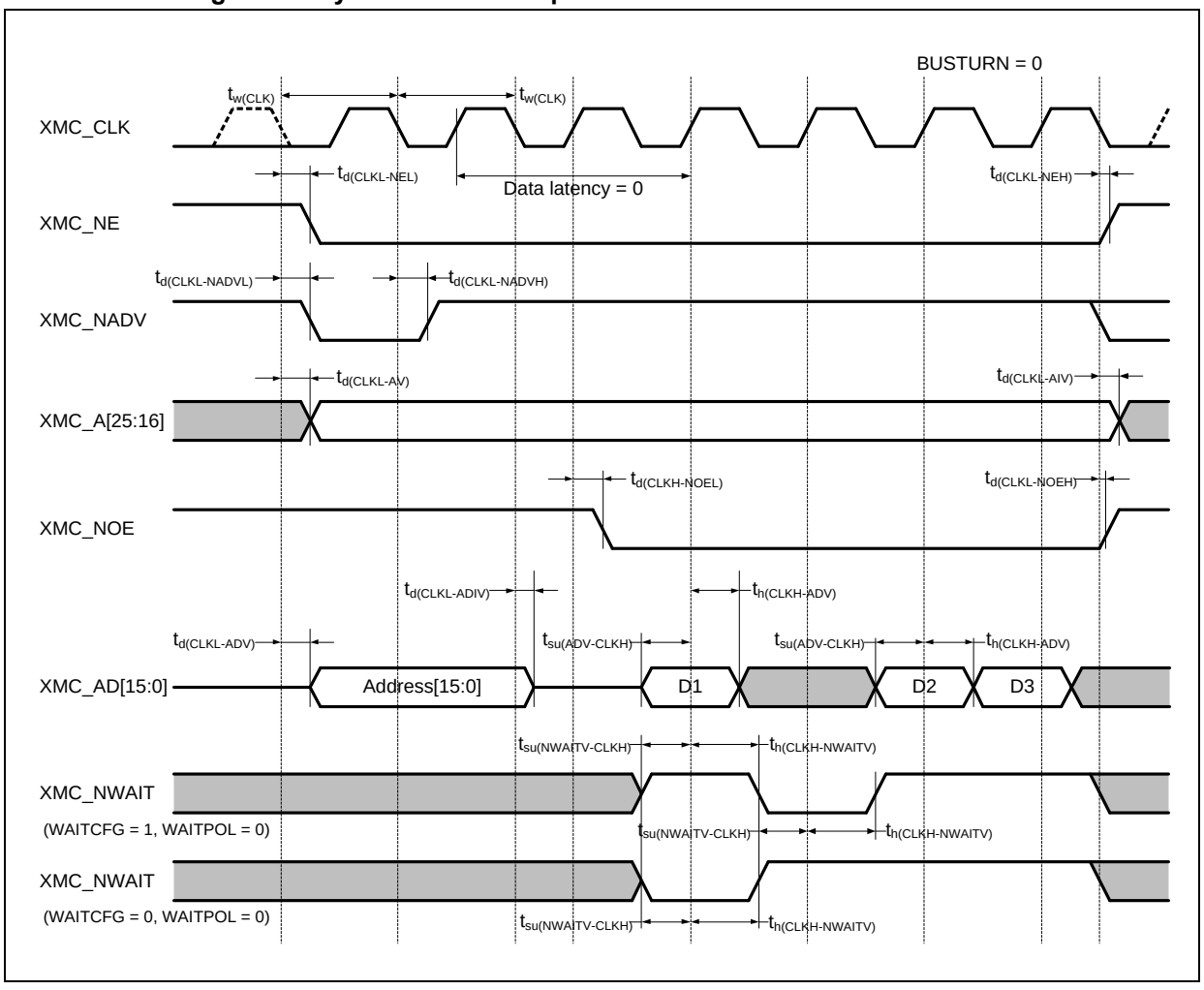
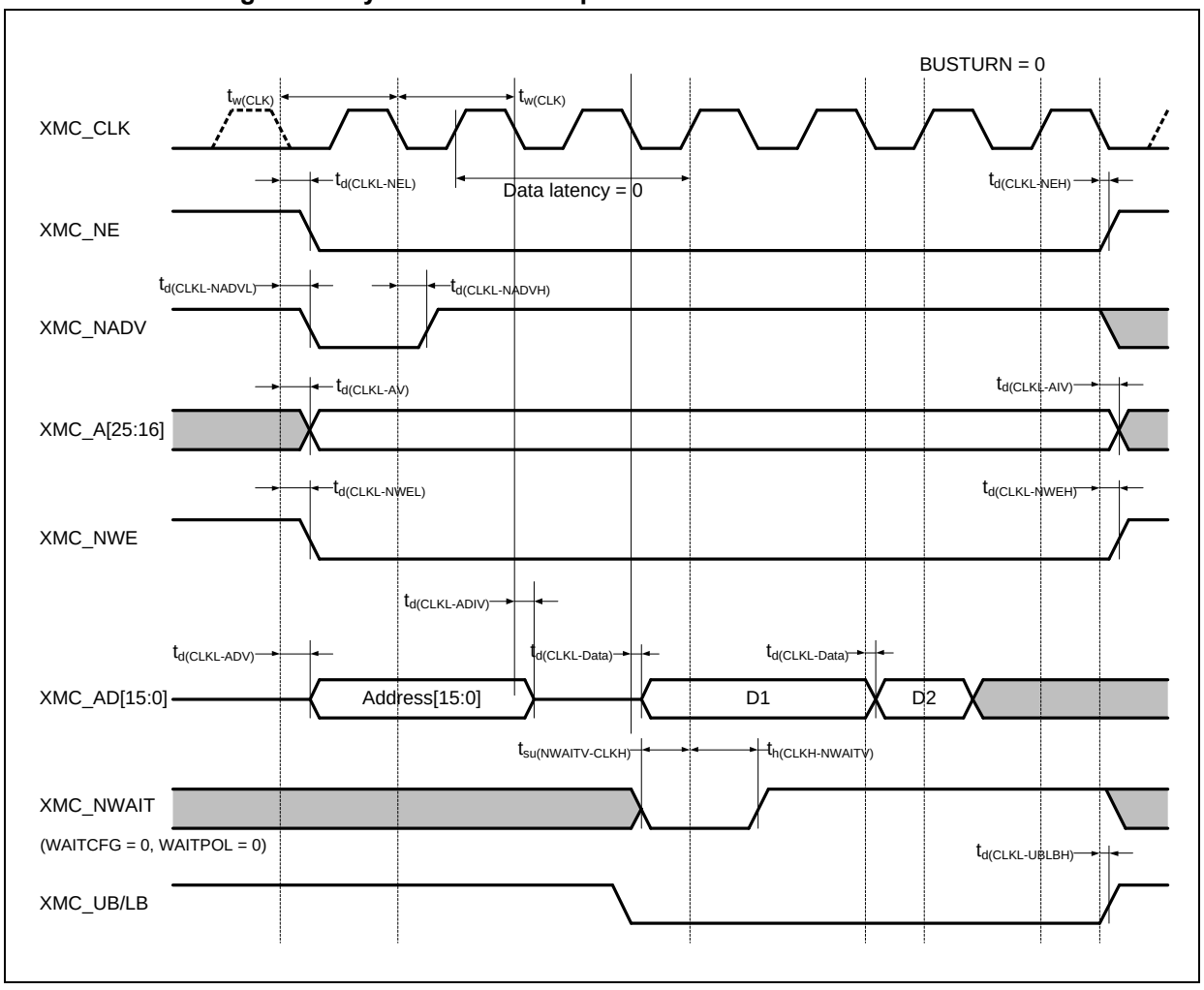


Table 50. Synchronous multiplexed PSRAM write timings

Symbol	Parameter	Min	Max	Unit
$t_{w(CLK)}$	XMC_CLK period	20	-	ns
$t_{d(CLKL-NEL)}$	XMC_CLK low to XMC_NE low	-	2	ns
$t_{d(CLKL-NEH)}$	XMC_CLK low to XMC_NE high	1	-	ns
$t_{d(CLKL-NADVL)}$	XMC_CLK low to XMC_NADV low	-	4	ns
$t_{d(CLKL-NADVH)}$	XMC_CLK low to XMC_NADV high	1	-	ns
$t_{d(CLKL-AV)}$	XMC_CLK low to XMC_A valid	-	2	ns
$t_{d(CLKL-AIV)}$	XMC_CLK low to XMC_A invalid	0	-	ns
$t_{d(CLKL-NWEL)}$	XMC_CLK low to XMC_NWE low	-	1	ns
$t_{d(CLKL-NWEH)}$	XMC_CLK low to XMC_NWE high	0.5	-	ns
$t_{d(CLKL-ADV)}$	XMC_CLK low to XMC_AD valid	-	12	ns
$t_{d(CLKL-ADIV)}$	XMC_CLK low to XMC_AD invalid	3	-	ns
$t_{d(CLKL-Data)}$	XMC_AD after XMC_CLK low	-	6	ns
$t_{d(CLKL-UBLBH)}$	XMC_CLK low to XMC_UB/LB high	1	-	ns
$t_{su(NWAITV-CLKH)}$	XMC_NWAIT valid before XMC_CLK high	8	-	ns
$t_{h(CLKH-NWAITV)}$	XMC_NWAIT valid after XMC_CLK high	6	-	ns

Figure 25. Synchronous multiplexed PSRAM write waveforms



SDRAM controller timings and waveforms

GPIOs used for SDRAM are configured as large sourcing/sinking strength.

Table 51. SDRAM read timings

Symbol	Parameter	Condition	Min	Max	Unit
$1/t_{w(SDCLK)}$(1)	SDCLK frequency	LDO 1.3 V, T_A = 25 °C	-	192	MHz
		LDO 1.2 V, T_A = 25 °C	-	160	
		LDO 1.3/1.2 V, T_A = -40 ~ 105 °C	-	144	
		LDO 1.1 V, T_A = -40 ~ 105 °C	-	108	
$t_{su(SDCLKH\_Data)}$	Input data setup time	-	2	-	ns
$t_{h(SDCLKH\_Data)}$	Input data hold time	-	0	-	ns
$t_{d(SDCLKL\_Add)}$	Address valid time	-	-	1.5	ns
$t_{d(SDCLKL\_SDCS)}$	CS valid time	-	-	1	ns
$t_{h(SDCLKL\_SDCS)}$	CS hold time	-	0	-	ns
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	-	1	ns
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	-	0	-	ns
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	-	1	ns
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	-	0	-	ns

(1) Guaranteed by characterization results, not tested in production. The maximum clock frequency is highly relevant to the device and PCB layout. For detailed solutions, please contact your local Artery sales office.

Figure 26. SDRAM read waveforms

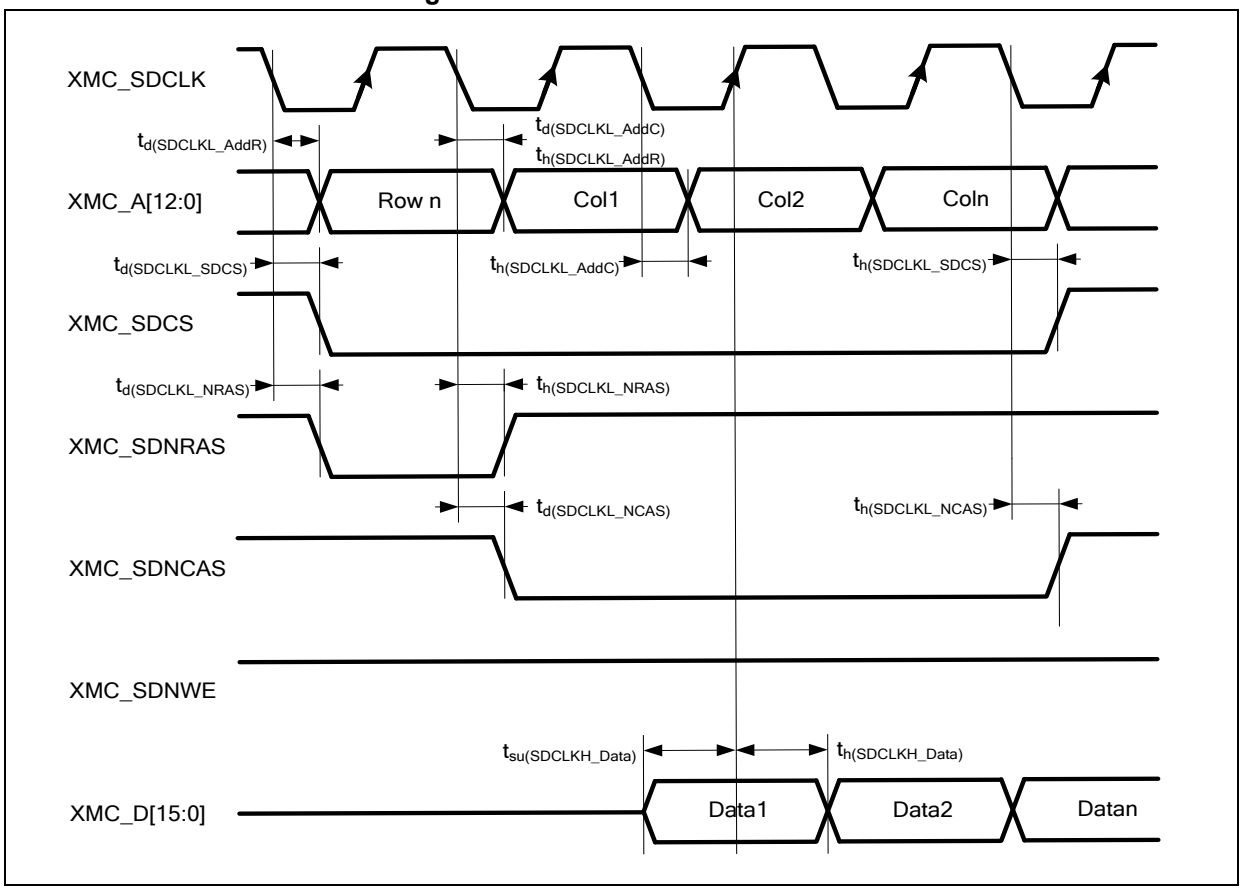
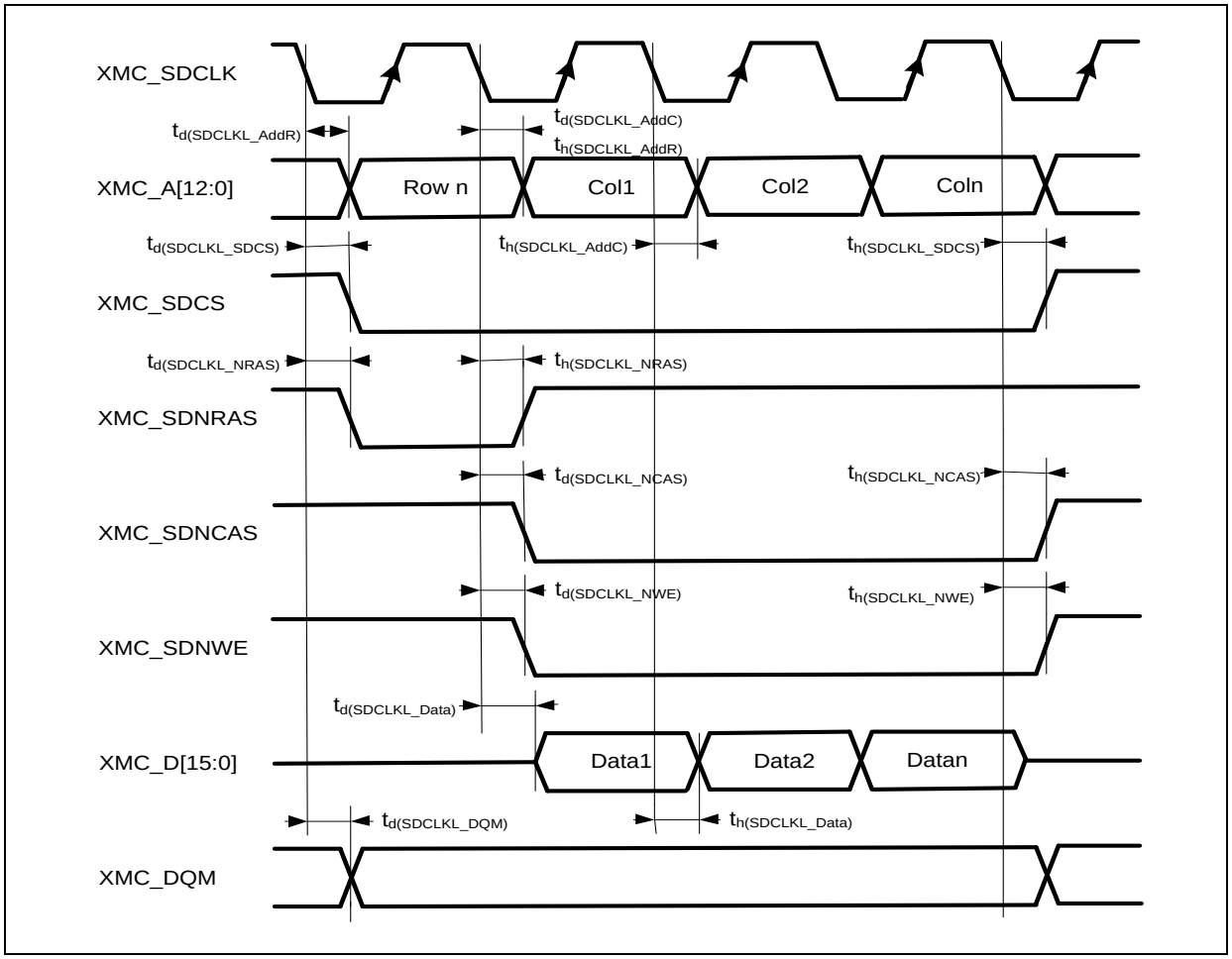


Table 52. SDRAM write timings

Symbol	Parameter	Condition	Min	Max	Unit
$1/t_{w(SDCLK)}$(1)	SDCLK frequency	LDO 1.3 V, T_A = 25 °C	-	192	MHz
		LDO 1.2 V, T_A = 25 °C	-	160	
		LDO 1.3/1.2 V, T_A = -40 ~ 105 °C	-	144	
		LDO 1.1 V, T_A = -40 ~ 105 °C	-	108	
$t_{d(SDCLKL\_Data)}$	Output data valid time	-	-	2.5	ns
$t_{h(SDCLKL\_Data)}$	Output data hold time	-	-1	-	ns
$t_{d(SDCLKL\_Add)}$	Address valid time	-	-	1.5	ns
$t_{d(SDCLKL\_SDNWE)}$	SDNWE valid time	-	-	1	ns
$t_{h(SDCLKL\_SDNWE)}$	SDNWE hold time	-	0	-	ns
$t_{d(SDCLKL\_SDCS)}$	CS valid time	-	-	1	ns
$t_{h(SDCLKL\_SDCS)}$	CS hold time	-	0	-	ns
$t_{d(SDCLKL\_SDNRAS)}$	SDNRAS valid time	-	-	1	ns
$t_{h(SDCLKL\_SDNRAS)}$	SDNRAS hold time	-	0	-	ns
$t_{d(SDCLKL\_SDNCAS)}$	SDNCAS valid time	-	-	1	ns
$t_{h(SDCLKL\_SDNCAS)}$	SDNCAS hold time	-	0	-	ns
$t_{d(SDCLKL\_DQM)}$	DQM valid time	-	-	1	ns
$t_{h(SDCLKL\_DQM)}$	DQM hold time	-	0	-	ns

(1) Guaranteed by characterization results, not tested in production. The maximum clock frequency is highly relevant to the device and PCB layout. For detailed solutions, please contact your local Artery sales office.

Figure 27. SDRAM write waveforms



4.3.14 TMR characteristics

The parameters given in the table below are guaranteed by design, not tested in production.

Table 53. TMR characteristics

Symbol	Parameter	Condition	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 192 MHz	5.21	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}/2$	MHz

4.3.15 SPI characteristics

Table 54. SPI characteristics(1)

Symbol	Parameter	Condition		Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})$	SPI clock frequency(2)(3)	Master mode	V_{DD} = 3.0 ~ 3.6 V	-	40	MHz
		slave receive mode	V_{DD} = 2.4 ~ 3.0 V	-	36	
		Slave transmit mode	V_{DD} = 3.0 ~ 3.6 V	-	32	
			V_{DD} = 2.4 ~ 3.0 V	-	25	
$t_{su(CS)}$	CS setup time	Slave mode		$2t_{PCLK}$	-	ns
$t_{h(CS)}$	CS hold time	Slave mode		$2t_{PCLK}$	-	ns
$t_{w(SCKH)}$ $t_{w(SCKL)}$	SCK high and low time	Master mode, prescaler factor = 2		t_{PCLK} - 3	t_{PCLK} + 3	ns
$t_{su(MI)}$	Data input setup time	Master mode		6	-	ns
$t_{su(SI)}$		Slave mode		5	-	
$t_{h(MI)}$	Data input hold time	Master mode		4	-	ns
$t_{h(SI)}$		Slave mode		5	-	
$t_{a(SO)}$(4)	Data output access time	Slave mode		t_{PCLK}	$2t_{PCLK}$ + 25	ns
$t_{dis(SO)}$(5)	Data output disable time	Slave mode		t_{PCLK}	$2t_{PCLK}$ + 25	ns
$t_{v(SO)}$	Data output valid time	Slave mode (after enable edge)		-	25	ns
$t_{v(MO)}$	Data output valid time	Master mode (after enable edge)		-	10	ns
$t_{h(SO)}$	Data output hold time	Slave mode (after enable edge)		9	-	ns
$t_{h(MO)}$		Master mode (after enable edge)		2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency should not exceed $f_{PCLK}/2$ in slave mode.
(3) Configure output as large sourcing/sinking strength. Guaranteed by characterization results, not tested in production. The maximum clock frequency is highly relevant to the device and PCB layout. For detailed solutions, please contact your local Artery sales office.
(4) Min time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 28. SPI timing diagram – slave mode and CPHA = 0

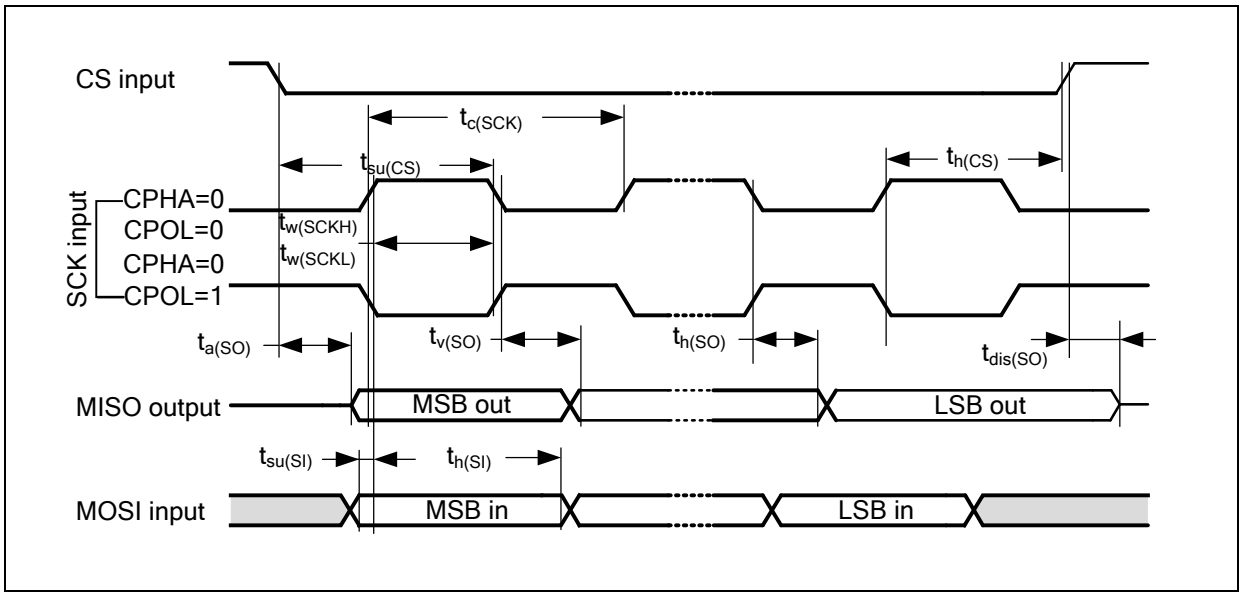


Figure 29. SPI timing diagram – slave mode and CPHA = 1

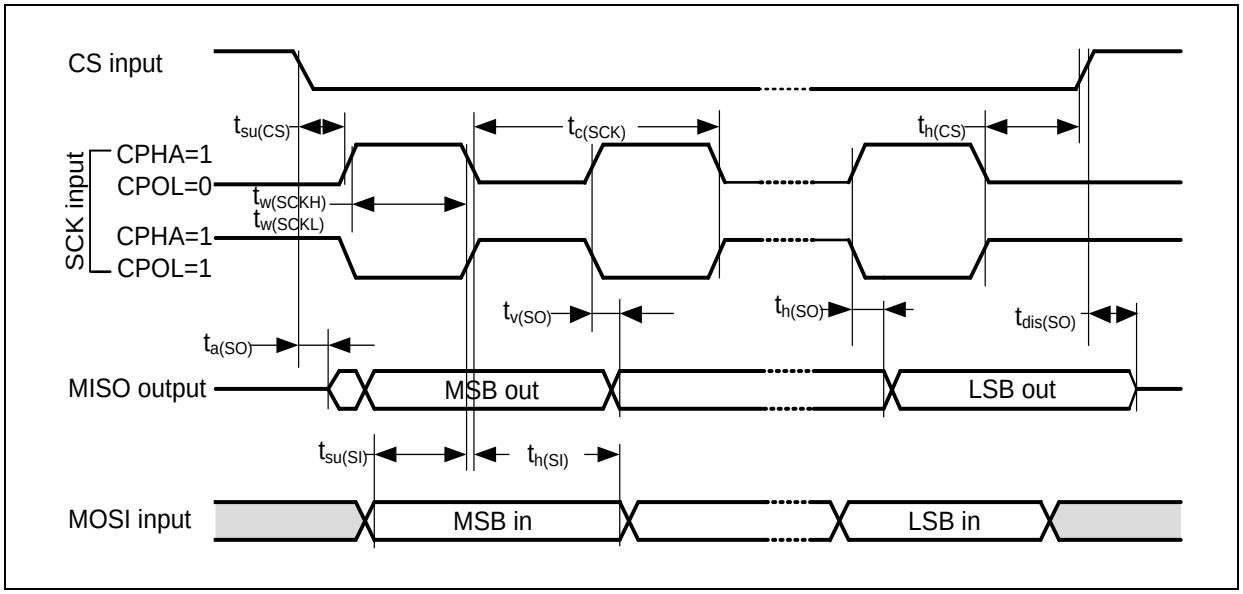
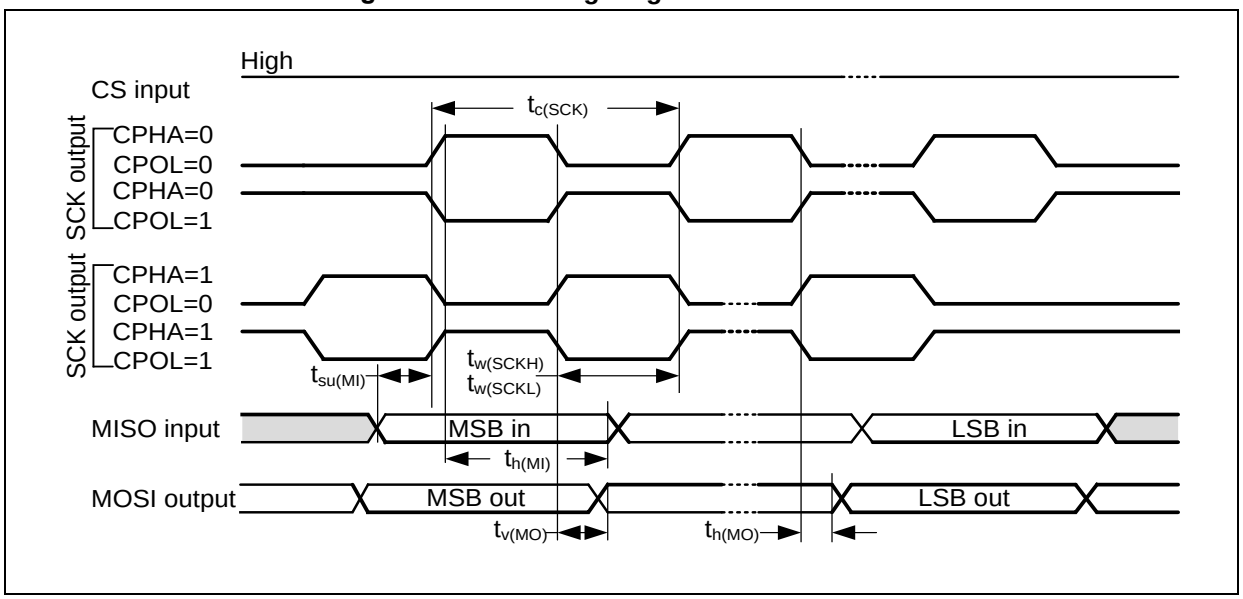


Figure 30. SPI timing diagram – master mode



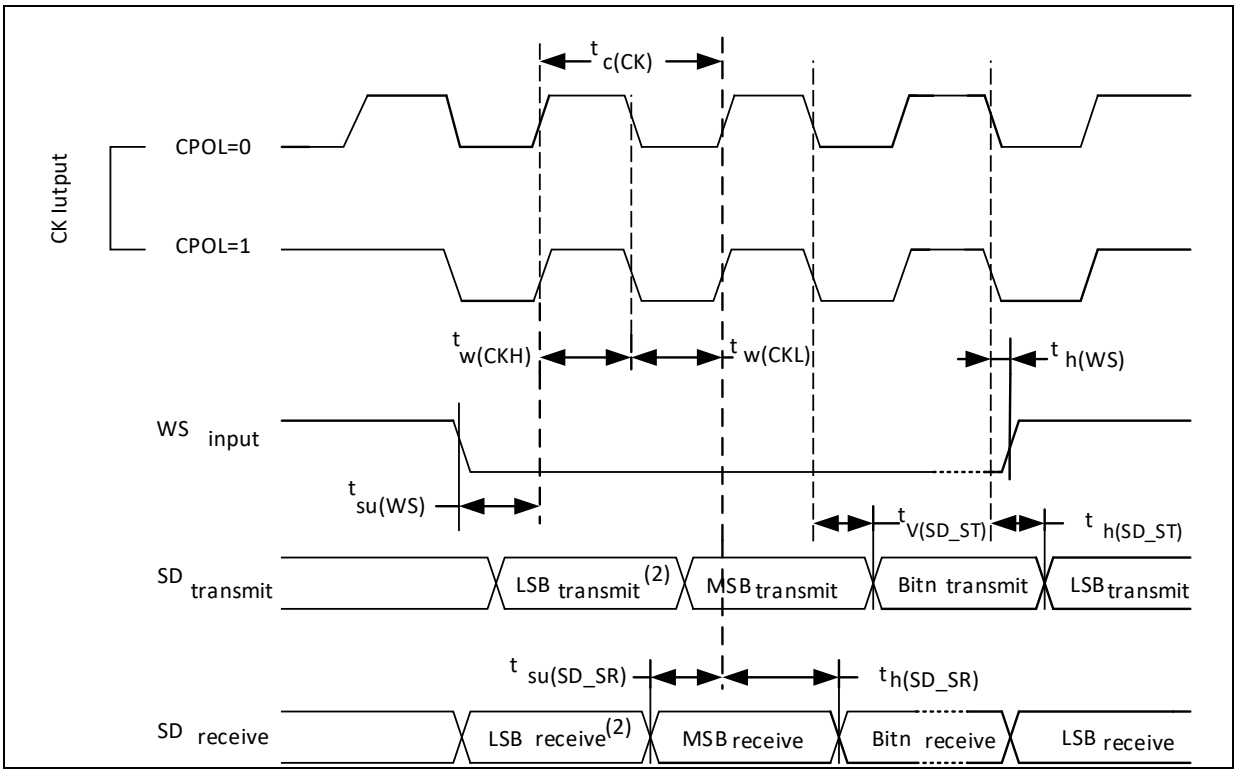
4.3.16 I²S / I²SF characteristics

Table 55. I²S/I²SF characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Load capacitance: C = 15 pF	-	12	ns
$t_{v(WS)}$	WS valid time	Master mode	0	4	
$t_{h(WS)}$	WS hold time	Master mode	0	4	
$t_{su(WS)}$	WS setup time	Slave mode	9	-	
$t_{h(WS)}$	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$		Slave receiver	2	-	
$t_{h(SD\_MR)}$	Data input hold time	Master receiver	0.5	-	
$t_{h(SD\_SR)}$		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_MT)}$	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD\_MT)}$	Data output hold time	Master transmitter (after enable edge)	0	-	

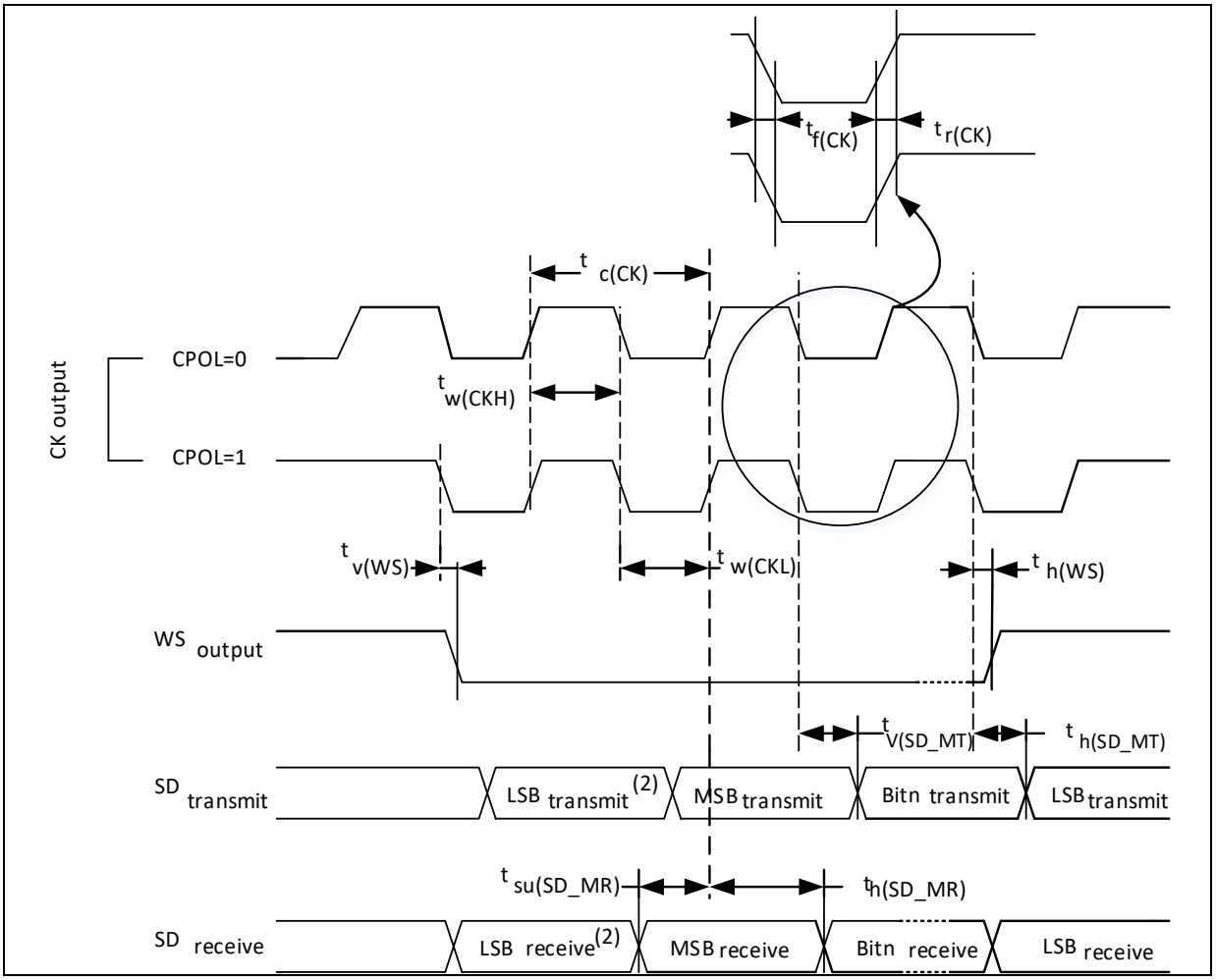
(1) Guaranteed by design, not tested in production.

Figure 31. I²S/I²SF slave mode timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 32. I²S/I²SF master mode timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

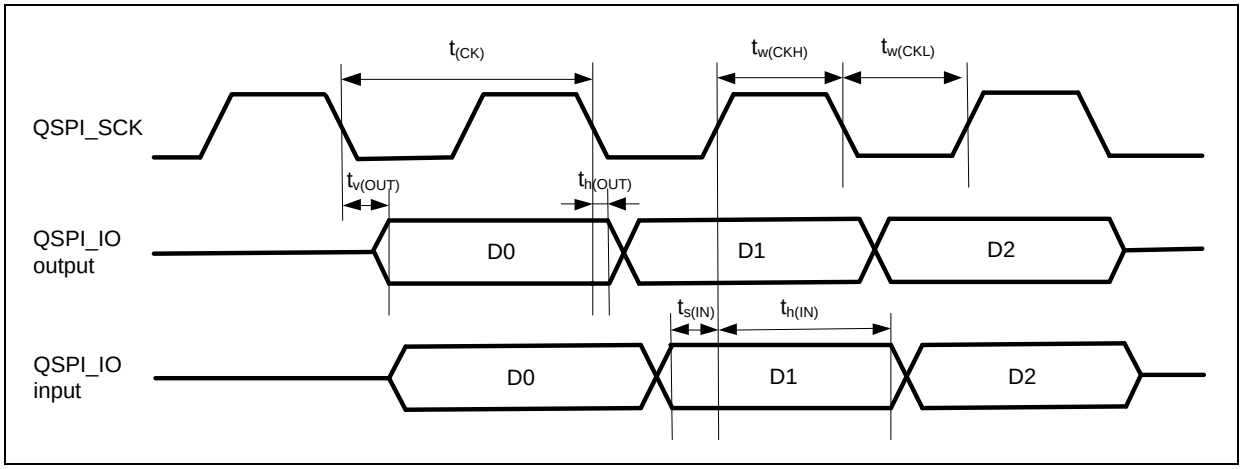
4.3.17 QSPI characteristics

Table 56. QSPI characteristics(1)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
f_{SCK} $1/t_{(CK)}$(2)	QSPI clock frequency	V_{DD} = 3.0 ~ 3.6 V	-	-	92	MHz
		V_{DD} = 2.4 ~ 3.0 V	-	-	80	
$t_{w(CKH)}$ $t_{w(CKL)}$	QSPI clock high and low time	-	($t_{(CK)}$ / 2) - 3	-	($t_{(CK)}$ / 2) + 3	ns
$t_{s(IN)}$	Data input setup time	-	2	-	-	ns
$t_{h(IN)}$	Data input hold time	-	4.5	-	-	ns
$t_{v(OUT)}$	Data output valid time	-	-	1.5	3	ns
$t_{h(OUT)}$	Data output hold time	-	0	-	-	ns

(1) Guaranteed by design, not tested in production.
(2) Guaranteed by characterization results, not tested in production. The maximum clock frequency is highly relevant to the device and PCB layout. For detailed solutions, please contact your local Artery sales office.

Figure 33. QSPI timing diagram



4.3.18 I²C characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain output, the PMOS connected between the GPIO pin and V_{DD} is disabled but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz) and fast mode plus (max. 1 MHz).

4.3.19 SDIO characteristics

Table 57. SD/MMC characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
f_{PP}	Clock frequency in data transfer mode	-	0	48	MHz
$t_{W(CKL)}$	Clock low time	f_{PP} = 48 MHz	8.5	-	ns
$t_{W(CKH)}$	Clock high time	f_{PP} = 48 MHz	8.5	-	
CMD, D input (referenced to CK)					
t_{ISU}	Clock setup time	f_{PP} = 48 MHz	7	-	ns
t_{IH}	Clock hold time	f_{PP} = 48 MHz	-4.5	-	
CMD, D output (referenced to CK)					
t_{OV} t_{OVD}	Output valid time	f_{PP} = 48 MHz	-	4	ns
t_{OH} t_{OHD}	Output hold time	f_{PP} = 48 MHz	0.5	-	

(1) Guaranteed by design, not tested in production.

Figure 34. SDIO high-speed mode

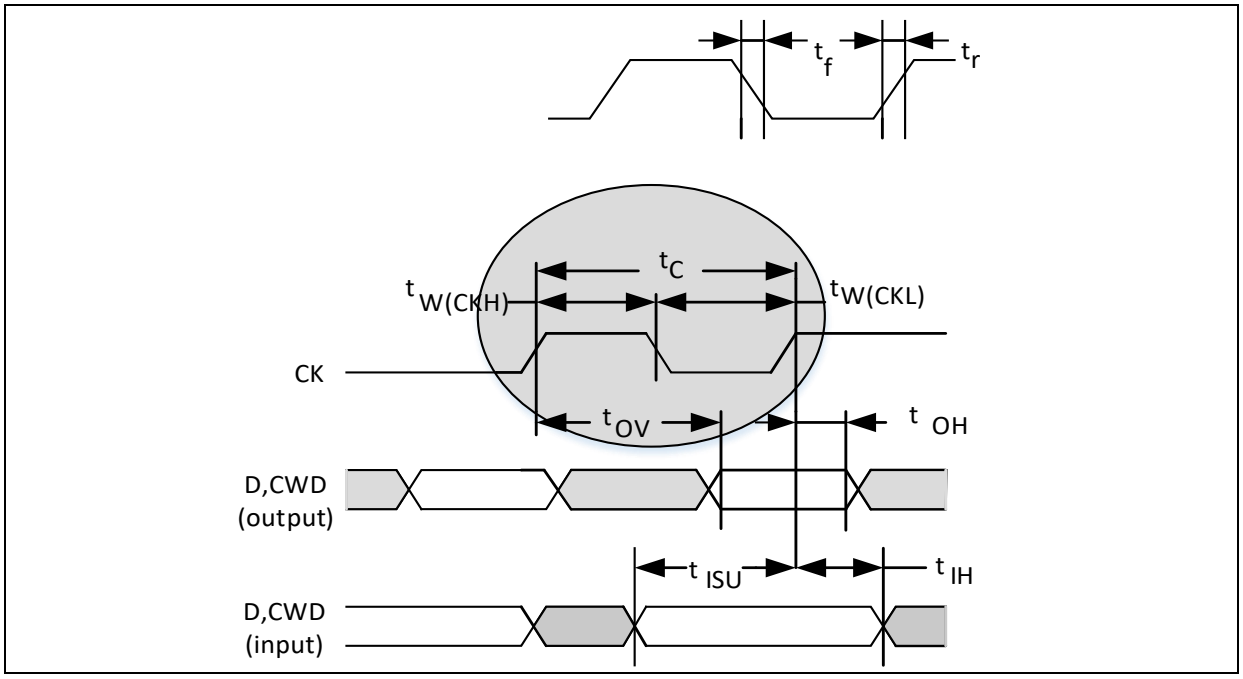
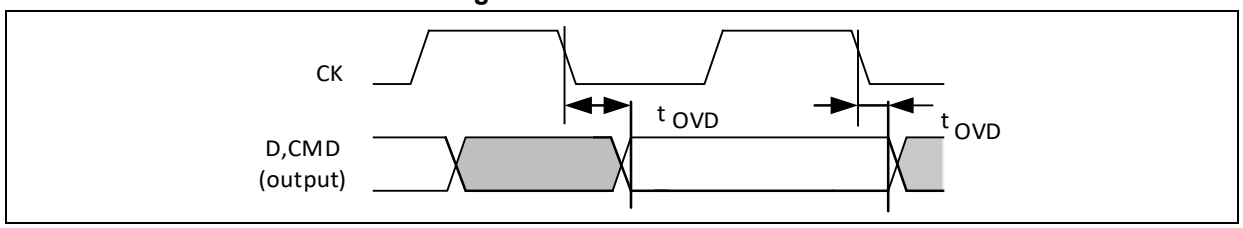


Figure 35. SD default mode



4.3.20 OTGFS characteristics

Table 58. OTGFS startup time

Symbol	Parameter	Max	Unit
$t_{STARTUP}$(1)	OTGFS transceiver startup time	1	µs

(1) Guaranteed by design, not tested in production.

Table 59. OTGFS DC electrical characteristics(1)(2)

Symbol		Parameter	Condition	Min	Typ	Max	Unit
Input levels	V_{DD}	OTGFS operating voltage	-	3.0(3)		3.6	V
	V_{DI}	Differential input sensitivity	I (OTGFS_D+/D-)	0.2		-	V
	V_{CM}	Differential common mode range	Include V_{DI} range	0.8		2.5	
	V_{SE}	Single ended receiver threshold	-	1.3		2.0	
Output levels	V_{OL}	Static output level low	R_L of 1.24 kΩ to 3.6 V(4)	-		0.3	V
	V_{OH}	Static output level high	R_L of 15 kΩ to V_{SS}(4)	2.8		3.6	
R_{PU}		OTGFS_D+ internal pull-up	Idle, V_{IN} = V_{SS}	0.97	1.24	1.58	kΩ
			Receive, V_{IN} = V_{SS}	1.66	2.26	3.09	
R_{PD}		OTGFS_D+/D- internal pull-down	V_{IN} = V_{DD}	15	19	25	kΩ

(1) All the voltages are measured from the local ground potential.
(2) Guaranteed by design, not tested in production.
(3) The AT32F455/456/457 USB functionality is ensured down to 2.7 V, but not the full USB electrical characteristics which are degraded in the 2.7 to 3.0 V voltage range.
(4) R_L is the load connected on the USB driver.

Figure 36. OTGFS timings: definition of data signal rise and fall time

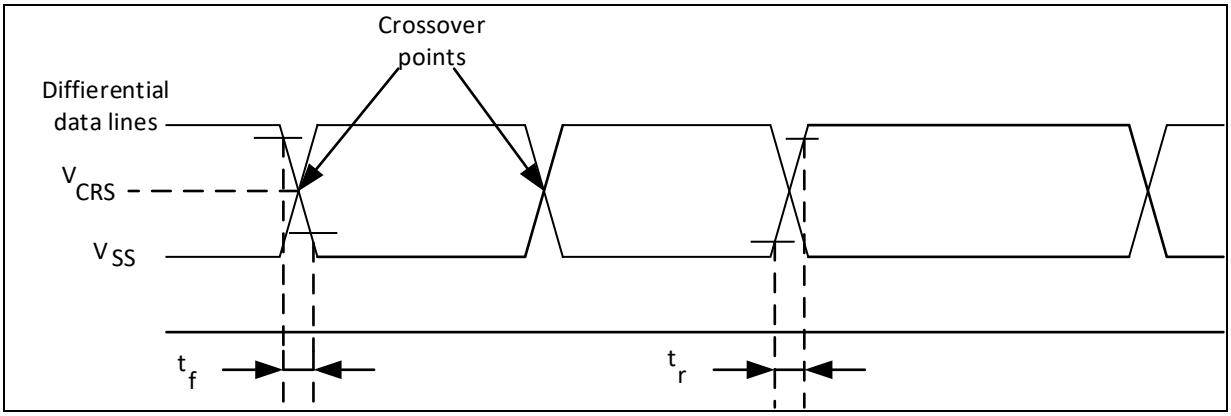


Table 60. OTGFS electrical characteristics(1)

Symbol	Parameter	Condition	Min	Max	Unit
t_r(2)	Rise time	C_L ≤ 50 pF	4	20	ns
t_f(2)	Fall time	C_L ≤ 50 pF	4	20	ns
t_{rfm}	Rise/fall time matching	t_r/t_f	90	110	%
V_{CRS}	Output signal crossover voltage	-	1.3	2.0	V

(1) Guaranteed by design, not tested in production.
(2) Measured from 10% to 90% of the data signal. For more details, refer to USB Specification Chapter 7 (version 2.0).

4.3.21 EMAC characteristics

Operating voltage

Table 61. EMAC DC electrical characteristics(1)

Symbol	Parameter	Min	Max	Unit
V_{DD}	EMAC operating voltage	3.0	3.6	V

(1) Guaranteed by design, not tested in production. All the voltages are measured from the local ground potential.

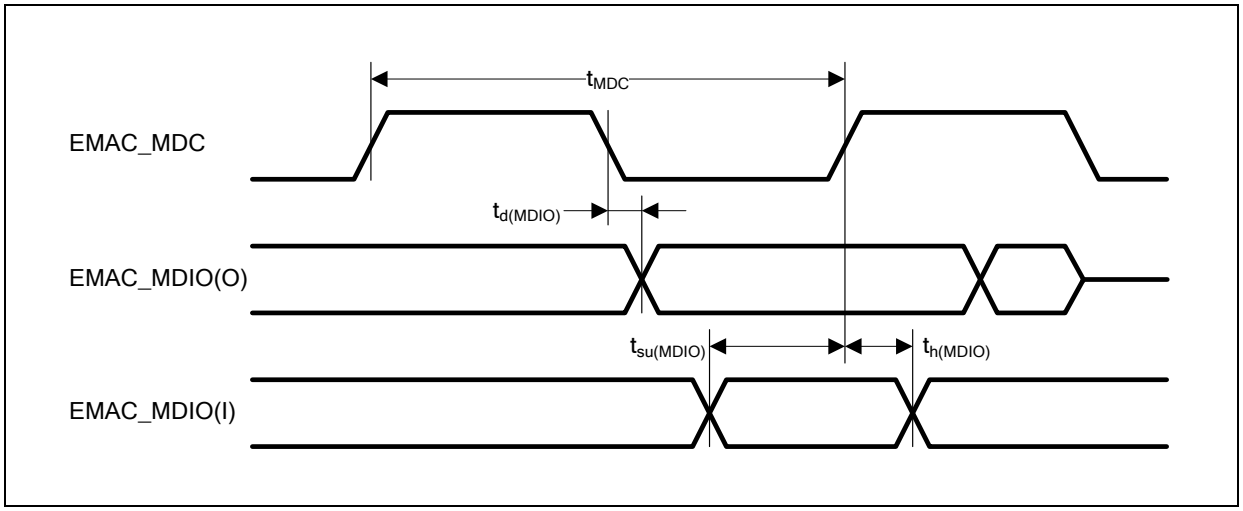
SMI (station management interface)

Table 62. Dynamic characteristics: EMAC signals for SMI(1)

Symbol	Parameter	Min	Typ	Max	Unit
t_{MDC}	MDC cycle time (1.96 MHz)	509	510	511	ns
$t_{d(MDIO)}$	MDIO write data valid time	12	14.5	17	
$t_{su(MDIO)}$	Read data setup time	35	-	-	
$t_{h(MDIO)}$	Read data hold time	15	-	-	

(1) Guaranteed by design, not tested in production.

Figure 37. EMAC SMI timing diagram



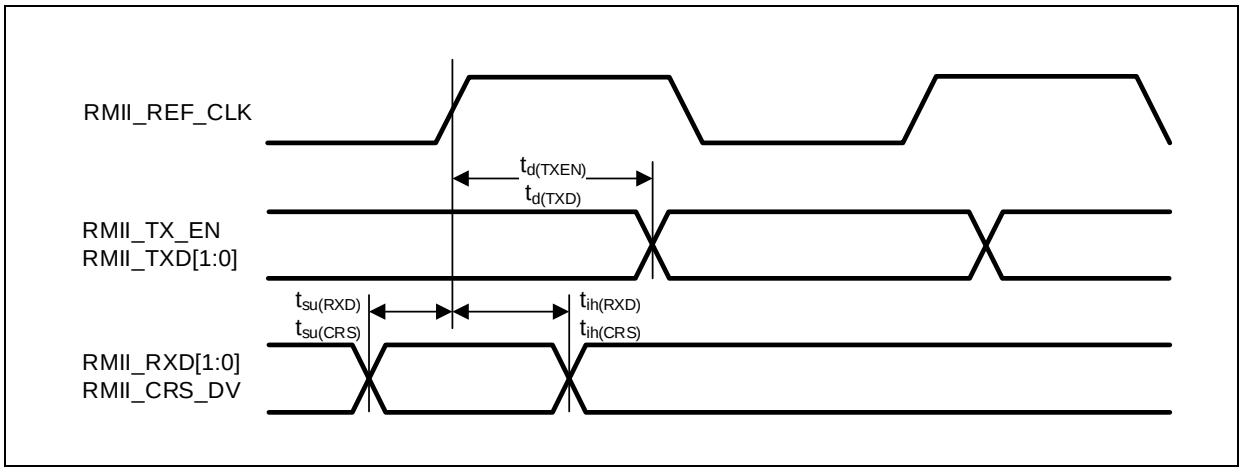
RMII

Table 63. Dynamic characteristics: EMAC signals for RMII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	4	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(DV)}$	Carrier sense setup time	6	-	-	
$t_{ih(DV)}$	Carrier sense hold time	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	8	10	16	
$t_{d(TXD)}$	Transmit data valid delay time	7	10	16	

(1) Guaranteed by design, not tested in production.

Figure 38. EMAC RMII timing diagram



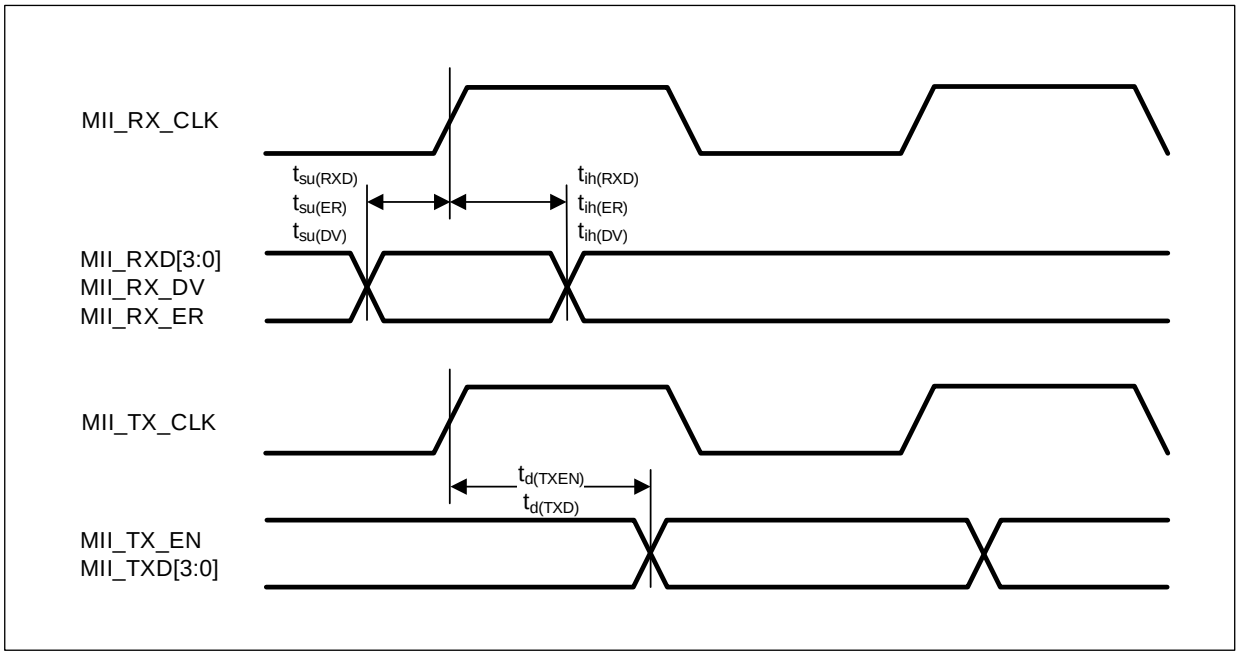
MII

Table 64. Dynamic characteristics: EMAC signals for MII(1)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{su(RXD)}$	Receive data setup time	8	-	-	ns
$t_{ih(RXD)}$	Receive data hold time	2	-	-	
$t_{su(DV)}$	Data valid setup time	6	-	-	
$t_{ih(DV)}$	Data valid hold time	1	-	-	
$t_{su(ER)}$	Error setup time	3	-	-	
$t_{ih(ER)}$	Error hold time	1	-	-	
$t_{d(TXEN)}$	Transmit enable valid delay time	14	16	18	
$t_{d(TXD)}$	Transmit data valid delay time	13	16	20	

(1) Guaranteed by design, not tested in production.

Figure 39. EMAC MII timing diagram



4.3.22 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 17*.

Note: It is recommended to perform a calibration after each power-up.

Table 65. ADC characteristics

Symbol	Parameter	Condition		Min	Typ	Max	Unit
V_{DDA}	Power supply	-		2.4	-	3.6	V
V_{REF+}(1)	Positive reference voltage	-		2.0	-	V_{DDA}	V
I_{DDA}(2)	Current on V_{DDA} input pin	f_{ADC} = 80 MHz		-	1800	2200	µA
I_{VREF+}(1)(2)	Current on V_{REF+} input pin	f_{ADC} = 80 MHz		-	410	510	µA
f_{ADC}	ADC clock frequency	-		0.6	-	80	MHz
f_S(3)	Sampling rate	12-bit resolution	Fast channels	0.04	-	5.33	MSPS
			Slow channels			4.21	
		10-bit resolution	Fast channels	0.047	-	6.15	
			Slow channels			4.71	
		8-bit resolution	Fast channels	0.055	-	7.27	
			Slow channels			5.33	
		6-bit resolution	Fast channels	0.067	-	8.88	
			Slow channels			6.15	
f_{TRIG}(3)	External trigger frequency	f_{ADC} = 80 MHz		-	-	4.44	MHz
		-		-	-	18	1/f_{ADC}
V_{AIN}(3)	Conversion voltage range(1)	-		0 (V_{REF-} internally connected to ground)	-	V_{REF+}	V
R_{AIN}(3)	External input impedance	-		See *Table 66*			Ω
C_{ADC}(3)	Internal sample and hold capacitor	-		-	10	-	pF
t_{lat}(3)	Preemptive trigger conversion latency	f_{ADC} = 80 MHz		-	-	37.5	ns
		-		-	-	3(4)	1/f_{ADC}
t_{latr}(3)	Ordinary trigger conversion latency	f_{ADC} = 80 MHz		-	-	25	ns
		-		-	-	2(4)	1/f_{ADC}
t_S(3)	Sampling time	f_{ADC} = 80 MHz		0.031	-	8.006	µs
		-		2.5	-	640.5	1/f_{ADC}
t_{STAB}(3)	Power-up time	-		45			1/f_{ADC}
t_{CONV}(3)	Total conversion time (including sampling time)	f_{ADC} = 80 MHz, 12-bit resolution		0.188	-	8.163	µs
		12-bit resolution		15 ~ 653 (t_S for sampling + 12.5 for successive approximation)			1/f_{ADC}

(1) V_{REF+} can be internally connected to V_{DDA} depending on the package.
(2) Guaranteed by characterization results, not tested in production.
(3) Guaranteed by design, not tested in production.
(4) For external triggers, a delay of 1/f_{PCLK2} must be added to the latency specified in *Table 65*.

Table 66 defines the maximum external impedance allowed for an error below 1 of LSB in 12-bit resolution.

Table 66. R_{AIN} max for f_{ADC} = 80 MHz

T_S (cycle)	t_S (µs)	R_{AIN} max (Ω)(1)	
		Fast channels	Slow channels
2.5	0.031	30	-
6.5	0.081	200	50
12.5	0.156	400	350
24.5	0.306	800	700
47.5	0.594	1700	1500
92.5	1.156	3000	2600
247.5	3.094	9000	8500
640.5	8.006	20000	19000

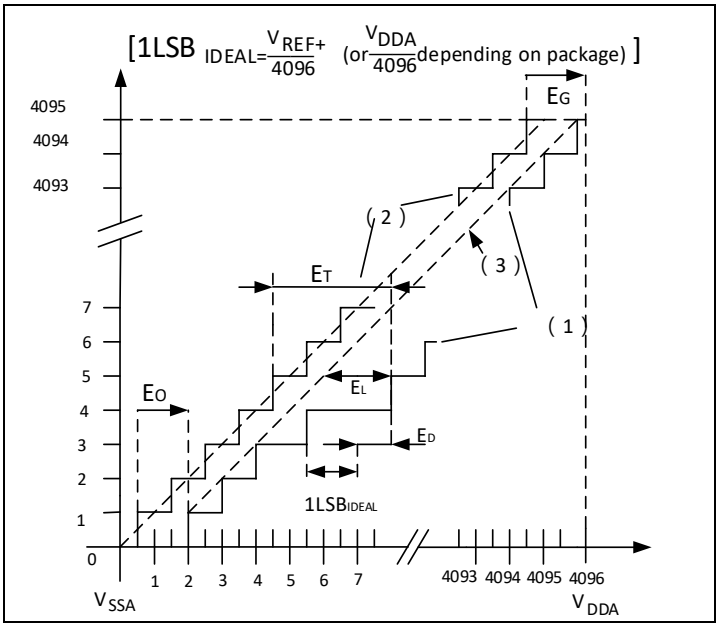
(1) Guaranteed by design.

Table 67. ADC accuracy(1)(2)

Symbol	Parameter	Test conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{ADC} = 80 MHz, R_{AIN} < 20 kΩ, V_{DDA} = 3.0 ~ 3.6 V, T_A = 25 °C V_{REF+} = V_{DDA}	±2.5	±4	LSB
EO	Offset error		-1	+0.5/-3	
EG	Gain error		+1.5	-0.5/+3	
ED	Differential linearity error		+1.2	+2/-1	
EL	Integral linearity error		±1.5	±2.5	
ET	Total unadjusted error	f_{ADC} = 80 MHz, R_{AIN} < 20 kΩ, V_{DDA} = 2.4 ~ 3.6 V, T_A = -40 ~ 105 °C V_{REF+} = 2.0 ~ 2.4 V	±3	±5	LSB
EO	Offset error		-1	+1/-3.5	
EG	Gain error		+1.5	-1/+3.5	
ED	Differential linearity error		+1.5	+2.5/-1	
EL	Integral linearity error		±2.5	±3.5	

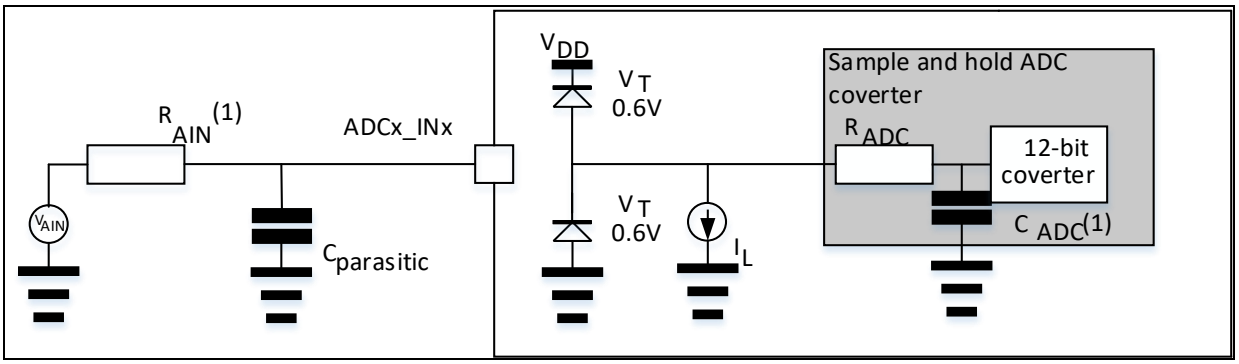
(1) ADC DC accuracy values are measured after internal calibration.
(2) Guaranteed by characterization results, not tested in production.

Figure 40. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 41. Typical connection diagram using the ADC

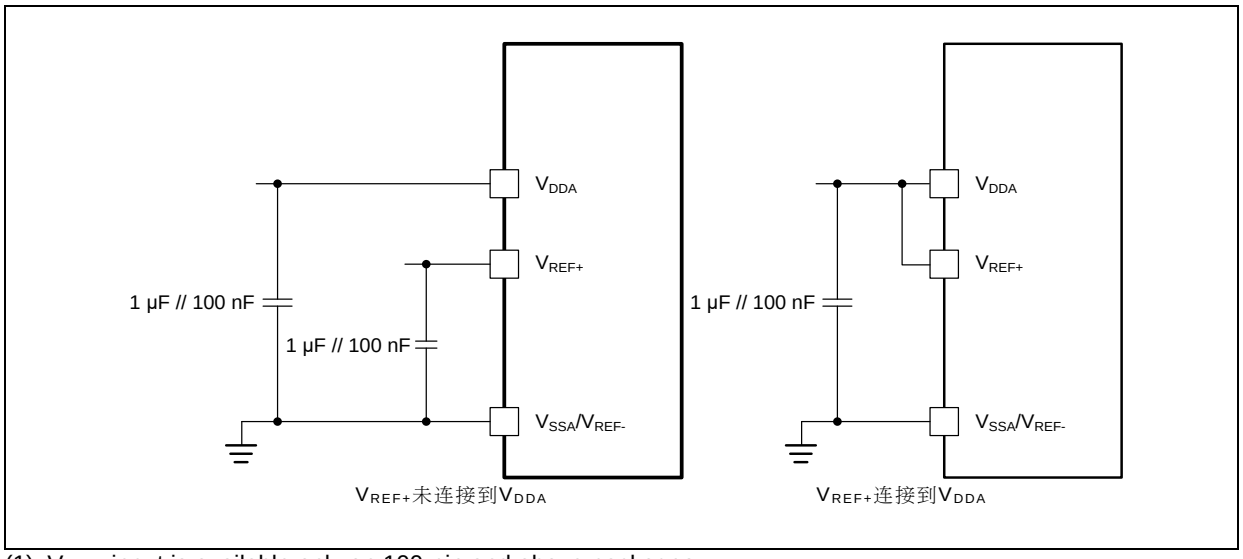


(1) Refer to *Table 65* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

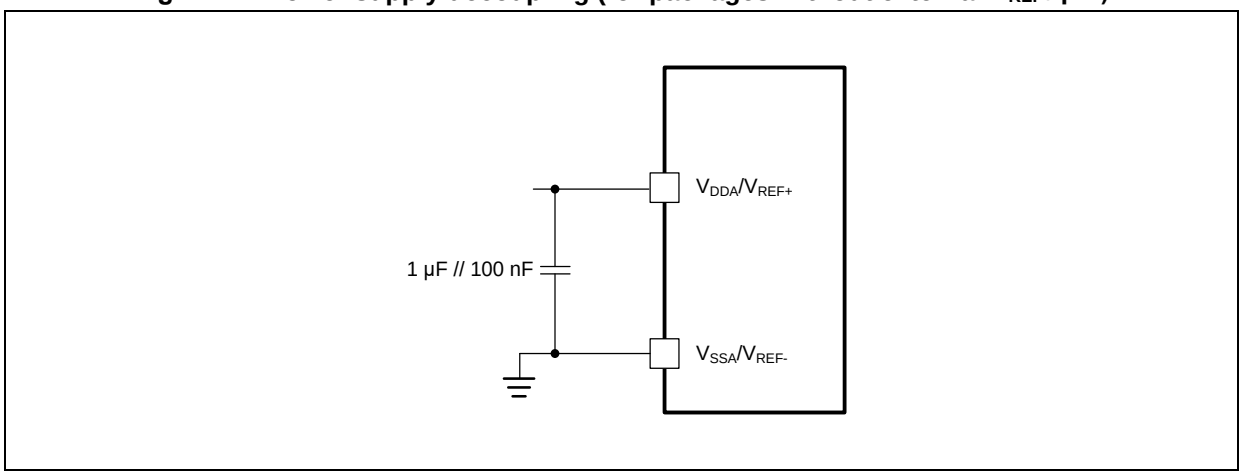
Power supply decoupling should be performed as shown in *Figure 42* or *Figure 43*, depending on whether V_{REF+} is connected to V_{DDA} or not. The 100 nF capacitors should be ceramic (good quality). They should be placed them as close as possible to the chip.

Figure 42. Power supply and reference decoupling (for packages with external V_{REF+} pin)



(1) V_{REF+} input is available only on 100-pin and above packages.

Figure 43. Power supply decoupling (for packages without external V_{REF+} pin)



(1) V_{REF+} input is available only on 100-pin and above packages.

4.3.23 Internal reference voltage (V_{INTRV}) characteristics

Table 68. Internal reference voltage characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	50	100	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

4.3.24 Temperature sensor (V_{TS}) characteristics

Table 69. Temperature sensor characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
T_L(1)	V_{TS} linearity with temperature	T_A = -20 ~ +85 °C	-	±1	±2	ºC
		T_A = -40 ~ +105 °C	-	-	±3	
Avg_Slope(1)(2)	Average slope	-	-4.11	-4.27	-4.42	mV/ºC
V_{25}(1)(2)	Voltage at 25 ºC	-	1.16	1.28	1.40	V
t_{START}(3)	Setup time	-	-	-	100	µs
T_{S_temp}(3)	ADC sampling time when reading the temperature	-	5.1	-	-	µs

(1) Guaranteed by characterization results, not tested in production.
(2) The temperature sensor output voltage changes linearly with temperature. The offset of this line varies from chip to chip due to process variation (up to 50 °C from one chip to another). The internal temperature sensor is more suited to applications that detect temperature variations instead of absolute temperatures. If accurate temperature readings are needed, an external temperature sensor part should be used.
(3) Guaranteed by design, not tested in production.

Obtain the temperature using the following formula:

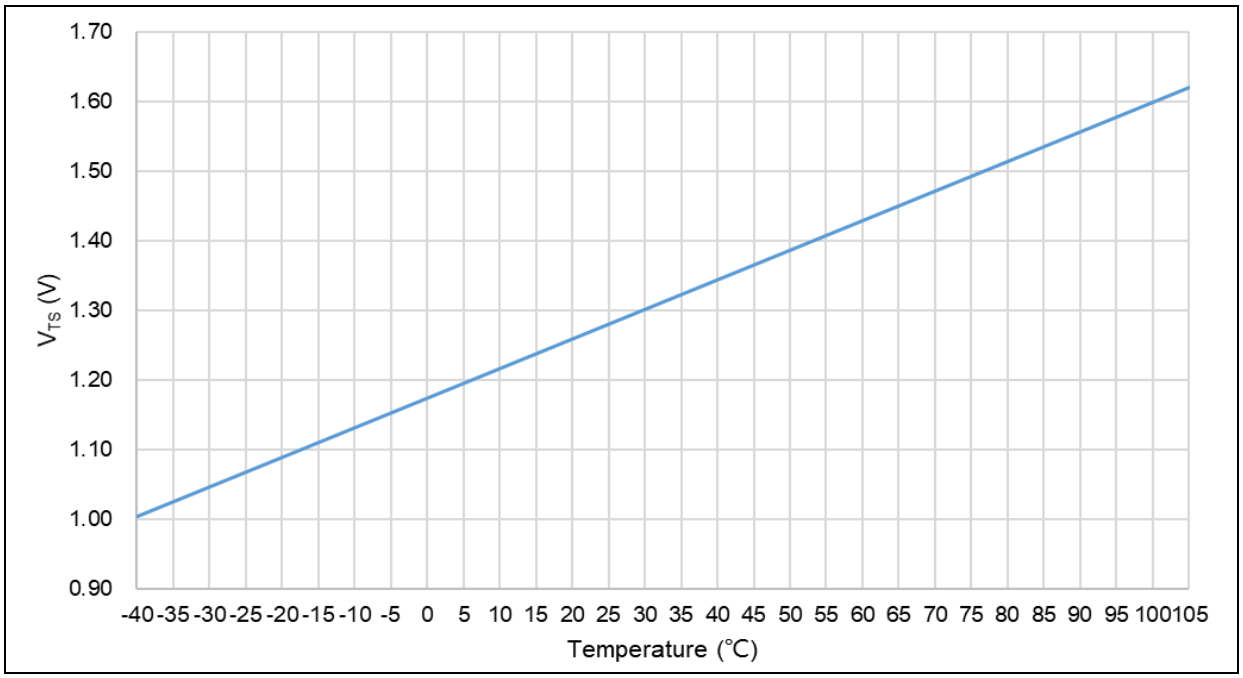
Temperature (°C) = {(V_{25} – V_{TS}) / Avg_Slope} + 25

where,

V_{25} = V_{TS} value for 25 °C

Avg_Slope = average slope for curve between temperature vs. V_{TS} (given in mV/°C)

Figure 44. V_{TS} vs. temperature



4.3.25 V_{BAT} voltage monitor characteristics

Table 70. V_{BAT} voltage monitor characteristics

Symbol	Parameter	Min	Typ	Max	Unit
R_{VBATM}(1)	String resistor value of the V_{BAT} monitor	-	40	-	kΩ
Q	Dividing factor of the V_{BAT} monitor	-	4	-	-
Q_{ET}(1)	Total error of Q	-1	-	+1	%
T_{S_VBATM}(2)	ADC sampling time when reading the voltage of the V_{BAT} monitor	5.1	-	-	μs

(1) Guaranteed by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

4.3.26 12-bit DAC characteristics

Table 71. DAC characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
V_{DDA}	Analog supply voltage	-	2.4	-	3.6	V
V_{REF+}(1)	Reference supply voltage	-	2.0	-	3.6	V
V_{SSA}	Ground	-	0	-	0	V
R_{LOAD}(2)	Load resistance with buffer ON	-	5	-	-	kΩ
R_O(2)	Impedance output with buffer OFF	-	-	13.2	16	kΩ
C_{LOAD}(2)	Capacitive load (buffer ON)	-	-	-	50	pF
DAC_OUT(2)	Lower DAC_OUT voltage with buffer ON	-	0.2	-	-	V
	Higher DAC_OUT voltage with buffer ON	-	-	-	V_{REF+} - 0.2	V
	Lower DAC_OUT voltage with buffer OFF	-	-	0.5	5	mV
	Higher DAC_OUT voltage with buffer OFF	-	-	-	V_{REF+} - 5 mV	V
I_{DDA}(3)	DAC DC current consumption in quiescent mode	No load, V_{REF+} = 3.6 V	-	370	515	μA
I_{VREF+}(1)(3)	DAC DC current consumption in quiescent mode	No load, V_{REF+} = 3.6 V	-	170	190	μA
DNL(3)	Differential non linearity	-	-	±0.5	±1.5	LSB
INL(3)	Integral non linearity (difference between measured value from code i and a line drawn between DAC_OUT max and DAC_OUT min)	-	-	±1	±2	LSB
Offset(3)	Offset error (difference between measured value at Code (0x800) and the ideal value = V_{REF+}/2)	-	-	10	15	mV
			-	10	20	LSB
Gain(3)	Gain error	-	-	0.2	0.5	%
$t_{SETTLING}$(2)	Setting time	R_{LOAD} ≥ 5 kΩ C_{LOAD} ≤ 50 pF	-	1	4	μs
Update rate(2)	Max frequency for a correct DAC_OUT change when small variation in the input code (from code i to i+1 LSB)	R_{LOAD} ≥ 5 kΩ C_{LOAD} ≤ 50 pF	-	-	1	MSPS
t_{WAKEUP}(2)	Wakeup time from off state (setting the EN bit in the DAC control register)	R_{LOAD} ≥ 5 kΩ C_{LOAD} ≤ 50 pF	-	1.2	4	μs

(1) V_{REF+} can be internally connected to V_{DDA} depending on the package.
(2) Guaranteed by design, not tested in production.
(3) Guaranteed by characterization results, not tested in production.

5 Package information

5.1 LQFP144 – 20 x 20 mm

Figure 45. LQFP144 – 20 x 20 mm 144-pin low-profile quad flat package outline

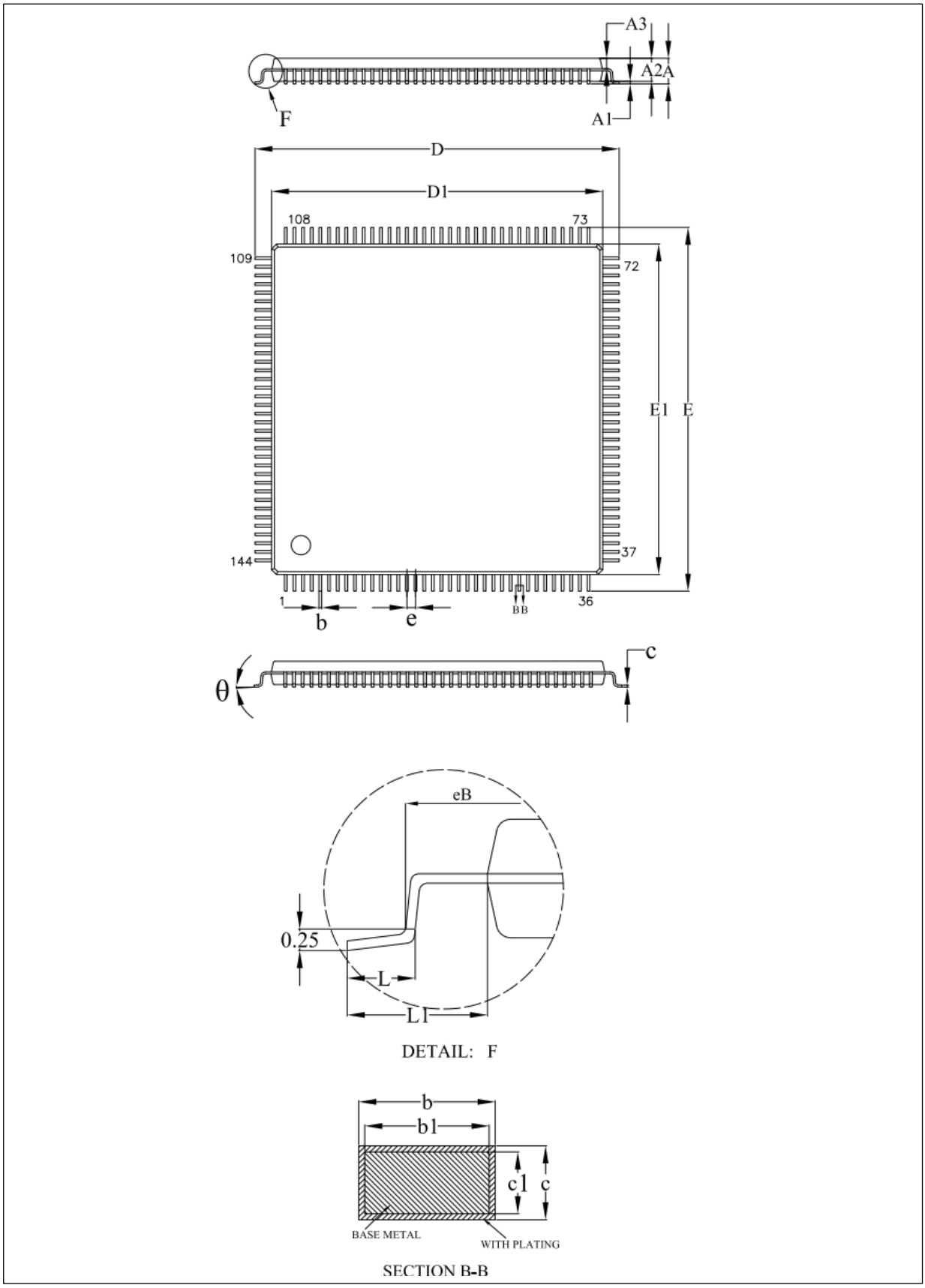


Table 72. LQFP144 – 20 x 20 mm 144-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
A3	0.59	0.64	0.69
b	0.18	-	0.26
b1	0.17	0.20	0.23
c	0.13	-	0.17
c1	0.12	0.13	0.14
D	21.80	22.00	22.20
D1	19.90	20.00	20.10
E	21.80	22.00	22.20
E1	19.90	20.00	20.10
e	0.50 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		
θ	0°	3.5°	7°

5.2 LQFP100 – 14 x 14 mm

Figure 46. LQFP100 – 14 x 14 mm 100-pin low-profile quad flat package outline

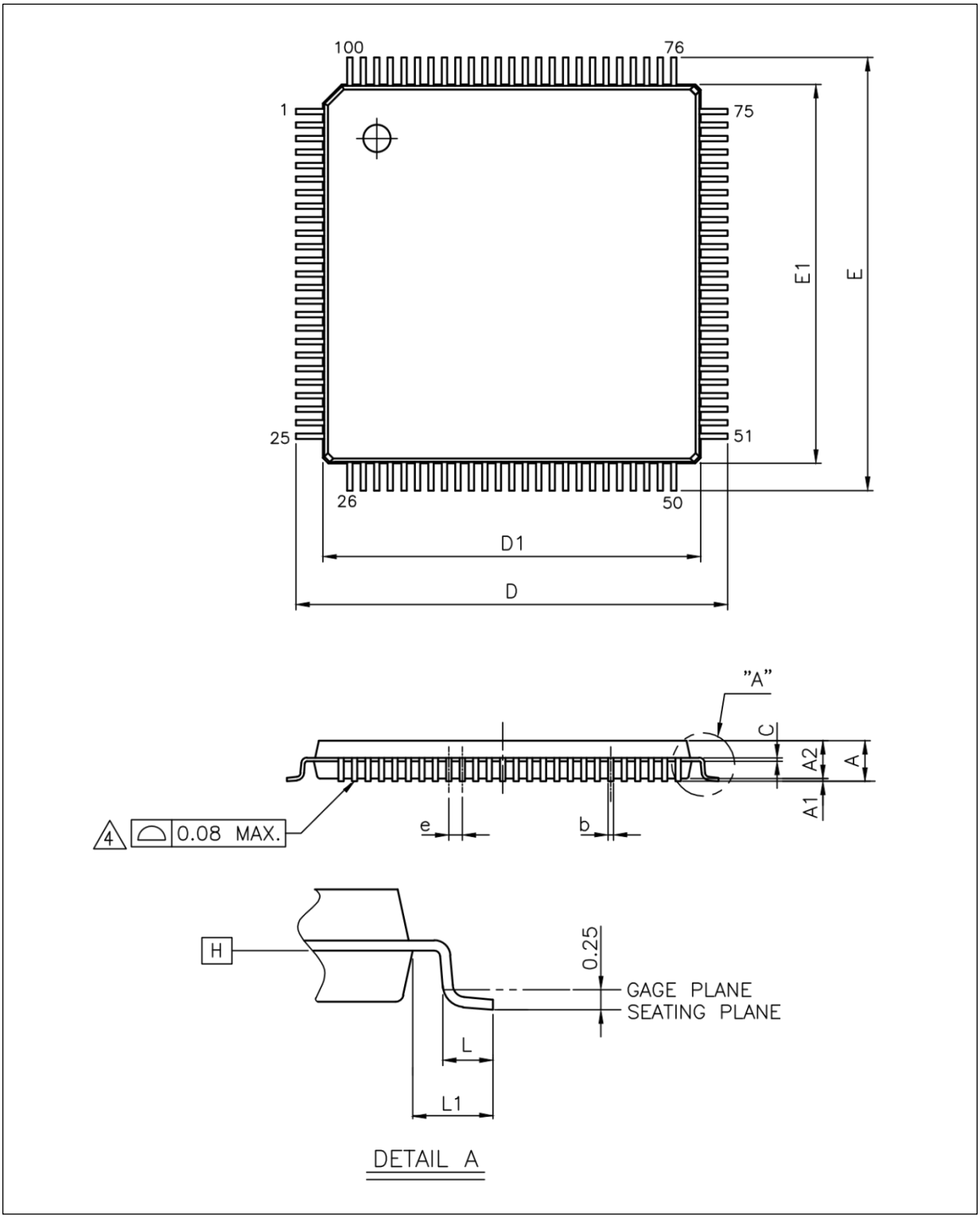


Table 73. LQFP100 – 14 x 14 mm 100-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.26
c	0.10	0.127	0.20
D	15.75	16.00	16.25
D1	13.90	14.00	14.10
E	15.75	16.00	16.25
E1	13.90	14.00	14.10
e	0.50 BSC.		
L	0.45	0.60	0.75
L1	1.00 REF.		

5.3 LQFP64 – 10 x 10 mm

Figure 47. LQFP64 – 10 x 10 mm 64-pin low-profile quad flat package outline

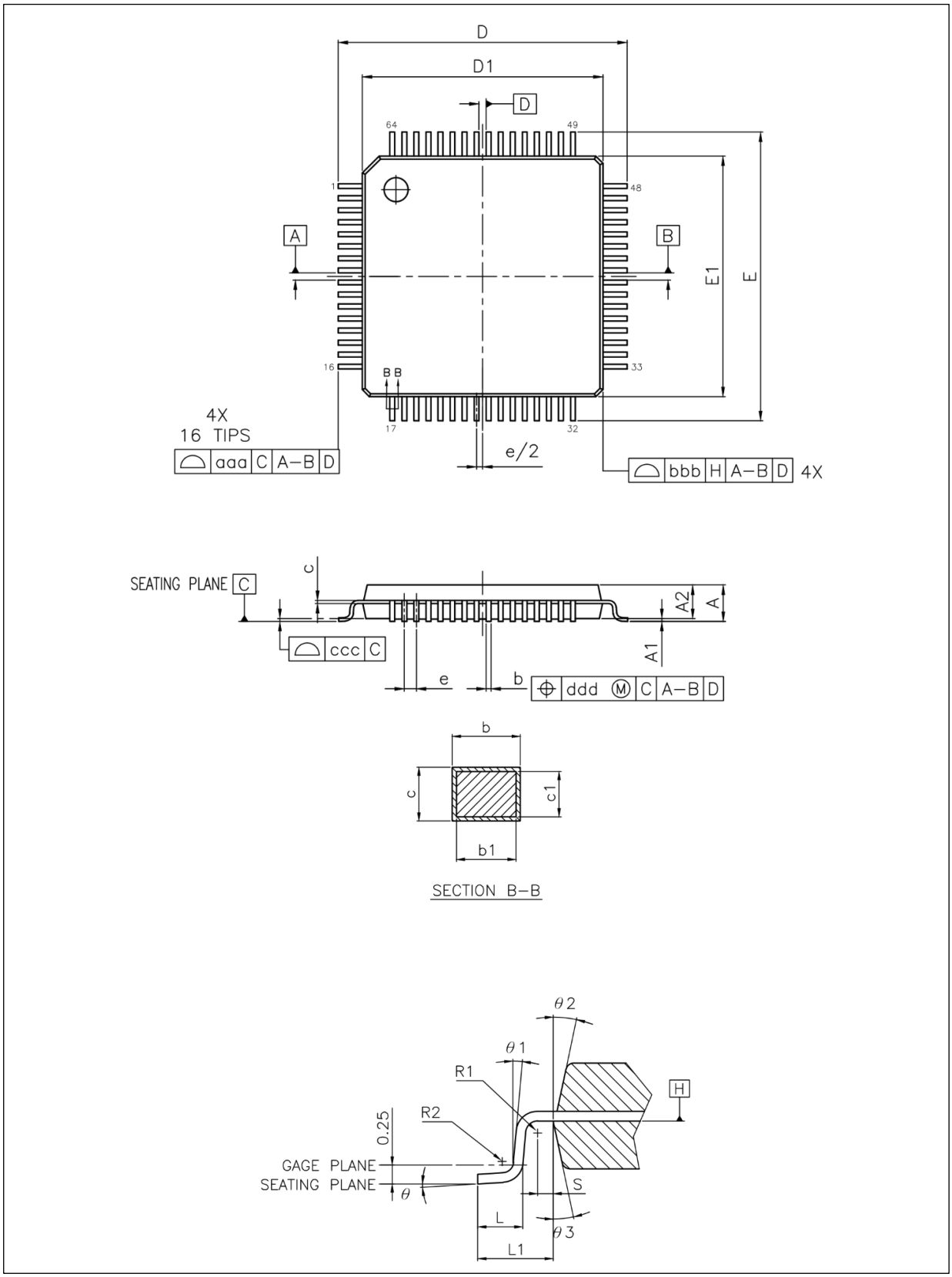


Table 74. LQFP64 – 10 x 10 mm 64-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.20	0.27
c	0.09	-	0.20
D	11.75	12.00	12.25
D1	9.90	10.00	10.10
E	11.75	12.00	12.25
E1	9.90	10.00	10.10
e	0.50 BSC.		
Θ	3.5° REF.		
L	0.45	0.60	0.75
L1	1.00 REF.		
ccc	0.08		

5.4 LQFP48 – 7 x 7 mm

Figure 48. LQFP48 – 7 x 7 mm 48-pin low-profile quad flat package outline

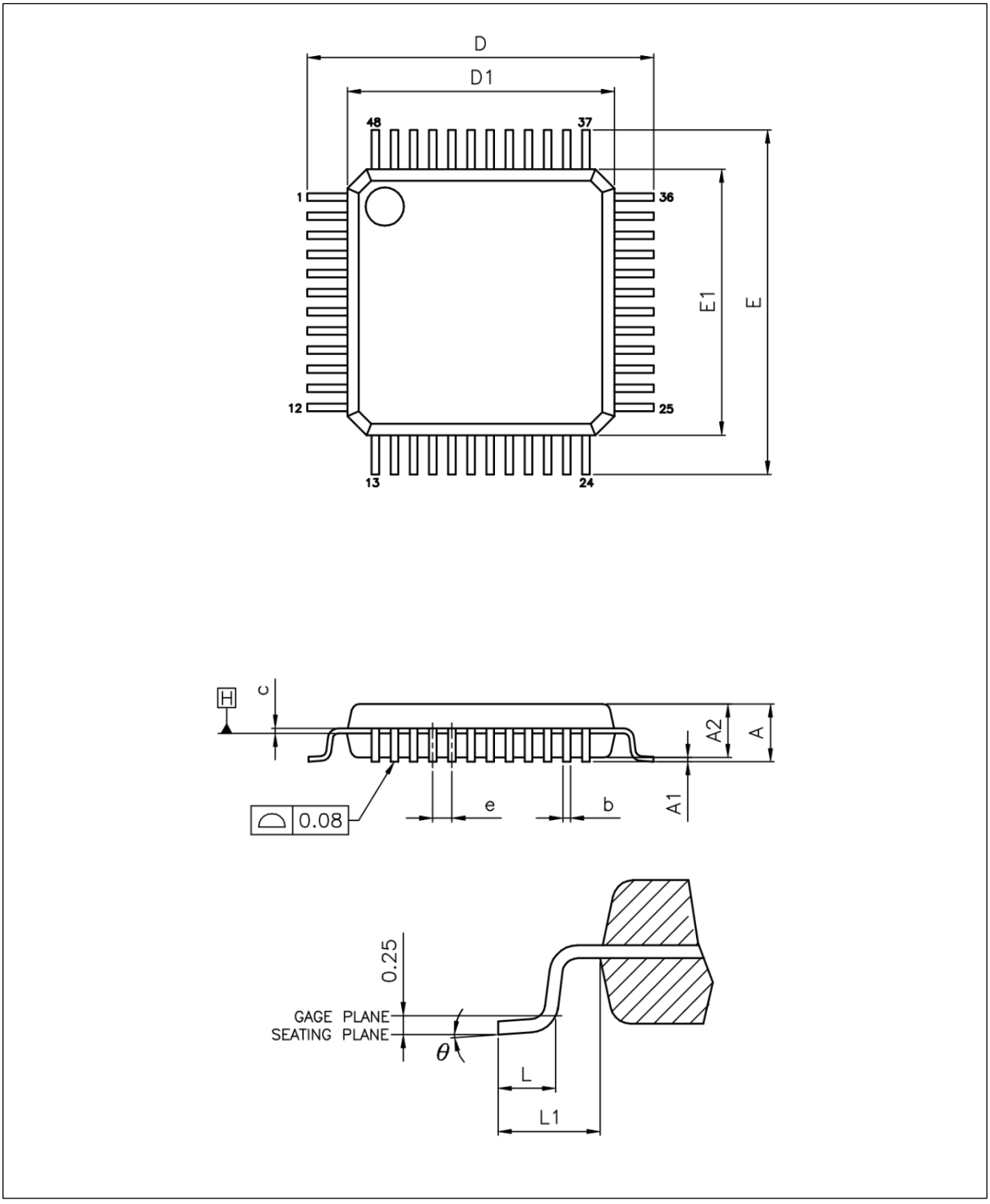


Table 75. LQFP48 – 7 x 7 mm 48-pin low-profile quad flat package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

5.5 QFN48 – 6 x 6 mm

Figure 49. QFN48 – 6 x 6 mm 48-pin quad flat no-leads package outline

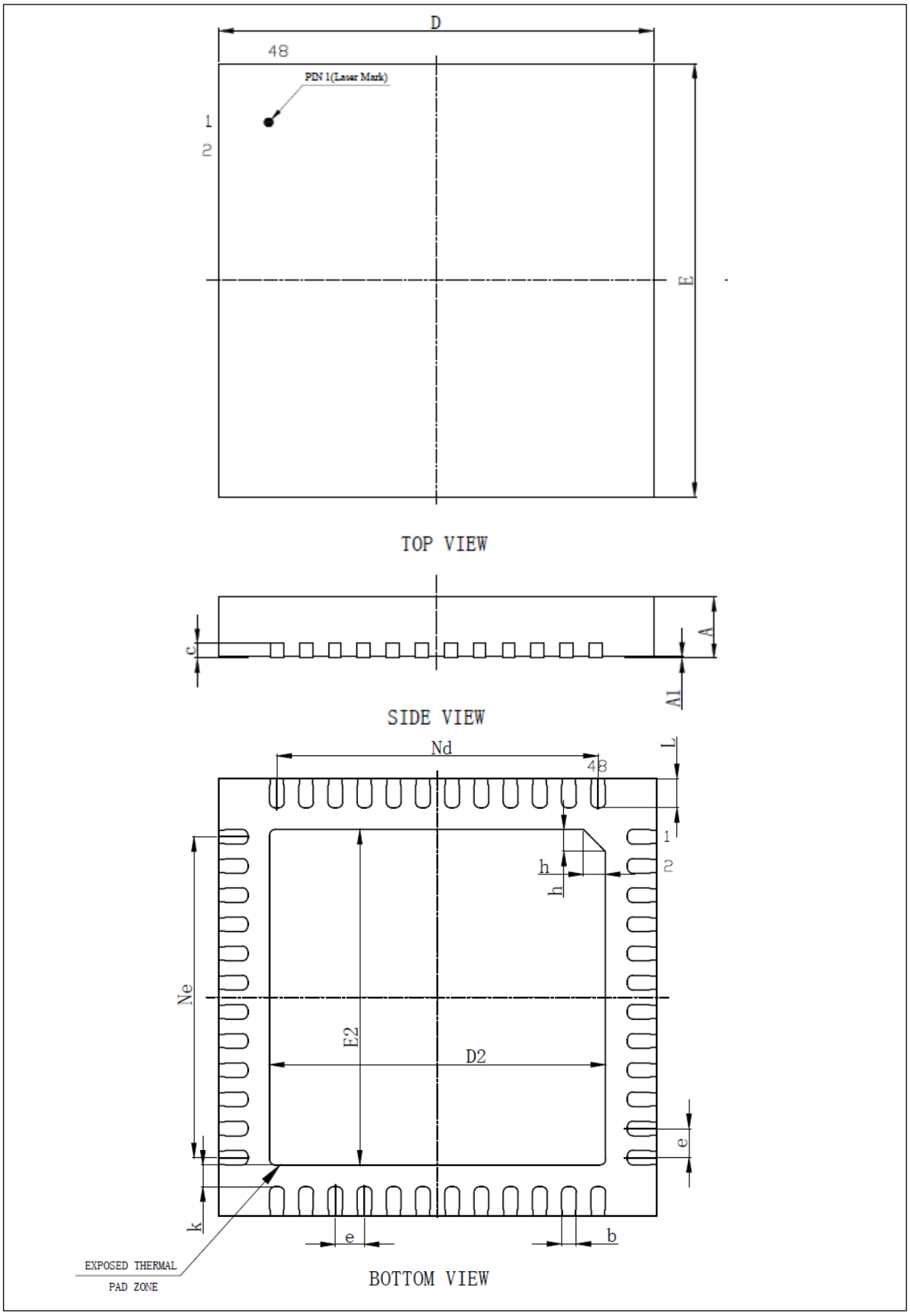
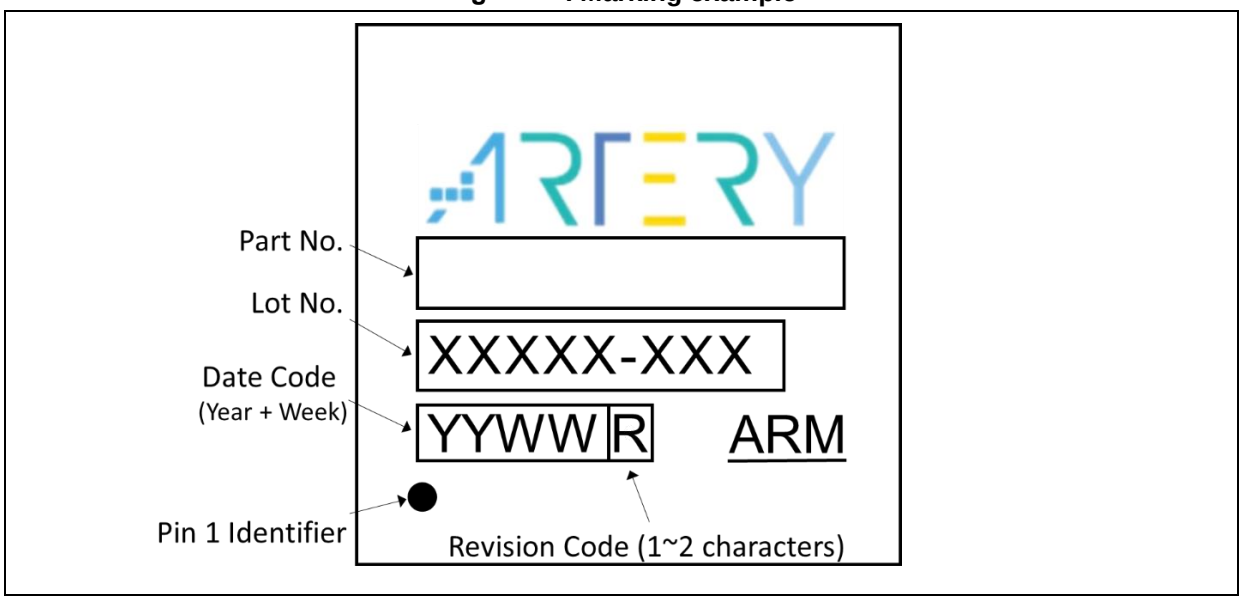


Table 76. QFN48 – 6 x 6 mm 48-pin quad flat no-leads package mechanical data

Symbol	millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.203 REF.		
D	5.90	6.00	6.10
D2	4.35	4.50	4.65
E	5.90	6.00	6.10
E2	4.35	4.50	4.65
e	0.40 BSC.		
Nd	4.40 BSC.		
Ne	4.40 BSC.		
h	0.35 REF.		
k	0.20	-	-
L	0.35	0.40	0.45

5.6 Device marking

Figure 50. Marking example



(1) Not in scale.

5.7 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6mm thickness. They are guaranteed by design, not tested in production.

Table 77. Package thermal characteristics

Symbol	Parameter	Values	Unit
Θ_{JA}	Thermal resistance junction-ambient — LQFP144 – 20 x 20 mm	67.2	°C/W
	Thermal resistance junction-ambient — LQFP100 – 14 x 14 mm	75.6	
	Thermal resistance junction-ambient — LQFP64 – 10 x 10 mm	80.6	
	Thermal resistance junction-ambient — LQFP48 – 7 x 7 mm	87.4	
	Thermal resistance junction-ambient — QFN48 – 6 x 6 mm	57.0	

6 Part numbering

Table 78. AT32F455/456/457 series part numbering

Example: AT32 F 4 5 7 Z E T 7

Product family

AT32 = ARM®-based 32-bit microcontroller

Product type

F = General-purpose

Core

4 = Cortex®-M4F

Product series

5 = Mainstream

Product application

7 = OTGFS + CANFD + EMAC series

6 = OTGFS + CANFD series

5 = OTGFS + CAN2.0 series

Pin count

Z = 144 pins

V = 100 pins

R = 64 pins

C = 48 pins

Internal Flash memory size

E = 512 Kbytes of Flash memory

C = 256 Kbytes of Flash memory

Package

T = LQFP

U = QFN

Temperature range

7 = -40 °C to +105 °C

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

7 Document revision history

Table 79. Document revision history

Date	Version	Revision note
2024.12.24	2.00	Initial release.

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