ARM®-based 32-bit Cortex®-M0+ MCU with 16 KB to 64 KB Flash, sLib, 10 timers, 1 ADC, 10 communication interfaces (1 CAN)

Features

- **Core: ARM® 32-bit Cortex®-M0+ CPU**
  - 80 MHz maximum frequency, with a memory protection unit (MPU), single-cycle multiplication
- **Hardware divider**
- **Memories**
  - 16 to 64 KB of internal Flash memory
  - 4 Kbytes of boot memory as a Bootloader, or as a general instruction/data memory (one-time-configurable)
  - sLib: configurable part of main Flash set as a library area with code executable but secured, non-readable
  - 9 Kbytes of SRAM (8 Kbytes with parity check)
- **Power control (PWC)**
  - 1.71 to 3.6 V power supply
  - Power-on reset (POR), low voltage reset (LVR) and power voltage monitoring (PVM)
  - Low power modes: Sleep, Deepsleep and Standby modes; 5 WKUP pins for wakeup from Standby mode
  - 5 x 32-bit battery powered registers (BPR)
- **Clock and reset management (CRM)**
  - 4 to 25 MHz crystal oscillator (HEXT)
  - Internal 48 MHz factory-trimmed HICK
  - 32 kHz crystal (LEXT)
  - Low speed internal clock (LICK)
- **Analog**
  - 1 x 12-bit 2 MSPS A/D converter, up to 15 external input channels; 12/10/8/6-bit configurable resolution; hardware over-sampling up to equivalent 16-bit resolution
  - Internal reference voltage (V_{INTRV})
- **DMA**
  - 1 x 5-channel DMA controller
- **Up to 39 fast GPIOs**
  - Core dedicated single-cycle GPIO bus
  - All mappable on 16 external interrupts (EXINT)
  - Almost all 5 V-tolerant
- **Up to 10 timers (TMR)**
  - 1 x 16-bit 7-channel advanced timer, including 3 pairs of complementary channels for PWM output, with dead-time generator and emergency brake
  - Up to 5 x 16-bit timers, each with 4 IC/OC /PWM or pulse counter and quadrature (incremental) encoder input
  - 1 x 16-bit basic timer
  - 2 x watchdog timers (general WDT and windowed WWDT)
  - SysTick timer: a 24-bit downcounter
- **ERTC: enhanced RTC, with alarm, subsecond accuracy, hardware calendar, and calibration**
- **Up to 10 communication interfaces**
  - 2 x I^2C interfaces (SMBus/PMBus) supporting fast mode plus (1 MHz), with wakeup from Deepsleep mode
  - 2 x SPIs (36 MHz), both with multiplexed as half-duplex I^2S
  - 4 x USARTs, supporting master synchronous SPI and modem control; with ISO7816 interface, LIN, IrDA, RS-485 driver enable; TX/RX swap; with wakeup from Deepsleep mode
  - CAN (2.0B Active) with 256 Kbytes of dedicated buffer
  - Infrared transmitter (IRTMR)
- **CRC calculation unit**
- **96-bit unique ID (UID)**
- **Serial wire debug (SWD) interface**
- **Operating temperature: -40 to +105 °C**

- **Packages**
  - LQFP48 7 x 7 mm
  - LQFP32 7 x 7 mm
  - QFN32 5 x 5 mm
  - QFN32 4 x 4 mm
  - QFN28 4 x 4 mm
  - QFN20 3 x 3 mm
  - TSSOP20 6.5 x 4.4 mm

Table 1. Device summary

Internal Flash	Part number
64 Kbytes	AT32L021C8T7, AT32L021K8T7, AT32L021K8U7, AT32L021K8U7-4, AT32L021G8U7, AT32L021F8U7, AT32L021F8P7
32 Kbytes	AT32L021C6T7, AT32L021K6T7, AT32L021K6U7, AT32L021K6U7-4, AT32L021G6U7, AT32L021F6U7, AT32L021F6P7
16 Kbytes	AT32L021C4T7, AT32L021K4T7, AT32L021K4U7, AT32L021K4U7-4, AT32L021G4U7, AT32L021F4U7, AT32L021F4P7

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1 Descriptions

The AT32L021 series is based on the high-performance ARM®Cortex®-M0+ 32-bit RISC core operating at a frequency of up to 80 MHz. The Cortex®-M0+ core features a memory protection unit (MPU) for application security. The device also offers a hardware divider (HWDIV) to improve computing efficiency as there is no divider in the Cortex®-M0+ core.

The AT32L021 series incorporates high-speed embedded memories (up to 64 Kbytes of internal Flash memory and 8+1 Kbytes of SRAM), and a wide range of enhanced GPIOs and peripherals connected to two APB buses. Any block of the embedded Flash memory can be protected by the “sLib”, functioning as a security area with code-executable only.

The AT32L021 series offers one 12-bit ADC, five general-purpose 16-bit timers, one advanced timer and one low-power ERTC, as well as standard and advanced communication interfaces: up to two I^2C interfaces, two SPIs (all multiplexed as I^2S), four USARTs, one CAN and one infrared transmitter.

The AT32L021 series operates in the -40 to +105 °C temperature range, from a 1.71 to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power application.

The AT32L021 offers devices in different package types. They are fully pin-to-pin, software and functionally compatible throughout the AT32L021 series, except that their peripheral configurations are not totally the same depending on the package type chosen.

Table 2. AT32L021 features and peripheral counts

Part number		AT32L021xxP7			AT32L021xxU7			AT32L021xxU7			AT32L021xxU7-4			AT32L021xxU7			AT32L021xxT7			AT32L021xxT7		
		F4	F6	F8	F4	F6	F8	G4	G6	G8	K4	K6	K8	K4	K6	K8	K4	K6	K8	C4	C6	C8
Frequency (MHz)		80																				
Int. Flash (KB)		16	32	64	16	32	64	16	32	64	16	32	64	16	32	64	16	32	64	16	32	64
SRAM (KB)		8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1	8+1
Timers	Advanced	1			1			1			1			1			1			1		
	16-bit general-purpose	5			5			5			5			5			5			5		
	Basic	1			1			1			1			1			1			1		
	SysTick	1			1			1			1			1			1			1		
	WDT	1			1			1			1			1			1			1		
	WWDT	1			1			1			1			1			1			1		
	ERTC	1			1			1			1			1			1			1		
Comm. interfaces	I^2C	2			2			2			2			2			2			2		
	SPI[1]	1[2]			1[2]			2			2			2			2			2		
	I^2S (half duplex)[1]	1[2]			1[2]			2			2			2			2			2		
	USART/UART	2/2[3]			2/2[3]			4/0			4/0			4/0			4/0			4/0		
	CAN	1			1			1			1			1			1			1		
	IRTMR	1			1			1			1			1			1			1		
Analog	12-bit ADC numbers/ external channels	1			1			1			1			1			1			1		
		9			9			10			11			11			10			15		
GPIO		15			15			23			27			27			25			39		
Operating temperatures		-40 °C to +105 °C																				
Packages		TSSOP20 6.5 x 4.4 mm			QFN20 3 x 3 mm			QFN28 4 x 4 mm			QFN32 4 x 4 mm			QFN32 5 x 5 mm			LQFP32 7 x 7 mm			LQFP48 7 x 7 mm		

(1) Half-duplex I^2S shares the same pin with SPI.
(2) Only supports SPI1/I^2S1.
(3) USART1 and USART4 only have TX and RX pins.

2 Functionality overview

2.1 ARM®Cortex®-M0+

The ARM®Cortex®-M0+ processor is the latest generation of ARM® core processor for embedded systems. It is a 32-bit RISC highly efficient processor featuring exceptional code efficiency, outstanding computing performance and advanced response to interrupts.

2.2 Hardware divider (HWDIV)

The hardware divider is capable of performing signed or unsigned 32-bit integer division operation, and producing 32-bit quotients and remainders.

2.3 Memory

2.3.1 Flash memory

Up to 64 Kbytes of embedded Flash memory is available for storing programs and data. Any part of the embedded Flash memory can be protected by the sLib (security library), a security area with code-executable only but non-readable. The “sLib” is a mechanism that protects the intelligence of solution venders and facilitates the second-level development by customers.

The AT32L021 series embeds 4 Kbytes of boot memory, in which the Bootloader is resided. If it is not needed, this boot memory can be used as a general instruction/data memory (one-time programmable) instead.

A User System Data block is available on the device for hardware configurations such as read/erase/write protection, watchdog self-enable and SRAM parity check. User System Data allows to set erase/write and read protection individually. There are two levels of memory access protection: low-level protection and high-level protection.

2.3.2 Memory protection unit (MPU)

The memory protection unit (MPU) is used to manage the CPU access to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area consists of up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory. The MPU is especially suitable for the applications where some critical or certified code must be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system).

2.3.3 Embedded SRAM

It is possible to configure the embedded SRAM as 9 Kbytes with no parity check (by default) or 8 Kbytes with parity check function. The SRAM is accessible at CPU clock speed with 0 wait state (for read/write access).

2.4 Interrupts

2.4.1 Nested vectored interrupt controller (NVIC)

The AT32L021 series embeds a nested vectored interrupt controller able to manage 4 priority levels and handle maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M0+. This hardware block provides flexible interrupt management features with minimal interrupt latency.

2.4.2 External interrupts (EXINT)

The external interrupt (EXINT), which is connected directly with NVIC, consists of 23 edge detector lines used to generate interrupt requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The external interrupt lines connects up to 16 GPIOs.

2.5 Power control (PWC)

2.5.1 Power supply schemes

- V_{DD} = 1.71 ~ 3.6 V: power supply for GPIOs and internal blocks such as voltage regulator (LDO), ERTC, external 32 kHz crystal (LEXT) and battery powered registers (BPR) through V_{DD} pin.
- V_{DDA} = 1.71 ~ 3.6 V: power supply for ADC through V_{DDA} pin. V_{DDA} and V_{SSA} must be the same voltage potential as V_{DD} and V_{SS}, respectively.

2.5.2 Reset and power voltage monitoring (POR / LVR / PVM)

The device has an integrated power-on reset (POR) and low voltage reset (PDR) circuitry. It is always active, and allows proper operation starting from/down to 1.71 V. The device remains in reset mode when V_{DD} is below a specified threshold (V_{LVR}) without the need for an external reset circuit.

The device embeds a power voltage monitor (PVM) that monitors the V_{DD} power supply and compares it to the V_{PVM} threshold. An interrupt is generated when V_{DD} drops below the V_{PVM} threshold and/or when V_{DD} rises above the V_{PVM} threshold. The PVM is enabled by software.

2.5.3 Voltage regulator (LDO)

The LDO has three operation modes: normal, low-power, and power down.

- Normal mode: used in Run/Sleep mode and in the Deepsleep mode.
- Low-power mode: can be used in the Deepsleep mode.
- Power down mode: used in Standby mode: The LDO output is in high impedance and the kernel circuitry is powered down but the contents of the registers and SRAM are lost.

The LDO always operates in normal mode after reset.

The LDO has the ability to adjust output voltage. Besides the default 1.2 V, it supports 1.0 V by software so as to provide best tradeoff between performance and power consumption. Different LDO voltages correspond to different AHB and APB clock frequencies, as shown in *Table 11* .Users should follow steps specified in the AT32L021 reference manual for LDO voltage adjustment and system clock configuration.

2.5.4 Low-power modes

The AT32L021 series supports three low-power modes:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Deepsleep mode**

  Deepsleep mode achieves the low power consumption while retaining the content of SRAM and registers. All clocks in the LDO domain are stopped, disabling the PLL, the HICK clock, and the HEXT crystal. The voltage regulator LDO can also be put in normal or low-power mode.

  The device can be woken up from Deepsleep mode by any of the EXINT line. The EXINT line source can be one of the 16 external GPIOs, the PVM output, the ERTC alarm/tamper detection/time stamp, or the wakeup events from I^2C1/USART1/USART2.

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal LDO is switched off so that the entire LDO domain is powered off. The PLL, the HICK clock and the HEXT crystal are also switched off. After entering Standby mode, SRAM and register contents are lost except for registers in the BPR domain and ERTC domain.

  The device exits Standby mode when an external reset (NRST pin), a WDT reset, a rising edge on the WKUPx pin, or an ERTC alarm/tamper detection/time stamp occurs.

Note: The corresponding clock sources of ERTC are not stopped by entering Deepsleep or Standby mode. WDT depends on the User System Data settings.

2.6 Boot modes

At startup, BOOT0 pin and nBOOT1 bit (in the User System Data) are used to select one out of three boot options:

- Boot from user Flash memory;
- Boot from boot memory;
- Boot from embedded SRAM.

The bootloader is stored in boot memory. It is used to reprogram the Flash memory through using USART1 or USART2. *Table 3* provides the pin configurations for Bootloader in AT32L021.

Table 3. Pin configurations for Bootloader

Peripherals	Pins
USART1	PA9: USART1_TX PA10: USART1_RX
USART2	PA2: USART2_TX PA3: USART2_RX

2.7 Clocks

On reset the internal 48 MHz clock (HICK) after being divided by 6 divider (8 MHz) is selected as the default CPU clock. An external 4 to 25 MHz clock (HEXT) can be selected, in which case it is monitored for failure. If failure is detected, HEXT will be switched off and the system automatically switches back to the internal HICK. A software interrupt is generated. Similarly, the system takes the same action once HEXT fails when it is used as the source of PLL.

Several prescalers are used for the configuration of the AHB and the APB (APB1 and APB2) frequency. The maximum frequency of the AHB and APB domains is 80 MHz.

2.8 General-purpose inputs/outputs (GPIO)

Each of the GPIO pins are in analog mode on reset. After reset, they can be configured by software as output (push-pull or open-drain with or without pull-up or pull-down), as input (floating with or without pull-up or pull-down), or as peripheral multiplexed function. Most of the GPIO pins are shared with digital or analog multiplexed functions. All GPIOs are high current-capable.

The GPIO configuration can be locked if needed by using a specific sequence in order to avoid spurious writing to the GPIOs registers.

GPIOs are directly controlled by the core dedicated single cycle bus, which allows fast GPIO toggling at a maximum of one system clock cycle.

2.9 Direct Memory Access Controller (DMA)

The AT32L021 series features a 5-channel general-purpose DMA. It is able to manage memory-to-memory, peripheral-to-memory, and memory-to-peripheral transfers.

The DMA controller supports circular buffer management, so that no user code intervention is needed when the controller reaches the end of the buffer.

Each channel is connected to dedicated hardware DMA requests, with support for software trigger on each channel. Configuration is made by software and the number of transfers between source and destination are independent.

The DMA can be used with the main peripherals: SPI, I^2S, I^2C, USART, all timers TMRx (except TMR14) and ADC.

2.10 Timers (TMR)

The AT32L021 devices include one advanced timer, five general-purpose timers, one basic timer and one SysTick timer.

The table below compares the features of the advanced, general-purpose, and basic timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Advanced	TMR1	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	3
General-purpose	TMR3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TMR14	16-bit	Up	Any integer between 1 and 65536	No	1	No
	TMR15	16-bit	Up	Any integer between 1 and 65536	Yes	2	1
	TMR16 TMR17	16-bit	Up	Any integer between 1 and 65536	Yes	1	1

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
Basic	TMR6	16-bit	Up	Any integer between 1 and 65536	Yes	No	No

2.10.1 Advanced timer (TMR1)

The advanced timer (TMR1) can be seen as a three-phase PWM generator assigned to six channels. They have complementary PWM outputs with programmable inserted dead-times. They can also be used as a complete general-purpose timer. These four independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge or center-aligned modes)
- One-cycle mode output

If configured as a standard 16-bit timer, it has the same features as the TMRx timers. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%).

In debug mode, the counter can be frozen and the PWM outputs disabled to turn off any power switch driven by these outputs.

Many features of the advanced timer are shared with those of the general-purpose TMRs which have the same architecture. The advanced timer can therefore work together with the TMR timers via the link feature for synchronization or event chaining.

2.10.2 General-purpose timers (TMR3, TMR14, TMR15, TMR16 and TMR17)

There are up to 5 synchronizable general-purpose timers embedded in the AT32L021 series.

- **TMR3**

  The TMR3 timer is based on a 16-bit auto-reload upcounter/downcounter and a 16-bit prescaler. It features four independent channels on the largest package, each for input capture, output compare, PWM or one-cycle mode output.

  It can work together with the advanced timer via the link feature for synchronization or event chaining. In debug mode, the counter can be frozen. TMR3 can be used to generate PWM outputs. It has an independent DMA request mechanism. It is also capable of handling incremental encoder signals and the digital outputs from 1 to 3 hall-effect sensors.

- **TMR14**

  The TMR14 timer is based on a 16-bit auto-reload upcounter, a 16-bit prescaler, and one independent channel for input capture/output compare, PWM, or one-cycle mode output. It can be synchronized with full-featured general-purpose timers. It can also be used as a simple time base. In debug mode, the counter can be frozen.

- **TMR15, TMR16 and TMR17**

  These three timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TMR15 features two channels and one complementary channel. TMR16 and TMR17 have one channel and one complementary channel, respectively. All channels can be used for input capture/output compare, PWM, or one-pulse mode output.

  They can work together via the Timer link feature for synchronization or event chaining.

  In debug mode, the counter can be frozen. These timers have independent DMA request generations.

2.10.3 Basic timer (TMR6)

This timer is used as a generic 16-bit time base.

2.10.4 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features include:

- A 24-bit downcounter
- Auto reload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source (HCLK or HCLK/8)

2.11 Watchdog (WDT)

The watchdog consists of a 12-bit downcounter and 8-bit prescaler. It is clocked by an independent internal LICK clock. As it operates independently from the main clock, it can operate in Deepsleep and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free running timer for application timeout management. It is self-enabling or not through the User System Data configuration. The counter can be frozen in debug mode.

2.12 Window watchdog (WWDT)

The window watchdog embeds a 7-bit downcounter that can be set as free running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

2.13 Enhanced real-time clock (ERTC) and battery powered registers (BPR)

The battery powered domain includes:

- Enhanced real-time clock (ERTC)
- 5 x 32-bit battery powered registers

The enhanced real-time clock (ERTC) is an independent BCD timer/counter. It supports the following features:

- Calendar with second, minute, hour (12 or 24 format), week day, date, month, year, in BCD (binary-coded decimal) format.
- The sub-seconds value in binary format.
- Automatic correction for 28, 29 (leap year), 30, and 31 days of the month.

- Programmable alarms with wake up from Stop or Standby mode capability.
- Correction of ERTC timer pulses from one to 32767 during runtime to synchronize ERTC with master clock
- Digital calibration circuit with an 1 ppm resolution to compensate for any deviation in crystal quartz accuracy
- Anti-tamper detection pins with programmable filer. MCU can be woke up from Deepsleep and Standby modes upon tamper event detection
- Timestamp function for calendar content saving. This function can be triggered by the event on timestamp on or by tamper event. MCU is woke up from Deepsleep and Standby modes upon a timestamp event detection
- Reference timer detection: a more precise second source clock (50 or 60 Hz) can be used to enhance calendar precision

The alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. Other 32-bit registers also contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

A prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The battery powered registers (BPR) are 32-bit registers used to store 20 bytes of user application data. Battery powered registers are not reset by a system, or when the device wakes up from the Standby mode.

2.14 Communication interfaces

2.14.1 Serial peripheral interface (SPI)

Two SPIs are able to communicate up to 36 Mbits/s in master and slave modes. The prescaler gives multiple master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC/SDHC modes. Both SPIs can be served by the DMA controller.

These SPI interfaces can be configured to operate in TI mode for communications in master mode and slave mode.

2.14.2 Inter-integrated sound interface (I^2S)

Two standard I^2S interfaces (multiplexed with SPI) are available, that can be operated in master mode or slave mode. These interfaces can be configured to operate with 16/24/32-bit resolution, as input or output channels. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When any of the I^2S interfaces is/are configured in master mode, the master clock can be output at 256 times the sampling frequency. Both I^2S can be served by the DMA controller.

2.14.3 Universal synchronous / asynchronous receiver transmitters (USART)

The AT32L021 series embeds four universal synchronous/asynchronous receivers/transmitters (USART1 ~ USART4).

These four USART interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode, and have LIN Master/Slave capability. These four USART interfaces also provide hardware management of the CTS and RTS signals, RS485 drive enable signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller. TX/RX pins are swappable.

Of these interfaces, USART1 and USART2 support a clock domain which is independent of the PCLK clock so that they are able to wake up MCU from Deepsleep mode.

2.14.4 Inter-integrated-circuit interface (I^2C)

Two I^2C bus interfaces can operate in multi-master mode and slave mode. They support the standard mode (up to 100 kHz), fast mode (up to 400 kHz) and fast mode plus (up to 1 MHz). Some of the GPIOs supports up to 20 mA current sinking capacity.

They support 7/10-bit addressing mode and 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is included.

Of these interfaces, I^2C1 has optional clock sources which are independent of PCLK clock so that it can have its communication speed configured outside the system clock, and can wake up MCU from Deepsleep mode upon an address matching event. There are configurable digital and analog filters inside the bus.

They can be served by DMA and they support SMBus 2.0/PMBus.

2.14.5 Controller area network (CAN)

The CAN is compliant with the 2.0A and 2.0B (active) specifications with a bit rate up to 1 Mbit/s. It can receive and transmit standard frames with 11-bit identifiers as well as extended frames with 29-bit identifiers. This CAN has three transmit mailboxes, two receive FIFOs with 3 stages, and 14 scalable filter banks. It also has a dedicated 256-Byte buffer which is not shared with any other peripherals.

To guarantee transmission quality, according to the clock accuracy requirements in CAN 2.0 specifications, the CAN clock source should be the PLL clock sourced by HEXT.

2.14.6 Infrared transmitter (IR)

The AT32L021 devices provide an infrared transmitter solution. The solution is based on the internal connection between TMR16 and TMR17. TMR17 is used to provide the carrier frequency, while TMR16 provides the main signals to send.

To generate infrared remote control signals, TMR16 channel 1 and TMR17 channel 1 must be correctly configured to generate correct waveforms. All standard IR pulse modulation modes can be obtained by programming two timer output compare channels.

2.15 Cyclic redundancy check (CRC) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial. Among other applications, CRC-based techniques are used to verify data transmission or storage integrity.

2.16 Analog-to-digital converter (ADC)

One 12-bit 2 MSPS analog-to-digital converter is embedded in the AT32L021 devices and shares up to 15 external channels and 3 internal channels connected to V_{SSA}, internal reference voltage (V_{INTRV}), and $V_{DDA,}$ respectively. The ADC controller can achieve single or sequence mode converstion. In sequence mode, automatic conversion is performed on a selected group of analog channels in single or sequential mode.

It has 12-bit, 10-bit, 8-bit or 6-bit configuration resolution. It also supports 2 times to 256 times hardware oversampling with up to equivalent 16-bit resolution.

The ADC can be served by the DMA controller.

Voltage monitoring feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

The events generated by the general-purpose timers (TMRx) and the advanced timer (TMR1) can be internally connected to the ADC ordinary channel trigger and preempted channel trigger, respectively, to allow the application to synchronize ADC conversion and timers.

The internal reference voltage (V_{INTRV}) offers a stable voltage output for the ADC. The V_{INTRV} is internally connected to the input channel ADC_IN17.

2.17 Serial wire debug (SWD)

The ARM® SWD interface is embedded, and is a serial wire debug port that enables a serial wire debug to be connected to the target for programming and debugging the target.

3 Pin functional definitions

Figure 1. AT32L021 LQFP48 pinout

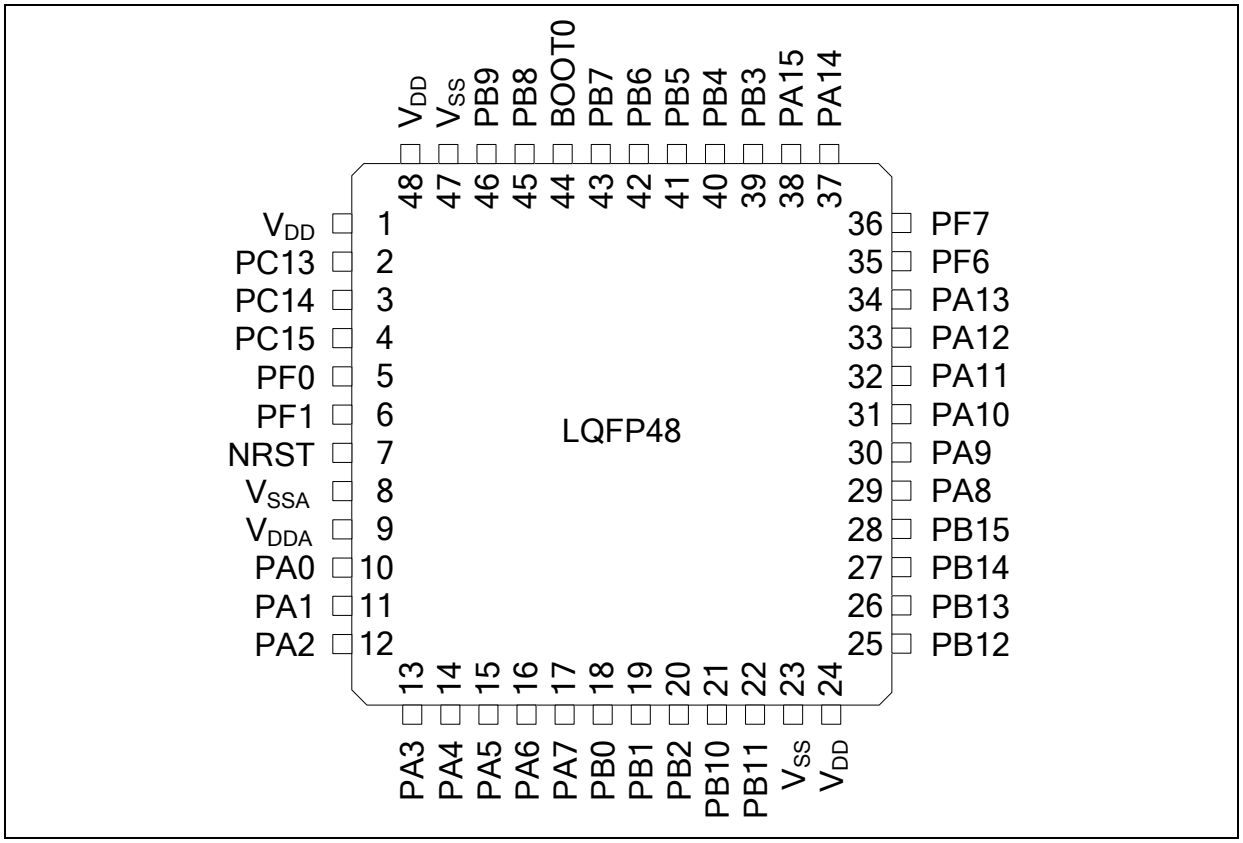


Figure 2. AT32L021 LQFP32 pinout

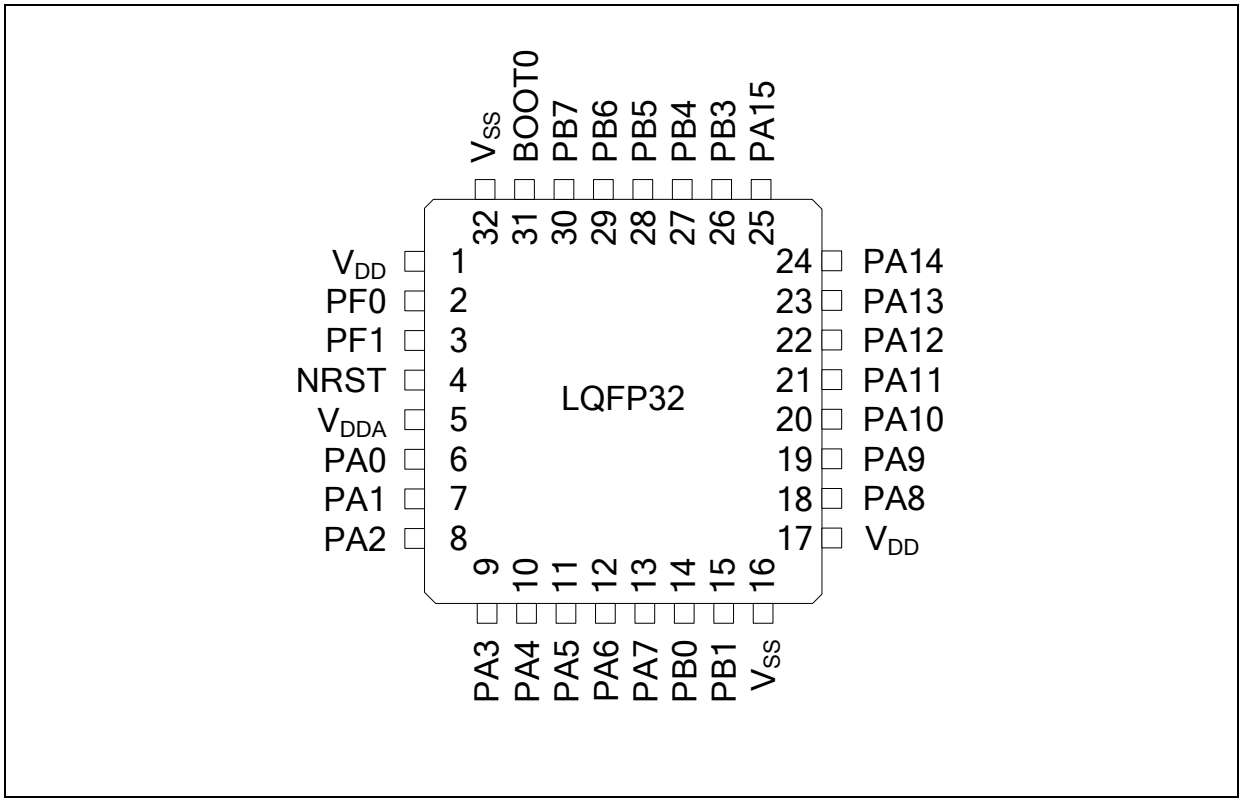


Figure 3. AT32L021 QFN32 pinout

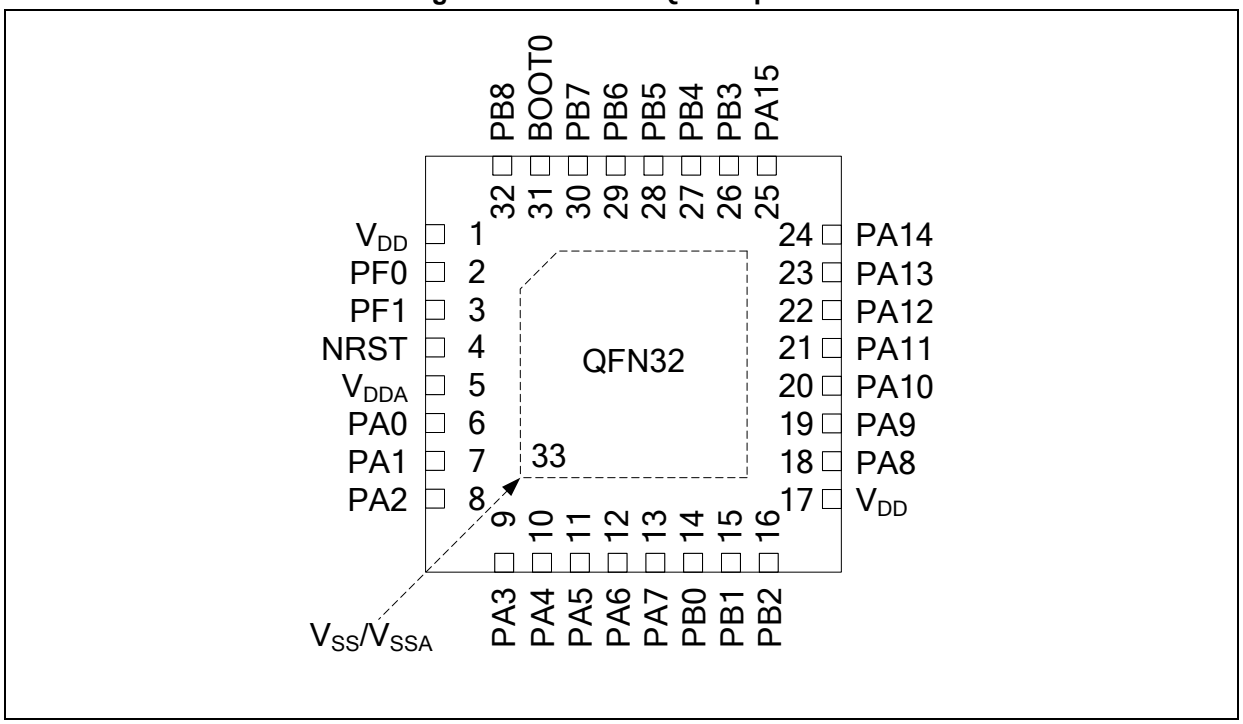


Figure 4. AT32L021 QFN28 pinout

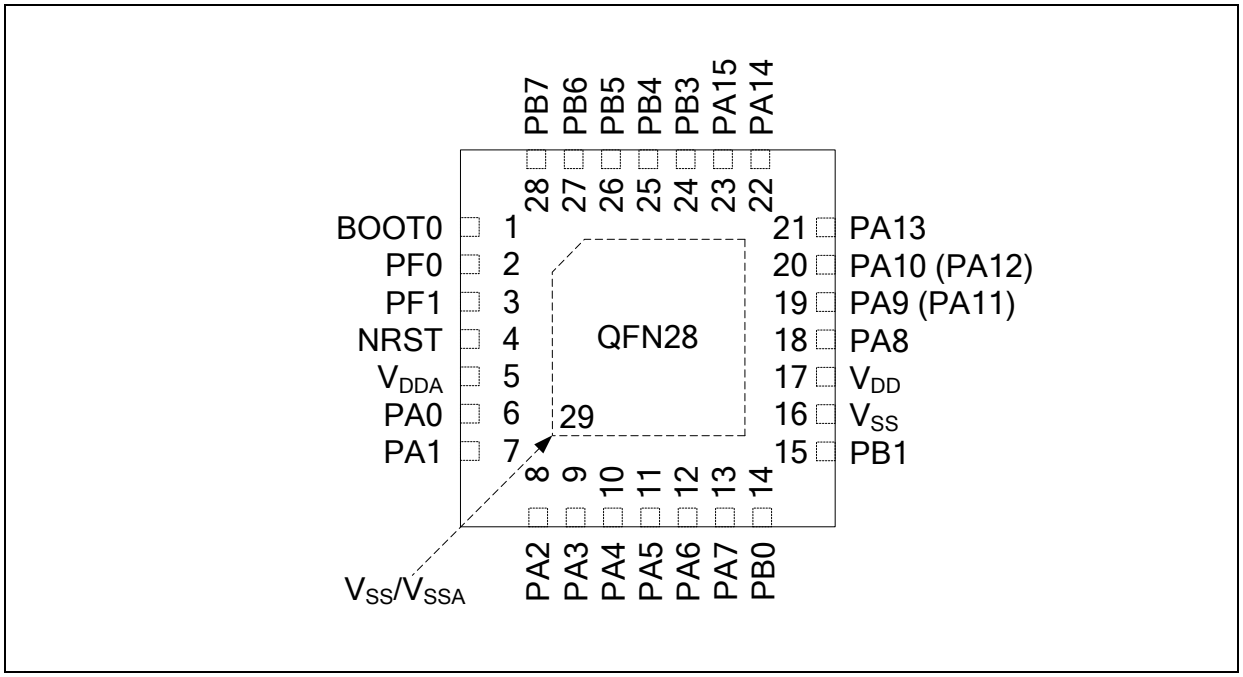


Figure 5. AT32L021 QFN20 pinout

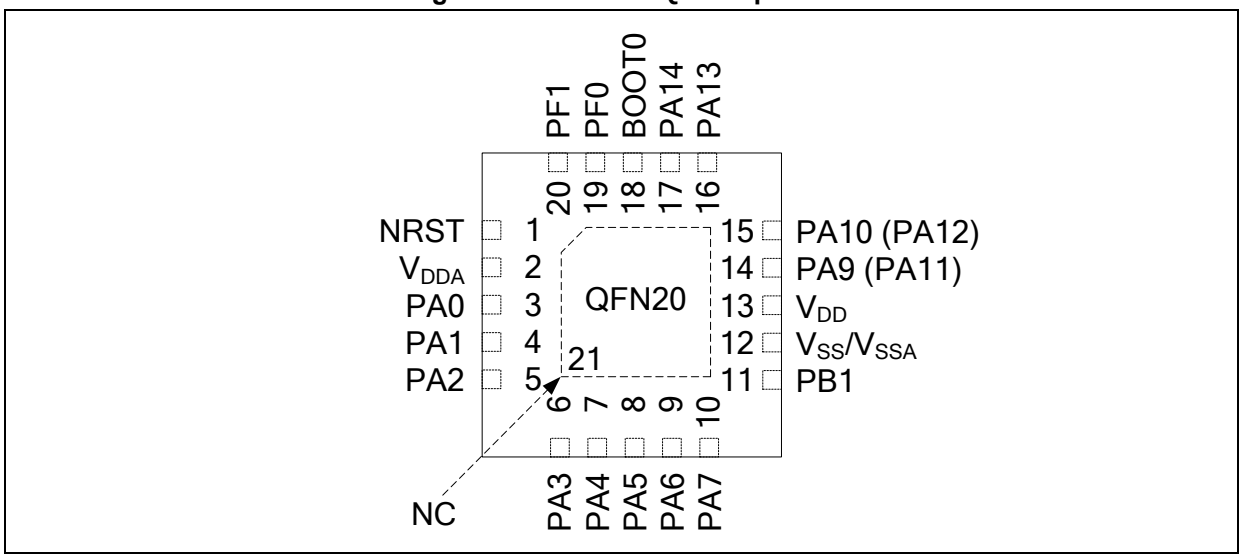
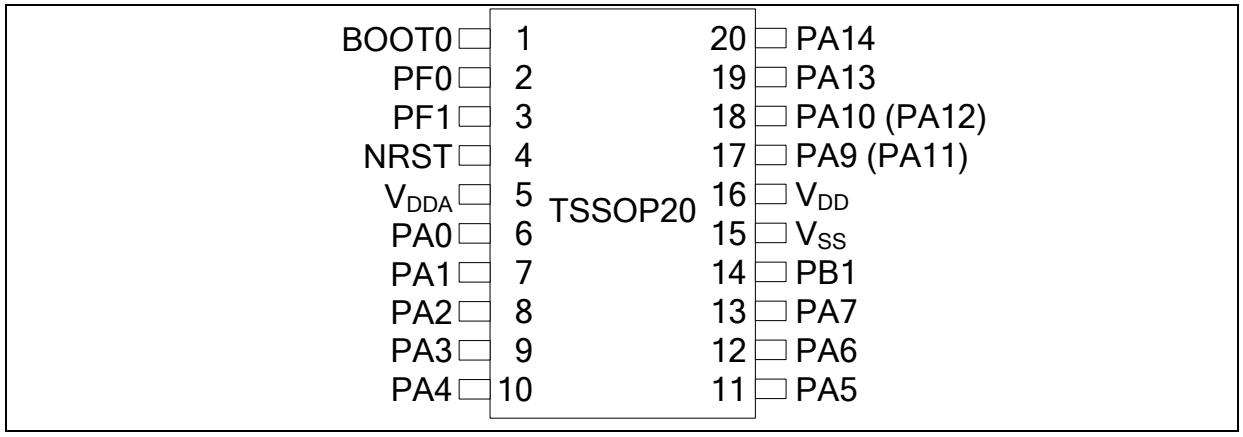


Figure 6. AT32L021 TSSOP20 pinout



The table below is the pin definition of the AT32L021. "-" presents there is no such pinout on the related package. Unless otherwise specified, the pins during and after reset have the same functions as those of actual ones, and all GPIOs are configured as analog modes during and after reset. Alternate functions of pins are enabled through the GPIOx_MUXx register, and additional functions are selected through peripheral registers.

Table 5. AT32L021 series pin definitions

Pin number						Pin name (after reset)	Pin type (1)	GPIO structure (2)	Alternate function	Additional function
TSSOP20	QFN20	QFN28	QFN32	LQFP32	LQFP48					
-	-	-	1	1	1	V_{DD}	S	-	Digital power supply	
-	-	-	-	-	2	PC13	I/O	FT	-	TAMP / WKUP2
-	-	-	-	-	3	PC14	I/O	TC	-	LEXT_IN
-	-	-	-	-	4	PC15	I/O	TC	-	LEXT_OUT
2	19	2	2	2	5	PF0	I/O	FT	I2C1_SDA / TMR1_CH1	HEXT_IN
3	20	3	3	3	6	PF1	I/O	FT	I2C1_SCL / TMR1_CH2C SPI2_CS / I2S2_WS	HEXT_OUT
4	1	4	4	4	7	NRST	I/O	R	Device reset input / internal reset output (active low)	
-	-	-	-	-	8	V_{SSA}	S	-	Analog ground	
5	2	5	5	5	9	V_{DDA}	S	-	Analog power supply	
6	3	6	6	6	10	PA0	I/O	FTa	USART2_RX / USART2_CTS / I2C2_SCL / USART4_TX / TMR1_EXT /	ADC_IN0 / WKUP1
7	4	7	7	7	11	PA1	I/O	FTa	USART2_RTS_DE / I2C2_SDA / USART4_RX / TMR15_CH1C / I2C1_SMBA / EVENTOUT	ADC_IN1
8	5	8	8	8	12	PA2	I/O	FTa	TMR15_CH1 / USART2_TX / CAN_RX	ADC_IN2 / WKUP4
9	6	9	9	9	13	PA3	I/O	FTa	TMR15_CH2 / USART2_RX / CAN_TX / I2S2_MCK	ADC_IN3
10	7	10	10	10	14	PA4	I/O	FTa	SPI1_CS / I2S1_WS / USART2_CK / TMR14_CH1 / I2C1_SCL / SPI2_CS / I2S2_WS	ADC_IN4
11	8	11	11	11	15	PA5	I/O	FTa	SPI1_SCK / I2S1_CK / USART3_CK / USART3_RX	ADC_IN5
12	9	12	12	12	16	PA6	I/O	FTa	SPI1_MISO / I2S1_MCK / TMR3_CH1 / TMR1_BRK / USART3_RX / USART3_CTS / TMR16_CH1 / I2S2_MCK / EVENTOUT	ADC_IN6
13	10	13	13	13	17	PA7	I/O	FTa	SPI1_MOSI / I2S1_SD / TMR3_CH2 / TMR1_CH1C / USART3_TX / TMR14_CH1 / TMR17_CH1 / EVENTOUT	ADC_IN7
-	-	14	14	14	18	PB0	I/O	FTa	TMR3_CH3 / TMR1_CH2C / USART2_RX / USART3_CK / EVENTOUT SPI1_MISO / I2S1_MCK	ADC_IN8

Pin number						Pin name (after reset)	Pin type (1)	GPIO structure (2)	Alternate function	Additional function
TSSOP20	QFN20	QFN28	QFN32	LQFP32	LQFP48					
14	11	15	15	15	19	PB1	I/O	FTa	TMR14_CH1 / TMR3_CH4 / TMR1_CH3C / USART2_CK / USART3_RTS_DE / SPI2_SCK / I2S2_CK / SPI1_MOSI / I2S1_SD	ADC_IN9
-	-	-	16	-	20	PB2	I/O	FTa	TMR3_EXT / I2C1_SMBA	ADC_IN10
-	-	-	-	-	21	PB10	I/O	FT	I2C2_SCL / USART3_TX / SPI2_SCK / I2S2_CK	-
-	-	-	-	-	22	PB11	I/O	FT	I2C2_SDA / EVENTOUT / USART3_RX	-
15	-	16	-	16	23	V_{SS}	S	-	Digital ground	
-	12	-	-	-	-	V_{SS}/V_{SSA}			Digital ground / Analog ground	
16	13	17	17	17	24	V_{DD}	S	-	Digital power supply	
-	-	-	-	-	25	PB12	I/O	FTa	SPI2_CS / I2S2_WS / EVENTOUT / TMR1_BRK / USART3_CK / TMR15_BRK / I2C2_SMBA	ADC_IN11
-	-	-	-	-	26	PB13	I/O	FTa	SPI2_SCK / I2S2_CK / TMR15_CH1C / TMR1_CH1C / CLKOUT / USART3_CTS / I2C2_SCL	ADC_IN12
-	-	-	-	-	27	PB14	I/O	FTa	SPI2_MISO / I2S2_MCK / TMR15_CH1 / TMR1_CH2C / USART3_RTS_DE / I2C2_SDA	ADC_IN13
-	-	-	-	-	28	PB15	I/O	FTa	SPI2_MOSI / I2S2_SD / TMR15_CH2 / TMR1_CH3C / TMR15_CH1C / RTC_REFIN	ADC_IN14 / WKUP7
-	-	18	18	18	29	PA8	I/O	FT	CLKOUT / USART1_CK / TMR1_CH1 / EVENTOUT / USART2_TX / I2C2_SCL	-
17	14	19	19	19	30	PA9	I/O	FT	TMR15_BRK / USART1_TX / TMR1_CH2 / I2C1_SCL / CLKOUT / I2C2_SMBA	-
18	15	20	20	20	31	PA10	I/O	FT	TMR17_BRK / USART1_RX / TMR1_CH3 / I2C1_SDA / RTC_REFIN / I2C2_SMBA	-
17(3)	14(3)	19(3)	21	21	32	PA11	I/O	FT	USART1_CTS / TMR1_CH4 / CAN_RX / I2C2_SCL / I2C1_SMBA / EVENTOUT	-
18(3)	15(3)	20(3)	22	22	33	PA12	I/O	FT	USART1_RTS_DE / TMR1_EXT / CAN_TX / I2C2_SDA / EVENTOUT	-
19	16	21	23	23	34	PA13 (SWDIO(4))	I/O	FT	IR_OUT / I2C1_SDA / SPI2_MISO / I2S2_MCK	-
-	-	-	-	-	35	PF6	I/O	FT	I2C2_SCL / USART4_RX	-
-	-	-	-	-	36	PF7	I/O	FT	I2C2_SDA / USART4_TX	-
20	17	22	24	24	37	PA14 (SWCLK(4))	I/O	FT	USART2_TX / I2C1_SMBA / SPI2_MOSI / I2S2_SD	-

Pin number						Pin name (after reset)	Pin type (1)	GPIO structure (2)	Alternate function	Additional function
TSSOP20	QFN20	QFN28	QFN32	LQFP32	LQFP48					
-	-	23	25	25	38	PA15	I/O	FT	SPI1_CS / I2S1_WS / USART2_RX / EVENTOUT / USART4_RTS_DE / SPI2_CS / I2S2_WS	-
-	-	24	26	26	39	PB3	I/O	FT	SPI1_SCK / I2S1_CK / EVENTOUT / USART1_RTS_DE / USART2_CTS / SPI2_SCK / I2S2_CK	-
-	-	25	27	27	40	PB4	I/O	FT	SPI1_MISO / I2S1_MCK / TMR3_CH1 / EVENTOUT / USART1_CTS / TMR17_BRK / SPI2_MISO / I2S2_MCK / I2C2_SDA	-
-	-	26	28	28	41	PB5	I/O	FT	SPI1_MOSI / I2S1_SD / TMR3_CH2 / TMR16_BRK / I2C1_SMBA / USART1_CK / USART2_RTS_DE / SPI2_MOSI / I2S2_SD	WKUP6
-	-	27	29	29	42	PB6	I/O	FT	USART1_TX / I2C1_SCL / TMR16_CH1C / USART4_CK / I2S1_MCK	-
-	-	28	30	30	43	PB7	I/O	FT	USART1_RX / I2C1_SDA / TMR17_CH1C / USART4_CTS	-
1	18	1	31	31	44	BOOT0	I	B	Boot mode select 0	
-	-	-	32	-	45	PB8	I/O	FTf	USART1_TX / I2C1_SCL / TMR16_CH1 / EVENTOUT / CAN_RX	
-	-	-	-	-	46	PB9	I/O	FTf	IR_OUT / I2C1_SDA / TMR17_CH1 / EVENTOUT / CAN_TX / I2S1_MCK / SPI2_CS / I2S2_WS	
-	-	-	-	32	47	V_{SS}	S	-	Digital ground	
-	-	-	-	-	48	V_{DD}	S	-	Digital power supply	
-	-	29	33	-	-	EPAD - V_{SS}/V_{SSA}	S	-	Digital ground / Digital ground	
-	21	-	-	-	-	EPAD - NC	-	-	Disconnected	

(1) I = input, O = output, S = supply.

(2) TC = standard level, FT = general 5 V-tolerant, FTa = 5 V-tolerant with analog functions, FTf = 5 V tolerant with 20 mA current sinking capacity, R = bidirectional reset pin with embedded weak pull-up resistor, B = dedicated BOOT0 pin with embedded weak pull-down resistor.

(3) PA11/PA12 and their alternate function can be remapped to replace the original PA9/PA10 and their alternate function by software.

(4) After reset, PA13/PA14 pins are configured as the alternate functions SWDIO/SWCLK, and the internal pull-up resistor on the SWDIO pin and the internal pull-down resistor on the SWCLK pin are activated.

4 Electrical characteristics

4.1 Parameter conditions

4.1.1 Minimum and maximum values

The minimum and maximum values are guaranteed in the worst conditions. Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. The minimum and maximum values represent the mean value plus or minus three times the standard deviation (mean ± 3σ).

4.1.2 Typical values

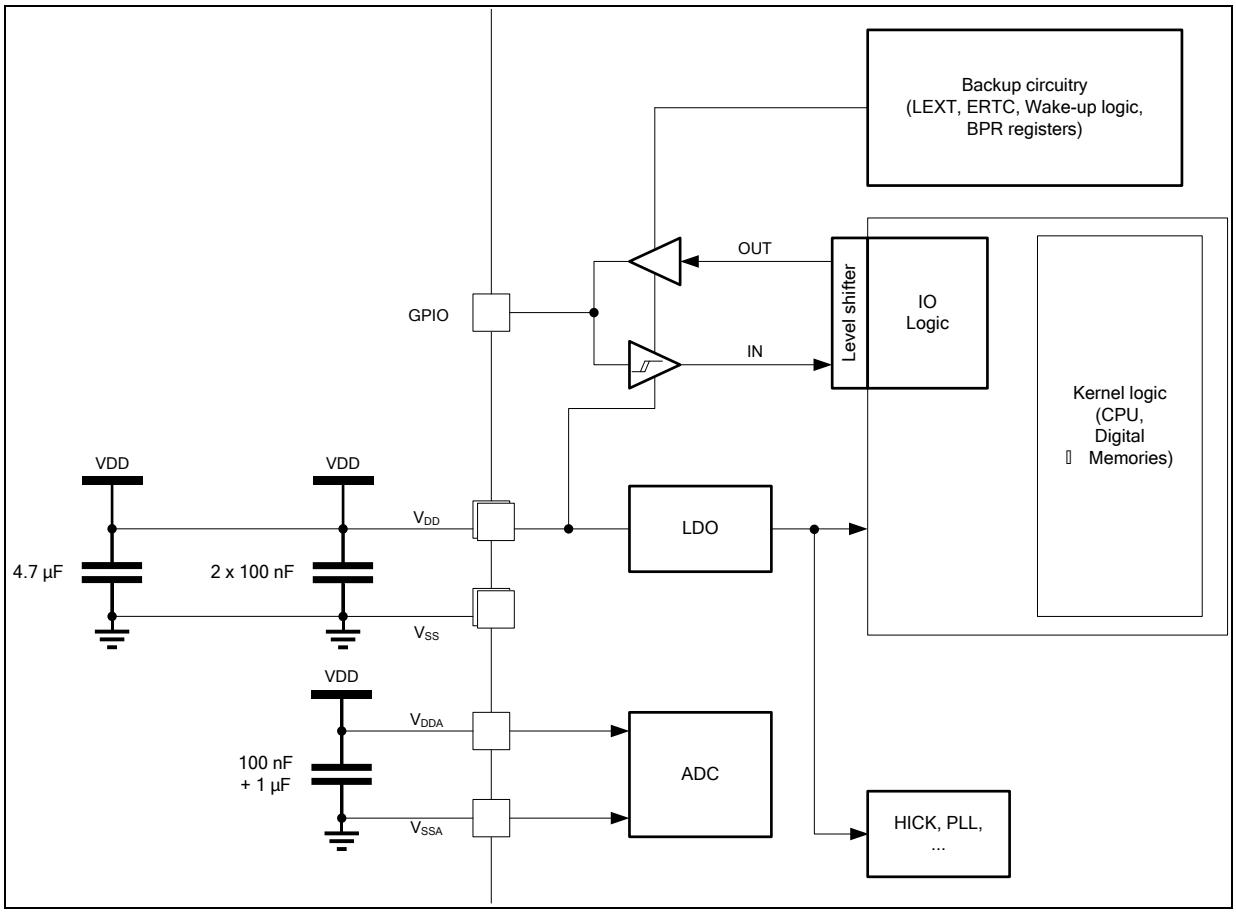
Typical data are based on T_A = 25 °C, V_{DD} = 3.3 V.

4.1.3 Typical curves

All typical curves are given only as design guidelines and are not tested.

4.1.4 Power supply scheme

Figure 7. Power supply scheme



4.2 Absolute maximum values

4.2.1 Ratings

If stresses were out of the absolute maximum ratings listed *Table 6*, *Table 7* and *Table 8*, it may cause permanent damage to the device. These are maximum stress ratings only that the device could bear, but the functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for an extended period of times may affect device reliability.

Table 6. Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD}-V_{SS}	External main supply voltage (including V_{DDA} and V_{DD})	-0.3	4.0	V
V_{IN}	Input voltage on FT and FTa pins	V_{SS}-0.3	6.0	
	Input voltage on TC pin	V_{SS}-0.3	4.0	
$\|\Delta V_{DDx}\|$	Variations between different V_{DD} power pins	-	50	mV
$\|V_{SSx}$-$V_{SS}\|$	Variations between all the different ground pins	-	50	

Table 7. Current characteristics

Symbol	Description	Max	Unit
I_{VDD}	Total current into V_{DD} power lines (source)	100	mA
I_{VSS}	Total current out of V_{SS} ground lines (sink)	100	
I_{IO}	Output current sunk by any GPIO and control pin	25	
	Output current source by any GPIO and control pin	-25	

Table 8. Temperature characteristics

Symbol	Description	Value	Unit
T_{STG}	Storage temperature range	-60 ~ +150	°C
T_J	Maximum junction temperature	125	

4.2.2 Electrical sensitivity

Based on three different tests (HBM, CDM, and LU) using specific measurement methods, the device is stressed in order to determine its performance in terms of electrical sensitivity.

Electrostatic discharge (ESD)

Electrostatic discharges are applied to the pins of each sample according to each pin combination. This test conforms to the JS-001-2017/JS-002-2018 standard.

Table 9. ESD values

Symbol	Parameter	Conditions	Class	Min	unit
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	T_A = +25 °C, conforms to JS-001-2017	2	±2000	V
$V_{ESD(CDM)}$	Electrostatic discharge voltage (charge device model)	T_A = +25 °C, conforms to JS-002-2018	III	±2000	

Static latch-up

Tests compliant with EIA/JESD78E latch-up standard are required to assess the latch-up performance:

- A supply overvoltage is applied to each power supply pin;
- A current injection is applied to each input, output and configurable GPIO pin.

Table 10. Static latch-up values

Symbol	Parameter	Conditions	Level/Class
LU	Static latch-up	T_A = +105 °C, conforms to EIA/JESD78E	II level A (±300 mA)

4.3 Specifications

4.3.1 General operating conditions

Table 11. General operating conditions

Symbol	Parameter	Conditions		Min	Max	Unit
f_{HCLK}	Internal AHB clock frequency	LDO voltage	1.2 V	0	80	MHz
			1.0 V	0	32	
$f_{PCLK1/2}$	Internal APB1/2 clock frequency	-		0	f_{HCLK}	MHz
V_{DD}	Digital operating voltage	-		1.71	3.6	V
V_{DDA}	Analog operating voltage	Must be the same potential as V_{DD}		V_{DD}		V
P_D	Power dissipation: T_A = 105 °C	LQFP48 (7 x 7 mm)		-	212	mW
		LQFP32 (7 x 7 mm)		-	216	
		QFN32 (5 x 5 mm)		-	312	
		QFN32 (4 x 4 mm)		-	280	
		QFN28 (4 x 4 mm)		-	275	
		QFN20 (3 x 3 mm)		-	233	
		TSSOP20 (6.5 x 4.4 mm)		-	183	
T_A	Ambient temperature	-		-40	105	°C

4.3.2 Operating conditions at power-up/power-down

Table 12. Operating conditions at power-up/power-down

Symbol	Parameter	Conditions	Min	Max	Unit
t_{VDD}	V_{DD} rise time rate	-	0	∞(1)	ms/V
	V_{DD} fall time rate		20	∞	μs/V

(1) When V_{DD} rise time rate is lower than 30 ms/V, it is recommended to operate GPIOs only after V_{DD} reaches the maximum V_{POR}. Refer to AT32L021 errata sheet for details.

4.3.3 Embedded reset and power control block characteristics

Table 13. Embedded reset and power control block characteristics(1)

Symbol	Parameter	Min	Typ	Max	Unit
V_{POR}	Power-on reset threshold	1.64	1.66	1.71	V
V_{LVR}	Low voltage reset threshold	1.62(2)	1.64	1.69	V
$V_{LVRhyst}$	LVR hysteresis	-	20	-	mV
$T_{RESTTEMPO}$	Reset temporization: CPU starts execution after V_{DD} keeps higher than V_{POR} for $T_{RSTTEMPO}$	-	3.3	-	ms

(1) Guaranteed by design, not tested in production.
(2) The product behavior is guaranteed by design down to the minimum V_{LVR} value.

Figure 8. Power-on reset and low voltage reset waveform

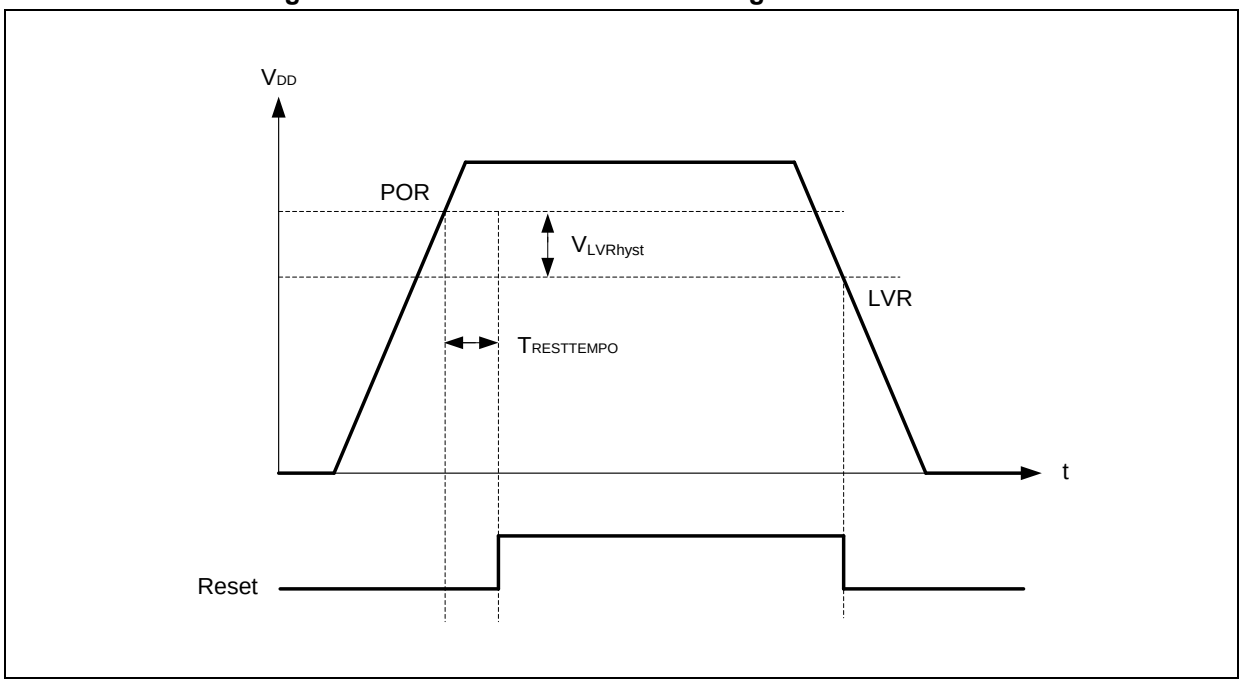


Table 14. Programmable voltage regulator characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PVM0}	PVM threshold 0 (PVMSEL[2:0] = 000)	Rising edge	2.09	2.15	2.21	V
		Falling edge	1.99	2.05	2.11	V
V_{PVM1}(1)	PVM threshold 1 (PVMSEL[2:0] = 001)	Rising edge	2.24	2.3	2.36	V
		Falling edge	2.14	2.2	2.26	V
V_{PVM2}(1)	PVM threshold 2 (PVMSEL[2:0] = 010)	Rising edge	2.39	2.45	2.51	V
		Falling edge	2.29	2.35	2.41	V
V_{PVM3}(1)	PVM threshold 3 (PVMSEL[2:0] = 011)	Rising edge	2.54	2.6	2.67	V
		Falling edge	2.44	2.5	2.57	V
V_{PVM4}(1)	PVM threshold 4 (PVMSEL[2:0] = 100)	Rising edge	2.69	2.75	2.82	V
		Falling edge	2.59	2.65	2.72	V
V_{PVM5}(1)	PVM threshold 5 (PVMSEL[2:0] = 101)	Rising edge	2.84	2.9	2.97	V
		Falling edge	2.74	2.8	2.87	V
V_{PVM6}	PVM threshold 6 (PVMSEL[2:0] = 110)	Rising edge	2.93	3	3.08	V
		Falling edge	2.83	2.9	2.98	V
V_{HYS_P}(1)	PVM hysteresis	-	-	100	-	mV
$I_{DD(PVM)}$(2)	PVM current consumption	-	-	0.6	1	μA

(1) Obtained by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

4.3.4 Memory characteristics

Table 15. Internal Flash memory characteristics(1)

Symbol	Parameter	Typ	Max	Unit
T_{PROG}	Programming time	60	65	μs
t_{ERASE}	Page erase time	6.6	8	ms
t_{ME}	Mass erase time	8.2	10	ms

(1) Guaranteed by design, not tested in production.

Table 16. Internal Flash memory endurance and data retention(1)

Symbol	Parameter	Conditions	Min(1)	Typ	Max	Unit
N_{END}	Endurance	T_A = -40 ~ 105 °C	100	-	-	kcycles
t_{RET}	Data retention	T_A = 105 °C	10	-	-	years

(1) Guaranteed by design, not tested in production.

4.3.5 Supply current characteristics

The current consumption is a function of several parameters and factors such as the operating voltage, ambient temperature, GPIO pin loading, device software configuration, operating frequencies, GPIO pin switching rate, and executed binary code. The current consumption is obtained by characterization results, not tested in production.

Typical and maximum current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- Flash memory access time depends on f_{HCLK} frequency (0 ~ 32 MHz: zero-wait state; 33 ~ 64 MHz: one-wait state; above 65 MHz: two-wait states).
- Prefetch is ON.
- $f_{PCLK1} = f_{HCLK}$, $f_{PCLK2} = f_{HCLK}$, $f_{ADCCLK} = f_{PCLK2}/4$.
- Unless otherwise specified, the typical values are measured with V_{DD} = 3.3 V and T_A = 25 °C condition and the maximum values are measured with V_{DD} = 3.6 V.

Table 17. Typical current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage（V）	Typ		Unit
					All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Run mode	High-speed external crystal (HEXT)(1)(2)	80 MHz	1.2	12.7	6.52	mA
			72 MHz	1.2	11.5	5.97	
			64 MHz	1.2	10.3	5.42	
			56 MHz	1.2	9.51	5.23	
			48 MHz	1.2	8.27	4.62	
			32 MHz	1.0	5.04	3.01	
			24 MHz	1.0	4.30	2.78	
			16 MHz	1.0	3.13	2.16	
			8 MHz	1.0	1.82	1.33	
			4 MHz	1.0	1.39	1.14	
			2 MHz	1.0	1.17	1.05	
			1 MHz	1.0	1.06	1.00	
			500 kHz	1.0	1.01	0.98	
			125 kHz	1.0	0.97	0.96	
		High-speed internal clock (HICK)(2)	80 MHz	1.2	12.7	6.57	mA
			72 MHz	1.2	11.5	6.02	
			64 MHz	1.2	10.4	5.47	
			56 MHz	1.2	9.55	5.27	
			48 MHz	1.2	8.29	4.66	
			32 MHz	1.0	5.02	3.02	
			24 MHz	1.0	4.29	2.79	
			16 MHz	1.0	3.14	2.18	
			8 MHz	1.0	1.84	1.36	
			4 MHz	1.0	1.42	1.17	
			2 MHz	1.0	1.20	1.08	
			1 MHz	1.0	1.10	1.04	
			500 kHz	1.0	1.04	1.01	
			125 kHz	1.0	1.00	1.00	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 18. Typical current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage（V）	Typ		Unit
					All peripherals enabled	All peripherals disabled	
I_{DD}	Supply current in Sleep mode	High-speed external crystal (HEXT)(1)(2)	80 MHz	1.2	10.2	3.10	mA
			72 MHz	1.2	9.26	2.89	
			64 MHz	1.2	8.34	2.68	
			56 MHz	1.2	7.78	2.84	
			48 MHz	1.2	6.81	2.57	
			32 MHz	1.0	4.22	1.87	
			24 MHz	1.0	3.68	1.92	
			16 MHz	1.0	2.73	1.60	
			8 MHz	1.0	1.62	1.05	
			4 MHz	1.0	1.29	1.00	
			2 MHz	1.0	1.12	0.98	
			1 MHz	1.0	1.04	0.97	
			500 kHz	1.0	1.00	0.96	
			125 kHz	1.0	0.97	0.96	
		High-speed internal clock (HICK)(2)	80 MHz	1.2	10.2	3.13	mA
			72 MHz	1.2	9.31	2.94	
			64 MHz	1.2	8.39	2.72	
			56 MHz	1.2	7.83	2.87	
			48 MHz	1.2	6.82	2.62	
			32 MHz	1.0	4.21	1.89	
			24 MHz	1.0	3.68	1.94	
			16 MHz	1.0	2.75	1.63	
			8 MHz	1.0	1.65	1.08	
			4 MHz	1.0	1.32	1.03	
			2 MHz	1.0	1.15	1.01	
			1 MHz	1.0	1.07	1.00	
			500 kHz	1.0	1.03	0.99	
			125 kHz	1.0	1.00	0.99	

(1) External clock is 8 MHz.
(2) PLL is ON when f_{HCLK} > 8 MHz.

Table 19. Maximum current consumption in Run mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage (V)	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Run mode	High-speed external crystal (HEXT) (1) All peripherals enabled	80 MHz	1.2	12.8	13.0	mA
			72 MHz	1.2	11.7	11.8	
			64 MHz	1.2	10.5	10.6	
			56 MHz	1.2	9.68	9.81	
			48 MHz	1.2	8.45	8.59	
			32 MHz	1.0	5.18	5.28	
			24 MHz	1.0	4.43	4.55	
			16 MHz	1.0	3.27	3.39	
			8 MHz	1.0	1.96	2.06	
		High-speed external crystal (HEXT) (1) All peripherals disabled	80 MHz	1.2	6.70	6.84	mA
			72 MHz	1.2	6.14	6.28	
			64 MHz	1.2	5.59	5.72	
			56 MHz	1.2	5.40	5.54	
			48 MHz	1.2	4.79	4.92	
			32 MHz	1.0	3.15	3.25	
			24 MHz	1.0	2.91	3.03	
			16 MHz	1.0	2.31	2.42	
			8 MHz	1.0	1.47	1.57	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.

Table 20. Maximum current consumption in Sleep mode

Symbol	Parameter	Conditions	f_{HCLK}	LDO voltage (V)	Max		Unit
					T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Sleep mode	High-speed external crystal (HEXT)(1) All peripherals enabled	80 MHz	1.2	10.4	10.5	mA
			72 MHz	1.2	9.43	9.56	
			64 MHz	1.2	8.49	8.64	
			56 MHz	1.2	7.95	8.09	
			48 MHz	1.2	6.97	7.10	
			32 MHz	1.0	4.36	4.46	
			24 MHz	1.0	3.82	3.92	
			16 MHz	1.0	2.88	2.98	
			8 MHz	1.0	1.77	1.87	
		High-speed external crystal (HEXT)(1) All peripherals disabled	80 MHz	1.2	3.26	3.39	mA
			72 MHz	1.2	3.05	3.17	
			64 MHz	1.2	2.84	2.96	
			56 MHz	1.2	3.00	3.12	
			48 MHz	1.2	2.73	3.04	
			32 MHz	1.0	2.01	2.31	
			24 MHz	1.0	2.06	2.17	
			16 MHz	1.0	1.75	1.85	
			8 MHz	1.0	1.19	1.29	

(1) External clock is 8 MHz. PLL is ON when f_{HCLK} > 8 MHz.

Table 21. Typical and maximum current consumption in Deepsleep and Standby modes

Symbol	Parameter	Conditions	Typ(1)			Max(2)			Unit
			V_{DD} = 1.71 V	V_{DD} = 2.4 V	V_{DD} = 3.3 V	T_A = 25 °C	T_A = 85 °C	T_A = 105 °C	
I_{DD}	Supply current in Deepsleep mode	LDO in low-power mode, HICK and HEXT OFF, WDT disabled	8.54	8.80	9.24	12.5	96.2	195.6	µA
	Supply current in Standby mode	LEXT and ERTC OFF	0.68	0.87	1.24	1.52	2.77	5.25	µA
		LEXT and ERTC ON (LEXTDRV = 0x3)	1.34	1.69	2.28	2.67	3.94	6.55	

(1) Typical values are measured at T_A = 25 °C.
(2) Obtained by characterization results, not tested in production.

Figure 9. Typical current consumption in Deepsleep mode with LDO in low-power mode vs. temperature at different V_{DD}

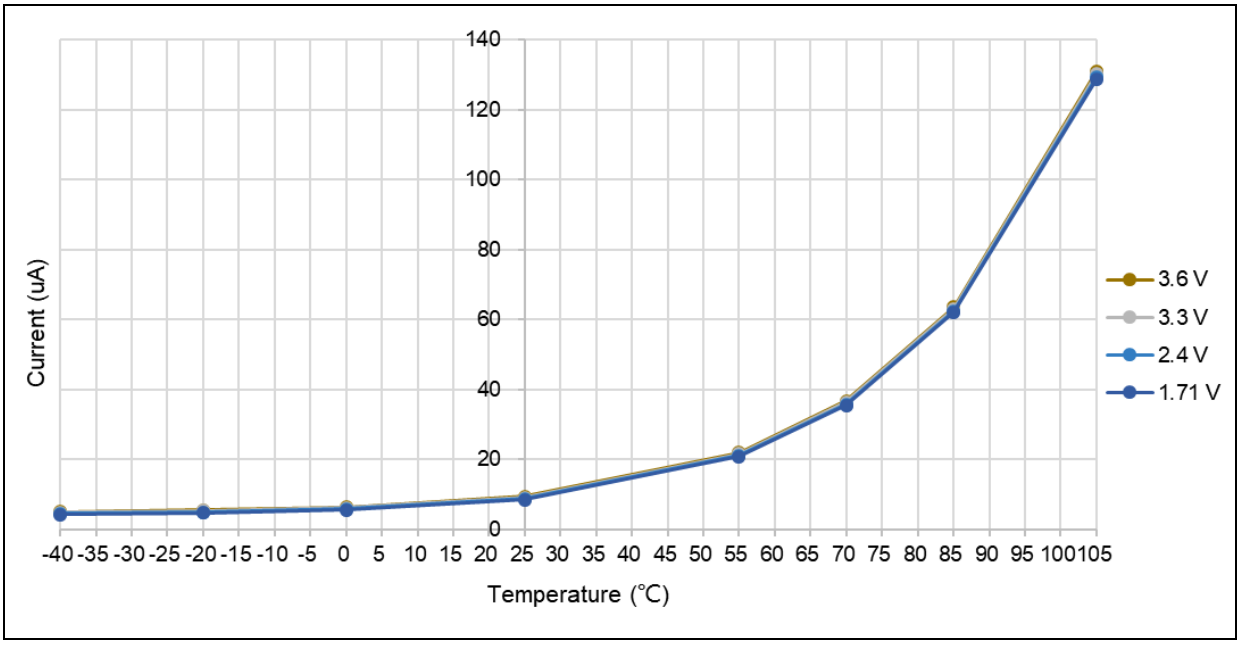
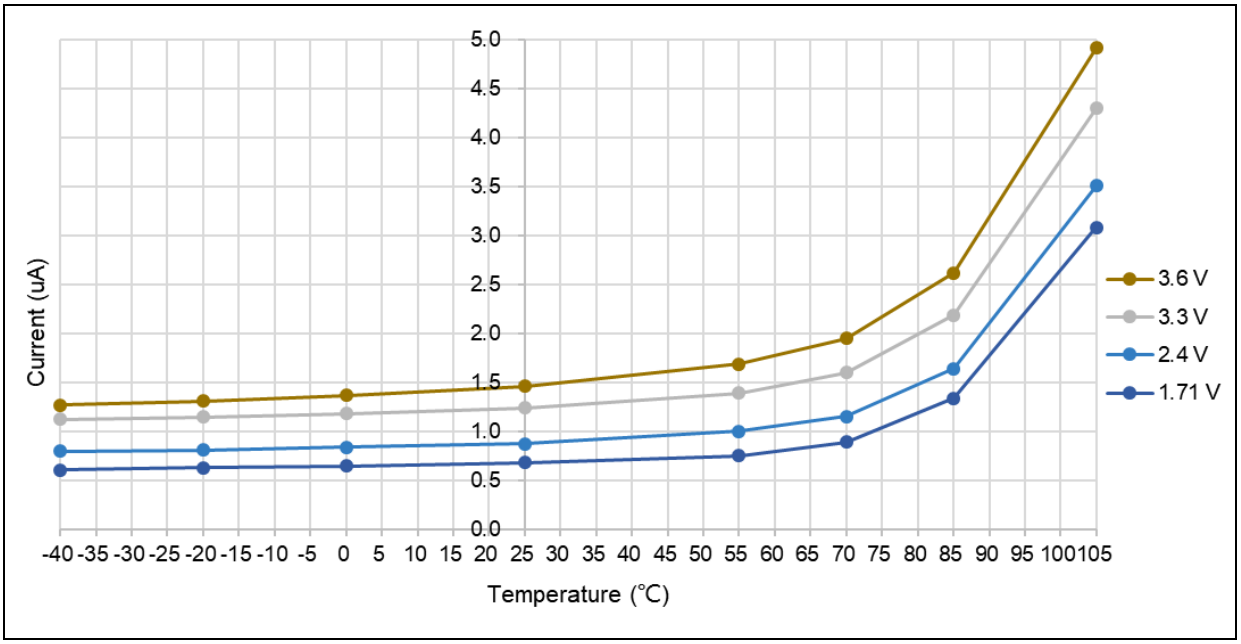


Figure 10. Typical current consumption in Standby mode vs. temperature at different V_{DD}



On-chip peripheral current consumption

The MCU is placed under the following conditions:

- All GPIO pins are in analog mode.
- The given value is calculated by measuring the current consumption difference between “all peripherals clocked OFF” and “only one peripheral clocked ON”.

Table 22. Peripheral current consumption

Peripheral		LDO voltage (V)		Unit
		1.2	1.0	
AHB	DMA1	2.66	2.22	μA/MHz
	SRAM	1.40	1.16	
	Flash	11.6	9.75	
	CRC	1.37	1.14	
	HWDIV	1.03	0.78	
GPIO	GPIOA	1.03	0.79	
	GPIOB	1.05	0.87	
	GPIOC	0.84	0.89	
	GPIOF	0.94	0.53	
APB1	TMR3	6.91	5.70	
	TMR6	1.26	0.98	
	TMR14	2.83	2.34	
	SPI2/I^{2}S2	3.22	2.67	
	USART2	5.16	4.31	
	USART3	2.95	2.49	
	USART4	2.88	2.49	
	I^{2}C1	6.63	5.65	
	I^{2}C2	6.40	5.34	
	CAN1	2.68	2.18	
	WWDT	0.64	0.50	
	PWC	0.98	0.75	
APB2	SCFG	0.63	0.57	
	SPI1/I^{2}S1	3.13	2.63	
	USART1	5.31	4.42	
	TMR1	9.70	8.08	
	TMR15	5.41	4.42	
	TMR16	4.08	3.22	
	TMR17	4.12	3.46	
	ADC1	3.54	2.95	

4.3.6 External clock source characteristics

High-speed external clock generated from a crystal / ceramic resonator

The high-speed external (HEXT) clock can be supplied with a 4 to 25 MHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

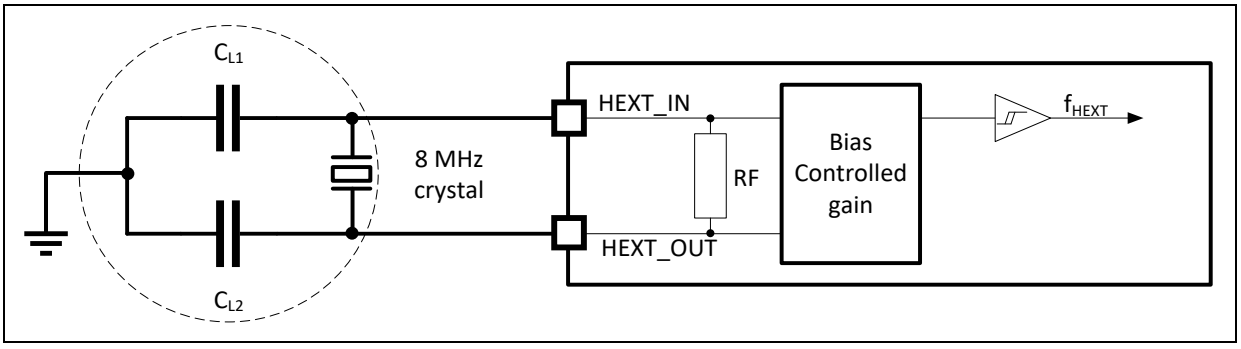
Table 23. HEXT 4 ~ 25 MHz crystal characteristics(1)(2)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT}	Oscillator frequency	-	4	8	25	MHz
$t_{SU(HEXT)}$(3)	Startup time	8 MHz, HEXTDRV = 0x1	-	2.2	-	ms
$I_{DD(HEXT)}$	Power consumption	8 MHz, HEXTDRV = 0x1	-	400	550	μA

(1) Oscillator characteristics given by the crystal/ceramic resonator manufacturer.
(2) Guaranteed by characterization results, not tested in production.
(3) $t_{SU(HEXT)}$ is the startup time measured from the moment HEXT is enabled (by software) to a stabilized 8 MHz oscillation is reached. This value is measured for a standard crystal resonator and it can vary significantly with the crystal manufacturer.

For C_{L1} and C_{L2}, it is recommended to use high-quality external ceramic capacitors in the 5 pF to 25 pF range (typ.), designed for high-frequency applications, and selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2} are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}. PCB and MCU pin capacitance must be included (10 pF can be used as a rough estimate of the combined pin and board capacitance) when sizing C_{L1} and C_{L2}.

Figure 11. HEXT typical application with an 8 MHz crystal



High-speed external clock generated from an external source

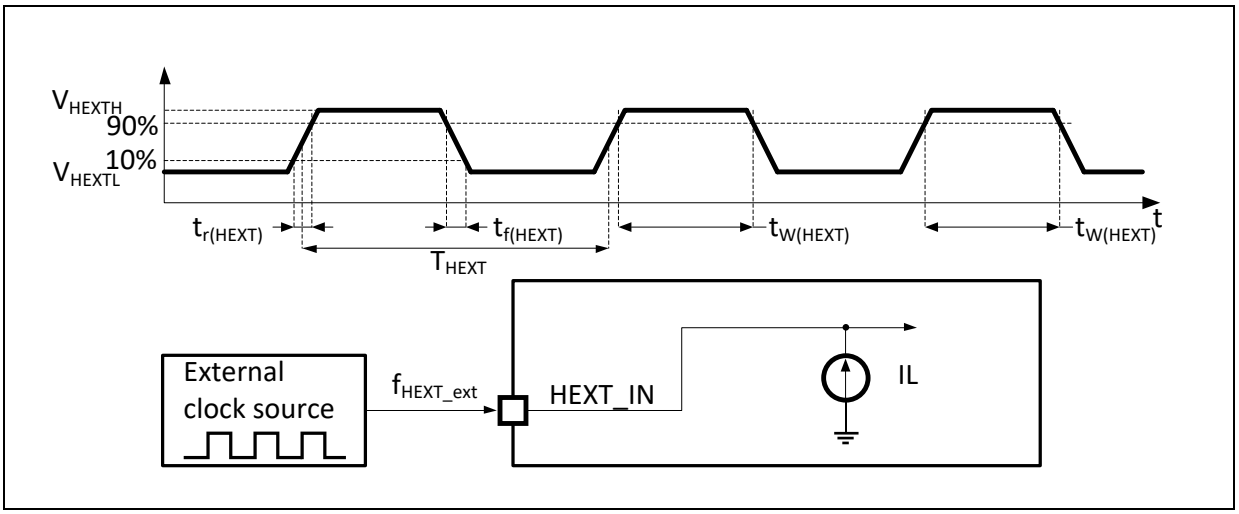
The characteristics given in the table below result from tests performed using a high-speed external clock source.

Table 24. HEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HEXT_ext}	User external clock source frequency (1)	-	1	8	25	MHz
V_{HEXTH}	HEXT_IN input pin high level voltage		0.7V_{DD}	-	V_{DD}	V
V_{HEXTL}	HEXT_IN input pin low level voltage		V_{SS}	-	0.3V_{DD}	
$t_{w(HEXT)}$ $t_{w(HEXT)}$	HEXT_IN high or low time(1)		5	-	-	ns
$t_{r(HEXT)}$ $t_{f(HEXT)}$	HEXT_IN rise or fall time(1)		-	-	20	
$C_{in(HEXT)}$	HEXT_IN input capacitance(1)	-	-	5	-	pF
$Duty_{(HEXT)}$	Duty cycle	-	45	-	55	%
I_L	HEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 12. HEXT external source AC timing diagram



Low-speed external clock generated from a crystal / ceramic resonator

The low-speed external (LEXT) clock can be supplied with a 32.768 kHz crystal/ceramic resonator oscillator. All the information given in this paragraph are based on characterization results obtained with typical external components specified in the table below. In the application, the resonator and the load capacitors have to be placed as close as possible to the oscillator pins in order to minimize output distortion and startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics (frequency, package, accuracy).

Table 25. LEXT 32.768 kHz crystal characteristics(1)(2)

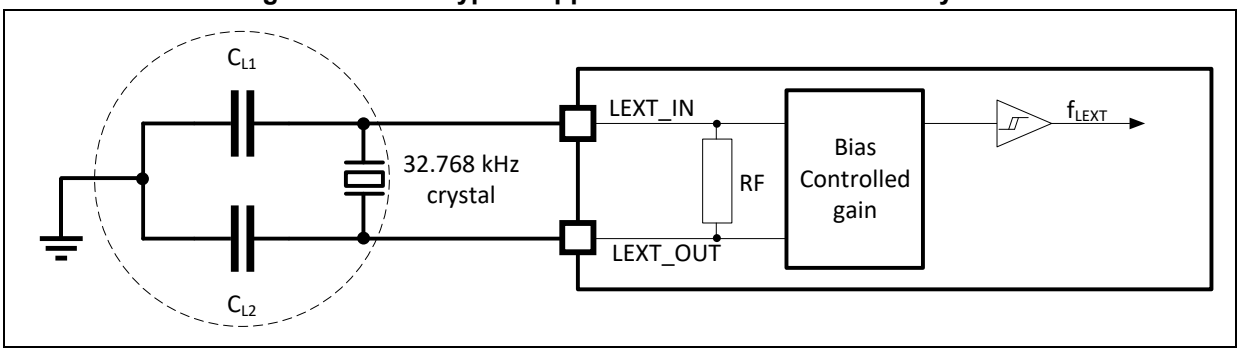
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{SU(LEXT)}$	Startup time	LEXTDRV = 0x3	-	90	-	ms
		LEXTDRV = 0x0		150	-	

(1) Oscillator characteristics are given by the crystal/ceramic resonator manufacturer.
(2) Obtained by characterization results, not tested in production.

For C_{L1} and C_{L2}, it is recommended to use high-quality ceramic capacitors in the 5 pF to 20 pF range selected to match the requirements of the crystal or resonator. C_{L1} and C_{L2}, are usually the same size. The crystal manufacturer typically specifies a load capacitance which is the series combination of C_{L1} and C_{L2}.

Load capacitance C_L has the following formula: $C_L = C_{L1} \times C_{L2} / (C_{L1} + C_{L2}) + C_{stray}$, where C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2 pF and 7 pF.

Figure 13. LEXT typical application with a 32.768 kHz crystal



Note: No external resistor is required between LEXT_IN and LEXT_OUT, and it is also prohibited to add it.

Low-speed external clock generated from an external source

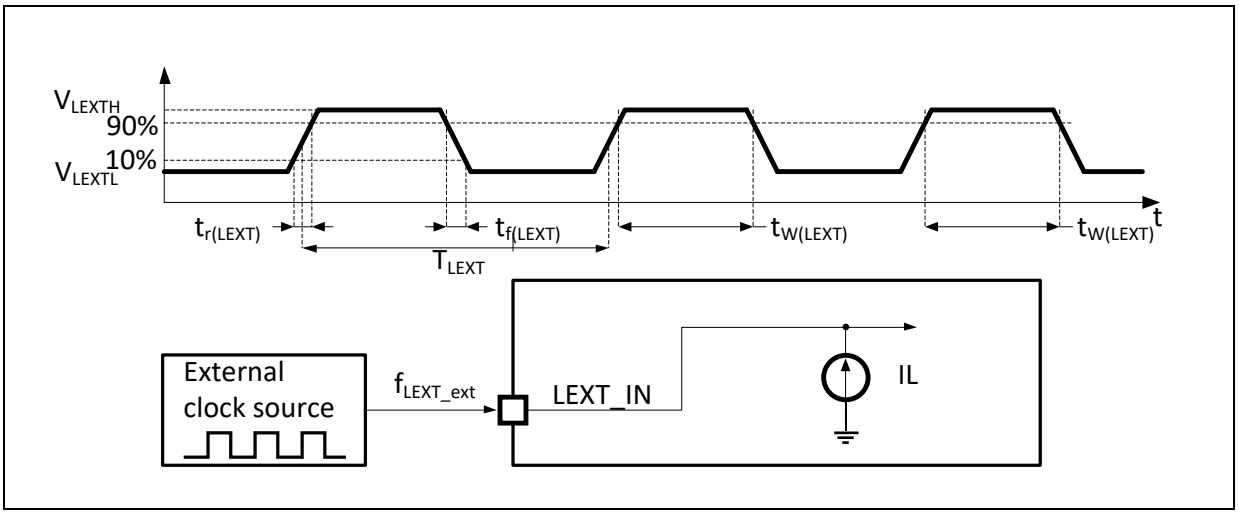
The characteristics given in the table below result from tests performed using a low-speed external clock source.

Table 26. LEXT external source characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LEXT_ext}	User external clock source frequency (1)	-	-	32.768	1000	kHz
V_{LEXTH}	LEXT_IN input pin high level voltage		$0.7V_{DD}$	-	V_{DD}	V
V_{LEXTL}	LEXT_IN input pin low level voltage		V_{SS}	-	$0.3V_{DD}$	
$t_{w(LEXT)}$ $t_{w(LEXT)}$	LEXT_IN high or low time(1)		450	-	-	ns
$t_{r(LEXT)}$ $t_{f(LEXT)}$	LEXT_IN rise or fall time(1)		-	-	50	
$C_{in(LEXT)}$	LEXT_IN input capacitance(1)	-	-	5	-	pF
$Duty_{(LEXT)}$	Duty cycle	-	30	-	70	%
I_L	LEXT_IN input leakage current	$V_{SS} \le V_{IN} \le V_{DD}$	-	-	±1	μA

(1) Guaranteed by design, not tested in production.

Figure 14. LEXT external source AC timing diagram



4.3.7 Internal clock source characteristics

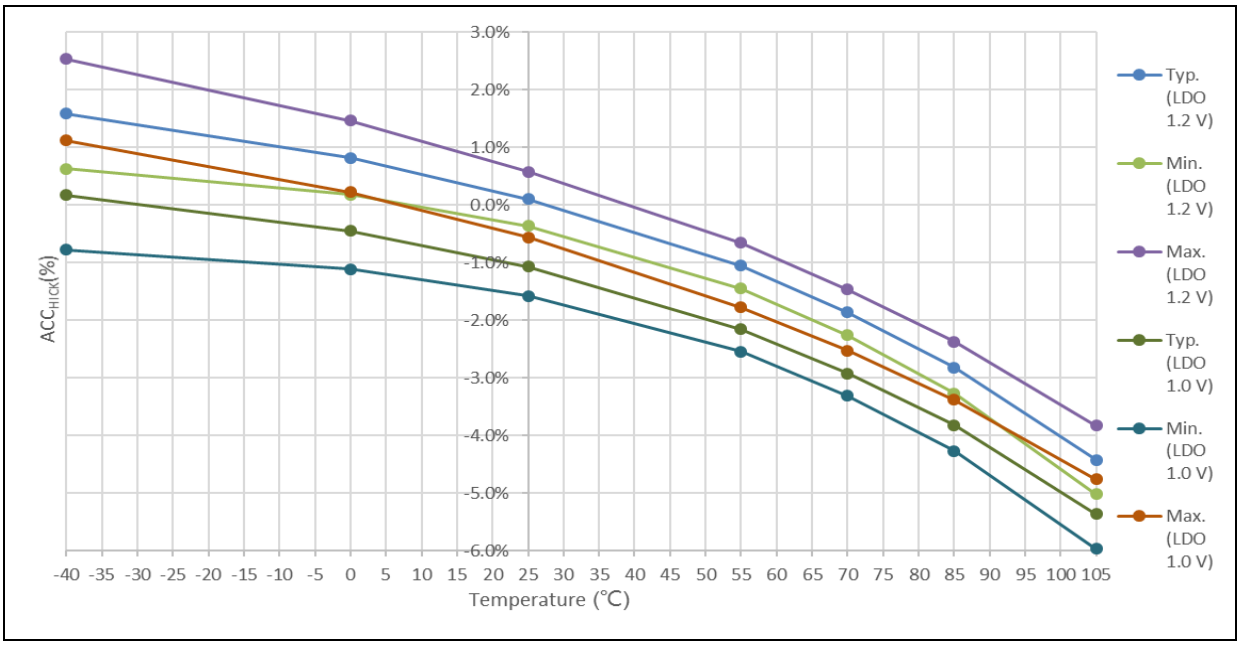
High-speed internal clock (HICK)

Table 27. HICK clock characteristics

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
f_{HICK}	Frequency	-			-	48	-	MHz
$DuCy_{(HICK)}$	Duty cycle	-			45	-	55	%
ACC_{HICK}	Accuracy of the HICK oscillator	User-trimmed with the CRM_CTRL register(1)			-1	-	1	%
		Factory-calibrated (2)	LDO = 1.2 V	T_A = -40 ~ 105 °C	-5.5	-	+3	
				T_A = -40 ~ 85 °C	-3.5	-	+3	
				T_A = 0 ~ 70 °C	-2.5	-	+1.5	
				T_A = 25 °C	-1	-	+1	
			LDO = 1.0 V	T_A = -40 ~ 105 °C	-6	-	+1.5	
				T_A = -40 ~ 85 °C	-4.5	-	+1.5	
				T_A = 0 ~ 70 °C	-3.5	-	+0.5	
				T_A = 25 °C	-2	-	0	
$t_{SU(HICK)}$(2)	HICK oscillator startup time	-			-	0.6	0.9	µs
$I_{DD(HICK)}$(2)	HICK oscillator power consumption	-			-	460	500	µA

(1) Guaranteed by design, not tested in production.
(2) Obtained by characterization results, not tested in production.

Figure 15. HICK clock accuracy vs. temperature



Low-speed internal clock (LICK)

Table 28. LICK clock characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{LICK}(1)	Frequency	-	32	43	50	kHz

(1) Obtained by characterization results, not tested in production.

4.3.8 PLL characteristics

Table 29. PLL characteristics

Symbol	Parameter	Min(1)	Typ	Max(1)	Unit
f_{PLL_IN}	PLL input clock(2)	2	8	16	MHz
	PLL input clock duty cycle	40	-	60	%
f_{PLL_OUT}	PLL multiplier output clock	16	-	80	MHz
t_{LOCK}	PLL lock time	-	-	200	µs
Jitter	Cycle-to-cycle jitter	-	-	300	ps

(1) Guaranteed by design, not tested in production.
(2) Take care of using the appropriate multiplier factors so as to have PLL input clock values compatible with the range defined by f_{PLL_OUT}.

4.3.9 Wakeup time from low-power mode

The wakeup times given in the table below is measured on a wakeup phase with the HICK. The clock source used to wake up the device depends from the current operating mode:

- Sleep mode: the clock source is the clock that was set before entering Sleep mode.
- Deepsleep or Standby mode: the clock source is the HICK.

Table 30. Low-power mode wakeup time

Symbol	Parameter	Typ	Unit
$t_{WUSLEEP}$	Wakeup from Sleep mode	4.7	µs
$t_{WUDEEPSLEEP}$	Wakeup from Deepsleep mode (LDO in low-power mode)	17	µs
$t_{WUSTDBY}$	Wakeup from Standby mode	72	µs

4.3.10 EMC characteristics

Susceptibility tests are performed on a sample basis during device characterization.

Functional EMS (electromagnetic susceptibility)

- **EFT:** A Burst of Fast Transient voltage (positive and negative) is applied to V_{DD} and V_{SS} through a coupling/decoupling network, until a functional disturbance occurs. This test is compliant with the IEC 61000-4-4 standard.

Table 31. EMS characteristics

Symbol	Parameter	Conditions	Level/Class
V_{EFT}	Fast transient voltage burst limits to be applied through coupling/decoupling network conforms to IEC 61000-4-4 on V_{DD} and V_{SS} pins to induce a functional disturbance, V_{DD} and V_{SS} input has one 47 µF capacitor and each V_{DD} and V_{SS} pin pair 0.1µF.	V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 80 MHz, ,LDO=1.2 V, conforms to IEC 61000-4-4	4/A (4 kV)
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 32 MHz, ,LDO=1.0 V, conforms to IEC 61000-4-4	
		V_{DD} = 3.3 V, LQFP48, T_A = +25 °C, f_{HCLK} = 8 MHz, LDO=1.0 V, conforms to IEC 61000-4-4	

EMC characterization and optimization are performed at component level with a typical application environment. It should be noted that good EMC performance is highly dependent on the user application and the software in particular. Therefore it is recommended that the user applies EMC software optimization and prequalification tests in relation with the EMC level requested for his application.

4.3.11 GPIO port characteristics

General input / output characteristics

All GPIOs are CMOS and TTL compliant.

Table 32. GPIO static characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	GPIO input low level voltage	-	-0.3	-	0.28 x V_{DD} + 0.1	V
V_{IH}	GPIO input high level voltage	-	0.31 x V_{DD} + 0.8	-	V_{DD} + 0.3	V
	FT, FTa and FTf GPIO input high level voltage	-		-	5.5	
V_{hys}	Schmitt trigger voltage hysteresis(1)	-	200	-	-	mV
			5% V_{DD}	-	-	-
I_{lkg}	Input floating mode leakage current (2)	V_{IN} = V_{SS} or V_{DD} TC GPIO	-	-	±1	µA
		V_{IN} = V_{SS} or V_{DD} ≤ V_{IN} ≤ 5.5 V FT, FTa and FTf GPIO	-	-	±1	
R_{PU}	Weak pull-up equivalent resistor (3)	V_{IN} = V_{SS}	60	75	200	kΩ
R_{PD}	Weak pull-down equivalent resistor (3)(4)	V_{IN} = V_{DD}	60	75	200	kΩ
C_{IO}	GPIO pin capacitance	-	-	9	-	pF

(1) Hysteresis voltage between Schmitt trigger switching levels. Guaranteed by characterization results, not tested in production.
(2) Leakage could be higher than the max if negative current is injected on adjacent pins.
(3) When the input is higher than V_{DD} + 0.3 V, the internal pull-up and pull-down resistors must be disabled for FT, FTa and FTf pins.
(4) The pull-down resistor of BOOT0 exists permanently.

All GPIOs are CMOS and TTL compliant (no software configuration required). Their characteristics cover more than the strict CMOS-technology or TTL parameters.

Output driving current

In the user application, the number of GPIO pins which can drive current must be controlled to respect the absolute maximum rating defined in Section *4.2.1.*

- The sum of the currents sourced by all GPIOs on V_{DD} plus the maximum Run consumption of the MCU sourced on V_{DD}, cannot exceed the absolute maximum rating I_{VDD} (see *Table 7*).
- The sum of the currents sunk by all GPIOs on V_{SS} plus the maximum Run consumption of the MCU sunk on V_{SS}, cannot not exceed the absolute maximum rating I_{VSS} (see *Table 7*).

Output voltage levels

All GPIOs are CMOS and TTL compliant.

Table 33. Output voltage characteristics(1)

Symbol	Parameter	Conditions	Min	Max	Unit
Normal sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 4 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 9 mA	-	1.3	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}	Output low level voltage	I_{IO} = 2 mA	-	0.4	V
V_{OH}	Output high level voltage	1.71 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Large sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 6 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 5 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 18 mA	-	1.3	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-1.3	-	
V_{OL}	Output low level voltage	I_{IO} = 5 mA	-	0.4	V
V_{OH}	Output high level voltage	1.71 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Maximum sourcing/sinking strength					
V_{OL}	Output low level voltage	CMOS standard, I_{IO} = 15 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	V_{DD}-0.4	-	
V_{OL}	Output low level voltage	TTL standard, I_{IO} = 12 mA	-	0.4	V
V_{OH}	Output high level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	2.4	-	
V_{OL}	Output low level voltage	I_{IO} = 12 mA	-	0.4	V
V_{OH}	Output high level voltage	1.71 V ≤ V_{DD} < 2.7 V	V_{DD}-0.4	-	
Ultra-high sinking strength					
V_{OL}	Output low level voltage	I_{IO} = 25 mA, 2.7 V ≤ V_{DD} ≤ 3.6 V	-	0.4	V
V_{OH}	Output high level voltage	I_{IO} = 16 mA, 1.71 V ≤ V_{DD} < 2.7 V			

(1) Obtained by characterization results, not tested in production.
(2) When ultra-high current sink capability is enabled, its V_{OH} is the same as that in maximum sourcing strength.

Input AC characteristics

The definition and values of input AC characteristics are given as follows.

Table 34. Input AC characteristics

Symbol	Parameter	Min	Max	Unit
$t_{EXINTpw}$(1)	Pulse width of external signals detected by EXINT controller	10	-	ns

(1) Obtained by characterization results, not tested in production.

4.3.12 NRST pin characteristics

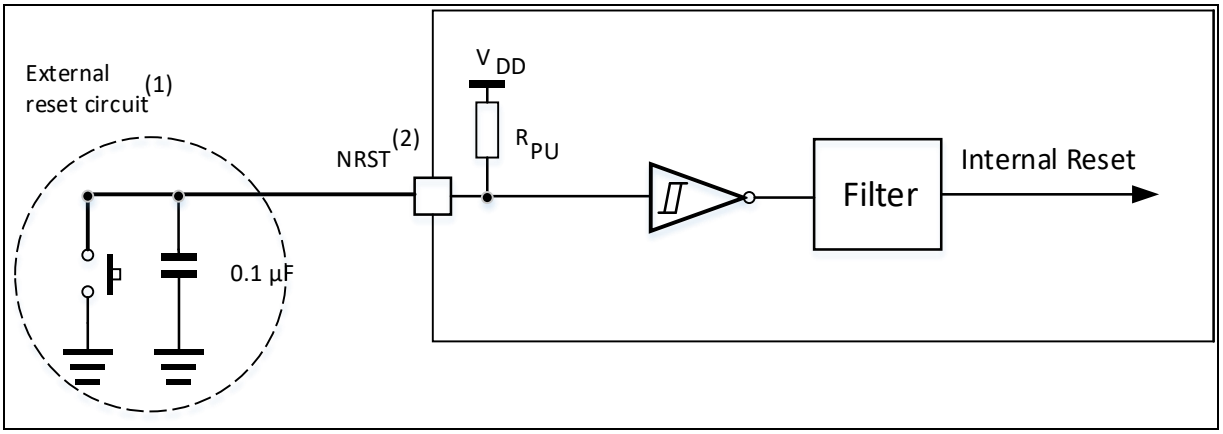
The NRST pin input driver uses CMOS technology. It is connected to a permanent pull-up resistor, R_{PU} (see the table below).

Table 35. NRST pin characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{IL(NRST)}$(1)	NRST input low level voltage	2.7 V ≤ V_{DD} ≤ 3.6 V	-0.3	-	0.8	V
		1.71 V ≤ V_{DD} < 2.7 V			0.5	
$V_{IH(NRST)}$(1)	NRST input high level voltage		2	-	V_{DD} + 0.3	V
$V_{hys(NRST)}$	NRST Schmitt trigger voltage hysteresis	2.7 V ≤ V_{DD} ≤ 3.6 V	-	400	-	mV
		1.71 V ≤ V_{DD} < 2.7 V		200		
R_{PU}	Weak pull-up equivalent resistor	V_{IN} = V_{SS}	30	40	50	kΩ
$t_{ILV(NRST)}$(1)	NRST input low level invalid time	-	-	-	40	µs
$t_{ILNV(NRST)}$(1)	NRST input low level valid time	-	62.5	-	-	µs

(1) Guaranteed by design, not tested in production.

Figure 16. Recommended NRST pin protection



(1) The reset network protects the device against parasitic resets.
(2) Users must ensure that the level on the NRST pin can go below the $V_{IL(NRST)}$ max level specified in *Table 35*. Otherwise, the reset will not be taken into account by the device.

4.3.13 TMR timer characteristics

The parameters given in the table below are guaranteed by design.

Table 36. TMR characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{res(TMR)}$	Timer resolution time	-	1	-	$t_{TMRxCLK}$
		$f_{TMRxCLK}$ = 80 MHz	12.5	-	ns
f_{EXT}	Timer external clock frequency on CH1 to CH4	-	0	$f_{TMRxCLK}$/2	MHz

4.3.14 SPI characteristics

Table 37. SPI characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
f_{SCK} $(1/t_{c(SCK)})^{(1)}$	SPI clock frequency$^{(2)(3)}$	2.4 V ≤ V_{DD} ≤ 3.6 V	-	36	MHz
		1.71 V ≤ V_{DD} < 2.4 V	-	24	
$t_{su(CS)}^{(1)}$	CS setup time	Slave mode	$4t_{PCLK}$	-	ns
$t_{h(CS)}^{(1)}$	CS hold time	Slave mode	$2t_{PCLK}$	-	ns
$t_{w(SCKH)}^{(1)}$ $t_{w(SCKL)}^{(1)}$	SCK high and low time	Master mode, prescaler factor = 4	$2t_{PCLK}$ - 3	$2t_{PCLK}$ + 3	ns
$t_{su(MI)}^{(1)}$	Data input setup time	Master mode	6	-	ns
$t_{su(SI)}^{(1)}$		Slave mode	5	-	
$t_{h(MI)}^{(1)}$	Data input hold time	Master mode	4	-	ns
$t_{h(SI)}^{(1)}$		Slave mode	5	-	
$t_{a(SO)}^{(1)(4)}$	Data output access time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{dis(SO)}^{(1)(5)}$	Data output disable time	Slave mode	t_{PCLK} - 2	$2t_{PCLK}$ + 2	ns
$t_{v(SO)}^{(1)}$	Data output valid time	Slave mode (after enable edge)	-	25	ns
$t_{v(MO)}^{(1)}$	Data output valid time	Master mode(after enable edge)	-	10	ns
$t_{h(SO)}^{(1)}$	Data output hold time	Slave mode (after enable edge)	9	-	ns
$t_{h(MO)}^{(1)}$		Master mode(after enable edge)	2	-	

(1) Guaranteed by design, not tested in production.
(2) The maximum SPI clock frequency in slave mode should not exceed $f_{PCLK}/2$.
(3) The maximum SPI clock frequency is highly related with devices and the PCB layout. For more details about the complete solution, please contact your local Artery sales representative.
(4) Min. time is for the minimum time to drive the output and the max time is for the maximum time to validate the data.
(5) Min. time is for the minimum time to invalidate the output and the max time is for the maximum time to put the data in Hi-Z.

Figure 17. SPI timing diagram – slave mode and CPHA = 0

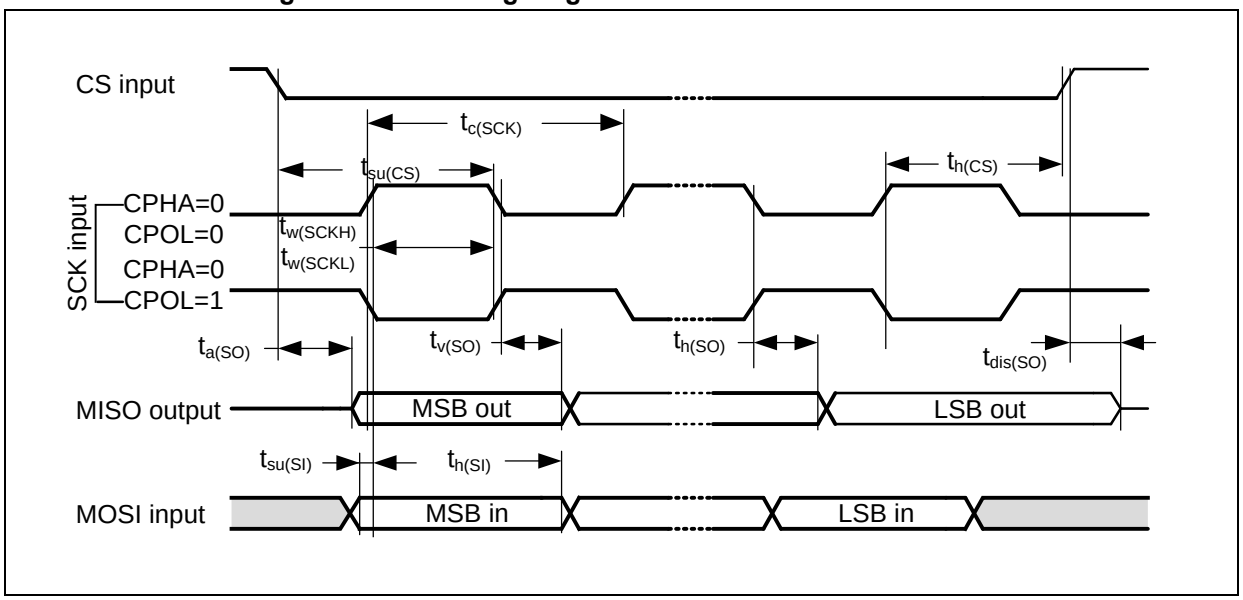


Figure 18. SPI timing diagram – slave mode and CPHA = 1

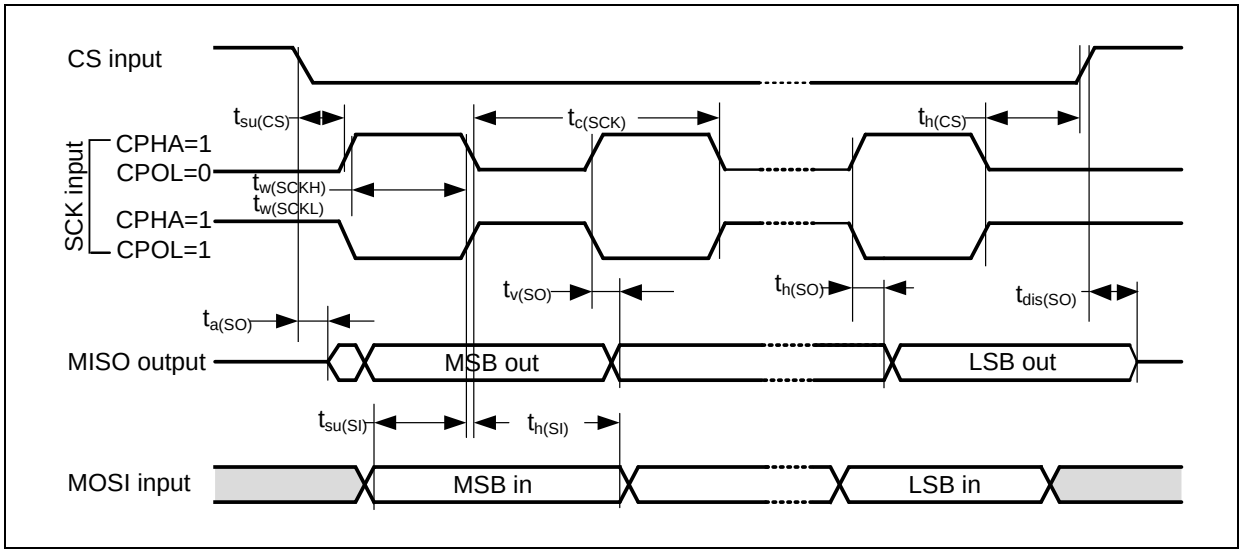
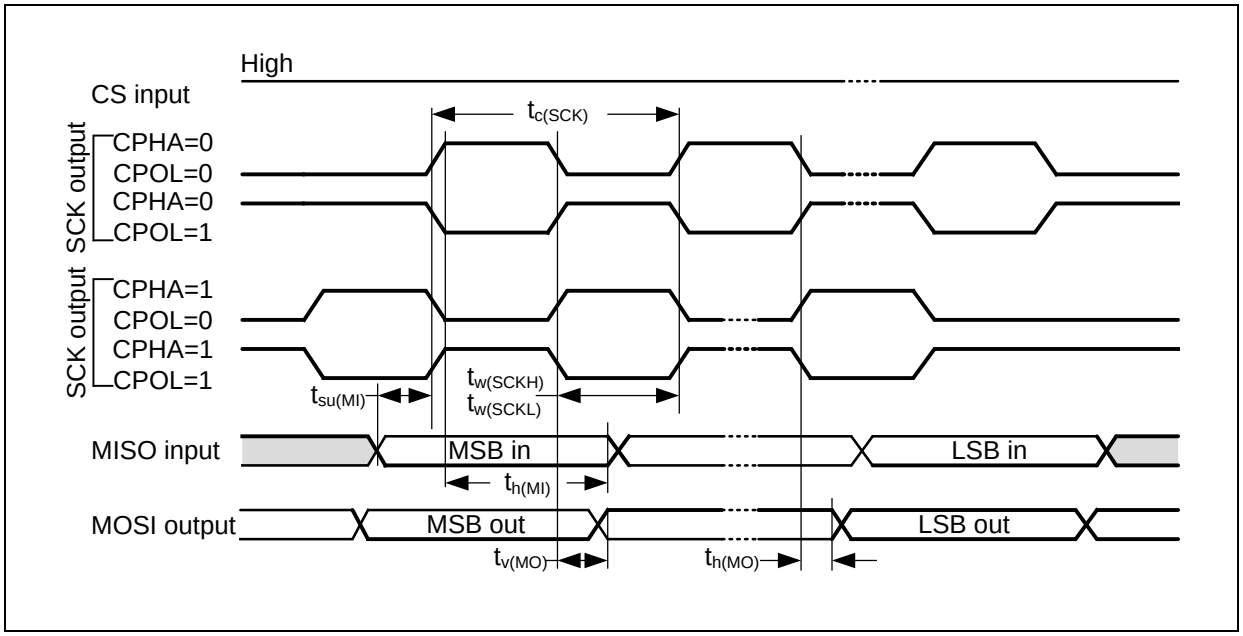


Figure 19. SPI timing diagram – master mode



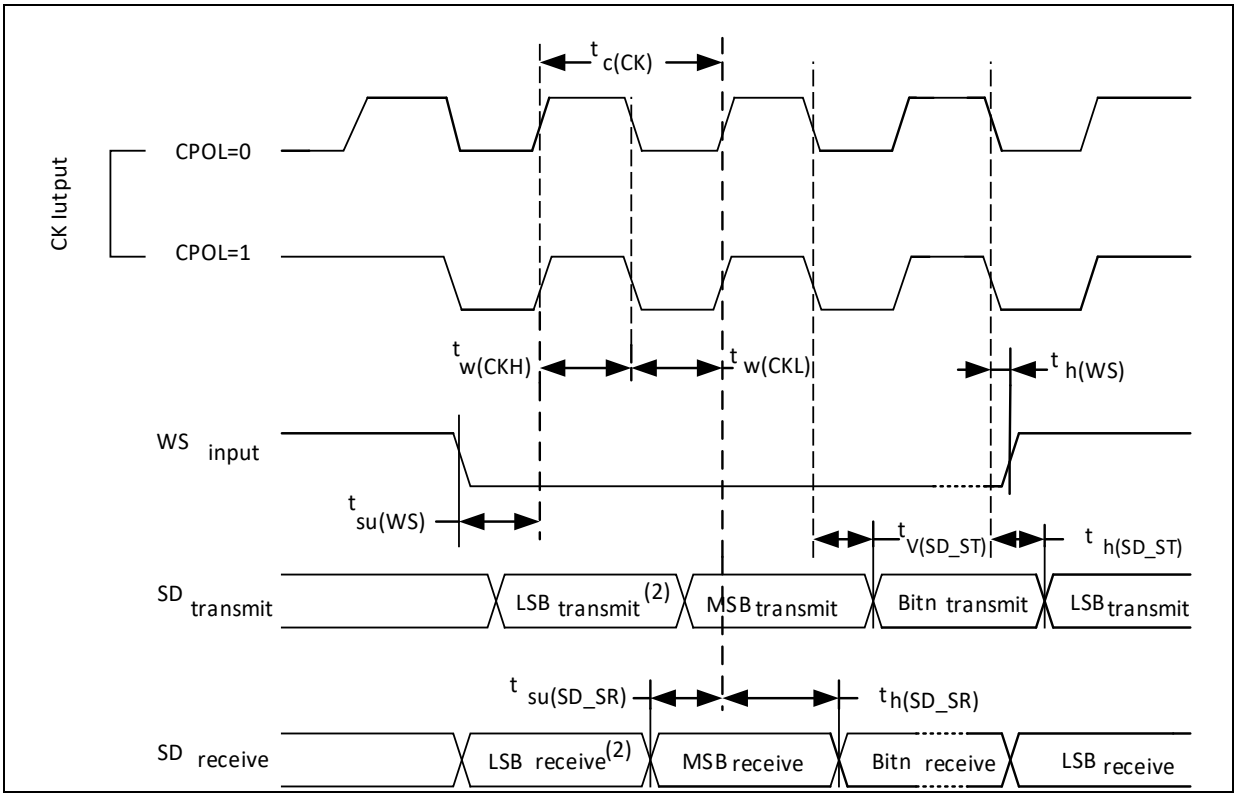
4.3.15 I²S characteristics

Table 38. I²S characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
$t_{r(CK)}$ $t_{f(CK)}$	I²S clock rise and fall time	Capacitive load: C = 15 pF	-	12	ns
$t_{v(WS)}$(1)	WS valid time	Master mode	0	4	
$t_{h(WS)}$(1)	WS hold time	Master mode	0	4	
$t_{su(WS)}$(1)	WS setup time	Slave mode	9	-	
$t_{h(WS)}$(1)	WS hold time	Slave mode	0	-	
$t_{su(SD\_MR)}$(1)	Data input setup time	Master receiver	6	-	
$t_{su(SD\_SR)}$(1)		Slave receiver	2	-	
$t_{h(SD\_MR)}$(1)(2)	Data input hold time	Master receiver	0.5	-	
$t_{h(SD\_SR)}$(1)(2)		Slave receiver	0.5	-	
$t_{v(SD\_ST)}$(1)(2)	Data output valid time	Slave transmitter (after enable edge)	-	20	
$t_{h(SD\_ST)}$(1)	Data output hold time	Slave transmitter (after enable edge)	9	-	
$t_{v(SD\_MT)}$(1)(2)	Data output valid time	Master transmitter (after enable edge)	-	15	
$t_{h(SD\_MT)}$(1)	Data output hold time	Master transmitter (after enable edge)	0	-	

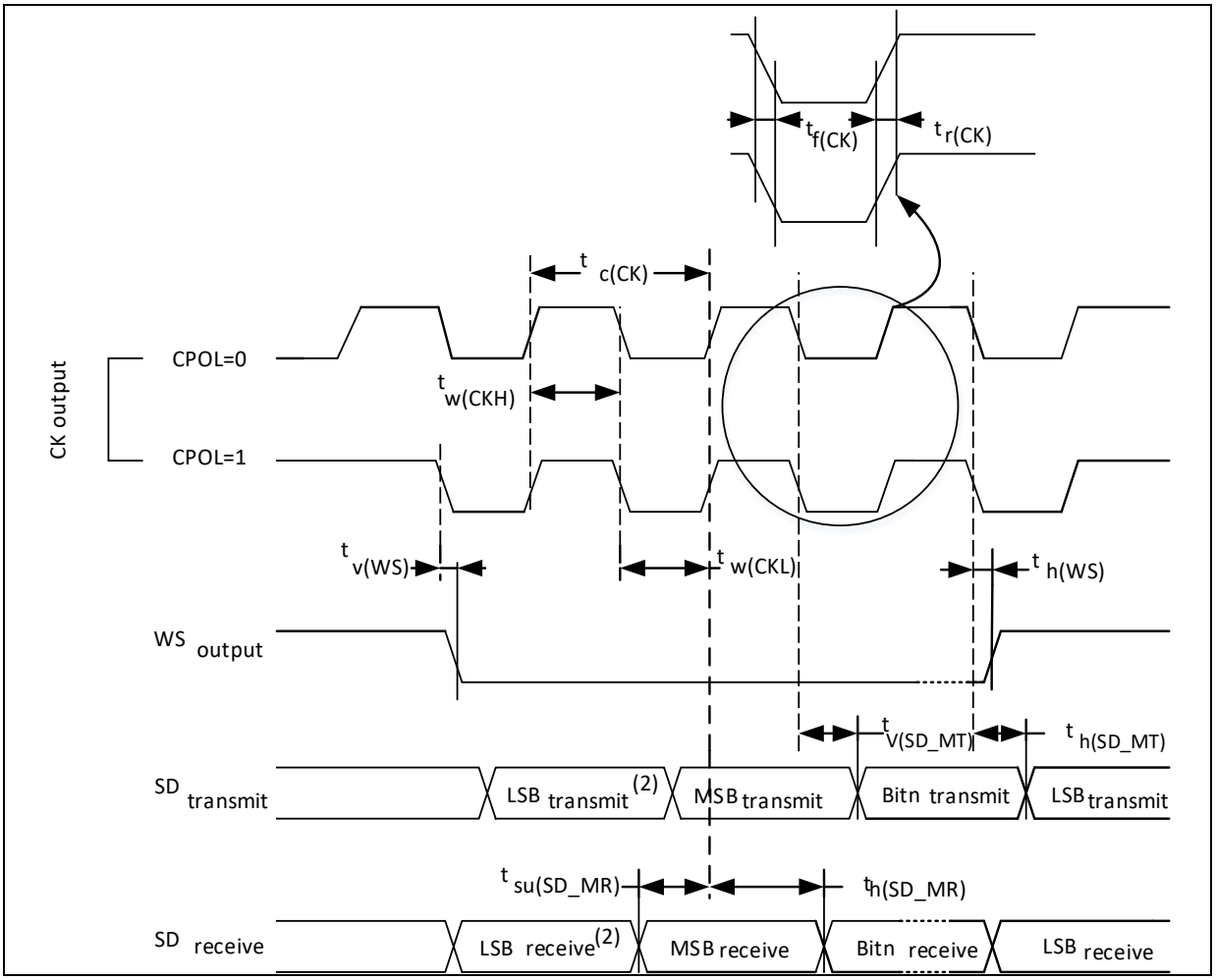
(1) Guaranteed by design, not tested in production.
(2) Depends on f_{PCLK}. For example, if f_{PCLK} = 8 MHz, then t_{PCLK} = 1/f_{PCLK} = 125 ns.

Figure 20. I²S slave timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

Figure 21. I²S master timing diagram (Philips protocol)



(1) LSB transmit/receive of the previously transmitted byte. No LSB transmit/receive is sent before the first byte.

4.3.16 I²C interface characteristics

GPIO pins SDA and SCL have limitation as follows: they are not “true” open-drain. When configured as open-drain, the PMOS connected between the GPIO pin and V_{DD} is disabled, but is still present.

I²C bus interface can support standard mode (max. 100 kHz), fast mode (max. 400 kHz) and fast mode plus (max.1 MHz).

4.3.17 12-bit ADC characteristics

Unless otherwise specified, the parameters given in the table below are preliminary values derived from tests performed under ambient temperature, f_{PCLK2} frequency and V_{DDA} supply voltage conditions summarized in *Table 11*.

Note: It is recommended to perform a calibration after each power-up.

Table 39. ADC characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DDA}	Power supply	-		1.71	-	3.6	V
I_{DDA}	Current on the V_{DDA} input pin	-		-	400(1)	475	μA
f_{ADC}	ADC clock frequency	2.4 V ≤ V_{DDA} ≤ 3.6 V		0.6	-	28	MHz
		1.71 V ≤ V_{DDA} < 2.4 V		0.6	-	14	
f_S(2)	Sampling rate	2.4 V ≤ V_{DDA} ≤ 3.6 V	12-bit resolution	0.056	-	2	MSPS
			10-bit resolution			2.33	
			8-bit resolution			2.8	
			6-bit resolution			3.11	
		1.71 V ≤ V_{DDA} < 2.4 V	12-bit resolution	0.056	-	1	
			10-bit resolution			1.17	
			8-bit resolution			1.4	
			6-bit resolution			1.56	
f_{TRIG}(2)	External trigger frequency	f_{ADC} = 28 MHz		-	-	1.65	MHz
		-		-	-	17	1/f_{ADC}
V_{AIN}	Conversion voltage range(3)	-		0 (V_{REF-} connected to ground)	-	V_{REF+}	V
R_{AIN}(2)	External input impedance	-		See *Table 40* and *Table 41*			Ω
C_{ADC}(2)	Internal sample and hold capacitor	-		-	5	-	pF
t_{CAL}(2)	Calibration time	f_{ADC} = 28 MHz		6.61			μs
		-		185			1/f_{ADC}
t_{latr}(2)	Trigger conversion latency	f_{ADC} = 28 MHz		-	-	71.4	ns
		-		-	-	2(4)	1/f_{ADC}
t_S(2)	Sampling time	f_{ADC} = 28 MHz		0.053	-	8.55	μs
		-		1.5	-	239.5	1/f_{ADC}
t_{STAB}(2)	Power-on time	-		42			1/f_{ADC}
t_{CONV}(2)	Total conversion time (including sampling time)	f_{ADC} = 28 MHz		0.5	-	9	μs
		-		14~252 (t_S for sampling + 12.5 for successive approximation)			1/f_{ADC}

(1) Obtained by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.
(3) V_{REF+} can be internally connected to V_{DDA}, and V_{REF-} can be internally connected to V_{SSA}.
(4) For external triggers, a delay of 1/f_{PCLK2} must be added to the latency specified in *Table 39*.

Table 40 and *Table 41* are used to determine the maximum external impedance allowed for an error below 1 LSB.

Table 40. R_{AIN} max for f_{ADC} = 28 MHz and 2.4 V ≤ V_{DDA} ≤ 3.6 V(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)			
		12-bit resolution	10-bit resolution	8-bit resolution	6-bit resolution
1.5	0.05	0.2	0.26	0.33	0.45
7.5	0.27	1.0	1.8	2.3	3.1
13.5	0.48	2.0	3.5	4.4	5.9
28.5	1.02	4.8	7.7	9.7	13.0
41.5	1.48	7.4	12.0	15.0	20.0
55.5	1.98	10.0	16.0	20.0	26.0
71.5	2.55	14.0	20.0	26.0	34.0
239.5	8.55	37.0	50.0	50.0	50.0

(1) Guaranteed by design.

Table 41. R_{AIN} max for f_{ADC} = 28 MHz and 1.71 V ≤ V_{DDA} < 2.4 V(1)

T_S (Cycle)	t_S (µs)	R_{AIN} max (kΩ)			
		12-bit resolution	10-bit resolution	8-bit resolution	6-bit resolution
1.5	0.05	0.1	0.16	0.24	0.34
7.5	0.27	0.9	1.7	2.2	3.0
13.5	0.48	1.3	3.4	4.3	5.8
28.5	1.02	3.1	7.6	9.6	12.0
41.5	1.48	5.1	11.0	14.0	19.0
55.5	1.98	7.2	15.0	19.0	25.0
71.5	2.55	9.9	19.0	25.0	33.0
239.5	8.55	34.0	50.0	50.0	50.0

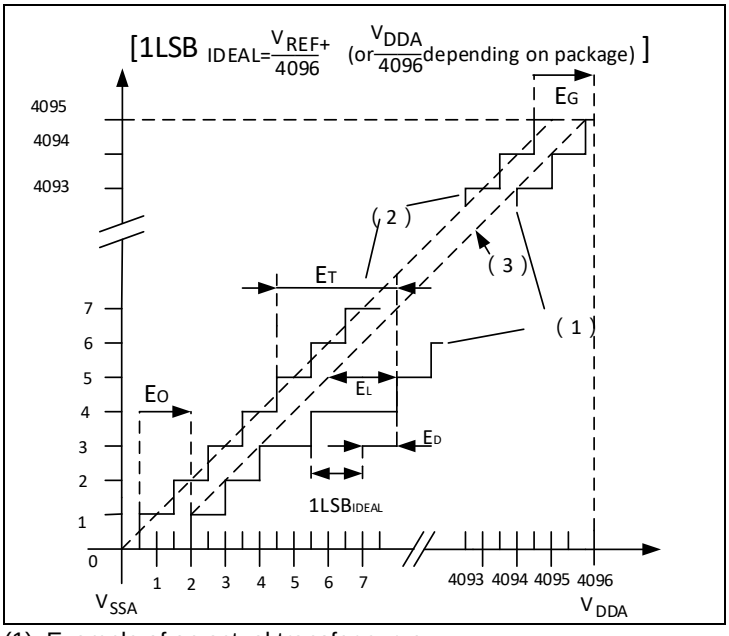
(1) Guaranteed by design.

Table 42. ADC accuracy(1)(2)

Symbol	Parameter	Conditions	Typ	Max	Unit
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 2.4~3.6 V, T_A = 25 ~ 105°C	±2.5	±3.5	LSB
EO	Offset error		±1.5	±2	
EG	Gain error		±1.5	±2.5	
ED	Differential linearity error		±0.8	+1.5/-1	
EL	Integral linearity error		±1.5	±2.5	
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.71~3.6 V, T_A = 25~ 105 °C	±3	±4.5	LSB
EO	Offset error		±1.5	+2/-3	
EG	Gain error		±1.5	+2/-3	
ED	Differential linearity error		±1	+1.5/-1	
EL	Integral linearity error		±2	±2.5	
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 28 MHz, RAIN < 10 kΩ, V_{DDA} = 2.4 ~ 3.6 V, TA = -40 ~ 105 °C	±4	±5	LSB
EO	Offset error		±1.5	+2/-3.5	
EG	Gain error		±1.5/-2.5	+2.5/-3.5	
ED	Differential linearity error		+2/-1	±2.5/-1	
EL	Integral linearity error		±2.5	±3.5	
ET	Total unadjusted error	f_{PCLK2} = 56 MHz, f_{ADC} = 14 MHz, R_{AIN} < 10 kΩ, V_{DDA} = 1.71~3.6 V, T_A = -40 ~ 105 °C	±3	±5.5	LSB
EO	Offset error		±1.5	+2/-4	
EG	Gain error		±2	+2/-3.5	
ED	Differential linearity error		+1.2/-1	+2.5/-1	
EL	Integral linearity error		±2	±4	

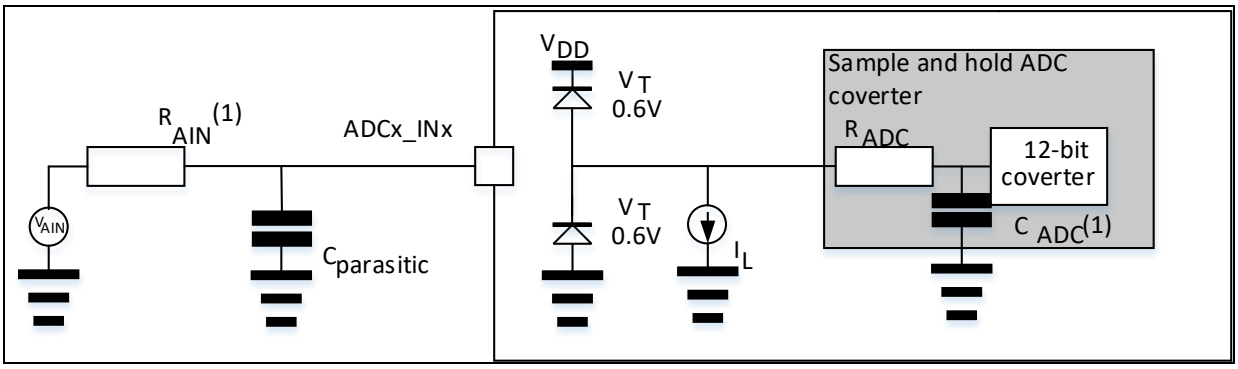
(1) ADC DC accuracy values are measured after internal calibration.
(2) Obtained by characterization results, not tested in production.

Figure 22. ADC accuracy characteristics



(1) Example of an actual transfer curve.
(2) Ideal transfer curve.
(3) End point correlation line.
(4) ET = Maximum deviation between the actual and the ideal transfer curves.
EO = Deviation between the first actual transition and the first ideal one.
EG = Deviation between the last ideal transition and the last actual one.
ED = Maximum deviation between actual steps and the ideal one.
EL = Maximum deviation between any actual transition and the end point correlation line.

Figure 23. Typical connection diagram using the ADC



(1) Refer to *Table 39* for the values of R_{AIN} and C_{ADC}.
(2) $C_{parasitic}$ represents the capacitance of the PCB (dependent on soldering and PCB layout quality) plus the pad capacitance (roughly 7 pF). A high $C_{parasitic}$ value will downgrade conversion accuracy. To remedy this, f_{ADC} should be reduced.

General PCB design guidelines

Power supply decoupling should be performed as shown in *Figure 7*. The 100 nF capacitors should be ceramic (good quality). They should be placed as close as possible to the chip.

4.3.18 Interface reference voltage (V_{INTRV}) characteristics

Table 43. Internal reference voltage characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{INTRV}(1)	Internal reference voltage	-	1.16	1.20	1.24	V
T_{Coeff}(1)	Temperature coefficient	-	-	80	150	ppm/°C
T_{S_VINTRV}(2)	ADC sampling time when reading the internal reference voltage	-	5.1	-	-	µs
$I_{DD(INTRV)}$(1)	Current consumption	-	-	50	60	µA

(1) Obtained by characterization results, not tested in production.
(2) Guaranteed by design, not tested in production.

5 Package information

5.1 LQFP48 – 7 x 7 mm

Figure 24. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package outline

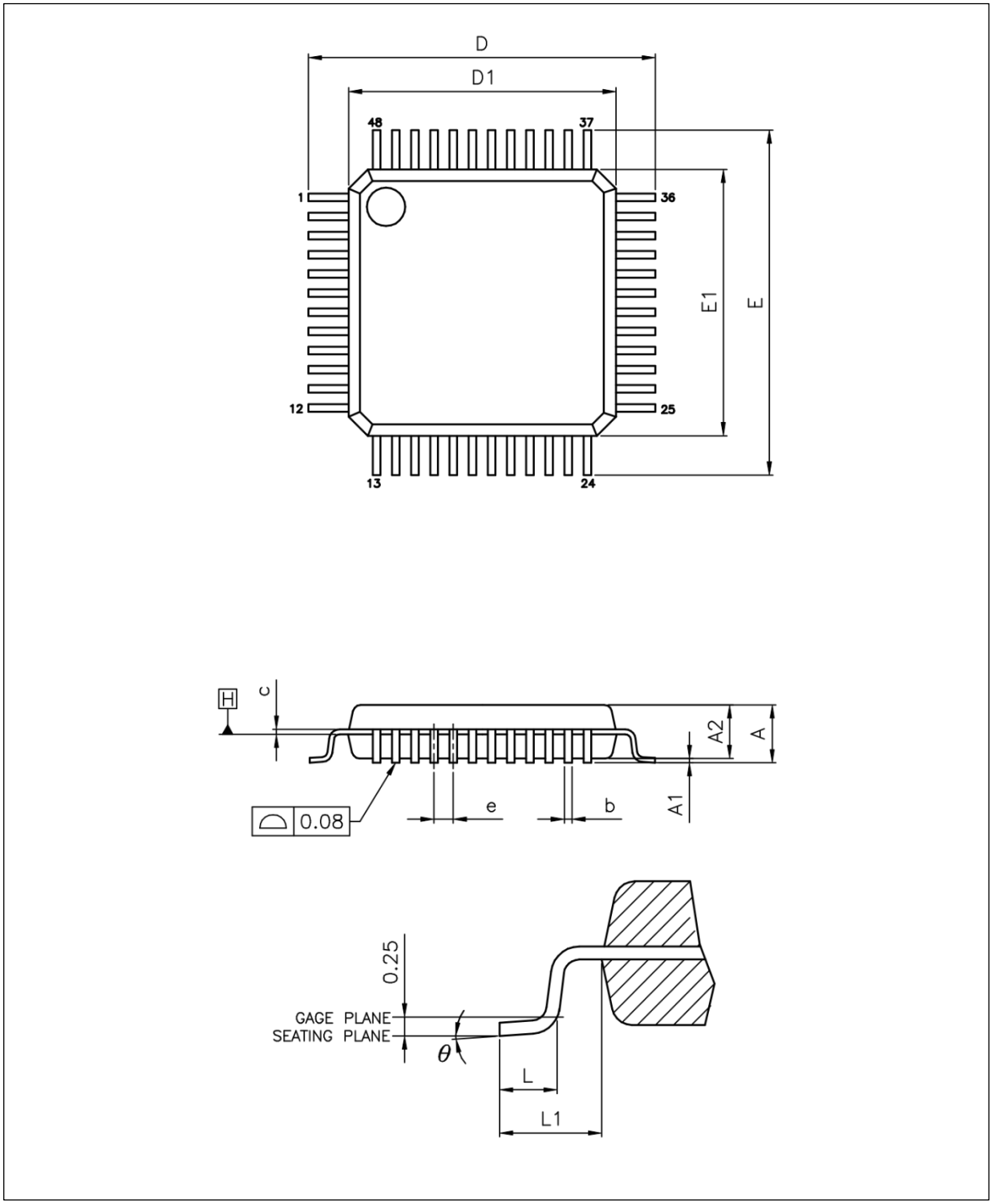


Table 44. LQFP48 – 7 x 7 mm 48 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	-	0.20
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.50 BSC.		
Θ	0°	3.5°	7°
L	0.45	0.60	0.75
L1	1.00 REF.		

5.2 LQFP32 – 7 x 7 mm

Figure 25. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package outline

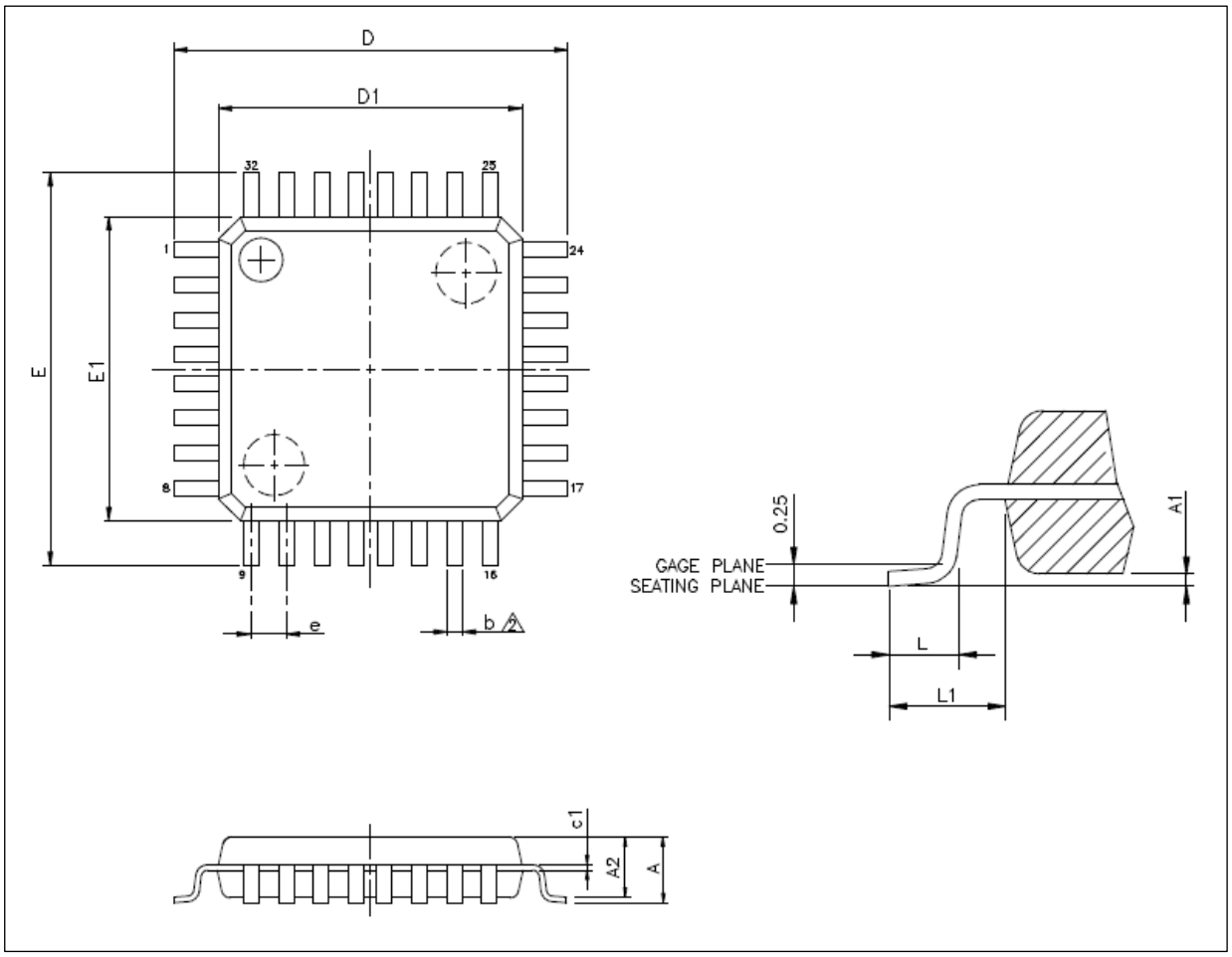


Table 45. LQFP32 – 7 x 7 mm 32 pin low-profile quad flat package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	-	1.45
b	0.30	-	0.45
c	0.09	-	0.16
D	8.80	9.00	9.20
D1	6.90	7.00	7.10
E	8.80	9.00	9.20
E1	6.90	7.00	7.10
e	0.80 BSC.		
L	0.45	-	0.75
L1	1.00 REF.		

5.3 QFN32 – 5 x 5 mm

Figure 26. QFN32 – 5 x 5 mm 32 pin quad flat no-leads package outline

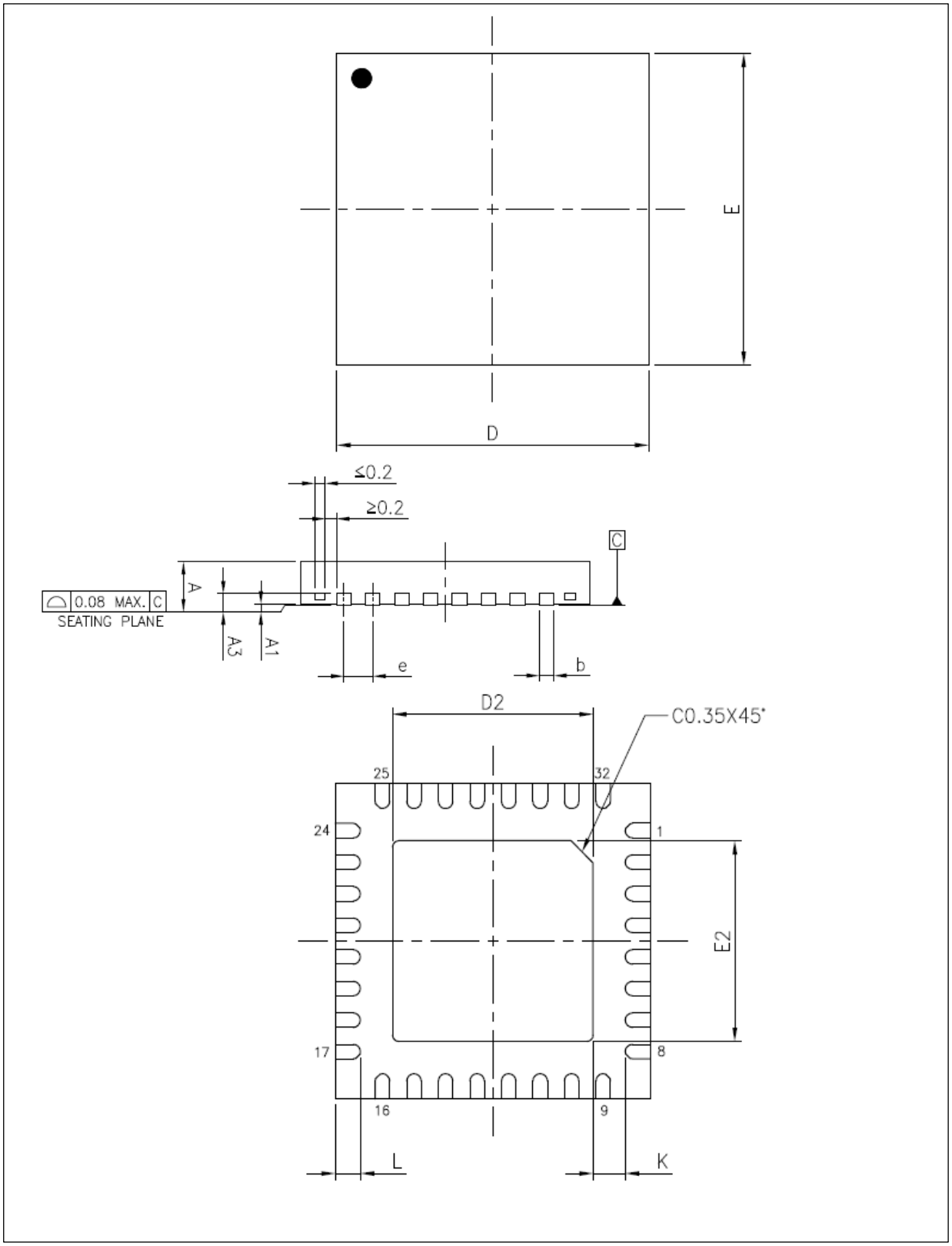


Table 46. QFN32 – 5 x 5 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.18	0.25	0.30
D	4.90	5.00	5.10
D2	3.20	3.25	3.30
E	4.90	5.00	5.10
E2	3.20	3.25	3.30
e		0.50 BSC.	
K	0.20	-	-
L	0.35	0.40	0.45

5.4 QFN32 – 4 x 4 mm

Figure 27. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package outline

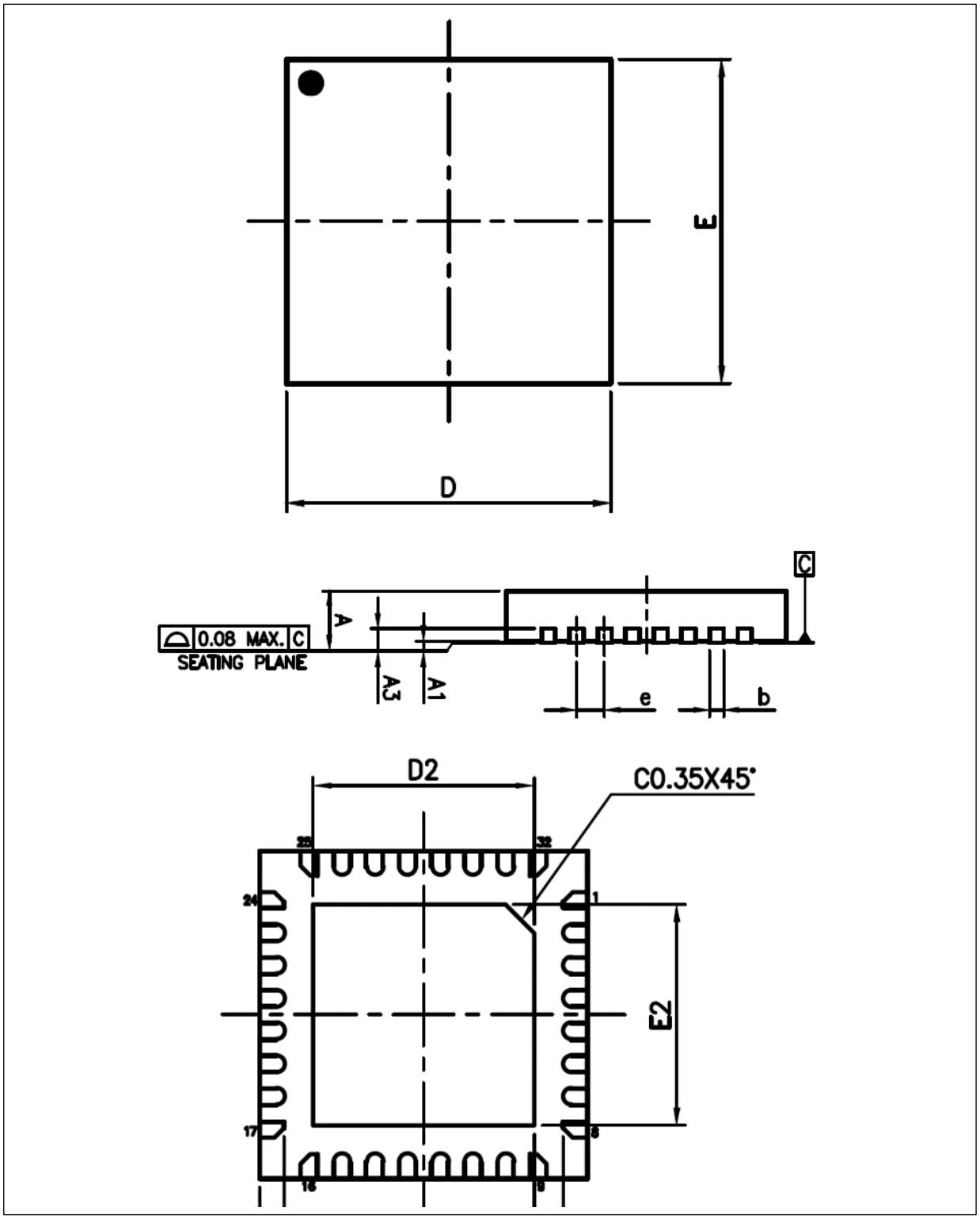


Table 47. QFN32 – 4 x 4 mm 32 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
A3		0.203 REF.	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC.	
K	0.20	-	-
L	0.25	0.30	0.35

5.5 QFN28 – 4 x 4 mm

Figure 28. QFN28 – 4 x 4 mm 28 pin quad flat no-leads package outline

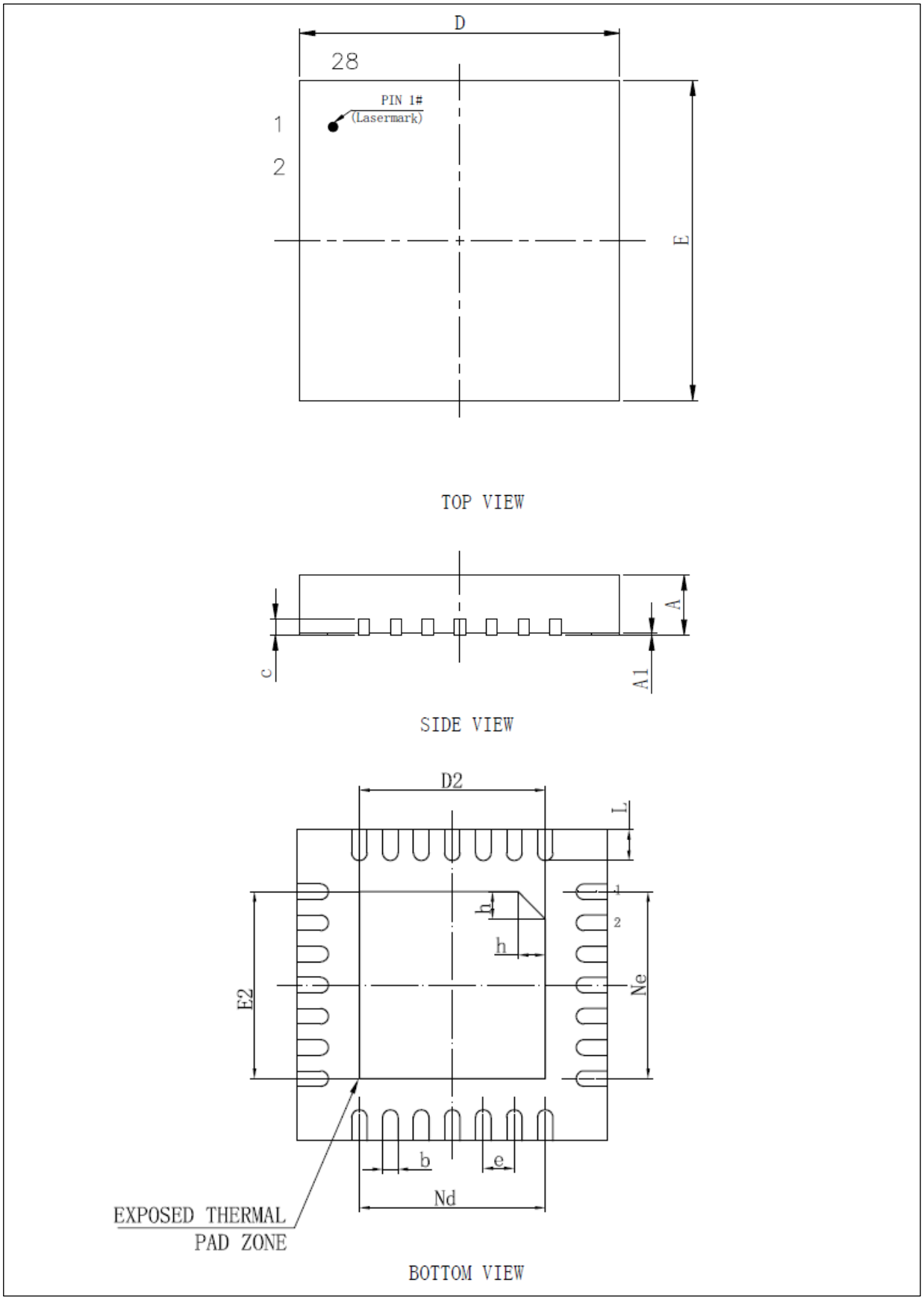


Table 48. QFN28 – 4 x 4 mm 28 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	3.90	4.00	4.10
D2	2.30	2.40	2.50
Nd	2.40 BSC.		
E	3.90	4.00	4.10
E2	2.30	2.40	2.50
Ne	2.40 BSC.		
e	0.40 BSC.		
L	0.35	0.40	0.45
h	0.30	0.35	0.40

5.6 QFN20 – 3 x 3 mm

Figure 29. QFN20 – 3 x 3 mm 20-pin quad flat no-leads package outline

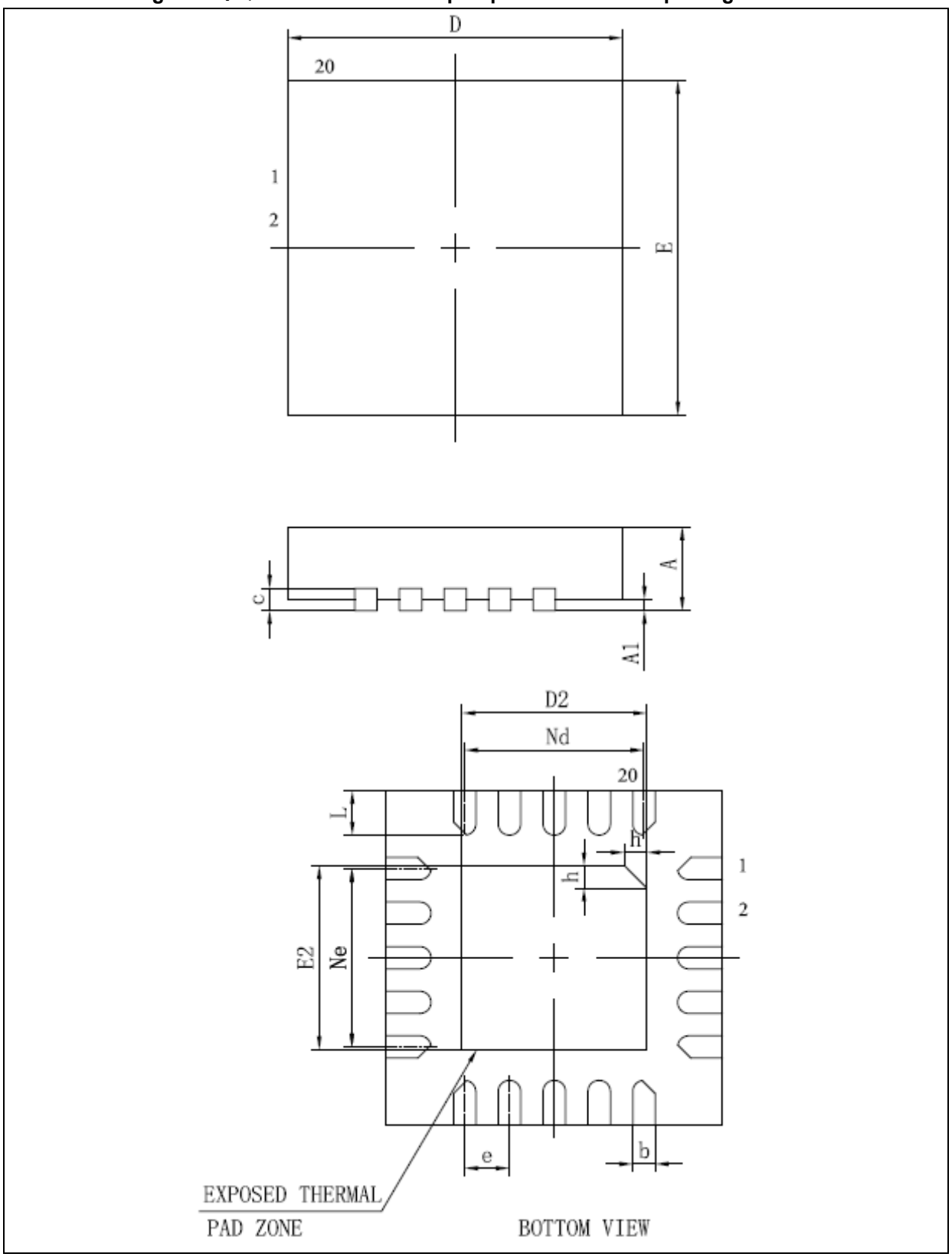


Table 49. QFN20 – 3 x 3 mm 20 pin quad flat no-leads package mechanical data

Symbol	Millimeters		
	Min	Typ	Max
A	0.70	0.75	0.80
A1	-	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	2.90	3.00	3.10
D2	1.55	1.65	1.75
Nd	1.60 BSC.		
E	2.90	3.00	3.10
E2	1.55	1.65	1.75
Ne	1.60 BSC.		
e	0.40 BSC.		
L	0.35	0.40	0.45
h	0.20	0.25	0.30

5.7 TSSOP20 – 6.5 x 4.4 mm

Figure 30. TSSOP20 – 6.5 x 4.4 mm 20-pin thin shrink small outline package

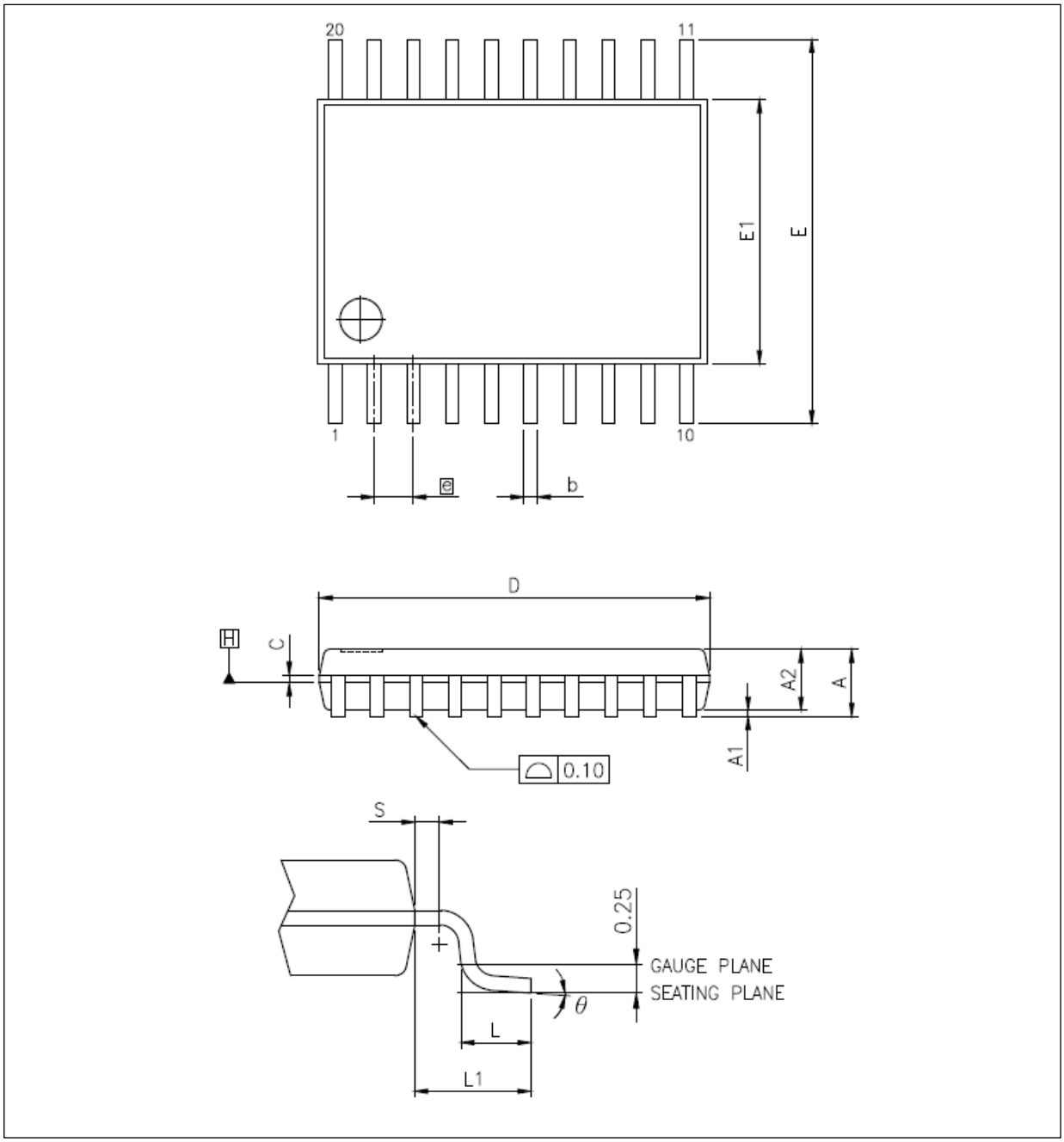


Table 50. TSSOP20 – 6.5 x 4.4 mm 20-pin thin shrink small outline package mechanical data

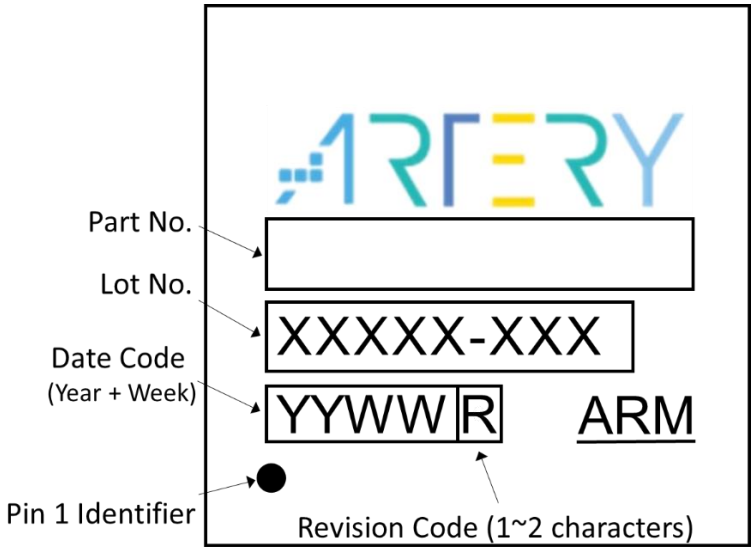
Symbol	Millimeters		
	Min	Typ	Max
A	-	-	1.20
A1	0.05	-	0.15
A2	0.80	1.00	1.05
b	0.19	-	0.30
c	0.09	-	0.20
D	6.40	6.50	6.60
E1	4.30	4.40	4.50
E	6.20	6.40	6.60
e	0.65 BSC.		
L1	1.00 REF.		
L	0.45	0.60	0.75
S	0.20	-	-
Θ	0°	-	8°

5.8 Device marking

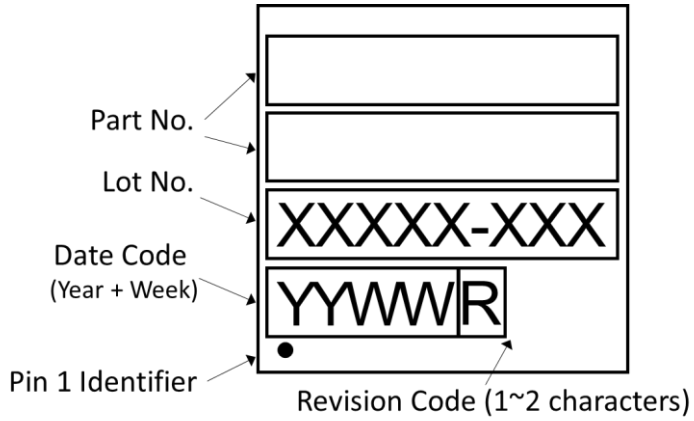
The AT32L021 devices may have the following markings, depending on the types of packages.

Figure 31. Marking example

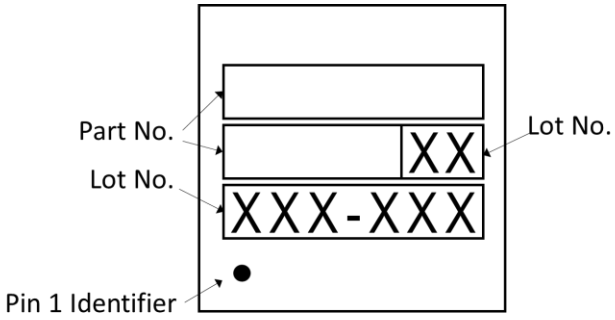
LQFP48, LQFP32, QFN32 (5 x 5 mm)



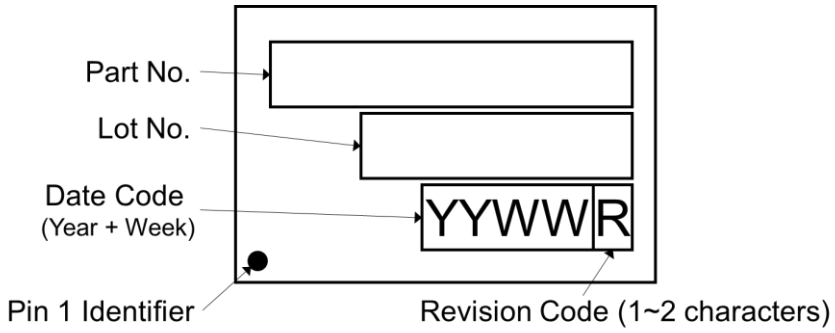
QFN32 (4 x 4 mm), QFN28



QFN20



TSSOP20



(1) Not in scale.

5.9 Thermal characteristics

Thermal characteristics are calculated based on two-layer board that uses FR-4 material in 1.6 mm thickness. They are guaranteed by design, not tested in production.

Table 51. Package thermal characteristics

Symbol	Parameter	Value	Unit
Θ_{JA}	Thermal resistance junction-ambient – LQFP48 – 7 x 7 mm	94.1	°C/W
	Thermal resistance junction-ambient – LQFP32 – 7 x 7 mm	92.4	
	Thermal resistance junction-ambient – QFN32 – 5 x 5 mm	64.1	
	Thermal resistance junction-ambient – QFN32 – 4 x 4 mm	71.3	
	Thermal resistance junction-ambient – QFN28 – 4 x 4 mm	72.7	
	Thermal resistance junction-ambient – QFN20 – 3 x 3 mm	85.5	
	Thermal resistance junction-ambient – TSSOP20 – 6.5 x 4.4 mm	109.1	

6 Part numbering

Table 52. AT32L021 series part numbering

Example: AT32 L 0 2 1 K 8 U 7 -4

Product family

AT32 = ARM®-based 32-bit microcontroller

Product type

L = Low power

Core

0 = Cortex®-M0+

Product series

2 = Value line

Product application

1 = Basic version

Pin count

C = 48 pins

K = 32 pins

G = 28 pins

F = 20 pins

Internal Flash memory size

8 = 64 Kbytes of Flash memory

6 = 32 Kbytes of Flash memory

4 = 16 Kbytes of Flash memory

Package

T = LQFP

U = QFN

P = TSSOP

Temperature range

7 = -40 °C to +105 °C

Package information

-4 = QFN32 - 4 x 4 mm

None = Other packages

For a list of available options (speed, package, etc.) or for more information concerning this device, please contact your local Artery sales office.

7 Document revision history

Table 53. Document revision history

Date	Version	Revision note
2024.1.10	2.00	Initial release.

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