Enterprise PCIe U.2 / U.3 SSD
Specification
X100P X100E

V1.5

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REVISION HISTORY

Revision	Draft Date	History	Publisher
1.0	2023-10-30	1st release	Katherine Chen
1.1	2024-02-23	Modify Table 1-2 Drive Security Type Modify 9.4 Power consumption methodologies	Katherine Chen
1.2	2024-03-22	Add LBAF	Katherine Chen
1.3	2024-06-27	Adjust the format in section 2.4.1	CC Yeh
1.4	2024-09-19	Modify 6 SUPPORTED COMMANDS	Katherine Chen
1.5	2024-03-25	Update performance data	Katherine Chen

PRODUCT OVERVIEW

X100P X100E

- Capacities
  - OP=7%: 960, 1920, 3840, 7680, 15360, 30720GB
  - OP=28%: 800, 1600, 3200, 6400, 12800, 25600GB
- Form Factor
  - U.2 / U.3
- PCIe Interface
  - PCIe Gen4x4
  - Single Port x4 lanes / Dual Port x2 lanes
  - PCIe AER (Advanced Error Reporting)
- Performance
  - Sequential Read: up to 7400MB/s
  - Sequential Write: up to 7000MB/s
  - Random Read: up to 1750K IOPS
  - Random Write: up to 490K IOPS
- Power Consumption[2]
  - Active Read (Avg. RMS): 19W
  - Active Write (Avg. RMS): 21W
  - Max. Idle Power: 8.6W
- DWPD
  - 1DWPD – 960, 1920, 3840, 7680, 15360, 30720 GB
  - 3DWPD – 800, 1600, 3200, 6400, 12800, 25600 GB
- TBW[3]
  - 800GB SSD – 4380TB
  - 960GB SSD – 1752TB
  - 1600GB SSD – 8760TB
  - 1920GB SSD – 3504TB
  - 3200GB SSD – 17520TB
  - 3840GB SSD – 7008TB
  - 6400GB SSD – 35040TB
  - 7680GB SSD – 14016TB
  - 12800GB SSD – 70080TB
  - 15360GB SSD – 28032TB
  - 25600GB SSD – 140160TB
  - 30720GB SSD – 56064TB
- LBAF: 512 / 512+8 / 4K / 4K+8 / 4K+64 Bytes
- MTBF[4]: 2,500,000 hours
- UBER: < 1 sector per 10^{18} bits read
- Advanced Flash Management
  - ECC
  - Static and Dynamic Wear Leveling
  - Bad Block Management
  - Deallocate (TRIM) Command
  - SMART
  - Over-Provision
  - Firmware Upgrade
- Temperature Range
  - Operation: 0°C ~ 70°C with specified airflow
  - Storage: -40°C ~ 85°C
- RoHS compliant
- Enterprise Features Support List:
  - Namespace
  - Dual Port / Single Port
  - Reservation
  - Metadata Protection Thermal throttling
  - Power Loss Protection
- Hardware AES-XTS 256-bit Encryption
- Support SMBus
- Support NVMe-MI (Management Interface)
- Data Retention – 3 months
- Physical Dimension:
  U.2 / U.3 15mm 100(L)x70(W)x15(H) mm^3
- Compliance
  - PCIe Express Base 4.0
  - NVMe 1.4
  - NVMe Management Interface Rev 1.1

NOTES:

1. Please see “Performance to Quality of Service (QoS)” Chapter 2.5. for details.
2. Please see “Power Consumption” Chapter 4.2 for details.
3. Please see “TBW (Terabytes Written) ” Chapter 3.2 for details.
4. MTBF is a prediction simulation based on Telcordia SR-332 model.

ORDERING INFORMATION

Capacity	Interface	Security	Part Number	Customized Part Number
800GB	Dual Port	Opal	XX106H01800GE221T0200	SC-EPW5970-800G
		Non-Opal	XX106H01800GE021T0200	
	Single Port	Opal	XP106H01800GE221T0200	SC-EPW0970-800G
		Non-Opal	XP106H01800GE021T0200	
960GB	Dual Port	Opal	XX106H01960GP221T0200	SC-EPM5970-960G
		Non-Opal	XX106H01960GP021T0200	
	Single Port	Opal	XP106H01960GP221T0200	SC-EPM0970-960G
		Non-Opal	XP106H01960GP021T0200	
1600GB	Dual Port	Opal	XX106H011T60E222T0400	SC-EPW5970-1600G
		Non-Opal	XX106H011T60E022T0400	
	Single Port	Opal	XP106H011T60E222T0400	SC-EPW0970-1600G
		Non-Opal	XP106H011T60E022T0400	
1920GB	Dual Port	Opal	XX106H011T92P222T0400	SC-EPM5970-1920G
		Non-Opal	XX106H011T92P022T0400	
	Single Port	Opal	XP106H011T92P222T0400	SC-EPM0970-1920G
		Non-Opal	XP106H011T92P022T0400	
3200GB	Dual Port	Opal	XX106H013T20E224T0900	SC-EPW5970-3200G
		Non-Opal	XX106H013T20E024T0900	
	Single Port	Opal	XP106H013T20E224T0900	SC-EPW0970-3200G
		Non-Opal	XP106H013T20E024T0900	
3840GB	Dual Port	Opal	XX106H013T84P224T0900	SC-EPM5970-3840G
		Non-Opal	XX106H013T84P024T0900	
	Single Port	Opal	XP106H013T84P224T0900	SC-EPM0970-3840G
		Non-Opal	XP106H013T84P024T0900	
6400GB	Dual Port	Opal	XX106H016T40E228T1900	SC-EPW5970-6400G
		Non-Opal	XX106H016T40E028T1900	
	Single Port	Opal	XP106H016T40E228T1900	SC-EPW0970-6400G
		Non-Opal	XP106H016T40E028T1900	
7680GB	Dual Port	Opal	XX106H017T68P228T1900	SC-EPM5970-7680G
		Non-Opal	XX106H017T68P028T1900	
	Single Port	Opal	XP106H017T68P228T1900	SC-EPM0970-7680G
		Non-Opal	XP106H017T68P028T1900	
12800GB	Dual Port	Opal	XX106H0112T8E2116T300	SC-EPW5970-12800G
		Non-Opal	XX106H0112T8E0116T300	
	Single Port	Opal	XP106H0112T8E2116T300	SC-EPW0970-12800G
		Non-Opal	XP106H0112T8E0116T300	
15360GB	Dual Port	Opal	XX106H0115T3P2116T300	SC-EPM5970-15360G
		Non-Opal	XX106H0115T3P0116T300	
	Single Port	Opal	XP106H0115T3P2116T300	SC-EPM0970-15360G
		Non-Opal	XP106H0115T3P0116T300	

Capacity	Interface	Security	Part Number	Customized Part Number
25600GB	Dual Port	Opal	XX106H0125T6E2132T700	SC-EPW5970-25600G
		Non-Opal	XX106H0125T6E0132T700	
	Single Port	Opal	XP106H0125T6E2132T700	SC-EPW0970-25600G
		Non-Opal	XP106H0125T6E0132T700	
30720GB	Dual Port	Opal	XX106H0130T7P2132T700	SC-EPM5970-30720G
		Non-Opal	XX106H0130T7P0132T700	
	Single Port	Opal	XP106H0130T7P2132T700	SC-EPM0970-30720G
		Non-Opal	XP106H0130T7P0132T700	

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1. INTRODUCTION

1.1. General Description

Phison's U.2 / U.3 Solid State Disk (SSD) delivers all the advantages of flash disk technology with PCIe Gen4x4 interface, including being fully compliant with standard U.2/U.3 form factor, providing low power consumption compared to traditional hard drive and hot-swapping when removing/replacing/upgrading flash disks. X100 series offers a wide range of capacities up to 30,720GB and its performance can reach up to 7400MB/s (for sequential read) and 7000MB/s (for sequential write) based on 3D TLC NAND flash with the DDR4. Moreover, the power consumption of X100 U.2/U.3 SSD is much lower than traditional hard drives, making it the best embedded solution for new platforms.

1.2. Controller Block Diagram

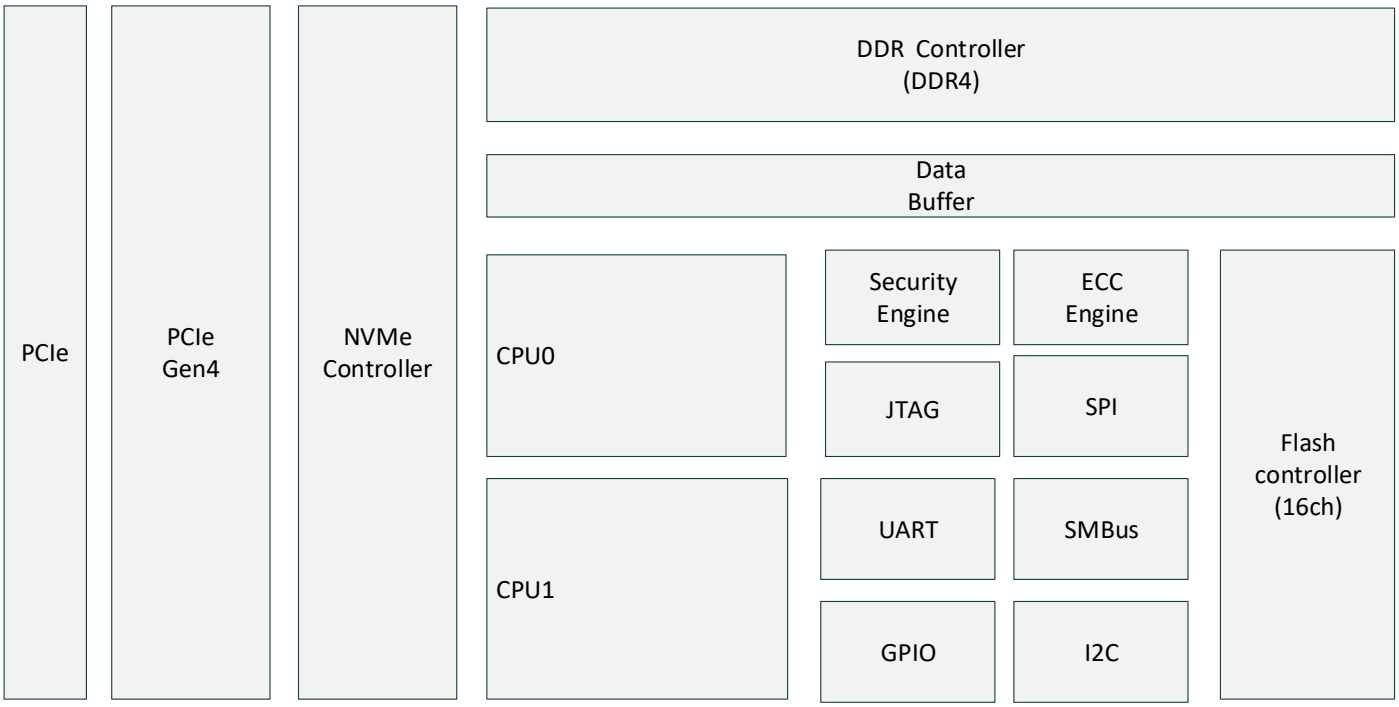


Figure 1-1 X100 U.3 PCIe SSD Controller Block Diagram

1.3. Product Block Diagram

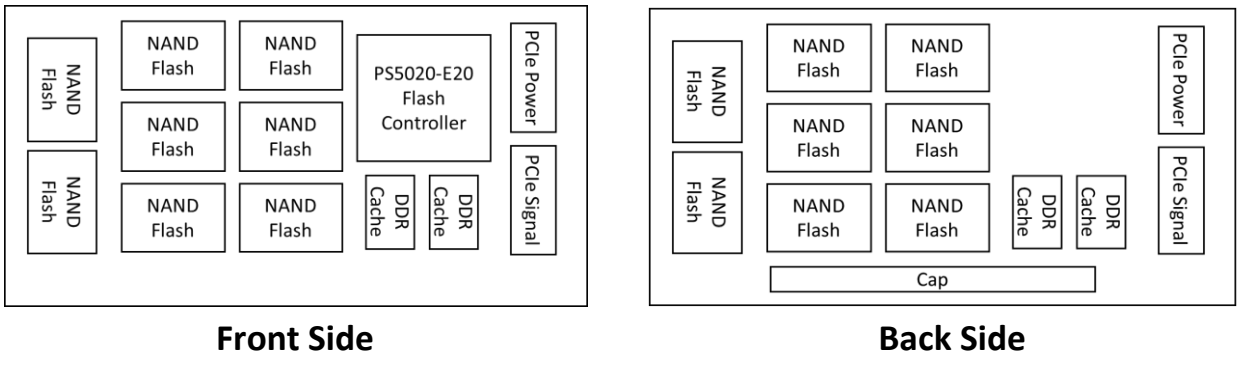


Figure 1-2 X100 U.3 PCIe SSD Product Block Diagram

1.4. Flash Management

1.4.1. Error Correction Code (ECC)

Flash memory cells will deteriorate with use, which might generate random bit errors in the stored data. Thus, X100 PCIE SSD applies the 445bit/4KB LDPC (Low Density Parity Check) of ECC algorithm, which can detect and correct errors occur during read process, ensure data been read correctly, as well as protect data from corruption.

1.4.2. Wear Leveling

NAND flash devices can only undergo a limited number of program/erase cycles, and in most cases, the flash media are not used evenly. If some areas get updated more frequently than others, the lifetime of the device would be reduced significantly. Thus, Wear Leveling is applied to extend the lifespan of NAND Flash by evenly distributing write and erase cycles across the media.

Phison provides advanced Wear Leveling algorithm, which can efficiently spread out the flash usage through the whole flash media area. Moreover, by implementing both dynamic and static Wear Leveling algorithms, the life expectancy of the NAND flash is greatly improved.

1.4.3. Bad Block Management

Bad blocks are blocks that do not function properly or contain more invalid bits causing stored data unstable, and their reliability is not guaranteed. Blocks that are identified and marked as bad by the manufacturer are referred to as “Early Bad Blocks”. Bad blocks that are developed during the lifespan of the flash are named “Later Bad Blocks”. Phison implements an efficient bad block management algorithm to detect the factory-produced bad blocks and manages bad blocks that appear with use. This practice prevents data being stored into bad blocks and further improves the data reliability.

1.4.4. TRIM

TRIM is a feature which helps improve the read/write performance and speed of solid-state drives (SSD). Unlike hard disk drives (HDD), SSDs are not able to overwrite existing data, so the available space gradually becomes smaller with each use. With the TRIM command, the operating system can inform the SSD which blocks of data are no longer in use and can be removed permanently. Thus, the SSD will perform the erase action, which prevents unused data from occupying blocks all the time.

1.4.5. SMART

SMART, an acronym for Self-Monitoring, Analysis and Reporting Technology, is an open standard that allows a disk drive to automatically detect its health and report potential failures. When a failure is recorded by SMART, users can

choose to replace the drive to prevent unexpected outage or data loss. Moreover, SMART can inform users of impending failures while there is still time to perform proactive actions, such as copy data to another device.

1.4.6. Over-Provision

Over Provisioning refers to the preserving additional area beyond user capacity in a SSD, which is not visible to users and cannot be used by them. With Over Provisioning, the performance and IOPS (Input/Output Operations per Second) are improved by providing the controller additional space to manage P/E cycles, which enhances the reliability and endurance as well. Moreover, the write amplification of the SSD becomes lower when the controller writes data to the flash.

1.4.7. Firmware Upgrade

Firmware can be considered as a set of instructions on how the device communicates with the host. Firmware will be upgradable when new features are added, compatibility issues are fixed, or read/write performance gets improved.

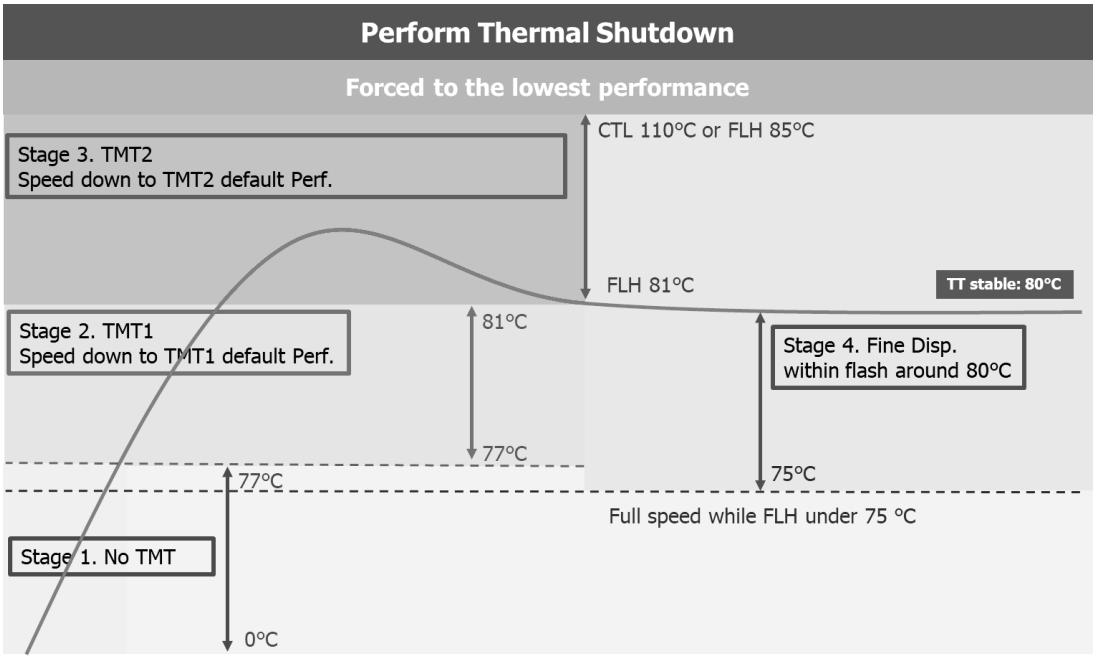
1.4.8. Thermal Throttling

The purpose of thermal throttling is to prevent any components in a SSD from over-heating during read and write operations. X100 is designed with multiple on-board thermal sensors and with their accuracy, firmware can apply different levels of throttling to achieve the purpose of protection efficiently and proactively via SMART reading.

Table 1-1 Thermal Throttling Mechanism

Item	Contents
Stage 1 No TMT	To monitor temperature every 1 secs, until flash temperature is over 77°C. Clock frequency mode 0
Stage 2 TMT1	When flash temp reaches TMT1 (flash 77°C), the drive will speed down to TMT1 performance (< 2000MB/s).
Stage 3 TMT2	When flash temp reaches TMT2 (flash 81°C), the drive will speed down to TMT2 performance (< 450MB/s).
Stage 4 TT Stable	Enter TT Dynamic Mechanism (keep TMT1 state 60 sec or TMT2 state 15 sec) Once CTRL (+/- 2) or FLH (+/- 1) temp change: 3% increase or decline of full performance in TMT1 to TMT2 temp range (75~81°C) 3% increase or 9% decline of full performance in TMT2 to Protect temp range (81~85°C)
TMT Protect	When the controller is over 110°C or flash is over 85°C , the drive will be forced to perform at the lowest performance (< 50 MB/s)
TMT Fatal	Perform thermal shutdown process when controller T_J is 120°C.
Resume No TMT	While flash is cooled down to 75°C or below, the performance will be back to full speed.

Figure 1-3 Thermal Throttling Mechanism



NOTES:

1. The temperature for TMT is based on T_{case}.(T_{case}: temperate value of on SSD thermal sensor)
2. TMT levels maybe varying by different workloads.

1.5. Advanced Device Security Features

1.5.1. Secure Erase

Secure Erase is a standard ATA command and will write all “0xFF” to fully wipe all the data on hard drives and SSDs. When this command is issued, SSD controller will erase its storage blocks and return to its factory default settings.

1.5.2. Physical Presence SID (PSID)

Physical Presence SID (PSID) is defined by TCG as a 32-character string and the purpose is to revert SSD back to its manufacturing setting. PSID code is printed on an SSD label.

1.5.3. Crypto Erase

Crypto Erase (TCG) is a feature that erases all data of an OPAL-activated SSD drive by resetting the cryptographic key of the disk. Since the key is modified, the previously encrypted data will become useless, achieving the purpose of data security.

1.5.4. TCG OPAL

Trusted Computing Group (TCG) provides a scalable infrastructure for managing encryption of user data in a Storage Device, as well as extensibility to enable feature. One set of capabilities defined in the Core Spec includes mechanisms for managing access control to user data stored on the Storage Device, including controlling media encryption, Key Management, and Read/Write Lock State.

1.5.5. IEEE1667

IEEE 1667 is supported but needs to be activated by vendor tool when needed, this is to prevent unintended eDrive implementation and the following necessity of Reverting by PSID before being able to re-install Operation System. Table 1-2 illustrates the types of Sanitize Operation supported

Table 1-2 Drive Security Type

Drive Security Type	AES-256 Encryption	Sanitize Operation			TCG Commands		IEEE 1667
		Overwrite	Block Erase	Crypto Erase	PSID Revert Process	Instant Security Erase	Windows eDrive
SED (TCG Opal)	Yes	No	Yes	Yes	Yes[1]	Yes[2]	Yes[3]
Non-SED	No	No	Yes	Yes	No	No	No

NOTES:

1. Crypto Erase is a feature that erases all data of AES encrypted data structure by resetting the cryptographic key of the disk. The previously encrypted data will become irretrievable.
2. Instant Security Erase is a feature that erases all data of SED drive with Opal-activated encrypted data structure by reverting SSD with PSID. Since the key is reset, the previously encrypted data cannot be accessed anymore.
3. IEEE 1667 is supported but needs to be activated by vendor tool when needed, this is to prevent unintended eDrive implementation and the following necessity of Reverting by PSID before being able to re-install Operation System.

1.6. SSD Lifetime Management

1.6.1. Terabytes Written (TBW)

TBW (Terabytes Written) is a measurement of SSDs' expected lifespan, which represents the amount of data written to the device. To calculate the TBW of an SSD, the following equation is applied:

TBW (TB) = [DWPD* SSD Capacity(GB)* Warranty Days]/ 1000

DWPD: Drive Writes Per Day

SSD Capacity: The SSD capacity is the specific capacity in total of an SSD.

Warranty Days: Years*365days

TBW in this document is based on **4K random write**.

1.6.2. Media Wear Indicator

Actual life indicator reported by SMART/Health Information Log Page (02h) Life Remaining by percentage.

1.6.3. Read Only Mode (End of Life)

When drive is aged by cumulated program/erase cycles, media worn-out may cause increasing numbers of later bad block. When the number of usable good blocks falls outside a defined usable range, the drive will notify Host through AER event and Critical Warning to enter Read Only Mode to prevent further data corruption. User should start to replace the drive with another one immediately.

1.7. Enterprise Feature

1.7.1. Namespace

Namespace is a collection of (LBA) accessible to host software. Host Divides an NVMe SSD into logically separate and individually addressable storage spaces. A namespace ID (NSID) is a unique ID and an identifier which can help the host to distinguish different namespace. So when we are going to read or write, the NSID is needed to be specified in the command to indicate which logic block we are going to operate. Each created NS, for a Host OS, is a separate disk, user can do partition and other operations in each NS.

1.7.2. Dual Port

Dual port is a function that SSD can be connected to two hosts at a time in the case of a single point of failure. If one data path fails, the available data path continues operation with minimal impact to Quality of Service (QoS).

1.7.3. Reservation

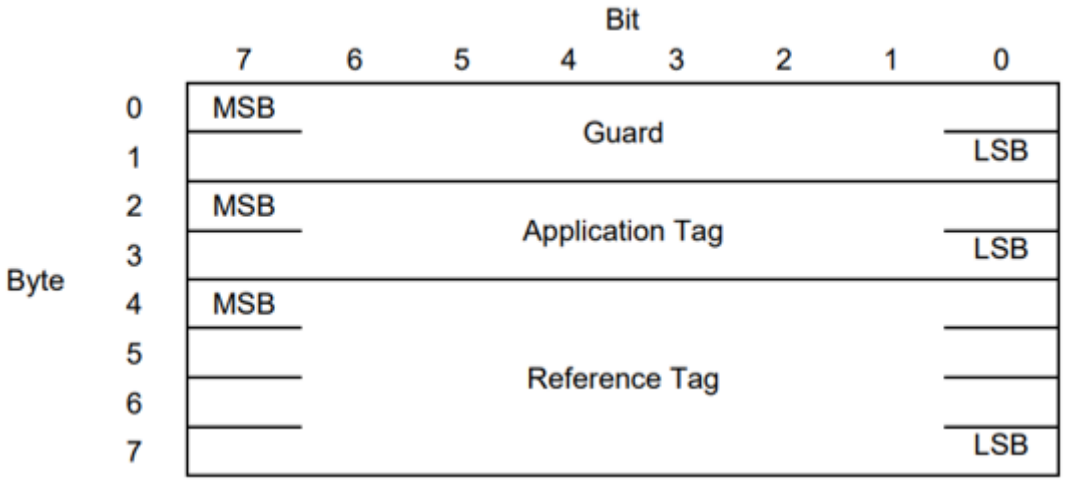
NVMe reservation commands manage the access authorization of multiple hosts to a single namespace. If a host submits a command to a namespace in the presence of a reservation and lacks sufficient rights, then the command will be aborted by the controller with a status of “Reservation Conflict”.

There are three level of hosts, reservation Holder, registrant and non-registrant. Basically, there is only one reservation holder for a shared namespace. And the second level “registrants”, are who have the reservation key, including the reservation holder. The non-registrant is the host who doesn’t have the reservation key.

1.7.4. Metadata Protection

Metadata protection is an End to End Data Protection mechanism to ensure data integrity during data transfer which is realized by transmitting protection info with the LBA data. There are two ways to implement the metadata, one is DIF (Data integrity Field), and it stored together with logic block data. Another way is DIX (Data integrity Extension), it is to put the metadata elsewhere. Figure 1-4 is the diagram of Metadata format.

Figure 1-4 The Diagram of Metadata Format



The "Guard" is a 16-bit CRC, which is calculated from the LBA; "Application Tag" and "Reference Tag" ensure that the data does not appear mismatch problem, such as LBA X uses LBA Y data. CRC check can detect whether the data is wrong, the latter can ensure that the data does not appear mismatch problem, such as LBA X uses LBA Y data, which situation is often caused by SSD firmware Bug.

2. PRODUCT SPECIFICATIONS

2.1. Electrical/Physical Interface

- PCIe Interface
- Compliant with NVMe 1.4
- PCIe Express Base Ver 4.0
- PCIe Gen 4 x 4 lanes & backward compatible to PCIe Gen 3, Gen 2 and Gen 1 Device Capacity
- PCIe Express SFF-8639 Module Specification Revision 4.0, Version1.0, SFF-TA-1001 r1.1

Table 2-1 User Capacity and Addressable Sectors

X100P

DWPD = 1	User Addressable Sectors	Bytes per Sector
960GB	1,875,385,008	512 Byte
1920GB	3,750,748,848	
3840GB	7,501,476,528	
7680GB	15,002,931,888	
15360GB	30,005,842,608	
30720GB	60,011,664,048	

X100E

DWPD = 3	User Addressable Sectors	Bytes per Sector
800GB	1,562,824,368	512 Byte
1600GB	3,125,627,568	
3200GB	6,251,233,968	
6400GB	12,502,446,768	
12800GB	25,004,872,368	
25600GB	50,009,723,568	

NOTES:

1. 1 Gigabyte (GB) is equal to 1,000,000,000 bytes; 1 sector is equal to 512 bytes.
2. The total actual usable capacity of the SSD may be less than the total physical capacity because internal NAND management, SSD format, SSD partition, operating system and so on.
3. The count of User Addressable Sectors is calculated by the formula of IDEMA.

2.2. Performance

2.2.1. Sequential Read/Write Performance and 4K Sustained Random Read/Write Performance

Table 2-2 Sequential Read/Write Performance and 4K Sustained Random Read/ Write Performance

Capacity	Model	Maximum Performance[1]			
		Sequential 512KB (QD=32, Workers=1)		4K Sustained Random (QD=128, , Workers=8)	
		Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
800GB	X100E	7,200	1,800	1,000,000	140,000

Capacity	Model	Maximum Performance[1]			
		Sequential 512KB (QD=32, Workers=1)		4K Sustained Random (QD=128, , Workers=8)	
		Read (MB/s)	Write (MB/s)	Read (IOPS)	Write (IOPS)
960GB	X100P	7,400	1,900	1,000,000	60,000
1600GB	X100E	7,400	3,600	1,750,000	300,000
1920GB	X100P	7,400	3,600	1,750,000	126,000
3200GB	X100E	7,400	6,900	1,750,000	460,000
3840GB	X100P	7,400	6,900	1,750,000	195,000
6400GB	X100E	7,400	7,000	1,750,000	460,000
7680GB	X100P	7,400	7,000	1,750,000	190,000
12800GB	X100E	7,400	7,000	1,750,000	490,000
15360GB	X100P	7,400	7,000	1,750,000	210,000
25600 GB	X100E	7,400	6,000	1,750,000	470,000
30720 GB	X100P	7,400	6,000	1,750,000	210,000

NOTES:

1. Performance was estimated based on 3D TLC NAND flash.
2. Performance may differ according to flash configuration and platform.
3. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.

2.3. Latency

2.3.1. Latency

Table 2-3 4KB Sustained Random Read/Write Latency

Capacity	Model	4K Sustained Random (QD=1, Workers=1)	
		Read	Write
		µs	*µs*
800GB	X100E	70	7
960GB	X100P	70	15
1600GB	X100E	70	7
1920GB	X100P	70	7
3200GB	X100E	70	7
3840GB	X100P	70	7
6400GB	X100E	70	7

Capacity	Model	4K Sustained Random (QD=1, Workers=1)	
		Read	Write
		µs	*µs*
7680GB	X100P	70	7
12800GB	X100E	70	7
15360GB	X100P	70	7
25600GB	X100E	70	7
30720GB	X100P	70	7

NOTES:

1. Performance was estimated based on 3D TLC NAND flash.
2. Performance may differ according to flash configuration and platform.
3. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.

2.4. IOPS Consistency

2.4.1. IOPS Consistency

Table 2-4 4KB Sustained Random Read/Write IOPS Consistency

Capacity	Model	4K Sustained Random (QD=8, Workers=4)	
		Read	Write
		%	%
800GB	X100E	99	99
960GB	X100P	99	99
1600GB	X100E	99	99
1920GB	X100P	99	99
3200GB	X100E	99	97
3840GB	X100P	99	95
6400GB	X100E	99	96
7680GB	X100P	99	99
12800GB	X100E	99	95
15360GB	X100P	99	98
25600GB	X100E	99	96
30720GB	X100P	99	95

NOTES:

1. Consistency Definition: 100% - [(mean_IOPS - min_IOPS) / mean_IOPS]*100

2. Performance was estimated based on 3D TLC NAND flash.
3. Performance may differ according to flash configuration and platform.
4. The tables are for reference only. Any criteria for accepting goods shall be further discussed based on different flash configurations.

2.5. Quality of Service (QoS=99%)

Table 2-5 4KB Sustained Random Read/Write Quality of Service (QoS=99%) 1ms =1000us

Capacity	Model	4KB Sustained Random Read/Write Quality of Service (QoS=99%) [1]			
		(QD=1, Workers=1)		(QD=8, Workers=4)	
		Read	Write	Read	Write
		µs	*µs*	*µs*	*µs*
800GB	X100E	80	10	180	220
960GB	X100P	80	15	180	500
1600GB	X100E	80	10	150	120
1920GB	X100P	80	10	150	260
3200GB	X100E	80	10	140	80
3840GB	X100P	80	10	140	180
6400GB	X100E	80	10	130	80
7680GB	X100P	80	10	130	170
12800GB	X100E	80	10	120	80
15360GB	X100P	80	10	120	160
25600GB	X100E	80	10	120	80
30720GB	X100P	80	10	120	150

2.6. Weight

Table 2-6 Weight

Capacity	**Weight (g)**
800GB	197
960GB	197
1600GB	198
1920GB	198
3200GB	200
3840GB	200
6400GB	203
7680GB	203
12800GB	205
15360GB	205

Capacity	Weight (g)
25600GB	208
30720GB	208

3. ENVIRONMENTAL SPECIFICATIONS

3.1. Environmental Conditions

3.1.1. Temperature and Humidity

Table 3-1 Temperature and Humidity Specification

Temperature	Operating	0°C to 70°C
	Non-operating	-40°C to 85°C
Relative Humidity	Operating	5% to 95%
	Non-operating	5% to 95%

3.1.2. Shock

Table 3-2 Shock

	Type	Acceleration	Pulse Duration
Shock	Operating	500G	2ms
		1000G	0.5ms
	Non-operating	500G	2ms
		1000G	0.5ms

3.1.3. Vibration

Table 3-3 Vibration

	Operating Type	Frequency	Amplitude
Vibration	Operating	200 to 2000 Hz	2.17 Grms
	Non-operating	10 - 2000 Hz	16.3 Grms
		2 -5 - 500 Hz	3 Grms

3.1.4. Altitude

Table 3-4 Altitude

	Operating Type	Value
Altitude	Operating	0 to 18,000 feet
	Non-operating	0 to 40,000 feet

3.2. TBW (Terabytes Written) and DWPD (Drive Write Per Day)

Table 3-5 TBW & DWPD

Capacity	Model Name	TBW	DWPD
800GB	X100E	4380	3
960GB	X100P	1752	1
1600GB	X100E	8760	3
1920GB	X100P	3504	1
3200GB	X100E	17520	3
3840GB	X100P	7008	1
6400GB	X100E	35040	3

Capacity	Model Name	TBW	DWPD
7680GB	X100P	14016	1
12800GB	X100E	70080	3
15360GB	X100P	28032	1
25600GB	X100E	140160	3
30720GB	X100P	56064	1

3.3. Power On/Off Cycles

The definition of power on/off cycles is that the power is withdrawn from the SSD device, and then restored. The test is to simulate the behavior that SSD still can be restored and active normally when host platforms go into suspend and shutdown.

3.4. UBER

Table 3-6 UBER

Capacity	Flash Type	UBER
800GB	3D NAND	< 1 sector per 10^{18} bits read
960GB		
1600GB		
1920GB		
3200GB		
3840GB		
6400GB		
7680GB		
15360GB		
12800GB		
25600GB		
30720GB		

NOTE:

1. UBER (Uncorrectable Bit Error Rates) means the uncorrectable error per bits read.

3.5. Mean Time Between Failures

Mean Time Between Failures(MTBF) is demonstrated through a 2,000-hour Reliability Demonstration Test.

Table 3-7 MTBF

Description	Value
Mean Time Between Failures	2.5 million hours

4. ELECTRICAL SPECIFICATIONS

4.1. Supply Voltage

Table 4-1 Supply Voltage

	800GB /960GB	1600GB /1920GB	3200GB /3840GB	6400GB /7680GB	12800GB /15360GB	25600GB /30720GB
12v	+/- 10%					
12v noise level	240mVp-p, 0-20MHz					
12v min off time	500ms					
3.3v aux	+/- 15%					

NOTE:

1. Minimum time between removed from SSD (Vcc < 100 mV) and power re-applied to the drive.

4.2. Power Consumption

Table 4-2 Power Consumption

Capacity	Random Read(Typ.,W)	Random Write(Typ.,W)	Sequential Read(Typ.,W)	Sequential Write(Typ., W)	Idle (Typ., W)
800GB	9.0	9.0	9.5	8.6	5.00
960GB	9.0	9.0	9.5	8.6	5.00
1600GB	12.8	12.5	10.4	13.3	5.51
1920GB	12.4	11.9	10.1	12.8	5.46
3200GB	13.8	16.4	11.0	18.3	5.83
3840GB	13.3	15.5	10.6	17.9	5.80
6400GB	15.9	17.8	11.9	19.9	5.88
7680GB	15.7	17.4	11.6	19.1	5.75
12800GB	16.5	20.2	12.6	20.8	7.43
15360GB	16.2	19.6	12.3	20.1	7.32
25600GB	18.5	20.4	13.8	20.3	8.46
30720GB	18.5	20.6	13.7	20.1	8.16

NOTE:

1. Power consumption is measured on full speed mode.

4.3. Inrush Current

Table 4-3 Inrush Current

Inrush current	800GB /960GB	1600GB /1920GB	3200GB /3840GB	6400GB /7680GB	12800GB /15360GB	25600GB /30720GB
12v	1.5A					

5. INTERFACE

5.1. PCIe U.3 and U.2 Pin Assignment and Descriptions

Figure 5-1 X100 U.3 PCIe SSD Pin Assignment

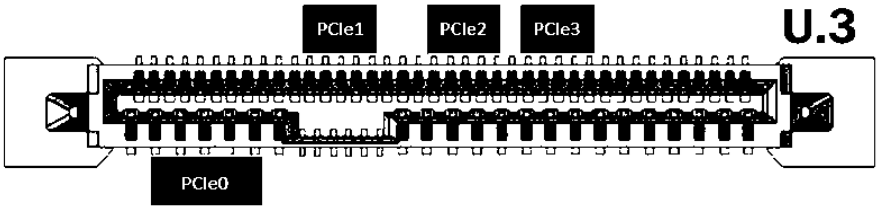


Figure 5-2 X100 U.2 PCIe SSD Pin Assignment

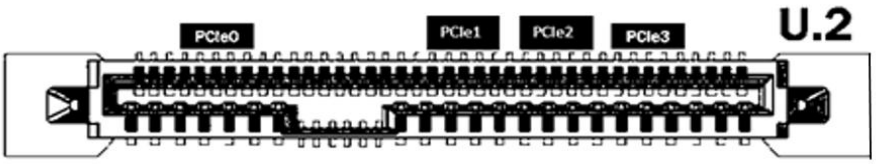


Table 5-1 Pin Assignment and Descriptions

Pin No.	Name	Type	Description
P1	WAKE#	Input	Reserved
P2	Reserved	Reserved	Reserved
P3	PWRDIS	Output	Power disable
P4	IfDet#	Input	Interface Type Detect
P5	Ground	Ground	Ground
P6	Ground	Ground	Ground
P7	+5V	Power	Reserved
P8	+5V	Power	Reserved
P9	+5V	Power	Reserved
P10	PRSNT#	Input	Presence detect
P11	Activity#	Input	Activity indicator
P12	Ground	Ground	Ground
P13	+12V Precharge	Power	+12V Precharge power
P14	+12V	Power	+12V power
P15	+12V	Power	+12V power
SG1	Ground	Ground	Ground
SG2	Ground	Ground	Ground
S1	Ground	Ground	Ground
S2	U.3 TX p0	Diff-Pair	Transmitter differential pair, U.3 Lane 0
S3	U.3 TX n0	Diff-Pair	Transmitter differential pair, U.3 Lane 0
S4	Ground	Ground	Ground
S5	U.3 RX n0	Diff-Pair	Receiver differential pair, U.3 Lane 0
S6	U.3 RX p0	Diff-Pair	Receiver differential pair, U.3 Lane 0

Pin No.	Name	Type	Description
S7	Ground	Ground	Ground
S8	Ground	Ground	Ground
S9	U.3 TX p1	Diff-Pair	Transmitter differential pair, U.3 Lane 1
S10	U.3 TX n1	Diff-Pair	Transmitter differential pair, U.3 Lane 1
S11	Ground	Ground	Ground
S12	U.3 RX n1	Diff-Pair	Receiver differential pair, U.3 Lane 1
S13	U.3 RX p1	Diff-Pair	Receiver differential pair, U.3 Lane 1
S14	Ground	Ground	Ground
S15	HPT0	Output	Host port type
S16	Ground	Ground	Ground
S17	U.3 TX p2/ U.2 TX p1	Diff-Pair	Transmitter differential pair, U.3 Lane 2, or U.2 Lane 1
S18	U.3 TX n2/ U.2 TX n1	Diff-Pair	Transmitter differential pair, U.3 Lane 2, or U.2 Lane 1
S19	Ground	Ground	Ground
S20	U.3 RX n2/ U.2 RX n1	Diff-Pair	Receiver differential pair, U.3 Lane 2, or U.2 Lane 1
S21	U.3 RX p2/ U.2 RX p1	Diff-Pair	Receiver differential pair, U.3 Lane 2, or U.2 Lane 1
S22	Ground	Ground	Ground
S23	U.3 TX p3/ U.2 TX p2	Diff-Pair	Transmitter differential pair, U.3 Lane 3, or U.2 Lane 2
S24	U.3 TX n3/ U.2 TX n2	Diff-Pair	Transmitter differential pair, U.3 Lane 3, or U.2 Lane 2
S25	Ground	Ground	Ground
S26	U.3 RX n3/ U.2 RX n2	Diff-Pair	Receiver differential pair, U.3 Lane 3, or U.2 Lane 2
S27	U.3 RX p3/ U.2 RX p2	Diff-Pair	Receiver differential pair, U.3 Lane 3, or U.2 Lane 2
S28	Ground	Ground	Ground
E1	REFCLKB+	Diff-Pair	Reference clock (differential pair) for second X2 port
E2	REFCLKB-	Diff-Pair	Reference clock (differential pair) for second X2 port
E3	+3.3 Vaux	Power	3.3 V auxiliary power
E4	CLKREQ#/PERSTB#	Bi-dir	Clock request/Fundamental reset for second x2 port
E5	PERST#	Output	Fundamental reset (if Dual port mode enabled, first x2 port)
E6	IFDet2#	Input	Interface Type Detect
E7	REFCLK+	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E8	REFCLK-	Diff-Pair	Reference clock (if dual-port enabled, first X2 port)
E9	Ground	Ground	Ground
E10	U.2 TX p0	Diff-Pair	Transmitter differential pair, U.2 Lane 0
E11	U.2 TX n0	Diff-Pair	Transmitter differential pair, U.2 Lane 0
E12	Ground	Diff-Pair	Ground
E13	U.2 RX n0	Diff-Pair	Receiver differential pair, U.2 Lane 0
E14	U.2 RX p0	Diff-Pair	Receiver differential pair, U.2 Lane 0
E15	Ground	Ground	Ground
E16	HPT1	Output	Host port type
E17	U.2 TX p3	Diff-Pair	Transmitter differential pair, U.2 Lane 3
E18	U.2 TX n3	Diff-Pair	Transmitter differential pair, U.2 Lane 3
E19	Ground	Ground	Ground

Pin No.	Name	Type	Description
E20	U.2 RX n3	Diff-Pair	Receiver differential pair, U.2 Lane 3
E21	U.2 RX p3	Diff-Pair	Receiver differential pair, U.2 Lane 3
E22	Ground	Ground	Ground
E23	SMCLK	Bi-Dir	SMBus (System Management Bus) clock
E24	SMDAT	Bi-Dir	SMBus (System Management Bus) data
E25	DualPortEn#	Output	Dual-port Enable

6. SUPPORTED COMMANDS

6.1. NVMe Command List

Table 6-1 Admin Command List

Identifier	O/M	Supported	Command Description
00h	M	Y	Delete I/O Submission Queue
01h	M	Y	Create I/O Submission Queue
02h	M	Y	Get Log Page
04h	M	Y	Delete I/O Completion Queue
05h	M	Y	Create I/O Completion Queue
06h	M	Y	Identify
08h	M	Y	Abort
09h	M	Y	Set Feature
0Ah	M	Y	Get Feature
0Ch	M	Y	Asynchronous Event Request
0Dh	O	Y	Namespace Management
10h	O	Y	Firmware Commit
11h	O	Y	Firmware Image Download
14h	O	Y	Device Self-test
15h	O	Y	Namespace Attachment
18h	O	N	Keep Alive
19h	O	-	Directive Send
1Ah	O	-	Directive Receive
1Ch	O	-	Virtualization Management
1Dh	O	Y	NVMe-MI Send
1Eh	O	Y	NVMe-MI Receive
7Ch	O	-	Doorbell Buffer Config
80h	O	Y	Format NVM
81h	O	Y	Security Send
82h	O	Y	Security Receive
84h	O	Y	Sanitize
86h	O	-	Get LBA Status

Table 6-2 I/O Commands

Identifier	O/M	Supported	Command Description
00h	M	Y	Flush
01h	M	Y	Write
02h	M	Y	Read
04h	O	Y	Write Uncorrectable
05h	O	Y	Compare
08h	O	Y	Write Zeroes
09h	O	Y	Dataset Management (Trim only)
0Ch	O	Y	Verify

Identifier	O/M	Supported	Command Description
0Dh	O	Y	Reservation Register
0Eh	O	Y	Reservation Report
11h	O	Y	Reservation Acquire
15h	O	Y	Reservation Release

Table 6-3 Set Feature Commands

Identifier	O/M	Supported	Command Description
00h	-	-	Reserved
01h	M	Y	Arbitration
02h	M	Y	Power Management
03h	O	-	LBA Range Type
04h	M	Y	Temperature Threshold
05h	M	Y	Error Recovery
06h	O	Y	Volatile Write Cache
07h	M	Y	Number Of Queues
08h	M	Y	Interrupt Coalescing
09h	M	Y	Interrupt Vector Configuration
0Ah	M	Y	Write Atomicity Normal
0Bh	M	Y	Asynchronous Event Configuration
0Ch	O	-	Autonomous Power State Transition
0Dh	O	-	Host Memory Buffer
0Eh	O	Y	Timestamp
0Fh	O	Y	Keep Alive Timer
10h	O	-	Host Controlled Thermal Management
11h	O	-	Non-Operational Power State Config
12h	O	-	Read Recovery Level Config
13h	O	-	Predictable Latency Mode Config
14h	O	-	Predictable Latency Mode Window
15h	O	-	LBA Status Information Attributes
16h	O	-	Host Behavior Support
17h	O	Y	Sanitize Config
18h	O	-	Endurance Group Event Configuration
19h - 77h	-	-	Reserved (NVMe Reserved)
78h – 7Dh	-	-	Reserved(NVMe MI Reserved)
7Eh	M	Y	Controller Metadata (NVMe MI)
7Fh	M	Y	Namespace Metadata (NVMe MI)
80h	O	-	Software Progress Marker
81h	O	Y	Host Identifier
82h	O	Y	Reservation Notification Mask
83h	O	Y	Reservation Persistence
84h	O	-	Namespace Write Protection Config
85h - BFh	-	-	Command Set Specific (Reserved)

Identifier	O/M	Supported	Command Description
C0h - FFh	O	-	Vendor Specific

Table 6-4 Get Log Page Commands

Identifier	O/M	Supported	Command Description
00h	-	-	Reserved
01h	M	Y	Error Information
02h	M	Y	SMART / Health Information
03h	M	Y	Firmware Slot Information
04h	O	Y	Changed Namespace List
05h	O	Y	Commands Supported and Effects
06h	O	Y	Device Self-test
07h	O	Y	Telemetry Host-Initiated
08h	O	Y	Telemetry Controller-Initiated
09h	O	-	Endurance Group Information
0Ah	O	-	Predictable Latency Per NVM Set
0Bh	O	-	Predictable Latency Event Aggregate
0Ch	O	-	Asymmetric Namespace Access
0Dh	O	Y	Persistent Event Log
0Eh	O	-	LBA Status Information
0Fh	O	-	Endurance Group Event Aggregate
10h - 7Fh	-	-	Reserved
80h	O	Y	Reservation Notification
81h	O	Y	Sanitize Status
82h - FFh	-	-	Reserved

Table 6-5 NVMe Management Interface Commands

Identifier	O/M	Supported	Command Description
00h	M	Y	Read NVMe-MI Data Structure
01h	M	Y	NVM Subsystem Health Status Poll
02h	M	Y	Controller Health Status Poll
03h	M	Y	Configuration Set
04h	M	Y	Configuration Get
05h	M	Y	VPD Read
06h	M	Y	VPD Write
07h	M	Y	Reset
08h	-	-	SES Receive
09h	-	-	SES Send
0Ah	O	-	Management Endpoint Buffer Read
0Bh	O	-	Management Endpoint Buffer Write
0Ch - BFh	O	-	Reserved
C0h - FFh	O	-	Vendor Specific

NOTES:

1. “Y” means “Support”.
2. “O” means “Option, default No support”.
3. “-” means “No support”.

Table 6-6 SMBus / I2C Elements Supported

SMBus/I2C Element	SMBus/I2C Address(8bit)	
	Hex Format	Binary format
FRU Information Device (for NVMe Storage Device)	A6h	1010_011xb
SMBus/I2C Management Endpoint	3Ah	0011_101xb
Basic Management Command	D4h	1101_010xb

6.2. Identify Device Data

The following table details the sector data returned by the IDENTIFY DEVICE command.

Table 6-7 Identify Controller Data Structure

Bytes	O/M	Description	Default Value
01:00	M	PCI Vendor ID (VID)	0x1987
03:02	M	PCI Subsystem Vendor ID (SSVID)	0x1987
23:04	M	Serial Number (SN)	TBD
63:24	M	Model Number (MN)	TBD
71:64	M	Firmware Revision (FR)	TBD
72	M	Recommended Arbitration Burst (RAB)	0x01
75:73	M	IEEE OUI Identifier (IEEE)	TBD*
76	O	Controller Multi-Path I/O and Namespace Sharing Capabilities (CMIC)	0x03
77	M	Maximum Data Transfer Size (MDTS)	0x09
79:78	M	Controller ID (CNTLID)	0x0001
83:80	M	Version (VER)	0x00010400
87:84	M	RTD3 Resume Latency (RTD3R)	0x001E8480 (2 Sec)
91:88	M	RTD3 Entry Latency (RTD3E)	0x00989680
95:92	M	Optional Asynchronous Events Supported (OAES)	0x00000300
99:96	M	Controller Attributes (CTRATT)	0x00000000
101:100	O	Read Recovery Levels Supported (RRLS):	0x0000
110:102	-	Reserved	0x00
111	M	Controller Type (CNTRLTYPE)	0x01
127:112	O	FRU Globally Unique Identifier (FGUID):	TBD
129:128	O	Command Retry Delay Time 1 (CRDT1):	0x0000
131:130	O	Command Retry Delay Time 2 (CRDT2):	0x0000
133:132	O	Command Retry Delay Time 3 (CRDT3):	0x0000
239:134		Reserved	
255:240	-	Refer to the NVMe Management Interface Specification for definition	0x00
257:256	M	Optional Admin Command Support (OACS)	0x005F
258	M	Abort Command Limit (ACL)	0x07

Bytes	O/M	Description	Default Value
259	M	Asynchronous Event Request Limit (AERL)	0x0E
260	M	Firmware Updates (FRMW)	0x1C
261	M	Log Page Attributes (LPA)	0x1E
262	M	Error Log Page Entries (ELPE)	0x3E
263	M	Number of Power States Support (NPSS)	3
264	M	Admin Vendor Specific Command Configuration (AVSCC)	0x01
265	O	Autonomous Power State Transition Attributes (APSTA)	0x00
267:266	M	Warning Composite Temperature Threshold (WCTEMP)	0x0157 (70C)
269:268	M	Critical Composite Temperature Threshold (CCTEMP)	0x0161 (80C)
271:270	O	Maximum Time for Firmware Activation (MTFA)	0x0032
275:272	O	Host Memory Buffer Preferred Size (HMPRE)	0x00000000
279:276	O	Host Memory Buffer Minimum Size (HMMIN)	0x00000000
295:280	O	Total NVM Capacity (TNVMCAP)	**
311:296	O	Unallocated NVM Capacity (UNVMCAP)	**
315:312	O	Replay Protected Memory Block Support (RPMBS)	0x00000000
317:316	O	Extended Device Self-test Time (EDSTT)	0x0002
318	O	Device Self-test Options (DSTO)	0x01
319	O	Firmware Update Granularity (FWUG)	0x01
321:320	O	Keep Alive Support (KAS)	0x0000
323:322	O	Host Controlled Thermal Management Attributes (HCTMA)	0x0001
325:324	O	Minimum Thermal Management Temperature (MNTMT)	0x0111
327:326	O	Maximum Thermal Management Temperature (MXTMT)	0x0157
331:328	O	Sanitize Capabilities (SANICAP)	0x60000003
335:332	O	Host Memory Buffer Minimum Descriptor Entry Size (HMMINDS):	0x00000000
337:336	O	Host Memory Maximum Descriptors Entries (HMMAXD):	0x0000
339:338	O	NVM Set Identifier Maximum (NSETIDMAX):	0x0000
341:340	O	Endurance Group Identifier Maximum (ENDGIDMAX):	0x0000
342	O	ANA Transition Time (ANATT):	0x00
343	O	Asymmetric Namespace Access Capabilities (ANACAP):	0x00
347:344	O	ANA Group Identifier Maximum (ANAGRPMAX):	0x00000000
351:348	O	Number of ANA Group Identifiers (NANAGRPID):	0x00000000
355:352	O	Persistent Event Log Size (PELS):	0x63
511:356		Reserved	0x0

Table 6-8 NVM Command Set Attributes

Description			
512	M	Submission Queue Entry Size (SQES)	0x66
513	M	Completion Queue Entry Size (CQES)	0x44
515:514		Maximum Outstanding Commands (MAXCMD)	0x0400 1 port 0x0200 2 port
519:516	M	Number of Namespaces (NN)	0x00000040
521:520	M	Optional NVM Command Support (ONCS)	0x00FF

Description			
523:522	M	Fused Operation Support (FUSES)	0x0000
524	M	Format NVM Attributes (FNA)	0x04
525	M	Volatile Write Cache (VWC)	0x06
527:526	M	Atomic Write Unit Normal (AWUN)	0x00FF
529:528	M	Atomic Write Unit Power Fail (AWUPF)	0x00FF
530	M	NVM Vendor Specific Command Configuration (NVSCC)	0x01
531	M	Namespace Write Protection Capabilities (NWPC):	0x00
533:532	O	Atomic Compare & Write Unit (ACWU)	0x0000
535:534	M	Reserved	0x0000
539:536	O	SGL Support (SGLS)	0x000F0001
543:540	O	Maximum Number of Allowed Namespaces (MNAN):	0x00000000
767:544	M	Reserved	0x00
1023:768	M	NVM Subsystem NVMe Qualified Name (SUBNQN):	TBD

Table 6-9 IO Command Set Attributes

Description			
2079:2048	M	Power State 0 Descriptor (PSD0)	
Bit[255:184]		Reserved	0x00
Bit[183:182]		Active Power Scale (APS)	0x0
Bit[181:179]		Reserved	0x0
Bit[178:176]		Active Power Workload (APW)	0x0
Bit[175:160]		Active Power (ACTP)	0x0
Bit[159:152]		Reserved	0x0
Bit[151:150]		Idle Power Scale (IPS)	0x0
Bit[149:144]		Reserved	0x0
Bit[143:128]		Idle Power (IDLP)	0x0
Bit[127:125]		Reserved	0x0
Bit[124:120]		Relative Write Latency (RWL)	0x0
Bit[119:117]		Reserved	0x0
Bit[116:112]		Relative Write Throughput (RWT)	0x0
Bit[111:109]		Reserved	0x0
Bit[108:104]		Relative Read Latency (RRL)	0x0
Bit[103:101]		Reserved	0x0
Bit[100:96]		Relative Read Throughput (RRT)	0x0
Bit[95:64]		Exit Latency (EXLAT)	0x0
Bit[63:32]		Entry Latency (ENLAT)	0x0
Bit[31:26]		Reserved	0x0
Bit[25]		Non-Operational State (NOPS)	0
Bit[24]		Max Power Scale (MPS)	0
Bit[23:16]		Reserved	0x0

Description			
Bit[15:0]		Maximum Power (MP)	0x9C4*
2111:2080	O	Power State 1 Descriptor (PSD1)	
Bit[255:184]		Reserved	0x00
Bit[183:182]		Active Power Scale (APS)	0x0
Bit[181:179]		Reserved	0x0
Bit[178:176]		Active Power Workload (APW)	0x0
Bit[175:160]		Active Power (ACTP)	0x0
Bit[159:152]		Reserved	0x0
Bit[151:150]		Idle Power Scale (IPS)	0x0
Bit[149:144]		Reserved	0x0
Bit[143:128]		Idle Power (IDLP)	0x0
Bit[127:125]		Reserved	0x0
Bit[124:120]		Relative Write Latency (RWL)	0x1
Bit[119:117]		Reserved	0x0
Bit[116:112]		Relative Write Throughput (RWT)	0x1
Bit[111:109]		Reserved	0x0
Bit[108:104]		Relative Read Latency (RRL)	0x1
Bit[103:101]		Reserved	0x0
Bit[100:96]		Relative Read Throughput (RRT)	0x1
Bit[95:64]		Exit Latency (EXLAT)	0x0
Bit[63:32]		Entry Latency (ENLAT)	0x0
Bit[31:26]		Reserved	0x0
Bit[25]		Non-Operational State (NOPS)	0
Bit[24]		Max Power Scale (MPS)	0
Bit[23:16]		Reserved	0x0
Bit[15:0]		Maximum Power (MP)	0xE6
2143:2112	O	Power State 2 Descriptor (PSD2)	
Bit[255:184]		Reserved	0x00
Bit[183:182]		Active Power Scale (APS)	0x0
Bit[181:179]		Reserved	0x0
Bit[178:176]		Active Power Workload (APW)	0x0
Bit[175:160]		Active Power (ACTP)	0x0
Bit[159:152]		Reserved	0x0
Bit[151:150]		Idle Power Scale (IPS)	0x0
Bit[149:144]		Reserved	0x0
Bit[143:128]		Idle Power (IDLP)	0x0
Bit[127:125]		Reserved	0x0
Bit[124:120]		Relative Write Latency (RWL)	0x2
Bit[119:117]		Reserved	0x0

Description			
Bit[116:112]		Relative Write Throughput (RWT)	0x2
Bit[111:109]		Reserved	0x0
Bit[108:104]		Relative Read Latency (RRL)	0x2
Bit[103:101]		Reserved	0x0
Bit[100:96]		Relative Read Throughput (RRT)	0x2
Bit[95:64]		Exit Latency (EXLAT)	0x0
Bit[63:32]		Entry Latency (ENLAT)	0x0
Bit[31:26]		Reserved	0x0
Bit[25]		Non-Operational State (NOPS)	0
Bit[24]		Max Power Scale (MPS)	0
Bit[23:16]		Reserved	0x0
Bit[15:0]		Maximum Power (MP)	0xB4
2175:2144	O	Power State 3 Descriptor (PSD3)	0x00
Bit[255:184]		Reserved	0x00
Bit[183:182]		Active Power Scale (APS)	0x0
Bit[181:179]		Reserved	0x0
Bit[178:176]		Active Power Workload (APW)	0x0
Bit[175:160]		Active Power (ACTP)	0x0
Bit[159:152]		Reserved	0x0
Bit[151:150]		Idle Power Scale (IPS)	0x0
Bit[149:144]		Reserved	0x0
Bit[143:128]		Idle Power (IDLP)	0x0
Bit[127:125]		Reserved	0x0
Bit[124:120]		Relative Write Latency (RWL)	0x3
Bit[119:117]		Reserved	0x0
Bit[116:112]		Relative Write Throughput (RWT)	0x3
Bit[111:109]		Reserved	0x0
Bit[108:104]		Relative Read Latency (RRL)	0x2
Bit[103:101]		Reserved	0x0
Bit[100:96]		Relative Read Throughput (RRT)	0x2
Bit[95:64]		Exit Latency (EXLAT)	0x0
Bit[63:32]		Entry Latency (ENLAT)	0x0
Bit[31:26]		Reserved	0x0
Bit[25]		Non-Operational State (NOPS)	0
Bit[24]		Max Power Scale (MPS)	0
Bit[23:16]		Reserved	0x0
Bit[15:0]		Maximum Power (MP)	0xB4
2207:2176	O	Power State 4 Descriptor (PSD4)	0x00
Bit[255:184]		Reserved	0x00

Description			
Bit[183:182]		Active Power Scale (APS)	0x0
Bit[181:179]		Reserved	0x0
Bit[178:176]		Active Power Workload (APW)	0x0
Bit[175:160]		Active Power (ACTP)	0x0
Bit[159:152]		Reserved	0x0
Bit[151:150]		Idle Power Scale (IPS)	0x0
Bit[149:144]		Reserved	0x0
Bit[143:128]		Idle Power (IDLP)	0x0
Bit[127:125]		Reserved	0x0
Bit[124:120]		Relative Write Latency (RWL)	0x4
Bit[119:117]		Reserved	0x0
Bit[116:112]		Relative Write Throughput (RWT)	0x4
Bit[111:109]		Reserved	0x0
Bit[108:104]		Relative Read Latency (RRL)	0x2
Bit[103:101]		Reserved	0x0
Bit[100:96]		Relative Read Throughput (RRT)	0x2
Bit[95:64]		Exit Latency (EXLAT)	0x0
Bit[63:32]		Entry Latency (ENLAT)	0x0
Bit[31:26]		Reserved	0x0
Bit[25]		Non-Operational State (NOPS)	0
Bit[24]		Max Power Scale (MPS)	0
Bit[23:16]		Reserved	0x0
Bit[15:0]		Maximum Power (MP)	0xB4
2239:2208	O	Power State 5 Descriptor (PSD5)	0x00
2271:2240	O	Power State 6 Descriptor (PSD6)	0x00
2303:2272	O	Power State 7 Descriptor (PSD7)	0x00
2335:2304	O	Power State 8 Descriptor (PSD8)	0x00
2367:2336	O	Power State 9 Descriptor (PSD9)	0x00
2399:2368	O	Power State 10 Descriptor (PSD10)	0x00
2431:2400	O	Power State 11 Descriptor (PSD11)	0x00
2463:2432	O	Power State 12 Descriptor (PSD12)	0x00
2495:2464	O	Power State 13 Descriptor (PSD13)	0x00
2527:2496	O	Power State 14 Descriptor (PSD14)	0x00
2559:2528	O	Power State 15 Descriptor (PSD15)	0x00
2591:2560	O	Power State 16 Descriptor (PSD16)	0x00
2623:2592	O	Power State 17 Descriptor (PSD17)	0x00
2655:2624	O	Power State 18 Descriptor (PSD18)	0x00
2687:2656	O	Power State 19 Descriptor (PSD19)	0x00
2719:2688	O	Power State 20 Descriptor (PSD20)	0x00

Description			
2751:2720	O	Power State 21 Descriptor (PSD21)	0x00
2783:2752	O	Power State 22 Descriptor (PSD22)	0x00
2815:2784	O	Power State 23 Descriptor (PSD23)	0x00
2847:2816	O	Power State 24 Descriptor (PSD24)	0x00
2879:2848	O	Power State 25 Descriptor (PSD25)	0x00
2911:2880	O	Power State 26 Descriptor (PSD26)	0x00
2943:2912	O	Power State 27 Descriptor (PSD27)	0x00
2975:2944	O	Power State 28 Descriptor (PSD28)	0x00
3007:2976	O	Power State 29 Descriptor (PSD29)	0x00
3039:3008	O	Power State 30 Descriptor (PSD30)	0x00
3071:3040	O	Power State 31 Descriptor (PSD31)	0x00
4095:3072	O	Vendor Specific.	0x00

NOTE:

* Maximum power of X100 production line

Table 6-10 IO Vendor Specific

Description			
4095:3072	O	Vendor Specific (VS)	Phison Reserved

NOTES:

* The OUI shall be a valid IEEE/RAC assigned identifier that may be registered at http://standards.ieee.org/develop/regauth/oui/public.html.

** Depends on the using of capacity

Table 6-11 Identify Namespace Data Structure & NVM Command Set Specific

Bytes	O/M	Description	Default Value
7:0	M	Namespace Size (NSZE)	TBD*
15:8	M	Namespace Capacity (NCAP)	TBD*
23:16	M	Namespace Utilization (NUSE)	TBD*
24	M	Namespace Features (NSFEAT)	0x1E
25	M	Number of LBA Formats (NLBAF)	0x04
26	M	Formatted LBA Size (FLBAS)	0x00
27	M	Metadata Capabilities (MC)	0x03
28	M	End-to-end Data Protection Capabilities (DPC)	0x1B
29	M	End-to-end Data Protection Type Settings (DPS)	0x00
30	O	Namespace Multi-path I/O and Namespace Sharing Capabilities (NMIC)	0x01
31	O	Reservation Capabilities (RESCAP)	0xAB
32	O	Format Progress Indicator (FPI)	0x00
33	O	Deallocate Logical Block Features (DLFEAT):	0x19
35:34	O	Namespace Atomic Write Unit Normal (NAWUN)	0x0000
37:36	O	Namespace Atomic Write Unit Power Fail (NAWUPF)	0x0000
39:38	O	Namespace Atomic Compare & Write Unit (NACWU)	0x0000

Bytes	O/M	Description	Default Value
41:40	O	Namespace Atomic Boundary Size Normal (NABSN)	0x0000
43:42	O	Namespace Atomic Boundary Offset (NABO)	0x0000
45:44	O	Namespace Atomic Boundary Size Power Fail (NABSPF)	0x0000
47:46	O	Namespace Optimal I/O Boundary (NOIOB):	0x0000
63:48	O	NVM Capacity (NVMCAP)	TBD*
65:64	O	Namespace Preferred Write Granularity (NPWG):	0x0000
67:66	O	Namespace Preferred Write Alignment (NPWA):	0x0000
69:68	O	Namespace Preferred Deallocate Granularity (NPDG):	0x0000
71:70	O	Namespace Preferred Deallocate Alignment (NPDA):	0x0000
73:72	O	Namespace Optimal Write Size (NOWS):	0x0000
91:74	-	Reserved	0x00
95:92	O	ANA Group Identifier (ANAGRPID):	0x00000000
98:96	-	Reserved	
99	O	Namespace Attributes (NSATTR):	0x00
101:100	O	NVM Set Identifier (NVMSETID):	0x0000
103:102	O	Endurance Group Identifier (NEDGID)	0x0000
119:104	O	Namespace Globally Unique Identifier (NGUID)	TBD**
127:120	O	IEEE Extended Unique Identifier (EUI64)	TBD**
131:128	M	LBA Format 0 Support (LBAF0)	0x02090000
135:132	O	LBA Format 1 Support (LBAF1)	0x00000000
139:136	O	LBA Format 2 Support (LBAF2)	0x00000000
143:140	O	LBA Format 3 Support (LBAF3)	0x00000000
147:144	O	LBA Format 4 Support (LBAF4)	0x00000000
151:148	O	LBA Format 5 Support (LBAF5)	0x00000000
155:152	O	LBA Format 6 Support (LBAF6)	0x00000000
159:156	O	LBA Format 7 Support (LBAF7)	0x00000000
163:160	O	LBA Format 8 Support (LBAF8)	0x00000000
167:164	O	LBA Format 9 Support (LBAF9)	0x00000000
171:168	O	LBA Format 10 Support (LBAF10)	0x00000000
175:172	O	LBA Format 11 Support (LBAF11)	0x00000000
179:176	O	LBA Format 12 Support (LBAF12)	0x00000000
183:180	O	LBA Format 13 Support (LBAF13)	0x00000000
187:184	O	LBA Format 14 Support (LBAF14)	0x00000000
191:188	O	LBA Format 15 Support (LBAF15)	0x00000000
383:192		Reserved	0x00
4095:384	O	Vendor Specific (VS)	0x00

NOTES:

*According to IDEMA SPEC

** According to IEEE EUI-64 SPEC

Table 6-12 List of Identify Namespace Data Structure for Each Capacity

Capacity (GB)	Byte [7:0]: Namespace Size (NSZE)(Hex)	Byte [7:0]: Namespace Size (NSZE)(Dec)
1600	BA4D4AB0	1,600,321,314,816
1920	DF8FE2B0	1,920,383,410,176
3200	1749A42B0	3,200,631,791,616
3840	1BF1F72B0	3,840,755,982,336
6400	5D268656000	6,401,252,745,216
7680	6FC7D256000	7,681,501,126,656
12800	BA4D0256000	12,802,494,652,416
15360	DF8F9A56000	15,362,991,415,296
25600	17499FA56000	25,604,978,466,816
30720	1BF1F2A56000	30,725,971,992,576

6.3. SMART Attributes

Table 6-13 SMART Attributes (Log Identifier 02h)

Bytes Index	Bytes	Description
[0]	1	Critical Warning
[2:1]	2	Composite Temperature
[3]	1	Available Spare
[4]	1	Available Spare Threshold
[5]	1	Percentage Used
[31:6]	26	Reserved
[47:32]	16	Data Units Read
[63:48]	16	Data Units Written
[79:64]	16	Host Read Commands
[95:80]	16	Host Write Commands
[111:96]	16	Controller Busy Time
[127:112]	16	Power Cycles
[143:128]	16	Power On Hours
[159:144]	16	Unsafe Shutdowns
[175:160]	16	Media and Data Integrity Errors
[191:176]	16	Number of Error Information Log Entries
[195:192]	4	Warning Composite Temperature Time
[199:196]	4	Critical Composite Temperature Time
[201:200]	2	Temperature Sensor 1 (Current Temperature)
[203:202]	2	Temperature Sensor 2 (N/A)
[205:204]	2	Temperature Sensor 3 (N/A)
[207:206]	2	Temperature Sensor 4 (N/A)
[209:208]	2	Temperature Sensor 5 (N/A)
[211:210]	2	Temperature Sensor 6 (N/A)
[213:212]	2	Temperature Sensor 7 (N/A)

Bytes Index	Bytes	Description
[215:214]	2	Temperature Sensor 8 (N/A)
[219:216]	4	Thermal Management Temperature 1 Transition Count
[223:220]	4	Thermal Management Temperature 2 Transition Count
[227:224]	4	Total Time For Thermal Management Temperature 1 (seconds)
[231:228]	4	Total Time For Thermal Management Temperature 2 (seconds)
[511:232]	280	Reserved

Table 6-14 SMART Attributes (Log Identifier C0h)

Bytes Index	Bytes	Description
[15:0]	16	Physical Media Units Written
[31:16]	16	Physical Media Units Read
[39:32]	8	Bad User NAND Blocks
[47:40]	8	Bad System NAND Blocks
[55:48]	8	XOR Recovery Count
[63:56]	8	Uncorrectable Read Error Count
[71:64]	8	Soft ECC Error Count
[79:72]	8	End to End Correction Counts
[80]	1	System Data % Used
[87:81]	7	Refresh Counts
[95:88]	8	User Data Erase Counts
[97:96]	2	Thermal Throttling Status and Count
[103:98]	6	DSSD Specification Version
[111:104]	8	PCIe Correctable Error Count
[115:112]	4	Incomplete Shutdowns
[119:116]	4	Reserved
[120]	1	% Free Blocks
[127:121]	7	Reserved
[129:128]	2	Capacitor Health
[135:130]	6	Reserved
[143:136]	8	Unaligned I/O
[151:144]	8	Security Version Number
[159:152]	8	Total NUSE
[175:160]	16	PLP Start Count
[191:176]	16	Endurance Estimate
[199:192]	8	PCIe Link Retraining Count
[493:200]	294	Reserved
[495:494]	2	Log Page Version
[511:496]	16	Log Page GUID

Table 6-15 SMART Attributes (Log Identifier D2h)

Bytes Index	Bytes	Description
[7:0]	8	Device Capacity

Bytes Index	Bytes	Description
[15:8]	8	User Capacity
[23:16]	8	NAND Read
[31:24]	8	NAND Write
[39:32]	8	NAND Erase Sector
[47:40]	8	Wear Range Delta(%)
[55:48]	8	SSD Life Used Percent D3
[56]	1	WP Water Mark
[58:57]	2	Highest temperature
[62:59]	4	Read Fail Count
[66:63]	4	Data E3D Error
[70:67]	4	PHY Error Count
[74:71]	4	Total Bad Block Count
[78:75]	4	Total Early Bad Block Count
[82:79]	4	Total Later Bad Block Count
[86:83]	4	Read Fail Count
[90:87]	4	Program Fail Count
[94:91]	4	Erase Failure Count
[102:95]	8	System Table Copy Count
[110:96]	8	ReadMoveTableCnt
[114:111]	4	Data read retry count
[118:115]	4	RAID ECC retry count
[122:119]	4	RAID ECC failed count
[130:123]	8	Total Erase Count
[134:131]	4	D2/D3 Max Erase Count
[138:135]	4	D2/D3 Average Erase Count
[142:139]	4	D2/D3 Min Erase Count
[150:143]	8	Background read count (N/A)
[154:151]	4	Host Write Uncorrectable Sector Count
[158:155]	4	PS3 Enter Success (N/A)
[162:159]	4	PS4 Enter Success (N/A)
[166:163]	4	Wear Leveling Count
[168:167]	2	Chip internal temperature
[170:169]	2	Thermal throttling
[172:171]	2	Thermal throttling time
[180:173]	8	FW Code Update Count
[188:181]	8	Flash UNC Error Count
[192:189]	4	HB retry count
[196:193]	4	SB retry count
[511:197]	315	Reserved

7. PHYSICAL DIMENSION

Figure 7-1 shows the case mechanical information of Phison X100 Series SSD in the U.2 / U.3 2.5-inch 15mm form factor. All dimensions are in millimeters.

Figure 7-1 U.2 / U.3 2.5-inch 15mm Mechanical information

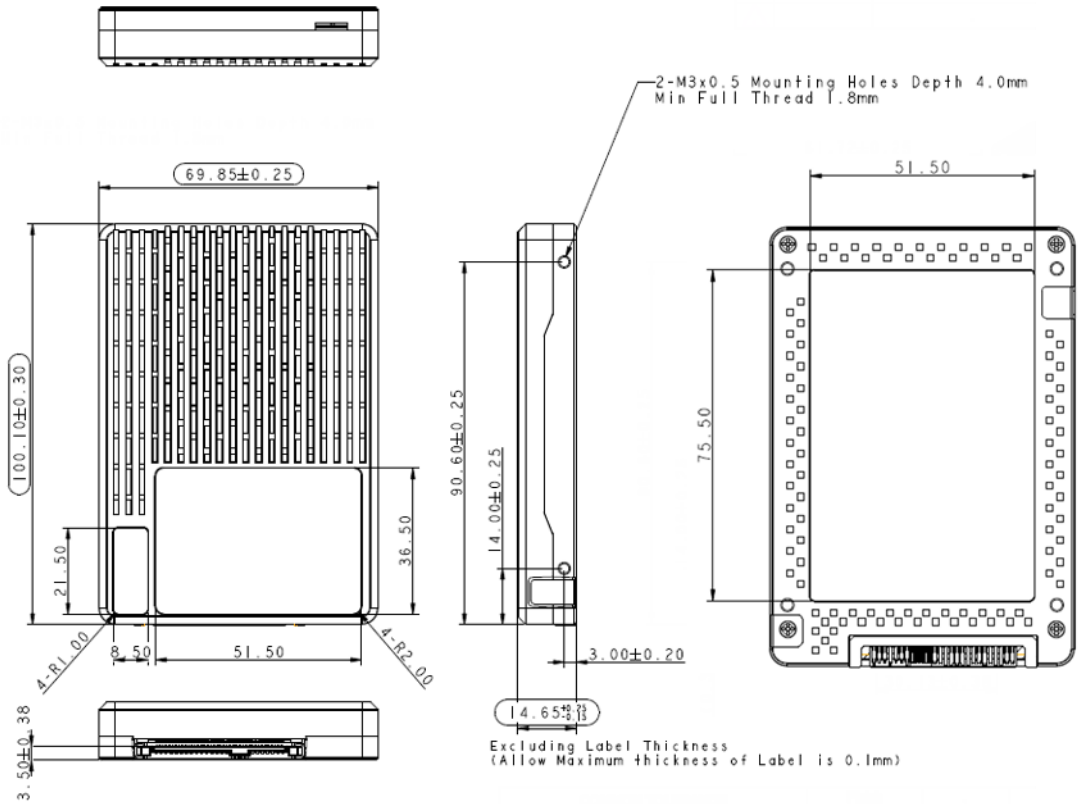


Table 7-1 U.2 / U.3 2.5-inch 15mm Length/Width/Height

	Nominal(mm)	Tolerance(mm)
Length	100.10	± 0.30
Width	69.85	± 0.25
Height	14.65	+0.25 / -0.15

Figure 7-2 shows the case mechanical information of Phison X100 Series SSD in the U.2 / U.3 pro 2.5-inch 15mm form factor. All dimensions are in millimeters.

Figure 7-2 U.2 / U.3 pro 2.5-inch 15mm Mechanical information

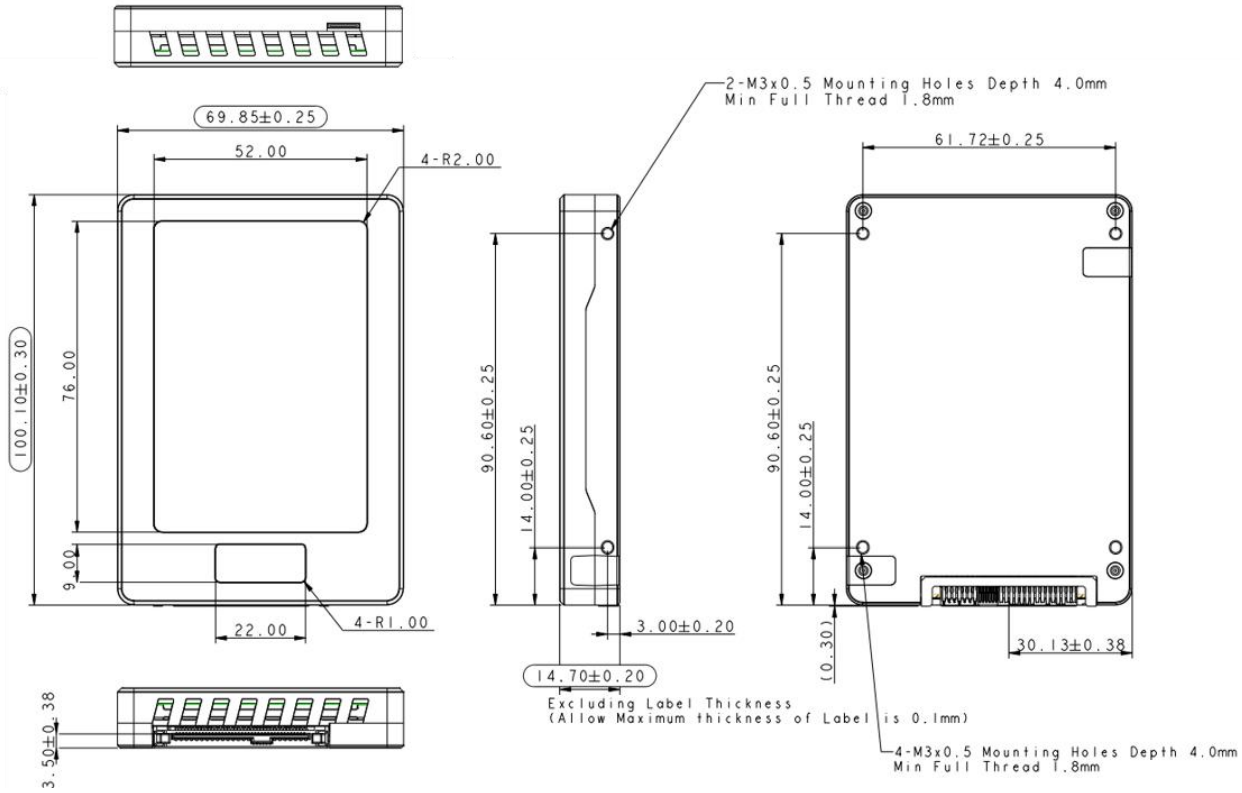


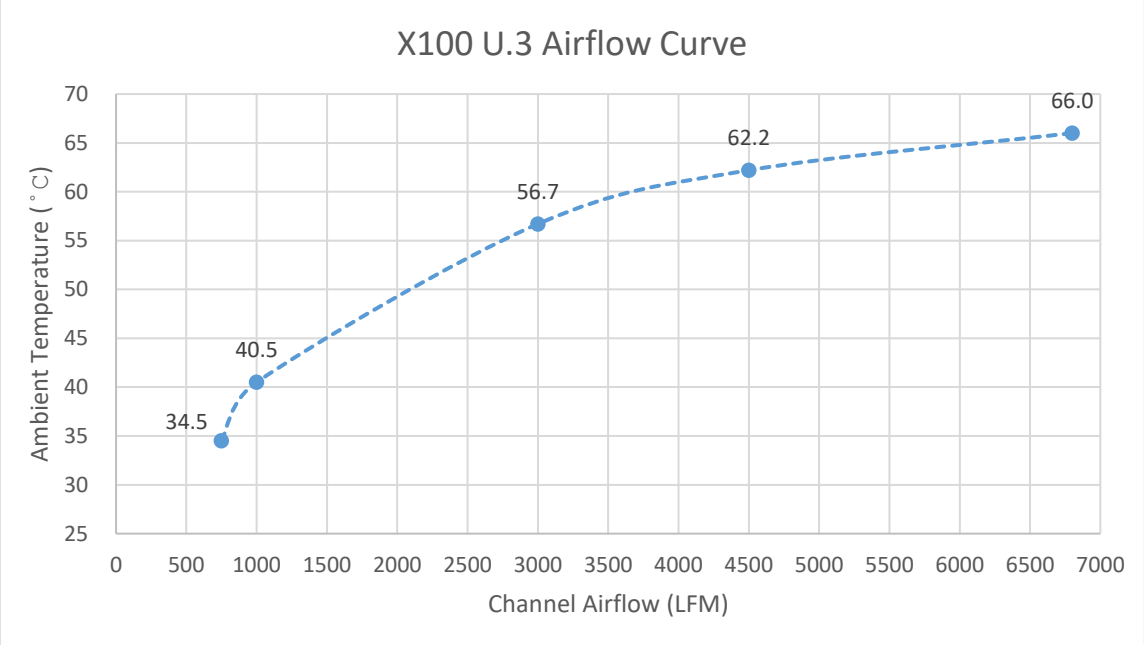
Table 7-2 U.2 / U.3 pro 2.5-inch 15mm Length/Width/Height

	Nominal(mm)	Tolerance(mm)
Length	100.10	± 0.30
Width	69.85	± 0.25
Height	14.70	± 0.20

8. AIR FLOW PROFILE

Figure 8-1 depicts the minimum airflow a U.3 (8TB) needs to operate without triggering thermal throttling at ambient temperatures varied from 35°C to 65°C.

Figure 8-1 X100 U.3 Airflow Curve



9. PERFORMANCE AND POWER SOP

The methodologies and platform used to obtain power consumption and performance data are listed in the following sections. Again, performance and power consumption may vary depending on the flash configuration and platform used.

9.1. Performance Test Platform

- Mother Board: ASUS PRIME X570-PRO
- CPU: AMD Ryzen 5 5600x 6-core processor x 12
- DRAM: Apacer DDR4 3200MHz 16GB
- OS version: Ubuntu 20.04.2 LTS

9.2. Performance methodologies

9.2.1. FIO Test procedure

■ Secure erase - > no need format drive

- 128K Seq. write/read
  1. Pre-con - 300% seq. write to full disk
     a. IO Depth = 32
     b. Number of jobs = 1
  2. Test script
     a. IO Depth = 32
     b. Number of Jobs= 1
     c. Test duration: 300secs

9.2.2. IOPS consistency Test procedure

■ Secure erase - > no need format drive

- 4k random write/read
  1. Pre-con - 300% 4K random write to full disk
     a. IO Depth = 1
     b. Number of jobs = 1
  2. Pre-con - 300% 4K random write to full disk
     c. IO Depth = 32
     d. Number of jobs =1
  3. Pre-con - 300% 4K random write to full disk
     e. IO Depth = 64
     f. Number of jobs = 8

9.2.3. Latency Test procedure

■ Secure erase - > no need format drive

- 4k random write/read
  1. Pre-con - 300% 4K random write to full disk
     a. IO Depth = 1
     b. Number of jobs = 1
  2. Pre-con - 300% 4K random write to full disk
     a. IO Depth = 32

b. Number of jobs = 1

3. Pre-con - 300% 4K random write to full disk
   a. IO Depth = 64
   b. Number of jobs = 8

9.2.4. QoS test procedure

- Secure erase - > no need format drive
  - 4k random write/read
    1. Pre-con - 300% 4K random write to full disk
       a. IO Depth = 1
       b. Number of jobs = 1
    2. Pre-con - 300% 4K random write to full disk
       a. IO Depth = 32
       b. Number of jobs = 1
    3. Pre-con - 300% 4K random write to full disk
       a. IO Depth = 64
       b. Number of jobs = 8

- Data collection Procedure:
  1. Run entire test script one time.
  2. Run each condition in the script for 300 seconds.
  3. Calculate average value for each condition.
  4. Get the average value, add some buffers and round down to the nearest 10th.
  5. Verify the numbers requested by PRD.

9.3. Power consumption Test Platform

Mother board: X570 AORUS MASTER Default string

CPU: AMD Ryzen 7 5800X 8-Core Processor

DRAM: DDR4 3200MHz 16GB

OS version: Ubuntu 16.04.3 LTS

9.4. Power consumption methodologies

9.4.1. Test Procedure

- 2T/4T/8T devices :
- Secure erase - > no need format drive -> Connect power board (Measure Current)
  - 2048k Seq. write/read
    1. Pre-con - 100% seq. write to full disk
       a. IO Depth = 1024
       b. Number of jobs = 1
    2. Test script (100% seq. write / 100% seq. read)
       a. IO Depth = 1024
       b. Number of Jobs= 1
       c. Test duration: 900secs (for each performance)
  - 4k random write/read
    1. Test script

- 100% ran. write / 100% ran. read / 70% ran. read + 30% ran. write / 30% ran. read + 70% ran. write
  a. IO Depth = 256
  b. Number of Jobs= 12
  c. Test duration: 900secs (for each performance)

- 16T/32T devices :
- Secure erase - > no need format drive -> Connect power board (Measure Current)
  - 128K Seq. write/read
    1. Pre-con - 100% seq. write to full disk
       c. IO Depth = 32
       d. Number of jobs = 1
    2. Test script (100% seq. write / 100% seq. read)
       d. IO Depth = 32
       e. Number of Jobs= 1
       f. Test duration: 900secs (for each performance)
  - 4k random write/read
    1. Test script
       - 100% ran. write / 100% ran. read / 70% ran. read + 30% ran. write / 30% ran. read + 70% ran. write
       d. IO Depth = 32
       e. Number of Jobs= 8
       f. Test duration: 900secs (for each performance)

- Data collection procedure – Max average value (over 500ms duration)
  a) Run entire test script one time.
  b) Run each condition in the script.
  c) Calculate average value for each condition and then select maximum average.
  d) Note the values for each condition.
  e) Take 3 samples of each capacity.

- Data collection procedure – Peak (1us resolution)
  a) Run entire test script one time.
  b) Run each condition in this script.
  c) Select the maximum value for each condition.
  d) Note the maximum as the peak value.
  e) Take 3 samples of each capacity.

- Data collection procedure – Power on
  a) Run power on procedure until drive is ready to use.
  b) Measure power to get maximum average power and maximum peak current.
  c) Take 3 samples of each capacity.

- Data collection procedure – Idle
  a) After completing each condition, Idle for 30 seconds.
  b) Do nothing and measure power to get the maximum average Idle power.
  c) Take 3 samples of each capacity.

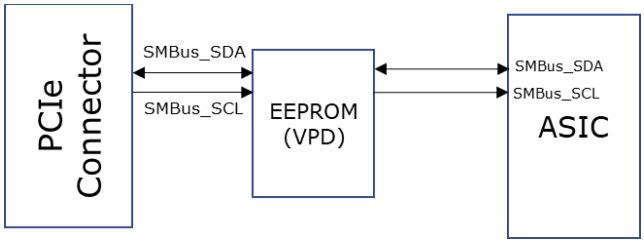
10. VITAL PRODUCT DATA

X100 U.2/U.3 devices can support Read and Write to Vital Product Data (VPD). Please refer to Figure 10-1 X100 U.3 PCIe SSD Controller Block Diagram for details on VPD Data Structure. VPD contains:

- Basic inventory information such as type and size of Enterprise PCIe SSD, manufacture, date, revision, and GUID.
- Power management data such as power level and power modes.
- Vendor specific data.

VPD is stored in a SMBus device with a slave address of 0xA6. VPD page can be read via SMBUS through address 0x53. Writes to the VPD page uses 0x53.

Figure 10-1 X100 U.3 PCIe SSD Controller Block Diagram



11. PCIE ID (APPENDIX)

Table 11-1 PCIe ID

ID Name	Description	U.3	PCIe Register Location	Identify Controller Location	Vital Product Data Location
Vendor ID (VID)	Vendor ID assigned by PCI-SIG	0x1BB1	PCI Header Offset 0x2	Identify Controller Data Structure Bytes 01:00	TBD
Device ID (DID)	Device ID assigned by vendor	0x5020	PCI Header Offset 0x0	N/A	TBD
Subsystem Vendor ID	Indicates Sub-system vendor ID	0x1987	PCI Header Offset 0x2C	Identify Controller Data Structure Bytes 03:02	TBD
Subsystem ID	Sub-system identifier	0x1987	PCI Header Offset 0x2E	N/A	TBD

12. PRODUCT WARRANTY POLICY

In the event the Product does not conform to the specification within Phison agreed warranty period and such inconformity is solely attributable to Phison's cause, Phison agrees at its discretion replace or repair the nonconforming Product. Notwithstanding the foregoing, the aforementioned warranty shall exclude the inconformity arising from, in relation to or associated with:

(1) alternation, modification, improper use, misuse or excessive use of the Product;

(2) failure to comply with Phison's instructions;

(3) Phison's compliance with customer (including customer's suppliers, subcontractors or downstream customers) indicated instructions, technologies, designs, specifications, materials, components, parts;

(4) combination of the Product with other materials, components, parts, goods, hardware, firmware or software not developed by Phison; or

(5) other error or failure not solely attributable to Phison's cause (including without limitation, normal wear or tear, manufacturing or assembly wastage, improper operation, virus, unauthorized maintenance or repair).

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