CH182 Ethernet PHY Transceiver

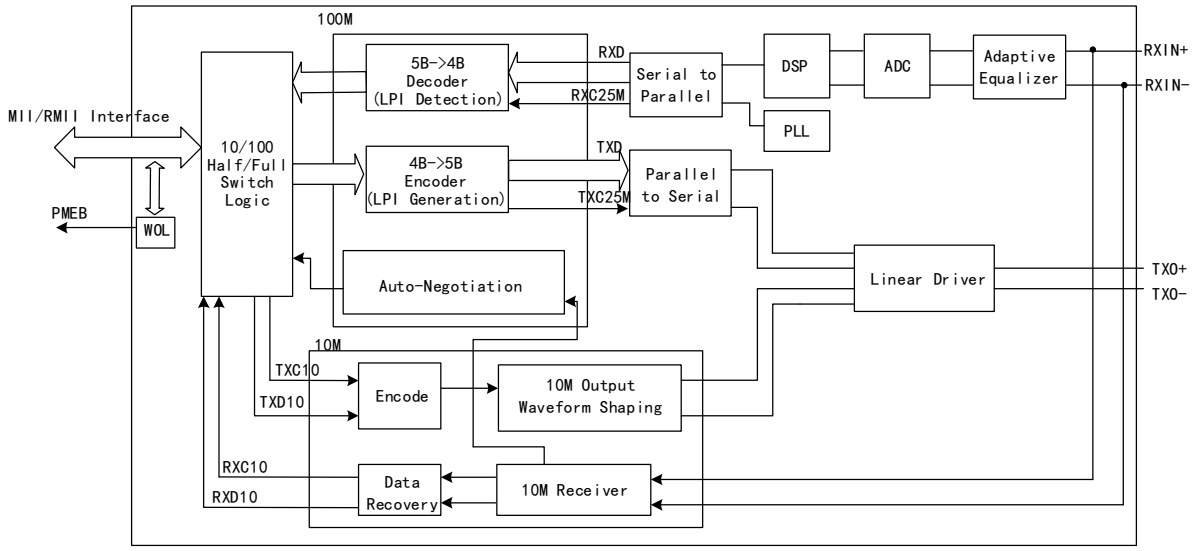
V1.1

http://wch-ic.com

1. Overview

CH182 is an industrial grade 10/100M Ethernet PHY transceiver with Auto-MDIX support. CH182 internally includes Physical Coding Sublayer (PCS), Physical Media Access Layer (PMA), Twisted Pair Physical Medium Dependent (TP-PMD), 10BASE-TX encoder/decoder, Twisted Pair Media Attachment Unit (TPMAU), MII and RMII interfaces, and other modules required for Ethernet Transceiver functions.

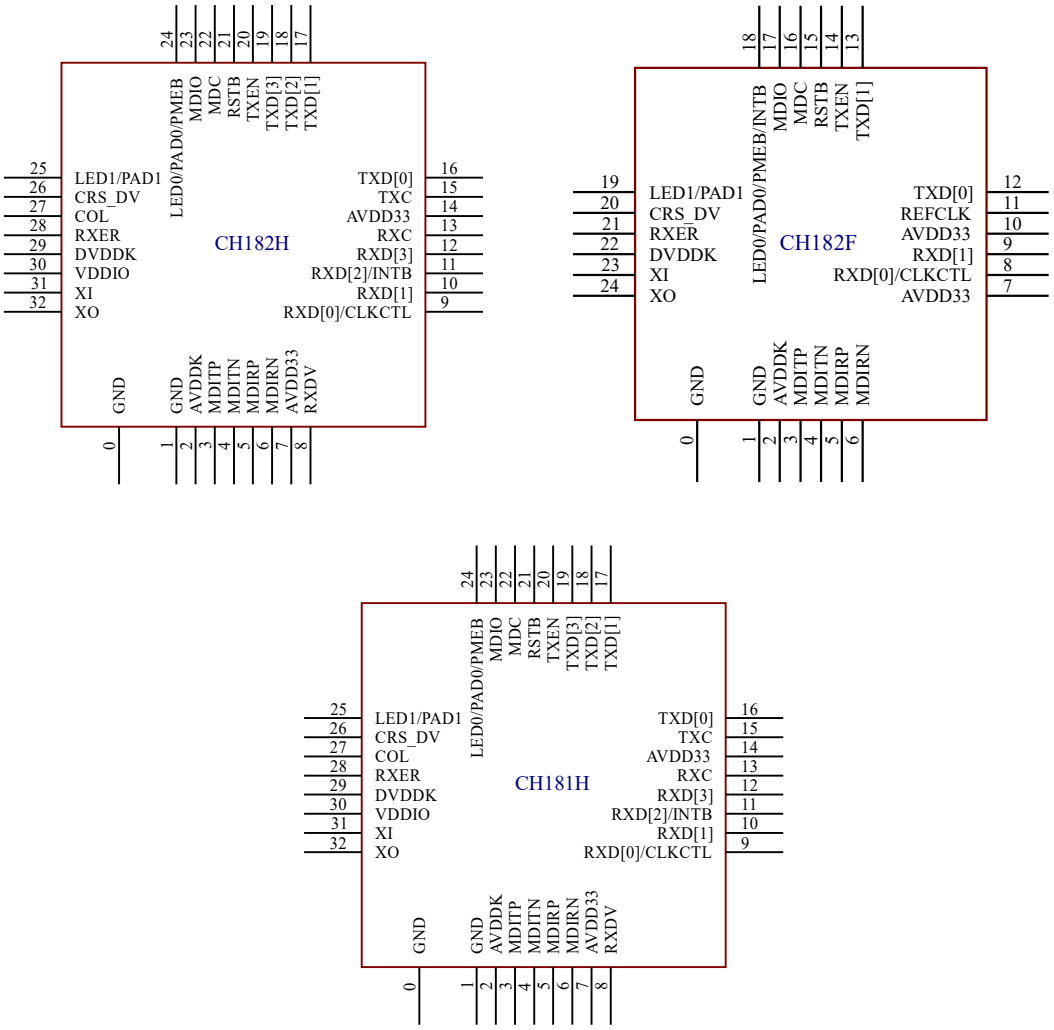
The following figure shows the block diagram of CH182.



2. Feature

- Low-power Ethernet physical layer transceiver PHYceiver implemented based on DSP algorithm.
- Support downtime mode.
- Support Auto-MDIX switching TX/RX and automatic identification of positive and negative signal lines.
- Support 10BASE-T and 100BASE-TX and auto-negotiation.
- Support both MII and RMII interface modes.
- Support full-duplex and half-duplex operation.
- Support UTP CAT5E and CAT6 twisted pair cable, support 120m transmission distance.
- Built-in LDO, supports independent I/O interface power supply for different voltage processors or MCUs.
- Built-in 50Ω impedance matching resistor, built-in capacitor required for 25MHz crystal oscillator, and streamlined peripheral circuitry.
- Optional support for external 50MHz clock input.
- Support WOL network wake-up.
- Support interrupt function.
- Support two types of network status LEDs.
- Available in QFN24 and QFN32 packages.

3. Package



Package form	Size	Pin spacing		Package description	Order model
QFN24-4×4	4.0*4.0mm	0.50mm	19.7mil	Quad Flat No-lead Package	CH182F
QFN32-5×5	5.0*5.0mm	0.50mm	19.7mil	Quad Flat No-lead Package	CH182H
QFN32-5×5	5.0*5.0mm	0.50mm	19.7mil	Quad Flat No-lead Package	CH181H

Note: CH182F only supports RMII interface mode.

All other CH182 contents are applicable to CH181 except where specifically marked.

4. Pin

181H Pin No.	182H Pin No.	182F Pin No.	Pin name	Type	Pin description
3	3	3	MDITP	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode; Differential input in 10BASE-T/100BASE-TX MDIX mode.
4	4	4	MDITN		
5	5	5	MDIRP	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode; Differential output in 10BASE-T/100BASE-TX MDIX mode.
6	6	6	MDIRN		
7	7	7	AVDD33	P	3.3V main power input, 1uF to ground capacitor is recommended to be placed close to the chip. Or 0.1uF ~ 4.7uF, support 10uF but need to parallel 0.1uF.
14	14	10	AVDD33	P	3.3V power input, 0.1uF capacitor to ground is recommended.
30	30	-	VDDIO	P	3.3V or 2.5V power input for I/O interface, external 0.1uF capacitor to ground
2	2	2	AVDDK	P	External 1uF to ground capacitor is placed close to the chip.
29	29	22	DVDDK	P	External 0.1uF (0.1uF ~ 1uF) capacitor to ground is placed close to the chip.
0	0	0	GND	P	Common ground terminal.
1	1	1	GND	P	Optional common ground terminal, recommended connection.
31	31	23	XI	I	Crystal input, external 25MHz crystal end required, or external 25MHz clock input.
32	32	24	XO	IO	Inverted output of crystal, need to connect the other end of 25MHz crystal externally. Or when XI is connected to GND, XO is used to input external 25MHz or 50MHz clock.
21	21	15	RSTB	I,PU	Reset input, active low.
8	8	-	RXDV	LI, O,PD	Receive data is valid. Outputs high on RXD[3:0] when data is received; It is pulled low when reception is complete; it is valid on the rising edge of RXC. PHY detects this pin during power-on reset to configure MAC interface mode: Default set low by internal pull-down resistor = MII interface mode; Optional external 4.7KΩ pull-up resistor = RMII interface mode.
9	9	8	RXD[0] /CLKCTL	LI, O,PD	Receive data bits. Driven by the PHY to provide parallel receive data to the MAC. During power-up PHY detects RXD[0] pin to configure RMII mode TXC direction: Default set low by internal pull-down resistor = TXC output clock; Optional external 4.7KΩ pull-up resistor = TXC input clock. PHY detection during power-up RXD[2] pin configuration LED0/1 pin function:
10	10	9	RXD[1]	O,PD	
11	11	-	RXD[2] /INTB	LI, O,PD	
12	12	-	RXD[3]	O,PD	

181H Pin No.	182H Pin No.	182F Pin No.	Pin name	Type	Pin description
					Low by internal pull-down resistor by default = LED function; Optional external 4.7KΩ pull-up resistor = WOL function. LED0 pin is used as PMEB, LED1 pin is not output and remains in pull-down state. In RMII mode, the RXD[2] pin is used as interrupt output INTB: 200KΩ recommended for external pull-up resistor to maintain LED functionality; or 4.7KΩ for the external pull-up resistor to select the WOL function.
-	-	18	INTB	O,OD	Interrupt output in RMII mode, open drain, active low. Low output if link state changes, duplex mode changes or auto-negotiation fails, high level is achieved by external 4.7KΩ pull-up resistor.
13	13	-	RXC	O,PD	Output receive clock. This pin provides a continuous operating clock for the RXD[3:0] and RXDV signals. RXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively.
26	26	20	CRS_DV	O,PD	Carrier detect/receive data is active. If the receive medium is not idle, output high.
27	27	-	COL	O,PD	The COL outputs high when a collision is detected.
28	28	21	RXER	O,PD	Receive error indication.
15	15	-	TXC /REFCLK	IO, PD	MII mode outputs the transmit clock and RMII mode outputs or inputs the reference clock. In MII mode: This pin provides continuous operating clocks for the TXD[3:0] and TXEN signals. TXC is 25MHz and 2.5MHz in 100Mbps and 10Mbps modes, respectively. In RMII mode: This pin is used to output or input the 50MHz reference clock REFCLK with the direction determined by the RXD[3]/CLKCTL pin or Page 7 register 16.
-	-	11	REFCLK	IO, PD	RMII mode output or input 50MHz reference clock. The direction is determined by the RXD[0]/CLKCTL pin or Page 7 register 16.
16	16	12	TXD[0]	I,PD	Transmit data bits. Driven by the MAC to provide parallel transmit data to the PHY. When TXEN is enabled, TXD[0:3] data is valid.
17	17	13	TXD[1]		
18	18	-	TXD[2]		
19	19	-	TXD[3]		
20	20	14	TXEN	I,PD	Transmit enable.
22	22	16	MDC	I,PU	Clock input for the SMI management interface.

<table>
<tr><th>181H Pin No.</th><th>182H Pin No.</th><th>182F Pin No.</th><th>Pin name</th><th>Type</th><th>Pin description</th></tr>
<tr><td></td><td></td><td></td><td></td><td></td><td>This pin inputs a serial clock synchronized with MDIO.
A pull-up resistor is built in to prevent the pin from floating.</td></tr>
<tr><td>23</td><td>23</td><td>17</td><td>MDIO</td><td>IO, PU</td><td>Data input and output for the SMI management interface.
This pin is used to input or output bi-directional serial data for management information.</td></tr>
<tr><td>24</td><td>24</td><td>18</td><td>PMEB</td><td>O,OD</td><td>WOL power management event output, active low.
Output low if a magic packet or wake-up frame is received.</td></tr>
<tr><td>24</td><td>24</td><td>18</td><td>LED0
/PAD0
/PMEB
/INTB</td><td>LI, O,PU</td><td rowspan="2">Address and custom LED settings for the SMI management interface of the PHY.
Default LED pins are for LED functions:
PHY address selected by PAD1 and PAD0: 00000 to 00011, default 01;
Legacy LED function selection with default LED_SEL of 11:
<table>
<tr><th>LED_SEL</th><th>00</th><th>01</th><th>10</th><th>11</th></tr>
<tr><td>LED0</td><td>ACT_{ALL}</td><td>$LINK_{ALL}$ /ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{ALL}</td><td>$LINK_{10}$ /ACT_{10}</td></tr>
<tr><td>LED1</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$</td><td>$LINK_{100}$ /ACT_{100}</td></tr>
<tr><td>LED2</td><td>Reserved</td><td>Reserved</td><td>Reserved</td><td>Reserved</td></tr>
</table>
Note: The CH181H LED blinks to determine the signal is the Ethernet carrier signal.</td></tr>
<tr><td>25</td><td>25</td><td>19</td><td>LED1
/PAD1</td><td>LI, O,PD</td></tr>
</table>

Note: I = input; O = output; I/O = input/output; P = power supply;
OD = open-drain output; PD = power-on reset internal pull-low; PU = power-on reset internal pull-high;
LI = pin status detected during power-up and latching input for functional configuration.

5. Register Description

Table 5-1 PHY register description

Register name	Address	Default value
Control register	0x00	3100h
Status register	0x01	7849h
PHY Identifier	0x02/0x03	7311h/9011h
Auto-Negotiation Advertisement	0x04	01e1h
Auto-Negotiation Link Partner Ability	0x05	0000h
Auto-Negotiation Expansion	0x06	0004h

Note: 1. Please refer to *IEEE 802.3 Protocol* and *CH182DS2* manual for the above registers;

2. Please refer to *CH182DS2* manual for the extended registers.

6. Function Description

6.1 MII and Management Interface

6.1.1 Data Transfer

The Media Independent Interface MII provides a standard interface between the PHY and MAC layers. the MII operates at 25MHz or 2.5MHz frequency and supports 100Mbps and 10Mbps transmit and receive functions respectively.

Transmit:
MAC sends TXEN signal according to the transmit clock signal TXC provided by PHY and transfers the data into 4-bit parallel through TXD[3:0] to PHY. during TXEN enable, PHY will sample TXD[3:0] by TXC.
Receive:
PHY provides receive clock signal RXC, sends out RXDV signal, and converts the received data into 4-bit parallel via RXD[3:0] to MAC. crs_DV and COL signals are used for collision detection and processing. mac samples RXD[3:0] according to RXC.

6.1.2 Serial Management Interface SMI

MAC layer devices can use the MDC/MDIO management interface to control and configure PHY devices, and can control several different PHY chips by configuring the PHY address. The frame structure transmitted on the MDC/MDIO management interface is shown in the following table.

Table 6-1 Management frame format table

	Management frame fields							
	Preamble	Start	Operation	PHYAD	REGAD	TA	Data	Idle
Read	1…1	01	10	AAAAA	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write	1…1	01	01	AAAAA	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Table 6-2 Serial management frame description table

Name	Description
Preamble	MAC transmits 32 consecutive 1s and 32 MDC clock signals on MDIO for PHY synchronization.
Start	The start character of the frame is defined as 01.
Operation	Operation code. Read: 10; Write: 01.
PHYAD	PHY address, 5 bits wide, high 2 bits are always 0.
REGAD	Register address, 5 bits wide.
TA	The 2-bit steering character is used to avoid conflict during read operation. For read operation, during the 2-bit time of TA, the MAC controller keeps MDIO in high resistance state, while the PHY device keeps 1-bit high resistance state first and outputs 0 signal at the 2nd bit. During write operation, the MAC controller drives MDIO to output a 10 signal during this 2-bit time of TA, while the PHY maintains a high resistance state.
Data	16-bit data field.

Idle	The signal is in a high resistance state, and the pull-up resistor of PHY ensures that the MDIO line is at a pull-up high level.

Figure 6-1 Read cycle diagram

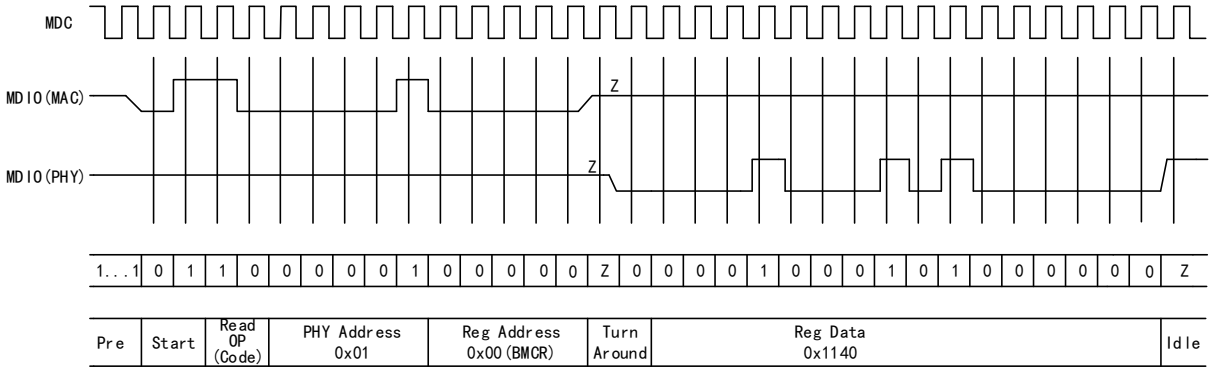
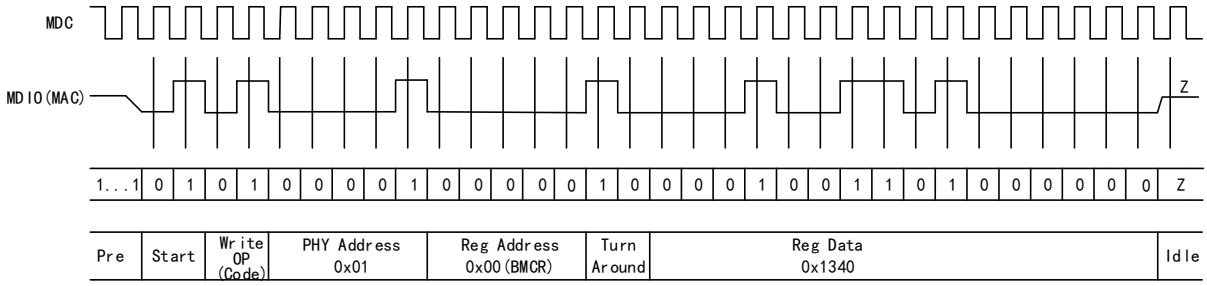


Figure 6-2 Write cycle diagram



6.2 Interrupt

When a corresponding state change is detected, PHY will output interrupt pin INTB low to generate an interrupt event. the MAC receives the state change and accesses page 0 register 30 through the MDC/MDIO interface in response.

Once the MAC reads page 0 register 30 through the MDC/MDIO, the interrupt pin INTB will end low and be pulled high by the pull-up resistor.

Note: 1. RXD[2]/INTB pin is only used for interrupt function in RMII mode.

2. Interrupt function is disabled by default, please refer to page 7 register 19-bit 13~bit 11 to enable interrupt function.

6.3 Auto-negotiation and Parallel Detection

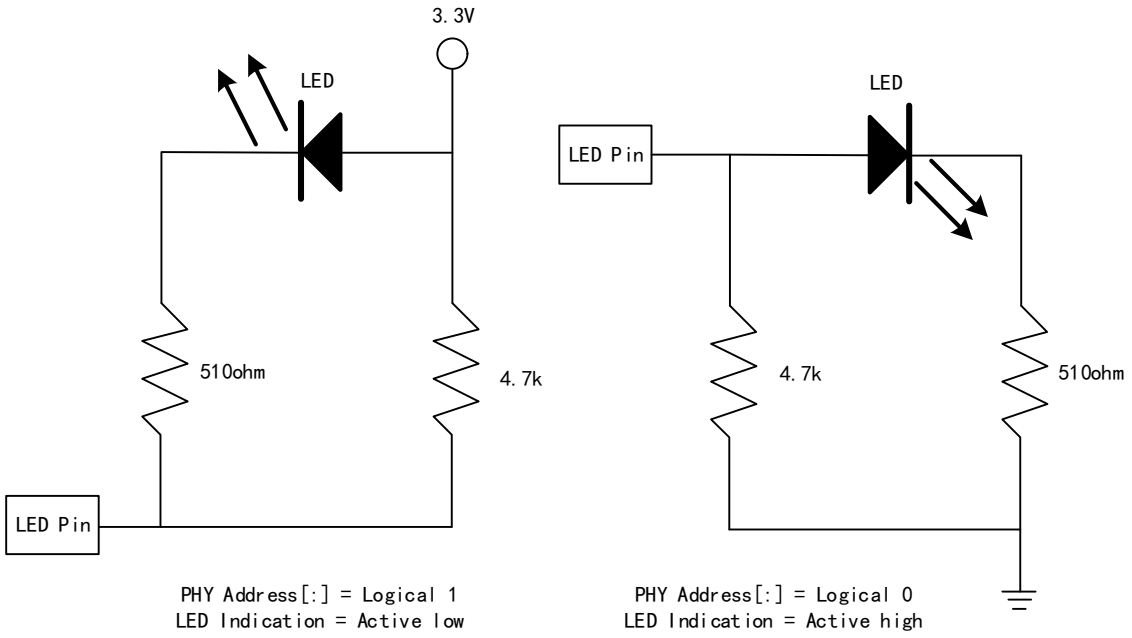
CH182 supports IEEE 802.3u protocol and is compatible with other Ethernet transceiver Transceivers that support auto-negotiation. CH182 can automatically detect the network connection and determine the highest possible speed and duplex configuration between two devices. If the peer does not support auto-negotiation, the CH182 will enable half-duplex mode and enter parallel detection mode. the CH182 will send a fast link pulse FLP by default and wait for the peer to respond, if FLP is received, the auto-negotiation process will continue; if a normal link pulse NLP is received or a 100Mbps IDLE signal is received, the CH182 will negotiate through parallel detection to 10Mbps half-duplex mode or 100Mbps half-duplex mode.

6.4 LED Function

6.4.1 LED and PHY Address

Since the PHY address configuration shares pins with LEDs, the external combination of PHY address and LED usage must be considered to avoid conflicts. Specifically, when using the LED pin to drive the LED directly, its PHY address depends on the input level of the PAD1/PAD0 pin during power-up. The default PAD1 has an internal pull-down resistor and PAD0 has an internal pull-up resistor, and the corresponding default PHY address is 00001. As shown in Figure 6-3 below, if the PAD1 pin is connected to an external pull-up resistor, the LED1 drive output is active low (left figure); if the PAD0 pin is connected to an external pull-down resistor, the LED0 drive output is active high (right figure). Pull high or pull low. If LED indication is not required, the LED and its current limiting resistor (330Ω ~ 820Ω) can be removed.

Figure 6-3 LED and PHY address configuration diagram



6.4.2 Link Monitor

The link monitor detects link integrity, such as LINK10, LINK100, LINK10/ACT, or LINK100/ACT. The specified link LED pin is driven to an active level whenever the link status is established; once the cable is disconnected, the link LED pin is driven to an inactive level, indicating that there is no network connection.

6.4.3 LED Indication

In 10/100M mode, the RX LED blinks to indicate that data is being received.
In 10/100M mode, the TX LED blinks to indicate that data is being sent.
In 10/100M mode, the TX/RX LED blinks to indicate that data is being sent or received.
In 10/100M mode, the LINK/ACT LED blinks to indicate a successful connection. When this LED is on for a long time, it indicates that there is a connection problem.
The LED customization function is supported in 10/100M mode and can be enabled or disabled via page 7 register bit 19 [3].

6.5 Power-down Low-power Mode

Table 6-3 Low power mode configuration

Mode	Description
PWD	Set bit 11 of register 0 to 1 to put the PHY into power-down mode PWD. In PWD mode, PHY will turn off all analog/digital functions except MDC/MDIO management interface. In PWD mode, MAC wakes up PHY via MDC/MDIO, note that PHY does not provide clock at this time.

6.6 10M/100M Transmit and Receive

6.6.1 100BASE-TX Transmit and Receive

100BASE-TX transmit.
The 4-bit data TXD[3:0] to be sent is encoded by 4B/5B and transmitted through the 25MHz TXC clock signal, which is sent to the linear driver output after parallel-serial conversion.

100BASE-TX receive.
The received signal is compensated by the adaptive equalizer, processed by the ADC module and DSP module, sent to the serial-parallel converter module, and then passed to the MII or RMII interface after 5B/4B decoding.

6.6.2 10BASE-T Transmit and Receive

10BASE-T transmit.
The 4-bit data TXD[3:0] to be sent is transmitted through the TXC signal at 2.5MHz, encoded, and fed to the 10M waveform generator to drive the output of the linear driver module.

10BASE-T receive.
The received signal is passed through the 10M receiver and the data is restored and passed to the MII or RMII interface.

6.7 Automatic Polarity Correction

Automatic correction of polarity errors for receive pairs in 10BASE-T mode and no consideration of polarity in 100BASE-TX mode. In 10BASE-T mode, polarity errors are corrected by detecting validly spaced link pulses. Detection starts with the MDI cross-detection phase and is locked when the 10BASE-T link is connected. The polarity state is unlocked when the link is disconnected.

6.8 Wake-on-LAN (WOL)

6.8.1 Magic Package and Wake-up Frame Format

The CH182 can monitor the network for wake-up frames or magic packets and output low on receipt of such packets or wake-up events via the power management event pin PMEB (where B indicates low active) to wake up the system,

and then the MAC and system can return to a normal state to handle subsequent work. the PMEB pin needs to be pulled high to the supply voltage via a 4.7KΩ resistor, which defaults to high level.
The magic packet wake-up will be triggered only when the following conditions are met:

- The destination address of the received magic packet is recognizable by the CH182. For example, with the device MAC address as the destination address;
- The received magic packet does not contain CRC errors;
- Magic packet pattern match. For example, any part of the packet contains: 6*FFh+MISC (optional) + 16*DID (destination ID).

A wake-up frame event occurs only when the following conditions are met:

- The destination address of the received wake-up frame is recognizable by the CH182, e.g., with the device MAC address as the destination address;
- The received wake-up frame does not contain CRC errors;
- The 16-bit CRC of the received wake-up frame matches the 16-bit CRC sample of the local wake-up frame, which can also be configured to allow direct group wake-up.

6.8.2 Wake-on-LAN with Low Level Output

When PHY receives a wake-up frame or magic packet from the opposite end, the PMEB pin outputs a low active level and the MAC or system recognizes the low level and wakes up. the PMEB pin is set by the system or MAC to restore the high level.

6.8.3 Wake-on-LAN with Low Level Pulse Output

When the PHY receives a wake-up frame or magic packet from the other side, the PMEB pin will output low for a selectable period of time and the MAC or system wakes up after recognizing the low level pulse.

6.8.4 Wake-on-LAN Pin Type (MII mode)

Name	Type	Normal			Enable WOL
		100M	10M	Idle	
TXC	O/PD	25MHz output	2.5MHz output	2.5MHz output	O(2.5M/25M)/L/PD[1]
TXEN	I/PD	I	I	I	I/PD
TXD[3:0]	I/PD	I	I	I	I/PD
RXC	O/PD	25MHz output	2.5MHz output	2.5MHz output	O(2.5M/25M)/L/PD[2]
COL	O/PD	O	O	O	O/L/PD[3]
CRS_DV	O/PD	O	O	O	O/L/PD[3]
RXDV	O/PD	O	O	O	O/L/PD[3]
RXD[0]	O/PD	O	O	O	O/L/PD[3]
RXD[1]	O/PD	O	O	O	O/L/PD[3]
RXD[2]	LI/O/PD	O	O	O	O/L/PD[3]
RXD[3]	O/PD	O	O	O	O/L/PD[3]
RXER	O/PD	O	O	O	O/L/PD[3]
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 1: Setting Isolate = 1 (register 0 bit 10) will suspend TXC with pin type L.
Note 2: Setting Isolate = 1 (register 0 bit 10) will suspend RXC with pin type L.
Note 3: Setting Isolate = 1 (register 0 bit 10) will suspend RX all interface signals with pin type L.

6.8.5 Wake-on-LAN Pin Type (RMII mode)

Name	Type	Normal			Enable WOL
		100M	10M	Idle	
TXC (REFCLK)[4]	IO/PD	50MHz Input/output	50MHz Input/output	50MHz Input/output	I/O(50M)[4]
TXEN	I/PD	I	I	I	I/PD
TXD[0:1]	I/PD	I	I	I	I/PD
CRS_DV	O/PD	O	O	O	O/L/PD[3]
RXD[0]	LI/O/PD	O	O	O	O/L/PD[3]
RXD[1]	O/PD	O	O	O	O/L/PD[3]
RXER	O/PD	O	O	O	O/L/PD[3]
MDC	I/PU	I	I	I	I/PU
MDIO	IO/PU	IO	IO	IO	IO/PU

Note 4: Setting Isolate = 1 (register 0 bit 10) will suspend TXC with pin type L;
If TXC/REFCLK is in input mode (MAC to PHY), then REFCLK cannot be suspended while WOL is enabled;
if TXC/REFCLK is in output mode (PHY to MAC), then REFCLK is not recommended to be suspended;
Note 3: Setting Isolate = 1 (register 0 bit 10) will suspend RX all interface signals with pin type L.

7. Electrical Characteristics

7.1 Absolute Maximum Value

(Critical or exceeding the absolute maximum value will likely cause the chip to work improperly or even be damaged)

Table 7-1 Absolute maximum parameter table

Symbol	Parameter		Min.	Typ.	Max.	Unit
AVDD33	Supply voltage		-0.4	3.3	4.0	V
AVDDK	Internal analog power supply LDO decoupling terminal voltage		-0.2		1.8	V
DVDDK	Internal digital power supply LDO decoupling terminal voltage		-0.2		1.8	V
VDDIO	Interface I/O pin supply voltage		-0.4		4.0	V
V_{IO}	Control the voltage on the interface pins (VIO power)		-0.4		VIO+0.4	V
V_{IOX}	Voltage on Ethernet pins (AVDD33 power supply)		-0.4		AVDD33+0.4	V
T_s	Storage temperature range		-65		+150	℃
T_J	Junction temperature range		-40		+125	℃
T_A	Ambient temperature	CH182	-40		+85	℃
		CH181H	-10		70	

7.2 Operating Voltage and DC Characteristics

Table 7-2 DC Characteristics Parameter Table (AVDD33=3.3V，VIO=3.3V，TA=25℃)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AVDD33	Supply voltage	AVDD33 pin	3.2	3.3	3.45	V
VDDIO	Interface I/O pin supply voltage	VDDIO pin	2.3	3.3	3.5	V
V_{IL}	Input low voltage		0	-	0.8	V
V_{IH}	Input high voltage		2.0	-	VIO	V
I_{IL}	Input low leakage current	Input voltage 0V	-5		5	uA
I_{IH}	Input high leakage current	Input voltage VIO	-5		5	uA
V_{OL}	Output low voltage	IOL = 8mA	-	-	0.4	V
V_{OH}	Output high voltage	IOH = -8mA	VIO-0.4	-	-	V
Rpu	Resistance value of the built-in pull-up resistor		35	60	100	KΩ
Rpd	Resistance value of the built-in pull-down resistor		35	60	100	KΩ
V_{LVR}	Voltage threshold for power supply low voltage reset		2.7	2.9	3.1	V

7.3 Supply Current Characteristics

Table 7-3 Current consumption Table (AVDD33=3.3V，VIO=3.3V，TA=25℃)

Symbol	Parameter	Condition (All currents, including network transformers)	Typ.		Unit
			MII mode	RMII mode	
I_{DD}	100BASE-TX	Transfer status	60.0	60.4	mA
		Idle status	61.2	61.4	
	10BASE-T	Transfer status	28.8	34.2	mA
		Idle status	25.8	28.1	
	Link Down	Disconnected status	38.5	38.4	mA
	Power Down	Shutdown status	0.2	0.2	

7.4 Power-on Timing

Figure 7-1 Power-on timing diagram

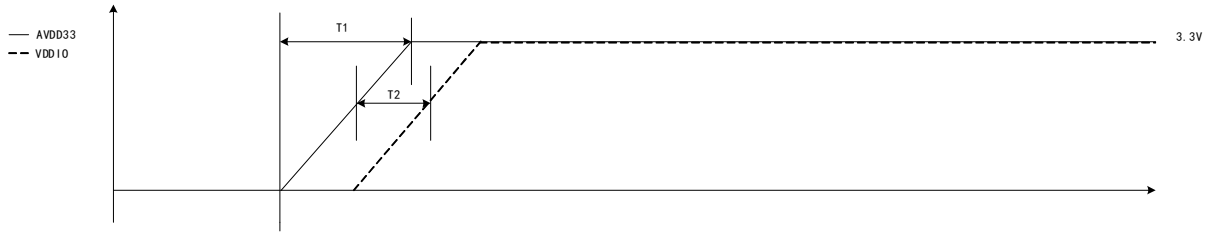
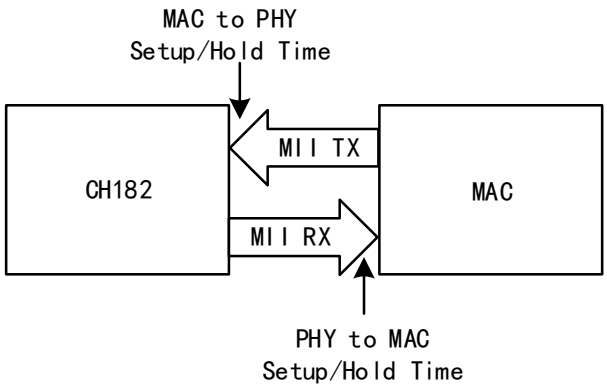


Table 7-4 Power-on timing table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Voltage rise time when AVDD33 is powered on	1		10000	us
T2	Delay time of VDDIO power supply relative to AVDD33 power supply	0	0	1	ms
Tpor	Power-on reset time of PHY chip (PHY accessible thereafter)	15	17	20	ms
Trst	Reset time after RSTB low pulse (PHY accessible thereafter)	1		4	ms

7.5 MII Transmit Cycle Timing

Figure 7-2 MII interface setting/holding time diagram



The packet sending process from MAC to PHY on the MII interface is as follows:

Figure 7-3 Timing diagram of MII transmit cycle

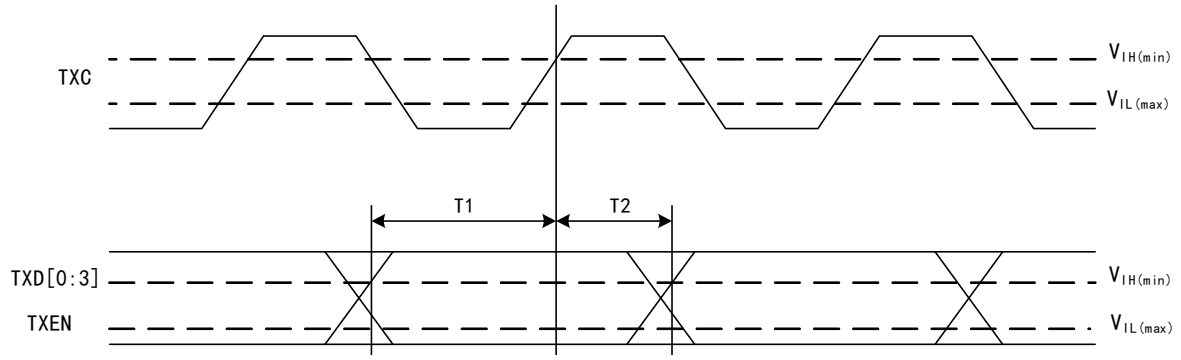


Table 7-5 MII transmission cycle timing table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T1	TXEN, TXD[0:3] build to TXC rising edge	100Mbps	7			ns
		10Mbps	5			ns
T2	TXEN, TXD[0:3] is held after the rising edge of TXC	100Mbps	0			ns
		10Mbps	0			ns

7.6 MII Receive Cycle Timing

The packet sending process from PHY to MAC on MII interface is as follows.

Figure 7-4 Timing diagram of MII receive cycle

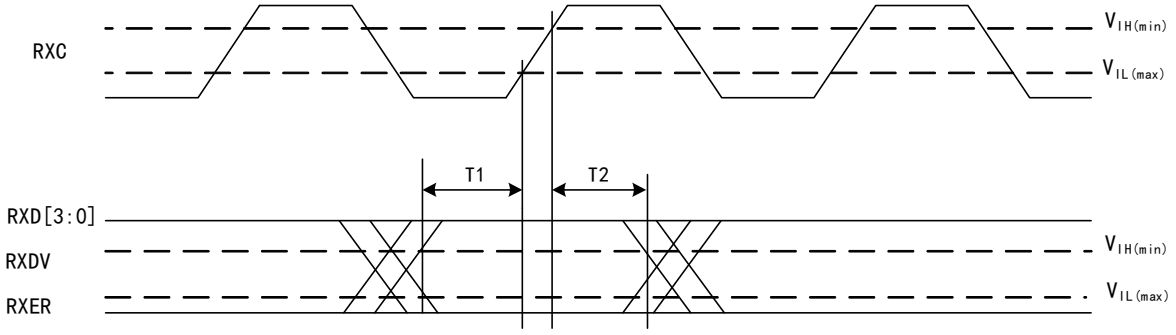


Table 7-6 MII reception cycle timing table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
T1	RXER, RXDV, RXD[0:3] established to RXC rising edge	100Mbps	5			ns
		10Mbps	5			ns
T2	RXER, RXDV, RXD[0:3] are held after the rising edge of RXC	100Mbps	10			ns
		10Mbps	10			ns

7.7 RMII Transmit and Receive Cycle Timing

Figure 7-5 Schematic diagram of RMII interface settings, hold time and output delay time

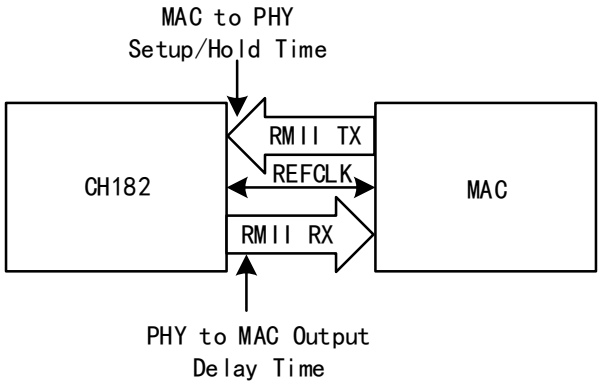


Figure 7-6 Timing diagram of RMII transmit and receive cycles

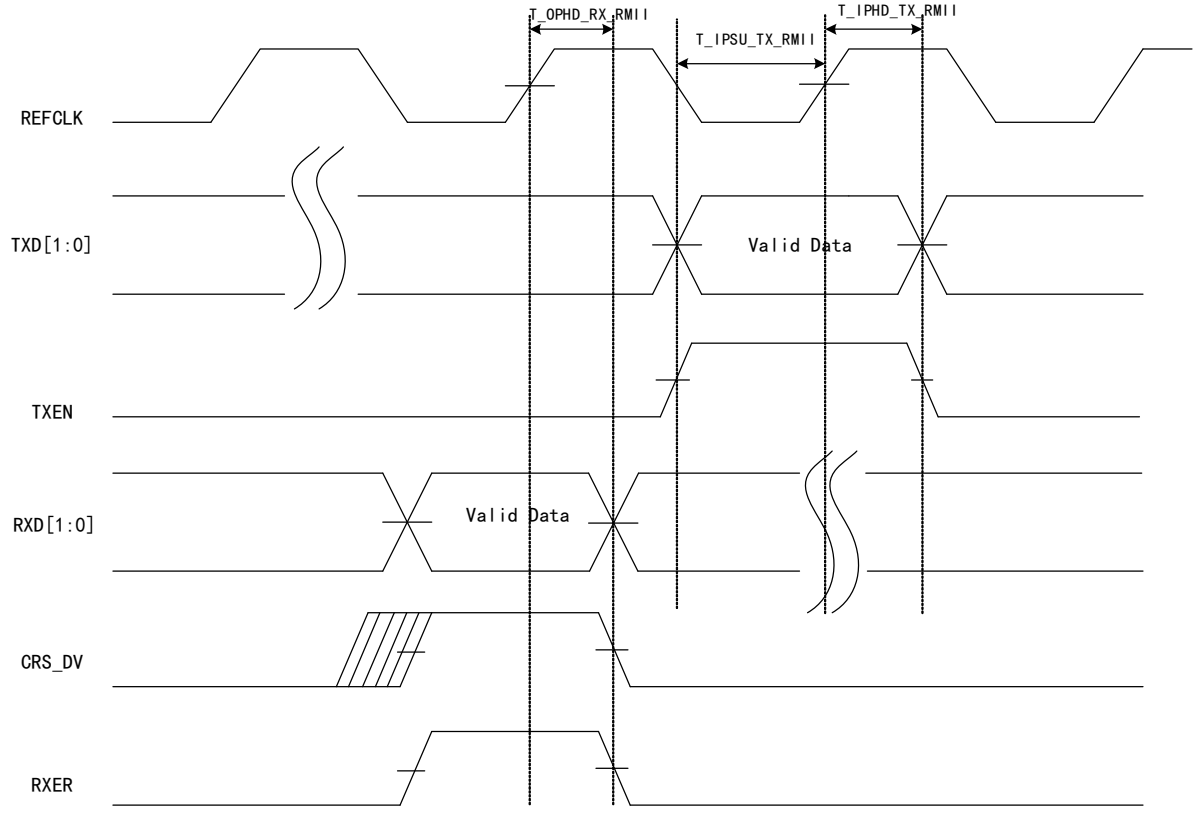


Table 7-7 Timing table of RMII transmission and reception cycles

Symbol	Parameter	Condition	Min.	Typ.	Max.
REFCLK Frequency	Reference clock frequency		50		MHz
REFCLK Duty Cycle	Duty cycle of the reference clock	40		60	%
T_IPSU_TX_RMII	TXD[1:0]/TXEN build time to REFCLK	5			ns
T_IPHD_TX_RMII	TXD[1:0]/TXEN hold time from REFCLK	2			ns
T_OPHD_RX_RMII	RXD[1:0]/CRS_DV/RXER delay time from REFCLK output	2			ns

Note:1. RMII TX timing can be adjusted by 16 bits [11:8] of page 7 register, adjustable resolution is about 1.5ns, default value is recommended;

2. RMII RX timing can be adjusted by page 7 register 16 bits [7:4], adjustable resolution is about 1.5ns, we suggest using the default value.

7.8 MDC/MDIO Timing

Figure 7-7 MDC/MDIO interface settings, hold time and effective time from MDC rising edge

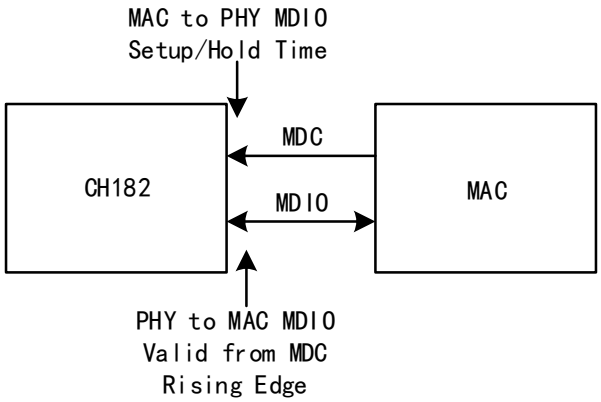


Figure 7-8 MDC/MDIO timing

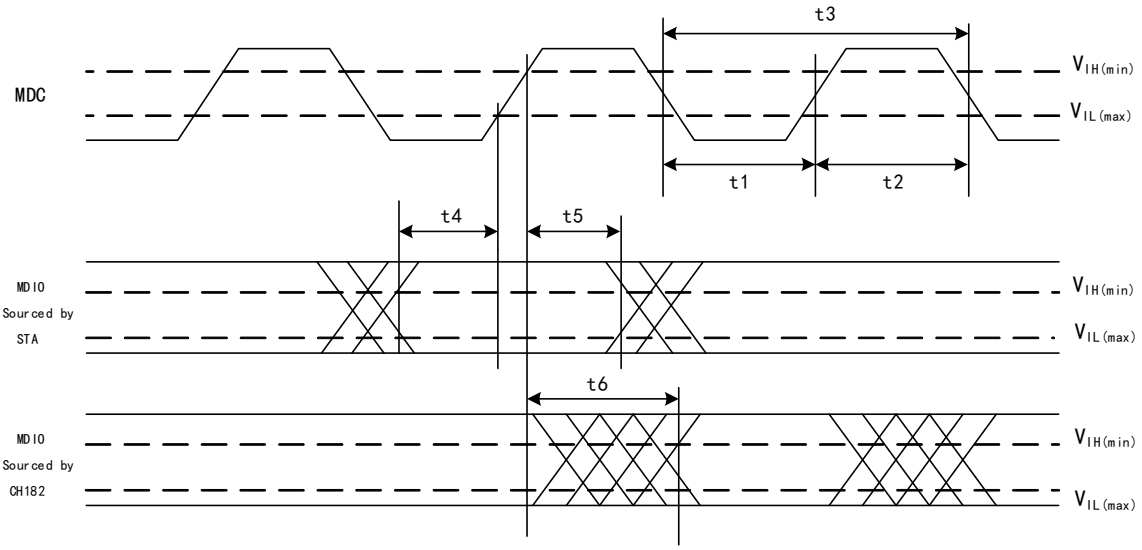


Table 7-8 MDC/MDIO timing table

Symbol	Parameter	Min.	Typ.	Max.	Unit
t1	MDC high pulse width	100			ns
t2	MDC low pulse width	100			ns
t3	MDC cycle	200			ns
t4	MDIO build to MDC rising edge	10			ns
t5	MDIO hold time from the rising edge of MDC	10			ns
t6	MDIO on the rising edge of MDC is valid	0	180		ns

7.9 Crystal Oscillator/clock Characteristics

Table 7-9 Crystal oscillator/clock characteristics table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TCKF	Crystal frequency	Recommended 20ppm	24.9995	25	25.0005	MHz
TPWH	OSC high pulse width	-	15	20	25	ns
TPWL	OSC low pulse width	-	15	20	25	ns

Note: The XI and XO pins already have the two oscillation capacitors required for an external crystal with a load capacitance of 12pF respectively, and only the crystal is required externally.

If an external crystal with a load capacitance of 20pF is selected, then XI and XO need to add an additional 15pF oscillation capacitor to ground respectively.

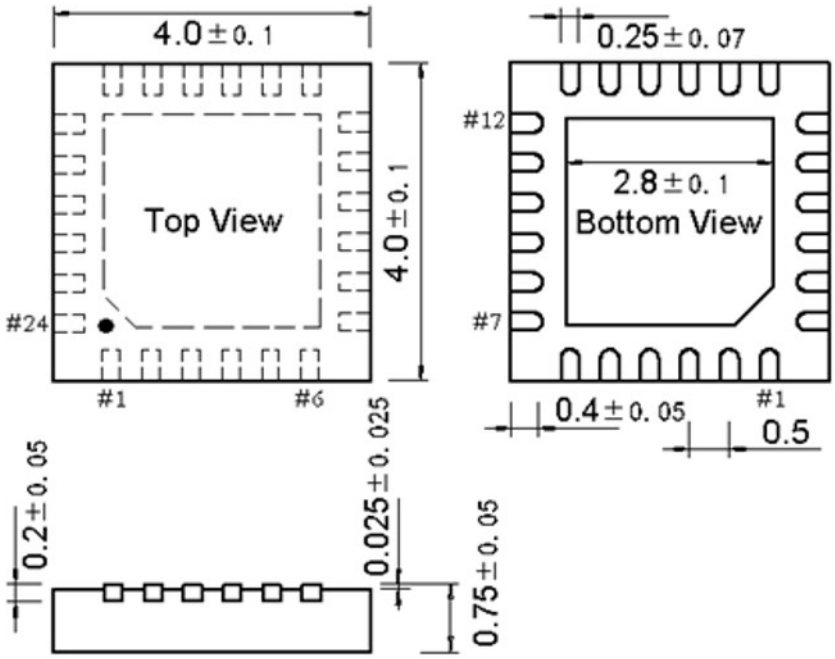
When the XI is connected to GND, it can support 25MHz or 50MHz external clock input from the XO pin.

8. Package

Note: The unit of dimensioning is mm (millimeter).

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2m.

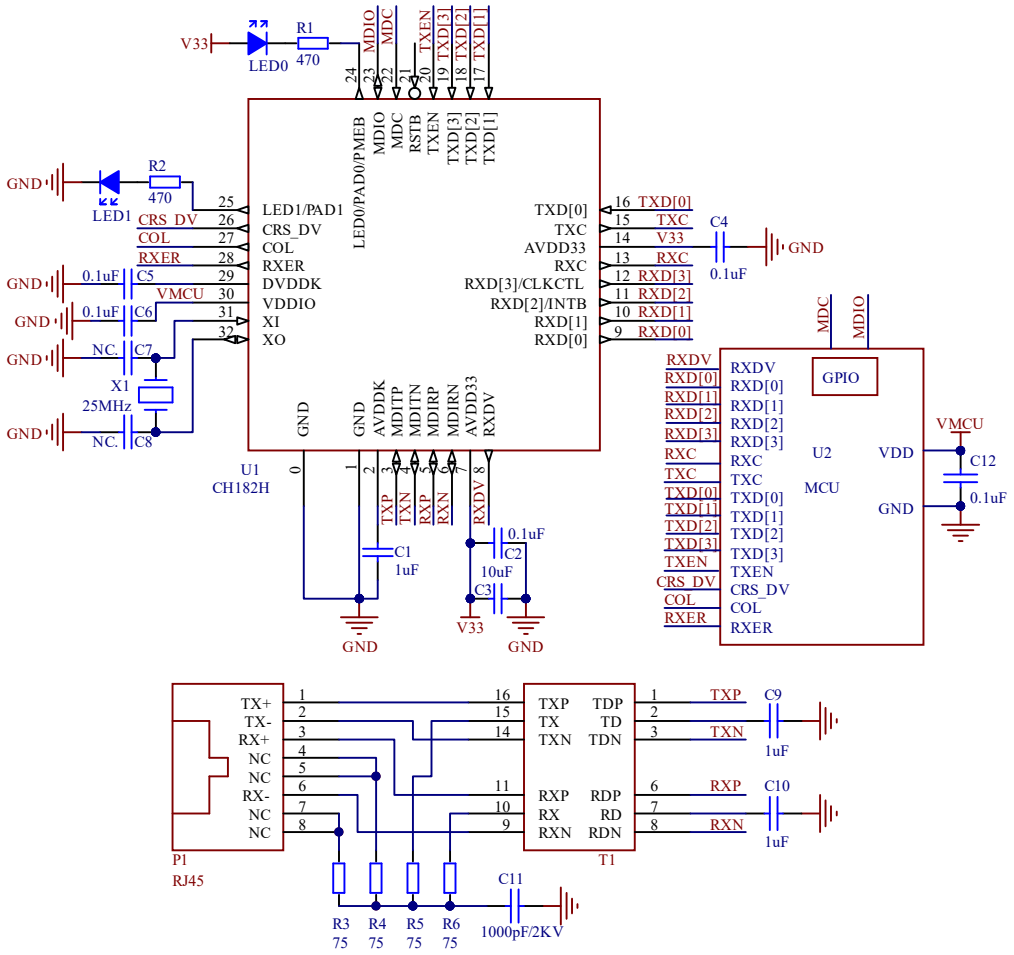
8.1 QFN24-4*4 Package



8.2 QFN32-5*5 Package

9. Application

9.1 MII Interface Application



CH182 has built in part of the oscillation capacitance of crystal X1, and C7 and C8 can be adjusted according to the crystal parameters. For the load capacitance of

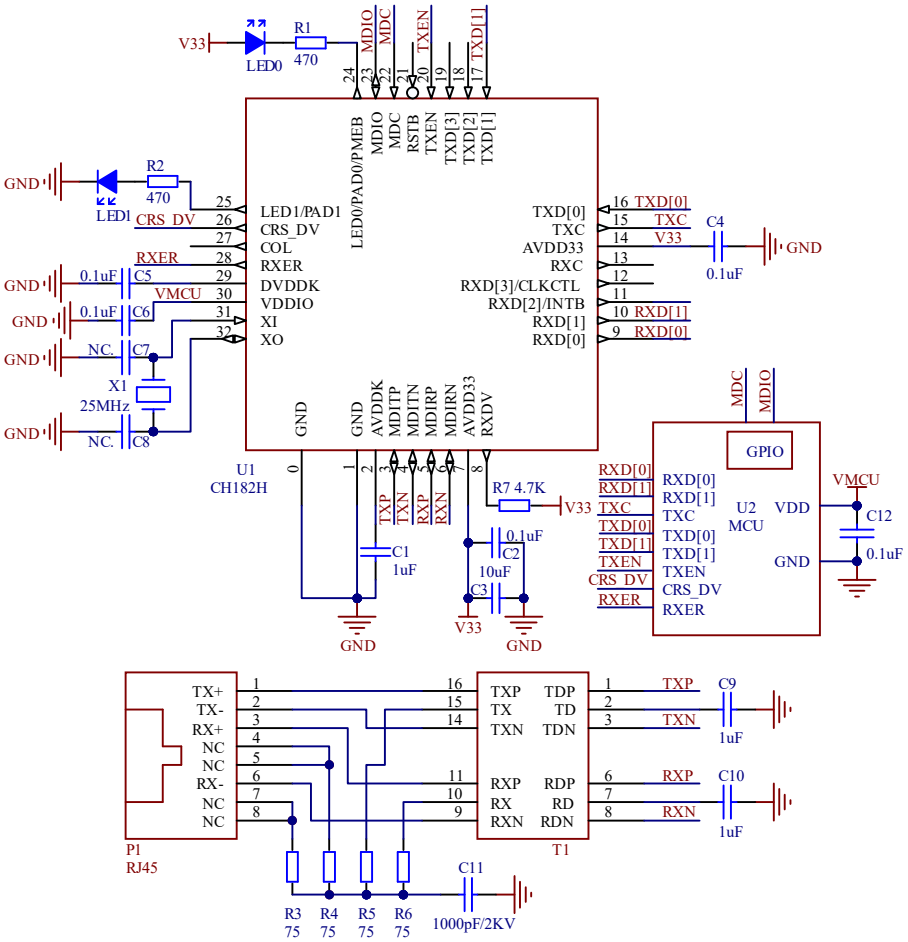
For X1 with a load capacitance of 12pF, C7 and C8 are not needed; for X1 with a load capacitance of 20pF, C7 and C8 are recommended to be 15pF each.

T1 is ethernet network transformer, its center tap is grounded through capacitor C9/C10 respectively, do not connect any power supply.

CH182 has built-in Ethernet 50Ω impedance matching resistor, do not connect 49.9Ω or 50Ω resistor externally, equivalent to voltage drive.

CH182 supports network transformer free, capacitor isolated Ethernet applications.

9.2 RMII Interface Application



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