FEATURES

- Implements CAN 2.0B at 1.0Mb/s:
  0-8 byte length data field
  Standard and extended data and remote frames
- Receive buffers, masks and filters:
  Two receive buffers with storage prioritized message storage
  Six 29-bit filters
  Two 29-bit masks
- Data byte filtering on the first two data bytes
- Three transmit buffers with prioritization and abort features the transmittance
- High-speed SPI Interface (10 MHz)
  SPI modes 0.0 and 1.1
- One-shot mode ensures message transmission is attempted only one time
- Clock out pin with programmable prescaler:
- Start-of-Frame (SOF) signal is available for monitoring the SOF signal
- Interrupt output pin INT with interrupt enable
- Buffer Full output pins can be configured as
  Interrupt output for each receive buffer
  General purpose outputs
- Request-to-Send (RTS) input pins individually can be configured as:
  Control pins to request transmission for each transmit buffer
  General purpose inputs
- Low-power CMOS technology:
  Operates from 4.5V to 5.5V
  5mA dynamic current (typical)
  1μA standby current (typical) (Sleep mode)
- Support temperature range:
  Industrial: -40℃-85℃

PRODUCT APPEARANCE

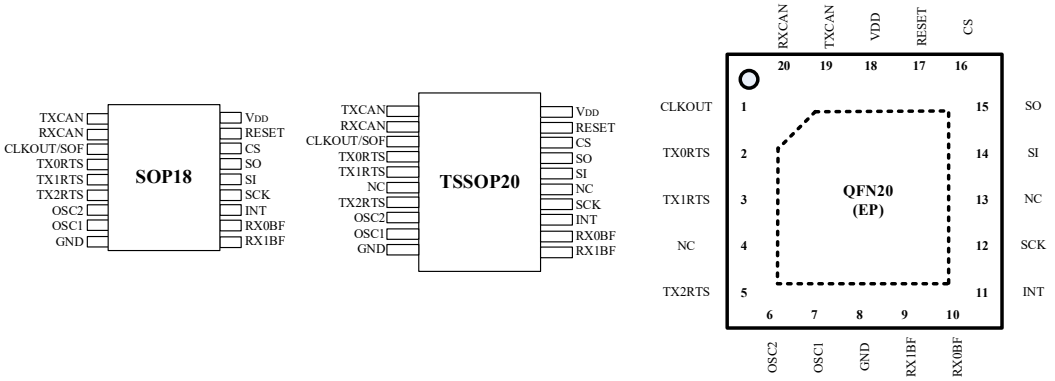
Provide environmentally friendly lead-free package

DESCRIPTION

The SIT2515 is a stand-alone Controller Area Network (CAN) controller that implements the CAN specification, version 2.0B. The chip is mainly used in automotive and industrial applications for data receiving and transmission.

It is capable of transmitting and receiving both standard and extended data and remote frames. The SIT2515 has two acceptance masks and six acceptance filters that are used to filter out unwanted messages, thereby reducing the host MCUs overhead. The SIT2515 communicates with MCU through the industry-standard SPI interface.

PIN CONFIGURATION



Note: EP (Exposed Pad), recommended grounding.

PIN DESCRIPTION

SOP18	TSSOP20	QFN20	Symbol	Description	Spare pin function
1	1	19	TXCAN	Transmit output pin to CAN bus.	
2	2	20	RXCAN	Receive input pin from CAN bus.	
3	3	1	CLKOUT/SOF	Clock output pin with programmable prescaler.	Start-of-Frame signal
4	4	2	TX0RTS	Transmit buffer TXB0 request-to-send. 100 kΩ internal pull-up to VDD.	General digital signal input, 100 kΩ internal pull-up to VDD.
5	5	3	TX1RTS	Transmit buffer TXB1. request-to-send. 100 kΩ internal pull-up to VDD.	General digital signal input, 100 kΩ internal pull-up to VDD.

SOP18	TSSOP20	QFN20	Symbol	Description	Spare pin function
	6, 15	4, 13	NC	No internal connection.	
6	7	5	TX2RTS	Transmit buffer TXB2 request-to-send. 100 kΩ internal pull-up to VDD.	General digital signal input, 100 kΩ internal pull-up to VDD.
7	8	6	OSC2	Oscillator output (Quartz resonator connection).	
8	9	7	OSC1	Oscillator input (Quartz resonator or external clock connection).	External clock input.
9	10	8	GND	Ground.	
10	11	9	RX1BF	Receive buffer RXB1 interrupt pin or general purpose digital output.	General purpose digital output.
11	12	10	RX0BF	Receive buffer RXB0 interrupt pin or general purpose digital output.	General purpose signal output.
12	13	11	INT	Interrupt output pin.	
13	14	12	SCK	SPI Clock input pin for SPI interface.	
14	16	14	SI	Data input pin for SPI interface.	
15	17	15	SO	Data output pin for SPI interface.	
16	18	16	CS	Chip select input pin for SPI interface.	
17	19	17	RESET	Active low device reset input.	
18	20	18	V_{DD}	Positive supply for logic and I/O pins.	

Note:
1 CAN-Controller Area Network
2 SPI-Serial Peripheral Interface

LIMITING VALUES

Parameter	Symbol	Value		Unit
		Min	Max	
Supply voltage	VCC		7	V
Input voltage (all pins)	VI	-0.6	VCC+1.0	V
Input voltage for RXCAN, CS, TXnRTS, SCK, SI pins at functional check mode	VI	-0.6	VCC+1.0	V
Ambient (storage) temperature	Ta	-60	125	℃

The maximum limit parameters mean that exceeding these values may cause irreversible damage to the device. Under these conditions, it is not conducive to the normal operation of the device. The continuous operation of the device at the maximum allowable rating may affect the reliability of the device. The reference point for all voltages is ground.

RECOMMENDED OPERATION MODES

Parameter	Symbol	Value		Unit
		Min	Max	
Supply voltage	VCC	4.5	5.5	V
Input voltage (all pins)	VI	0	VCC	V
Input voltage for RXCAN, CS, TXnRTS, SCK, SI pins at functional check mode	VI	-0.3	VCC+1.0	V
Ambient (operating) temperature	Ta	-40	85	℃

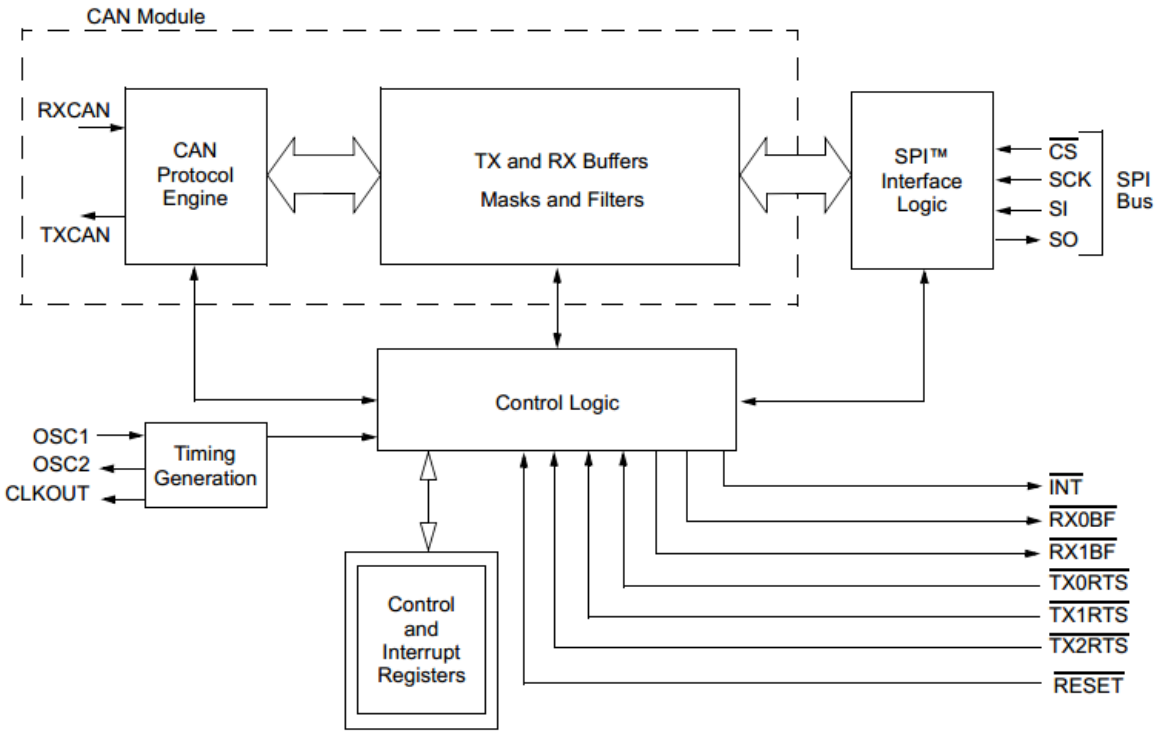


Fig 2 Block diagram

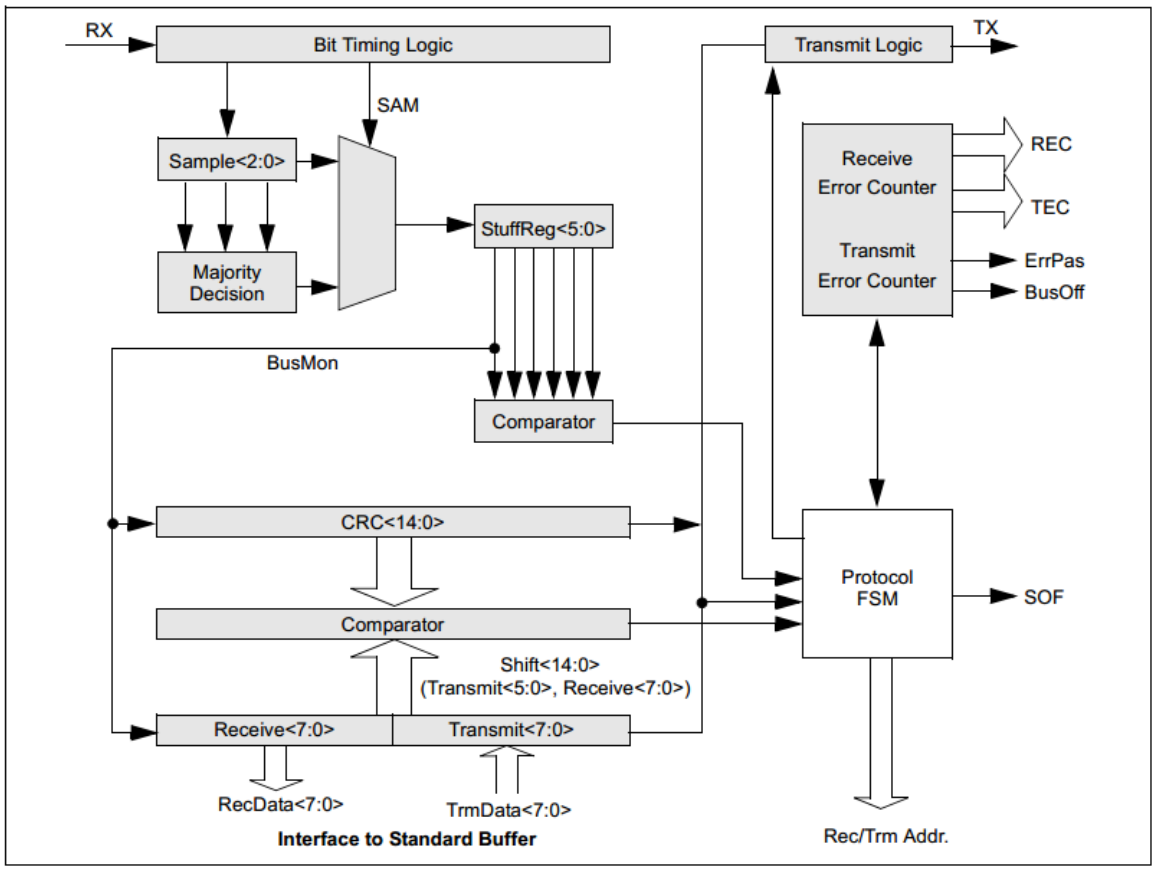


Fig 3 CAN core module block diagram

SIT2515 has three transmit and two receive buffers, two receive masks (one for each receive buffer), and a total of six receive filtering registers. Fig 4 shows a block diagram of these buffers and their connection to the core module of the CAN protocol:

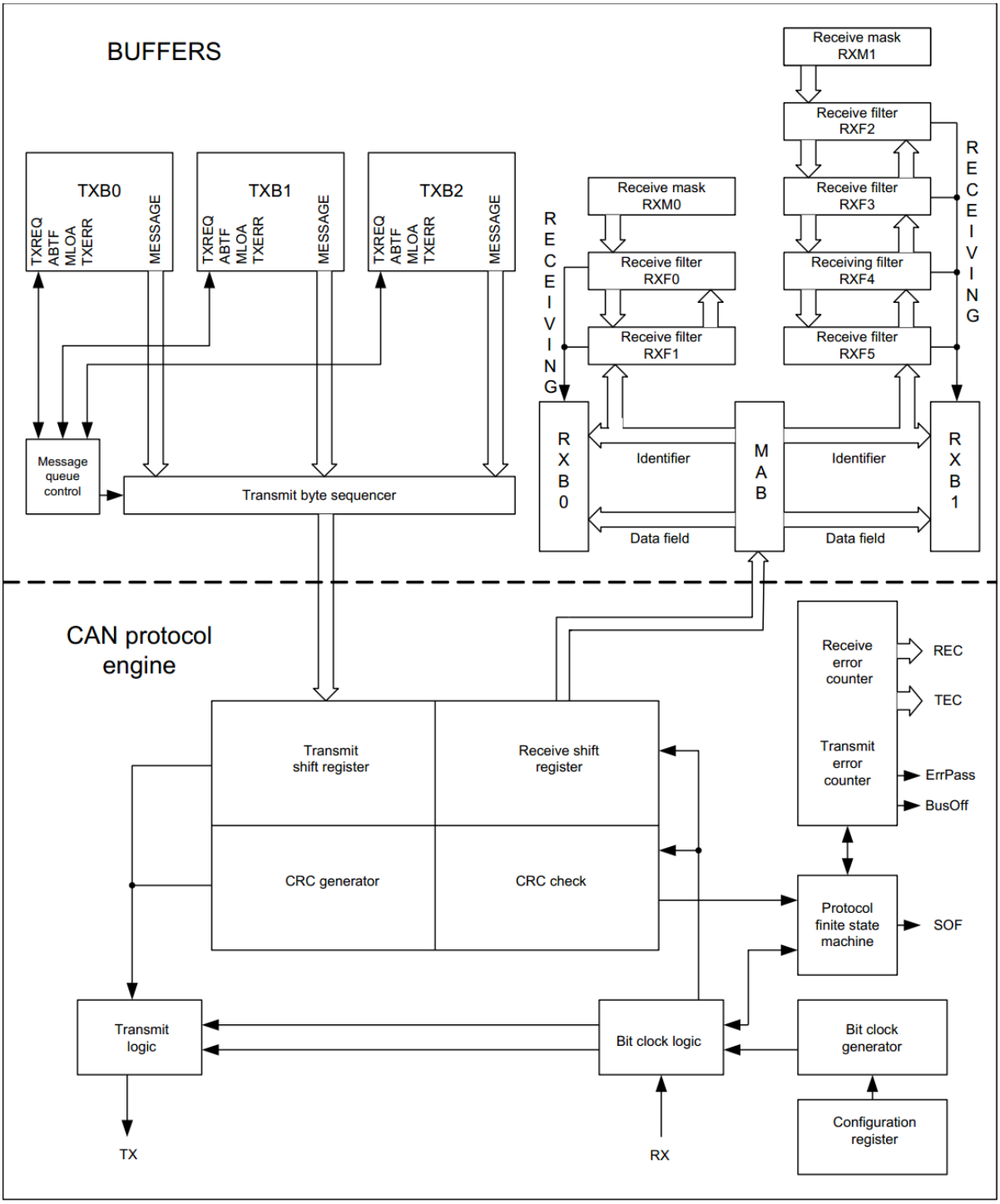


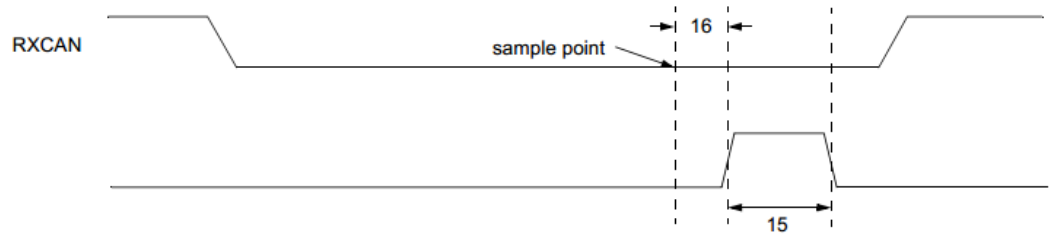
Fig 4 Block diagram of internal buffers and protocol core module

DC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Supply voltage	VDD		4.5		5.5	V
Register retention voltage	V_{RET}		2.4			V
High-level input voltage RXCAN	V_{IH1}		2		VDD+1	V
High-level input voltage SCK, CS, SI, TXnRTS	V_{IH2}		0.7VDD		VDD+1	V
High-level input voltage OSC1	V_{IH3}		0.85VDD		VDD	V
High-level input voltage RESET	V_{IH4}		0.85VDD		VDD	V
Low-level input voltage RXCAN	V_{IL1}		-0.3		0.15VDD	V
Low-level input voltage SCK, CS, SI, TXnRTS	V_{IL2}		-0.3		0.4	V
Low-level input voltage OSC1	V_{IL3}		VSS		0.3VDD	V
Low-level input voltage RESET	V_{IL4}		VSS		0.15VDD	V
Low-level output voltage TXCAN pin	V_{OL1}	I_{OL}=0.6mA V_{CC}=4.5V			0.6	V
Low-level output voltage RXnBF pin	V_{OL2}	I_{OL}=8.5mA V_{CC}=4.5V			0.6	V
Low-level output voltage SO, CLKOUT pins	V_{OL3}	I_{OL}=2.1mA V_{CC}=4.5V			0.6	V

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Low-level output voltage INT pin	V_{OL4}	I_{OL}=1.6mA V_{CC}=4.5V			0.6	V
High-level output voltage TXCAN pin	V_{OH1}	I_{OH}=-3.0mA V_{CC}=4.5V	3.8			V
High-level output voltage RXnBF pin	V_{OH2}	I_{OH}=-3.0mA V_{CC}=4.5V	3.8			V
High-level output voltage SO, CLKOUT pins	V_{OH3}	I_{OH}=--400uA V_{CC}=4.5V	4.0			V
High-level output voltage INT pin	V_{OH4}	I_{OH}=-1.0mA V_{CC}=4.5V	3.8			V
Low-level input leakage current RXCAN, SCK, SI, CS, RESET pins	I_{ILL1}	V_{IN}=0.0V V_{CC}=5.5V V_{CS}=V_{RESET}=5.5V			|-1|	µA
Low-level input leakage current OSC1 pin	I_{ILL2}				|-5|	
Low-level input leakage current SO, CLKOUT/SOF, RX0BF, RX1BF pins	I_{OLL1}				|-1|	
High-level input leakage current RXCAN, SCK, SI, CS, RESET pins	I_{ILH1}	V_{IN}=5.5V V_{CC}=5.5V V_{CS}=V_{RESET}=5.5V			1	µA
High-level input leakage current OSC1 pin	I_{ILH1}				5	
High-level output leakage current	I_{OLH1}				1	
Operating consumption current	I_{IOCC}	F_{OSC}=25MHz V_{CC}=5.5V			10	mA
Standby consumption current	I_{CCS}	V_{IN}=5.5V, V_{CC}=5.5V V_{CS}=V_{RESET}=5.5V			5	µA

AC CHARACTERISTICS

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
CAN-interface						
Wake-up noise filter	t_{WF}	V_{CC}=5.5V	100			ns
RESET pin						
RESET pin low time	t_{rl}	V_{CC}=2.7V	2			μs
CLKOUT pin						
CLKOUT pin high time	t_hCLKOUT	T_{OSC}=40ns	15			ns
CLKOUT pin low time	t_lCLKOUT	T_{OSC}=40ns	15			ns
CLKOUT pin rise time	t_rCLKOUT	0.3VDD-0.7VDD			5	ns
CLKOUT pin fall time	t_fCLKOUT	0.7VDD-0.3VDD			5	ns
CLOCKOUT propagation delay	t_dCLKOUT	In the sampling points measured, device as the receiving node and six points for frequency			100	ns
Start-Of-Frame high time 15	t_hSOF				$2T_{OSC}$	ns
Start-Of-Frame propagation delay 16	t_dSOF				$2T_{OSC}$+0.5T_Q	ns
						
SPI -interface						
Clock frequency	f_{CLK}				10	MHz
CS setup time	t_{CSS}		50			ns
CS hold time	t_{CSH}		50			ns
CS disable time	t_{CSD}		50			ns

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNIT
Data setup time (SI pin)	t_{SU}		10			ns
Data hold time (SI pin)	t_{HD}		10			ns
Clock high time	t_{HI}		45			ns
Clock low time	t_{LO}		45			ns
Clock delay time	t_{CLD}		50			ns
Clock enable time	t_{CLE}		50			ns
Output valid from clock low	t_V				45	ns
Output hold time (SO pin)	t_{HO}		0			ns
Output disable time (SO pin)	t_{DIS}				100	ns

ADDITIONAL DESCRIPTION

1 High-speed SPI interface

The SIT2515 is designed to interface directly with the Serial Peripheral Interface (SPI) port available on many microcontrollers and supports Mode 0.0 and Mode 1.1. Commands and data are sent to the device via the SI pin, with data being clocked in on the rising edge of SCK. Data is driven out by the SIT2515 (on the SO line) on the falling edge of SCK. The CS pin must be held low while any operation is performed.

The SIT2515 expects the first byte after CS lowered to be the instruction/command byte. This means that CS must be raised and then lowered again to input another command.

Table 1 contain complete list of bytes of SPI instruction set. On detail output and input diagram of both operation modes (Mode 0.0 & Mode 1.1) please refer to Fig 13 & 14.

Table 1 SPI instruction set

Instruction name	Instruction format	Description
RESTE	1100 0000	Resets internal registers to default state, set Configuration mode.
READ	0000 0011	Read data from register beginning at selected address.
Read RX Buffer	1001 0nm0	When reading a receive buffer, reduces the overhead of a normal read command by placing the address pointer at one of four locations, as indicated by “n, m”. **Note:** The associated RX flag bit (CANINTF.RXnIF) will be cleared after bringing CS high.
WRITE	0000 0010	Write data to register beginning at selected address.
Load TX Buffer	0100 0abc	When loading a transmit buffer, reduces the overhead of a normal Write command by placing the address pointer at one of six locations as indicated by “a, b, c”.
RTS (Message Request-To-Send)	1000 0nnn	Instructs controller to begin message transmission sequence for any of the transmit buffers.
Read Status	1010 0000	Quick polling command that reads several status bits for transmit and receive functions.
RX Status	1011 0000	Quick polling command that indicates filter match and message type (standard, extended and/or remote) of received

		message.
Bit Modify	0000 0101	Allows the user to set or clear individual bits in a particular register. **Note:** Not all registers can be bit-modified with this command. Executing this command on registers that are not bit-modified will force the mast to FFh.

The RESET instruction can be used to re-initialize the internal registers of the SIT2515 and set Configuration mode. This command provides the same functionality, via the SPI interface, as the RESET pin. The RESET instruction is a single-byte instruction that requires selecting the device by pulling CS low, sending the instruction byte and then raising CS. It is highly recommended that the reset command be sent (or the RESET pin be lowered) as part of the power-on initialization sequence (or lower RESET).

The READ instruction is started by lowering the CS pin. The READ instruction is then sent to the SIT2515 followed by the 8-bit address (A7 through A0). Next, the data stored in the register at the selected address will be shifted out on the SO pin. The internal address pointer is automatically incremented to the next address once each byte of data is shifted out. Therefore, it is possible to read the next consecutive register address by continuing to provide clock pulses. Any number of consecutive register locations can be read sequentially using this method. The read operation is terminated by raising the CS pin (Fig 4).

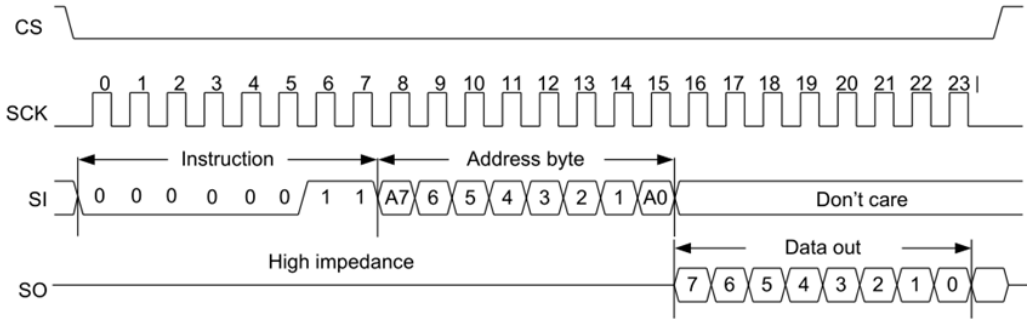
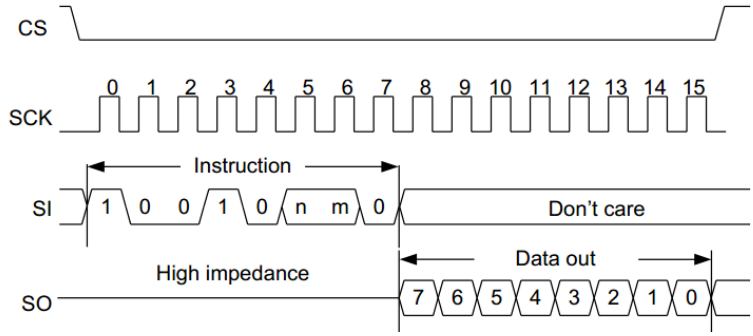


Fig 5 READ instruction

The Read RX Buffer instruction (Fig 5) provides a means to quickly address a receive buffer for reading. This instruction reduces the SPI overhead by one byte, the address byte. The command byte actually has four possible values that determine the address pointer location. Once the command byte is sent, the controller clocks out the data at the address location the same as the READ instruction (i.e., sequential reads are possible). This instruction further reduces the SPI overhead by automatically clearing the associated receive flag (CANINTF.RXnIF) when CS is raised at the end of the command.



n	m	Address pointer	Address
0	0	Receive buffer 0, Start at RXB0SIDH	0x61
0	1	Receive buffer 0, Start at RXB0D0	0x66
1	0	Receive buffer 1, Start at RXB1SIDH	0x71
1	1	Receive buffer 1, Start at RXB1D0	0x76

Fig 6 READ RX BUFFER instruction

The WRITE instruction is started by lowering the CS pin. Then the WRITE instruction is then sent to the SIT2515 followed by the address and at least one byte of data. It is possible to write to sequential registers by continuing to clock in data bytes, as long as CS is held low. Data will actually be written to the register on the rising edge of the SCK line for the D0 bit. If the CS line is brought high before eight bits are loaded, the write will be aborted for that data byte and previous bytes in the command will have been written. Refer to the timing diagram in Fig 6 for a more detailed illustration of the byte write sequence.

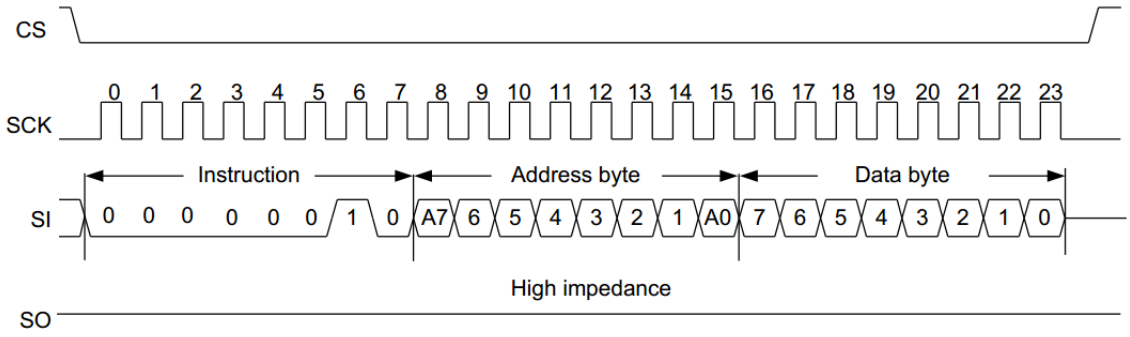
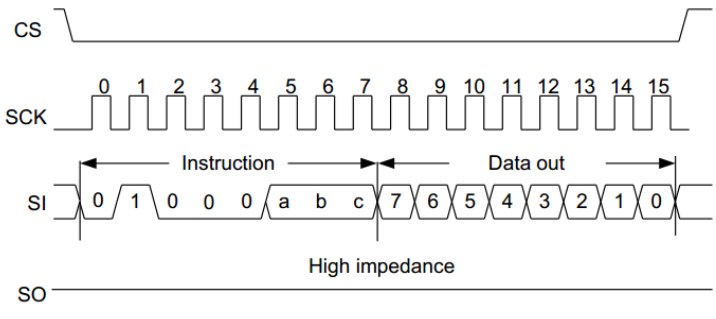


Fig 7 BYTE WRITE instruction

The Load TX Buffer instruction (Fig 9) permits to operate without the eight-bit address required by a normal write command. The eight-bit instruction sets the address pointer to one of six addresses to quickly write to a transmit buffer that points to the "ID" or "data" address of any of the three transmit buffers.



a	b	c	Address pointer	Address
0	0	0	Transmit buffer 0, Start at TXB0SIDH	0x31
0	0	1	Transmit buffer 0, Start at TXB0D0	0x36
0	1	0	Transmit buffer 1, start at TXB1SIDH	0x41
0	1	1	Transmit buffer 1, Start at TXB1D0	0x46
1	0	0	Transmit buffer 2, Start at TXB2SIDH	0x51
1	0	1	Transmit buffer 2, Start at TXB2D0	0x56

Fig 8 LOAD TX BUFFER instruction

The RTS command can be used to initiate message transmission for one or more of the transmit buffers. The SIT2515 is selected by lowering the CS pin. The RTS command byte is then sent. Shown in Fig 8, the last 3 bits of this command indicate which transmit buffer(s) are enabled to send. This command will set the TxBnCTRL. TXREQ bit for the respective buffer(s). Any or all of the last three bits can be set in a single command. If the RTS command is sent with nnn = 000, the command will be ignored.

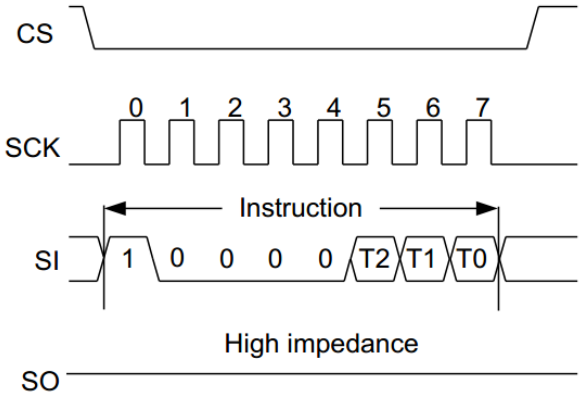


Fig 9 REQUEST-TO-SEND instruction (RTS)

The Read Status instruction allows single instruction access to some of the often used status bits for message reception and transmission. The SIT2515 is selected by lowering the CS pin and the read status command byte, shown in Fig 9, is sent to the SIT2515. Once the command byte is sent, the SIT2515 will return eight bits of data that contain the status. If additional clocks are sent after the first eight bits are transmitted, the SIT2515 will continue to output the status bits as long as the CS pin is held low and clocks are provided on SCK. Each status bit returned in this command may also be read by using the standard read command with the appropriate register address.

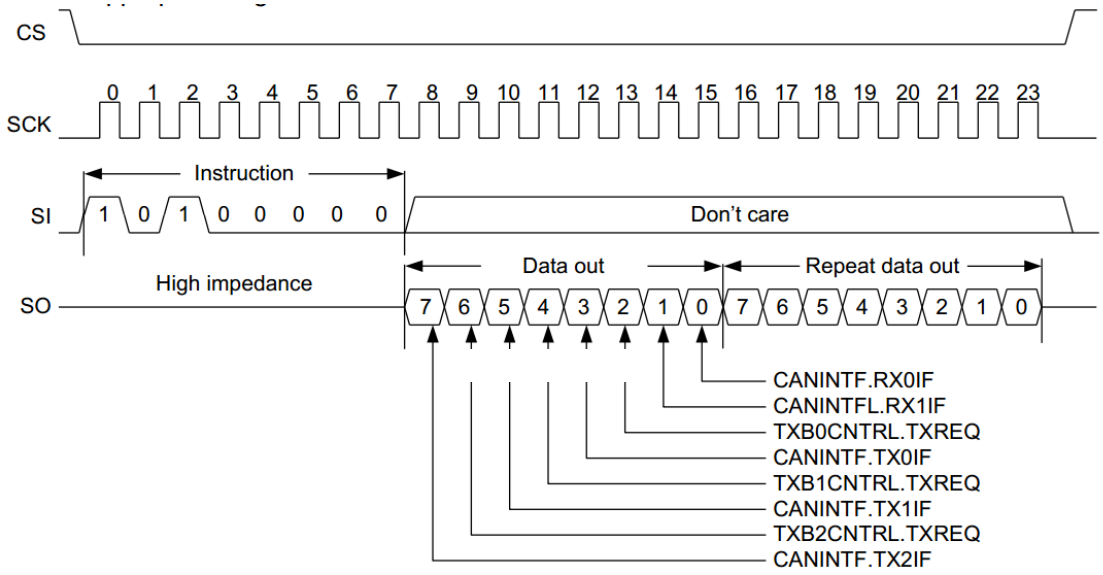
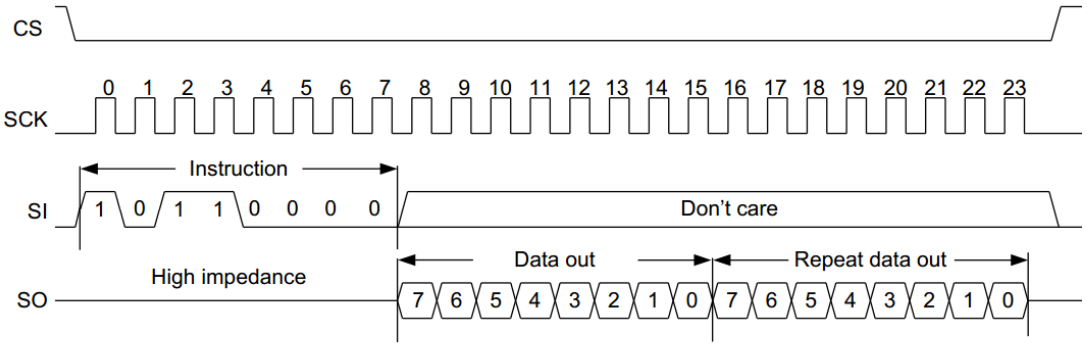


Fig 10 READ STATUS instruction

The RX Status instruction (Fig 10) is used to quickly determine which filter matched the message and message type (standard, extended, remote). After the command byte is sent, the controller will return 8 bits

of data that contain the status data. If more clocks are sent after the 8 bits are transmitted, the controller will continue to output the same status bits as long as the CS pin stays low and clocks are provided.



7	6	Received msg
0	0	No RX- message
0	1	Message in RXB0
1	0	Message in RXB1
1	1	Message in both buffers*

CANINTF.RXnIF are mapped in bits 7 & 6.

4	3	Received msg type.
0	0	Standard data frame
0	1	Standard remote frame
1	0	Extended data frame
1	1	Extended remote frame

Extended ID bit mapped in bit 4.
RTR bit mapped in bit 3 .

2	1	0	Filter match
0	0	0	RXF0
0	0	1	RXF1
0	1	0	RXF2
0	1	1	RXF3
1	0	0	RXF4
1	0	1	RXF5
1	1	0	RXF0 (rollover to RXB1)
1	1	1	RXF1 (rollover to RXB1)

* Buffer 0 has higher priority, therefore bits, 4:0 display RXB0.status

Fig 11 RX STATUS instruction

The Bit Modify instruction provides a means for setting or clearing individual bits in specific status and control registers. This command is available for registers BFPCTRL，TXRTSCTRL，CANCTRL，CNF3，CNF2，CNF1，CANINTE，CANINTF，EFLG，TXB0CTRL，TXB1CTRL，TXB2CTRL，RXB0CTRL。

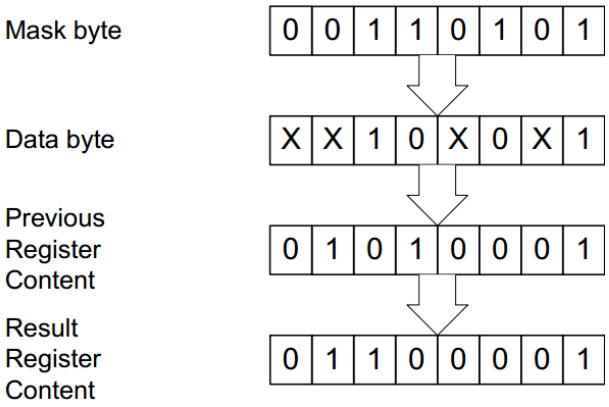


Fig 12 Bit Modify instruction

Note: Executing the Bit Modify command on registers that are not bit-modifiable will force the mask to FFh.

The chip is selected by lowering the CS pin then the Bit Modify command is applied to the SIT2515. The command is followed by the address of the register, the mask byte and finally the data byte. The mask byte determines which bits in the register will be allowed to change. A “1” in the mask byte will allow a bit in the register to change, while a “0” will not.

The data byte determines what value the modified bits in the register will be changed to. A “1” in the data byte will set the bit and a “0” will clear the bit, provided that the mask for that bit is set to a “1”.

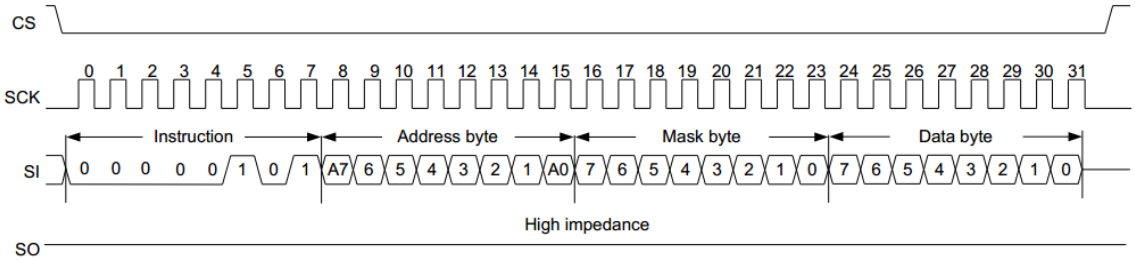


Fig 13 BIT MODIFY instruction

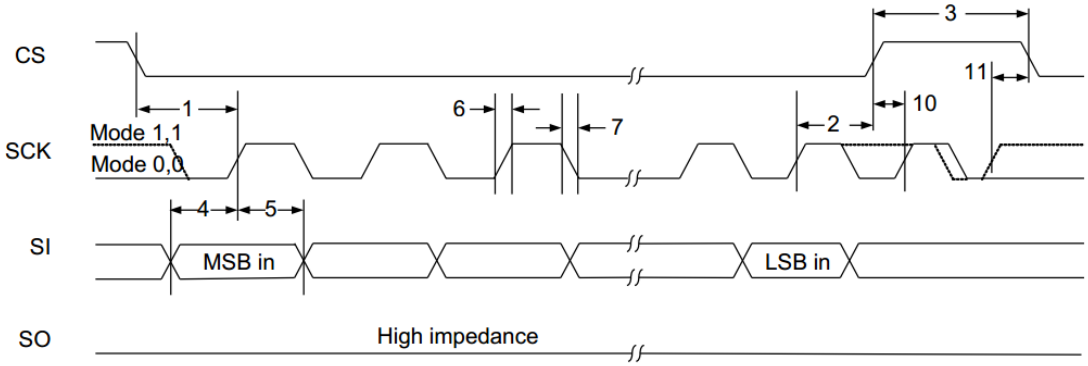


Fig 14 SPI- interface input timing

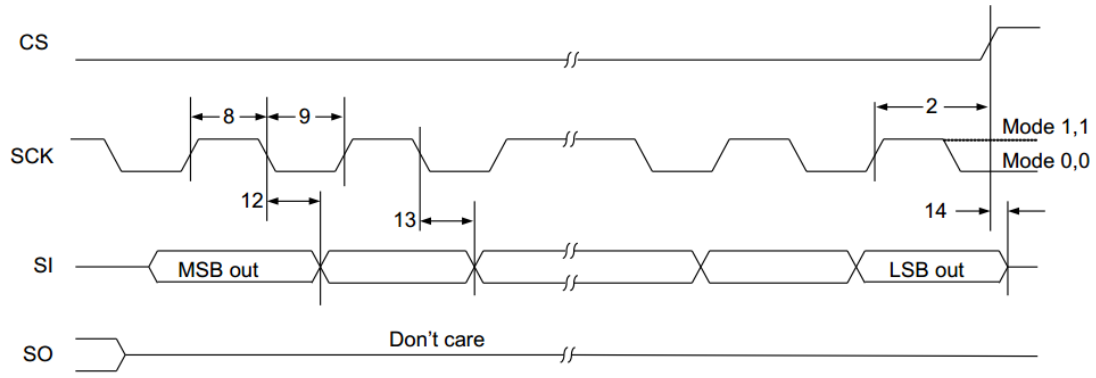


Fig 15 SPI- interface output timing

4 Typical application

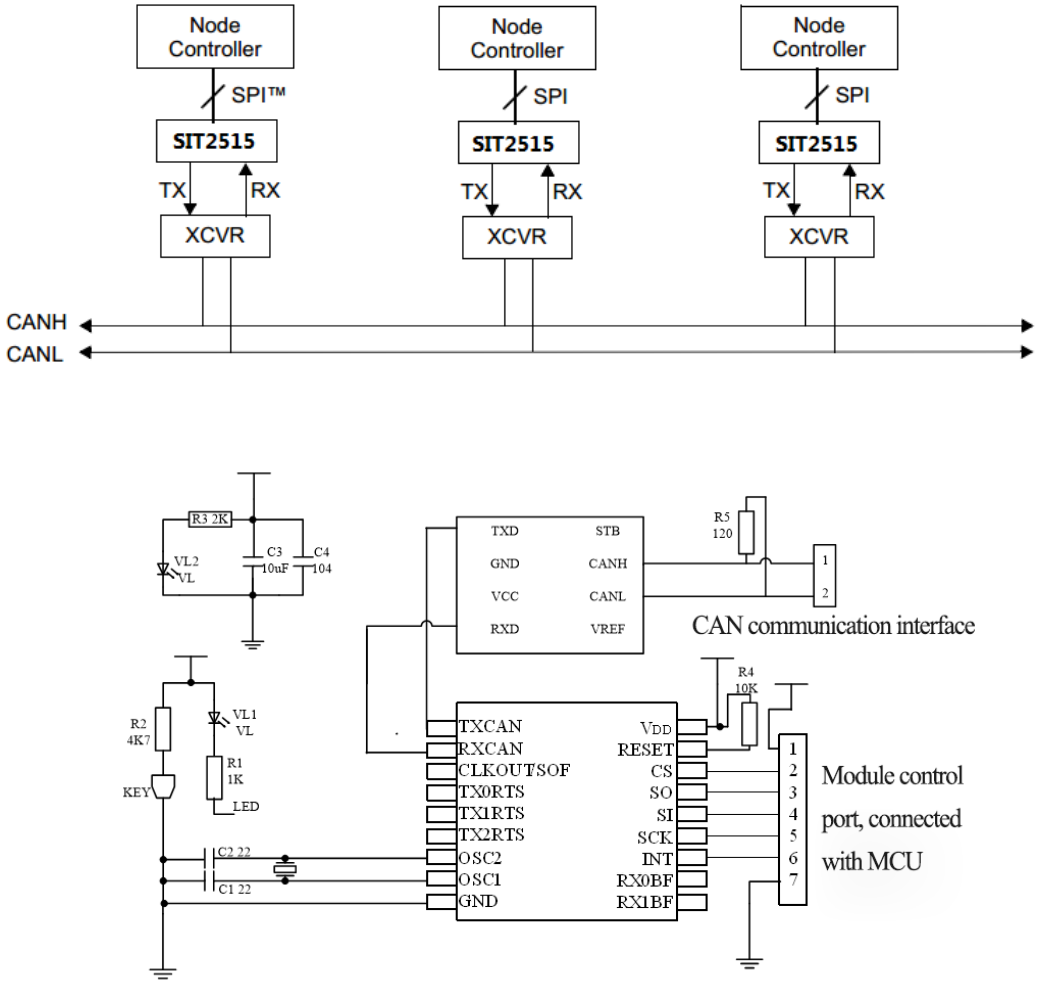
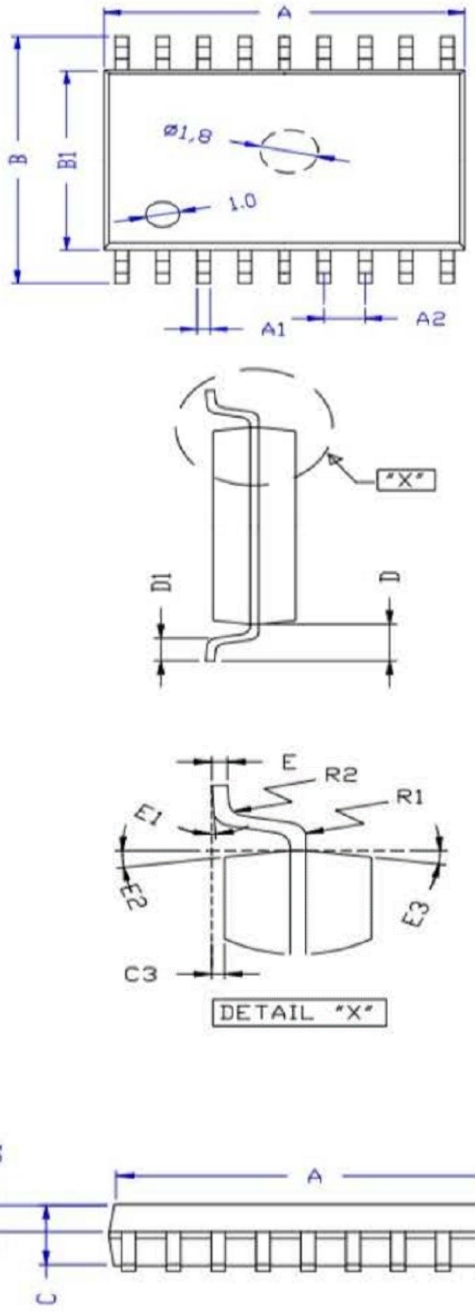


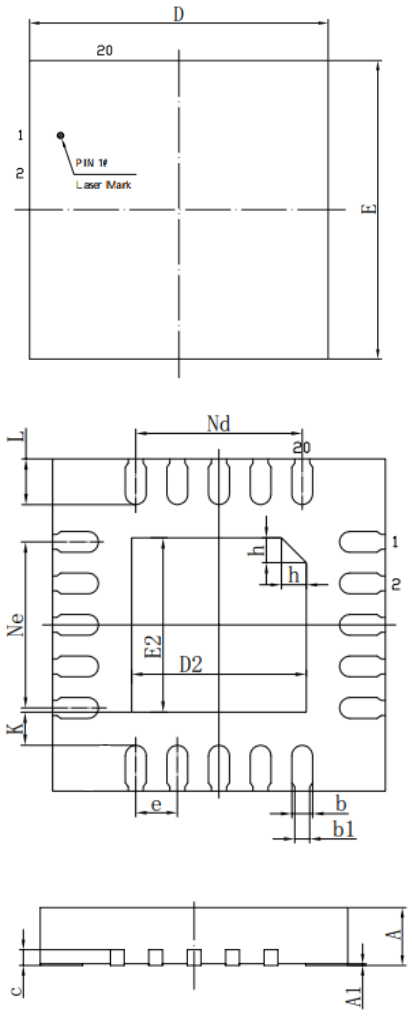
Fig 16 Typical application

SOP18 DIMENTIONS

PACKAGE SIZE		
Symbol	**Min./mm**	**Max./mm**
A	11.25	11.65
A1	0.40TYP	
A2	1.27TYP	
B	10.10	10.50
B1	7.30	7.70
C	2.24	2.44
C1	1.05TYP	
C2	0.20	0.33
C3	0.10	0.27
D	1.395 TYP	
D1	0.70	1.00
E	0.20	0.30
E1	0°	8°
E2	7°TYP	
E3	5°TYP	
R1	0.5°TYP	
R2	0.2°TYP	

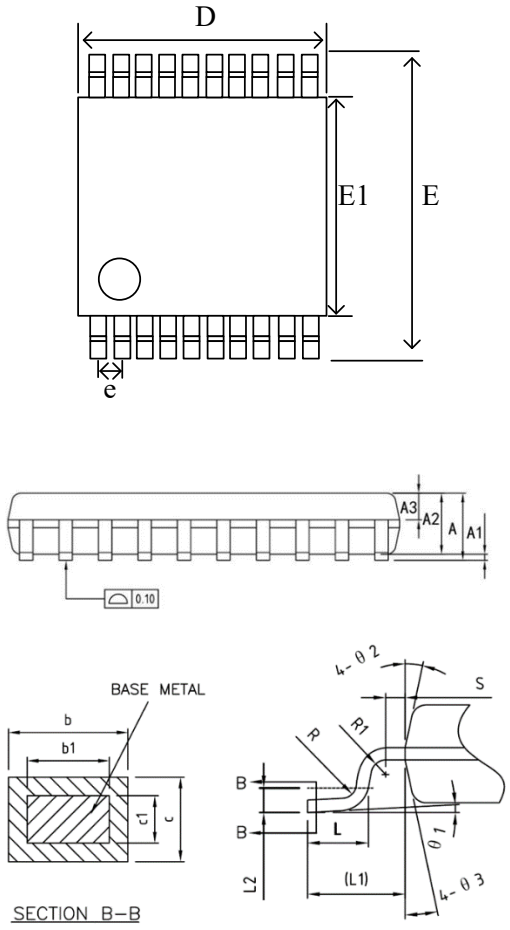


QFN20 DIMENTIONS



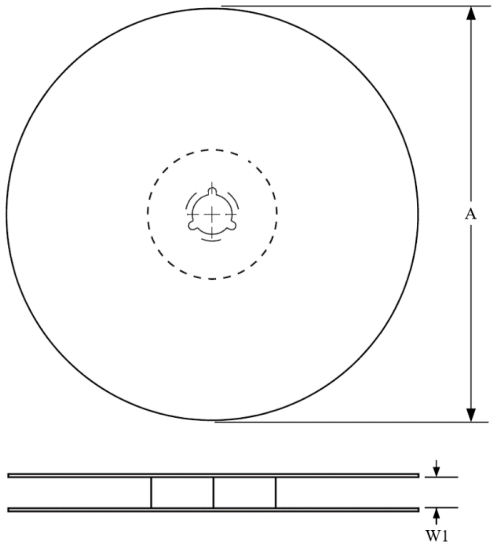
PACKAGE SIZE			
Symbol	**Min./mm**	**Typ./mm**	**Max./mm**
A	0.70	0.75	0.80
A1	0.00	0.02	0.06
b	0.20	0.25	0.30
b1	0.18REF		
c	0.203REF		
D	3.90	4.00	4.10
D2	2.00	2.10	2.20
Nd	2.00BCS		
Ne	2.00BCS		
e	0.50BCS		
E	3.90	4.00	4.10
E2	2.00	2.10	2.20
L	0.50	0.55	0.60
h	0.25	0.30	0.35
k	0.35	0.40	0.45

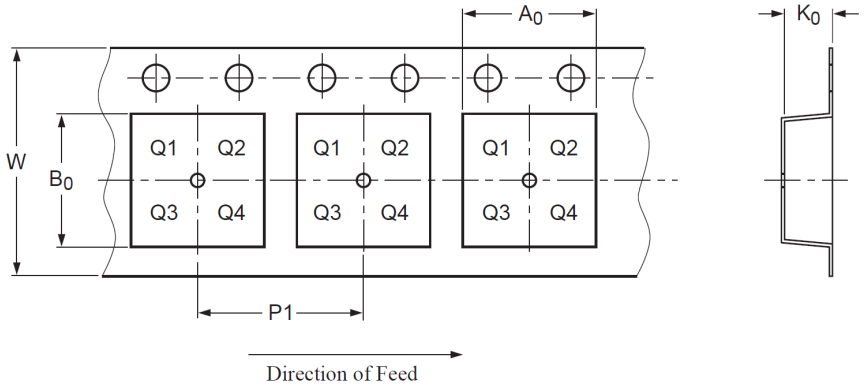
TSSOP20 DIMENTIONS



PACKAGE SIZE		
Symbol	**Min./mm**	**Max./mm**
A		1.20
A1	0.05	0.15
A2	0.90	1.05
A3	0.34	0.54
b	0.20	0.28
b1	0.20	0.24
c	0.10	0.19
c1	0.10	0.15
D	6.40	6.60
D1	4.00	4.40
E	6.25	6.55
E1	4.30	4.50
e	0.65BSC	
L	0.45	0.75
L1	1.00REF	
L2	0.25BCS	
R	0.09	
R1	0.09	
S	0.20	
θ1	0°	8°
θ2	10°	14°
θ3	10°	14°

TAPE AND REEL INFORMATION





PIN1 is in quadrant 1

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

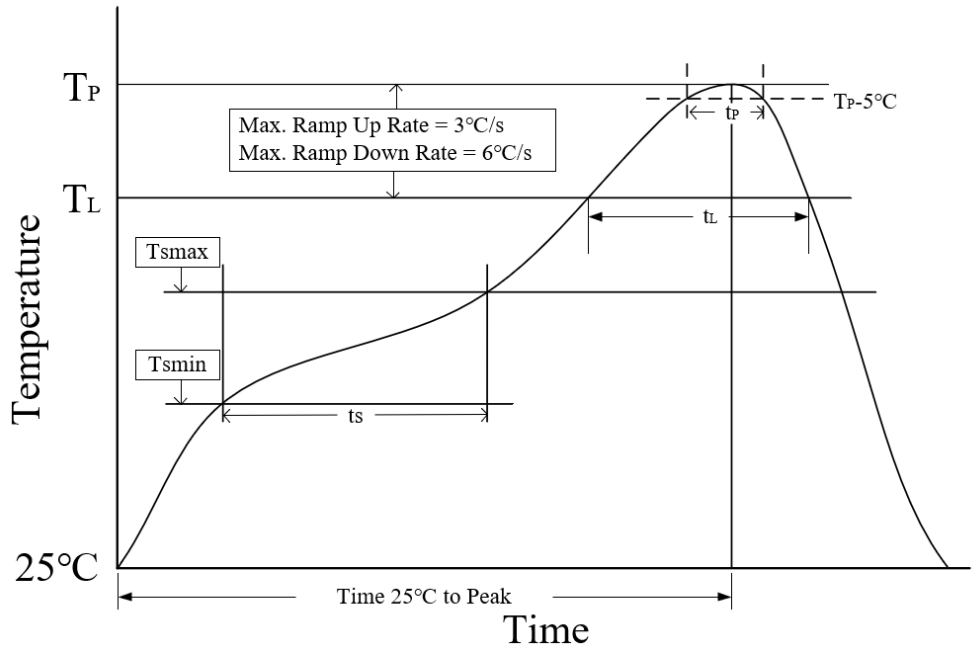
Package Type	Reel Diameter A (mm)	Tape width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)
QFN20	330	12.5±0.20	3.23±0.10	3.23±0.10	1.05±0.10	4.00±0.10	12.00±0.30
SOP18	490	105	10.95±0.10	12.05±0.10	2.75±0.10	12.00±0.10	24.00±0.20
TSSOP20	490	105	6.88±0.10	7.15±0.10	1.65±0.10	8.00±0.10	16.00±0.10

ORDERING INFORMATION

TYPE NUMBER	PACKAGE	PACKING
SIT2515T-I/SO	SOP18	Tape and reel
SIT2515T-I/ST	TSSOP20	Tape and reel
SIT2515T-I/ML	QFN20	Tape and reel

SOP18 is packed with 1500 pieces/disc in braided packaging; TSSOP20 is packed with 2500 pieces/disc in braided packaging; QFN20 is packed with 3000 pieces/disc in braided packaging.

REFLOW SOLDERING



Parameter	Lead-free soldering conditions
Ave ramp up rate (T_L to T_P)	3 °C/second max
Preheat time ts (T_{smin}=150 °C to T_{smax}=200 °C)	60-120 seconds
Melting time t_L (T_L=217 °C)	60-150 seconds
Peak temp T_P	260-265 °C
5°C below peak temperature t_P	30 seconds
Ave cooling rate (T_P to T_L)	6 °C/second max
Normal temperature 25℃ to peak temperature T_P time	8 minutes max

Important statement

SIT reserves the right to change the above-mentioned information without prior notice.

REVISION HISTORY

Version number	Data sheet status	Revision date
V1.0	Initial version.	November 2022