江苏长晶科技股份有限公司 JIANGSU CHANGJING ELECTRONICS TECHNOLOGY CO., LTD.

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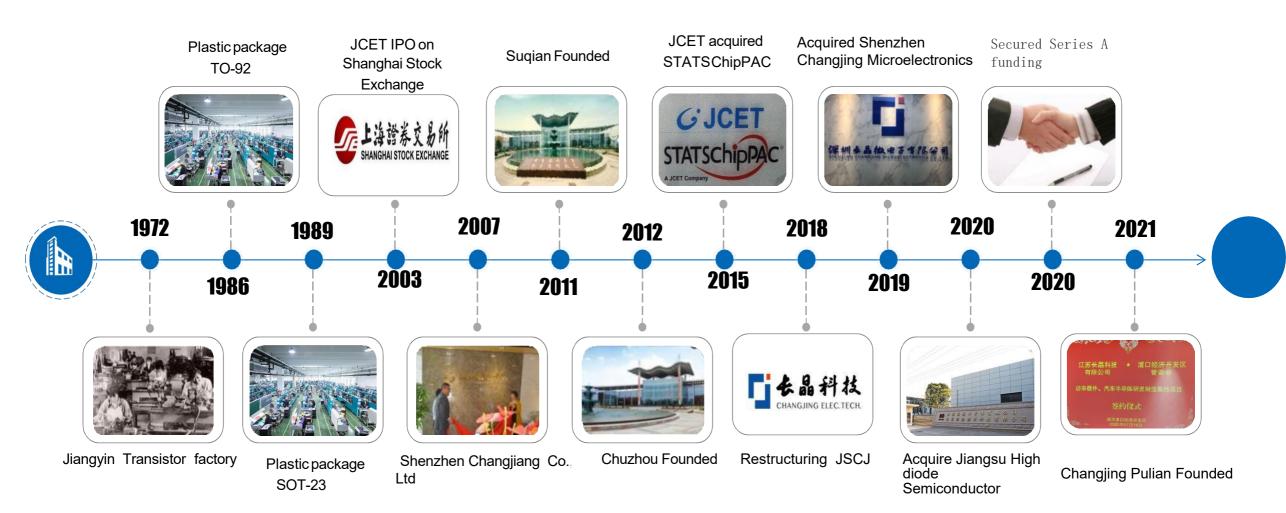


- > Founded in 2018 and headquartered in in Nanjing, Jiangsu
- > The company's predecessor was the discrete division of JCET (600584).
- Registered Capital is 55.5 million USD
- Provide 15,000 series and models ranging from diode, transistor ,MOSFETs, LDOs, DC-DCs, frequency devices, power devices,Auto-Motive devices etc.
- > Awarded China's Top 10 Semiconductor Power Device Enterprises in 2019
- Subsidiaries in Shenzhen and Hong Kong
 Offices are located in Peking , Beijing, Shanghai, Hangzhou, Wuhan, Suzhou, Hong kong, Taiwan.



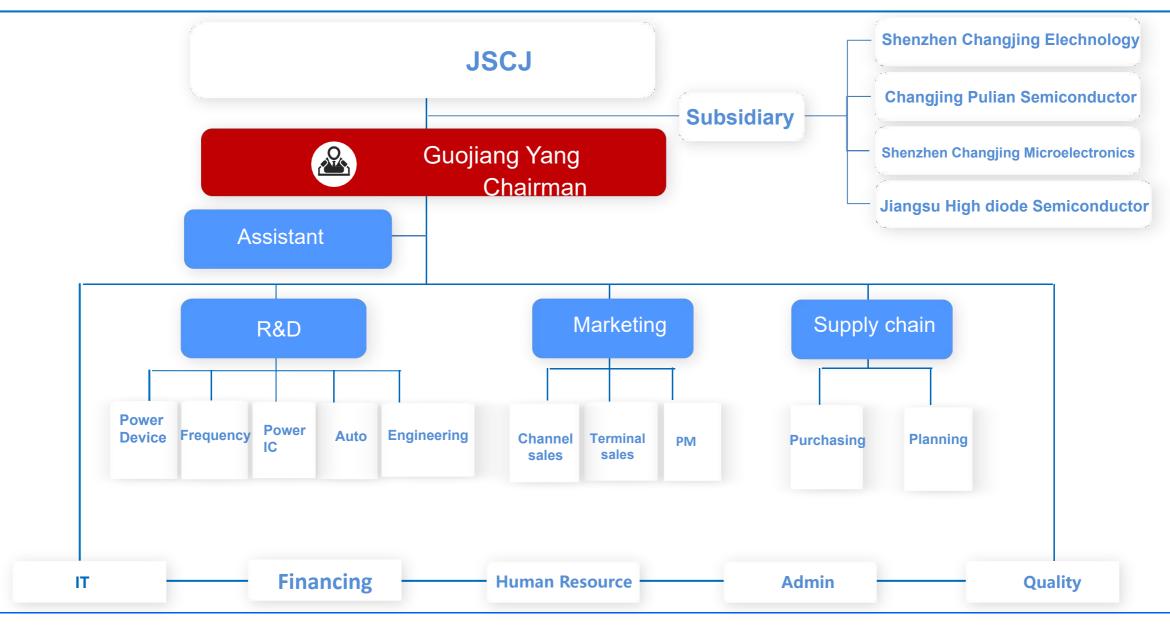








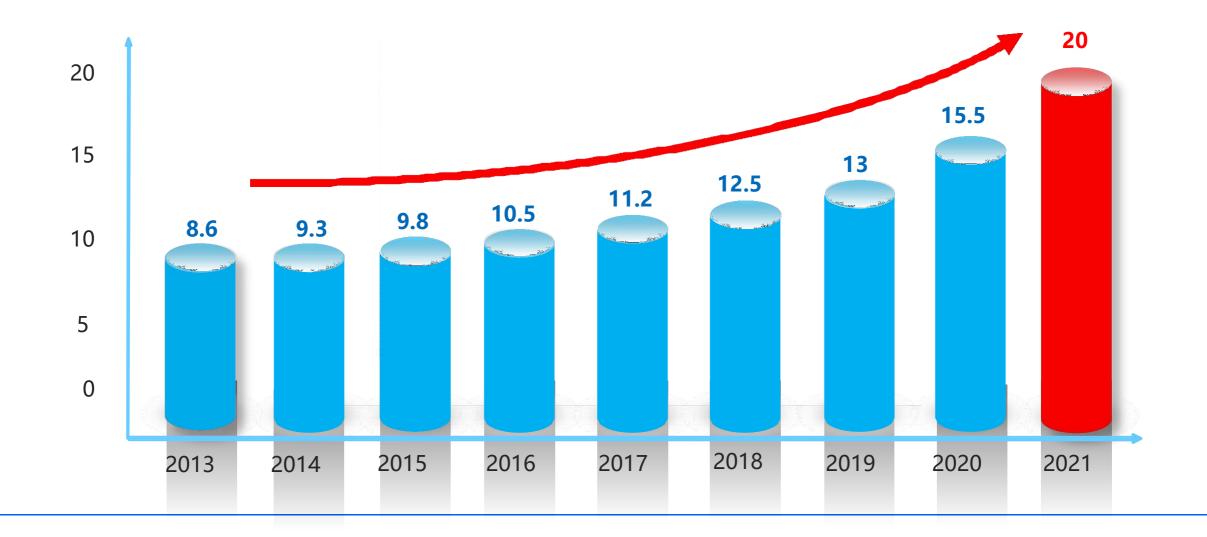






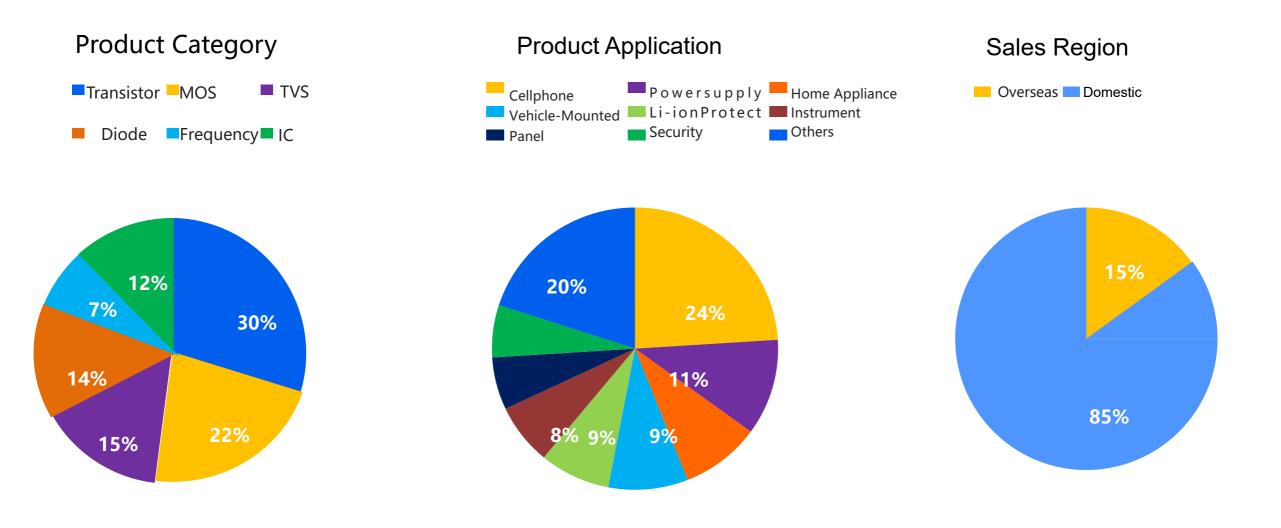


JSCJ — 2013-2018 including former JCET discrete components, sales(hundred million RMB)



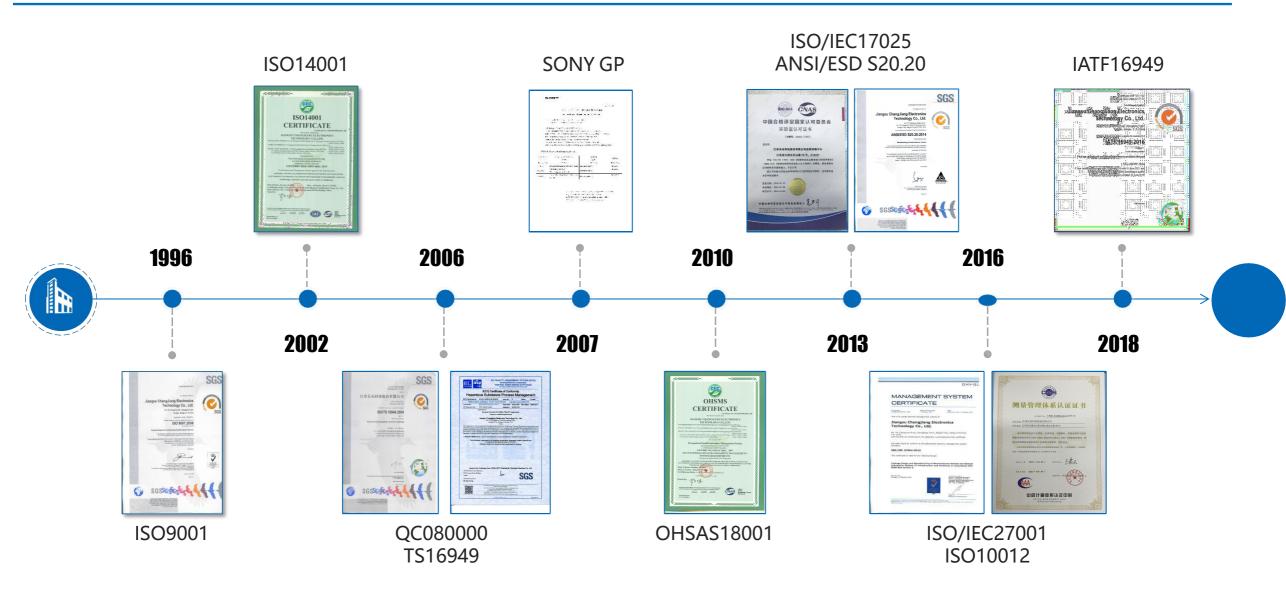
Product Distribution

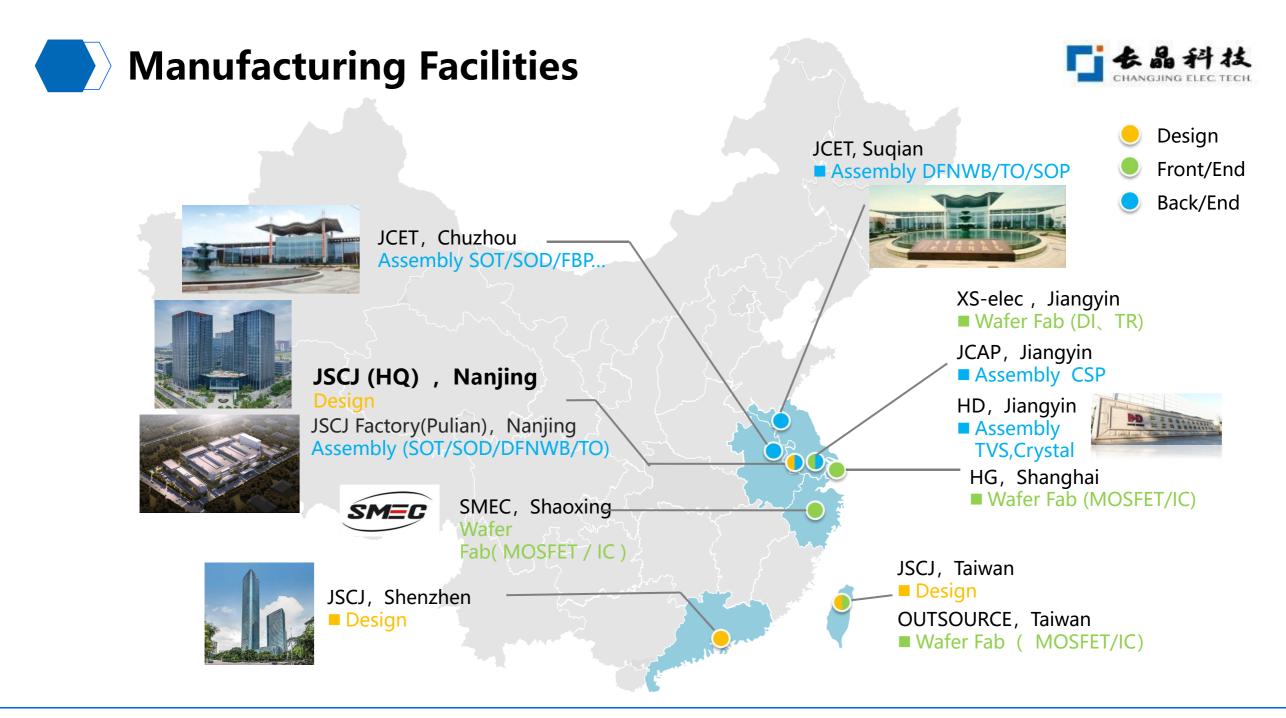
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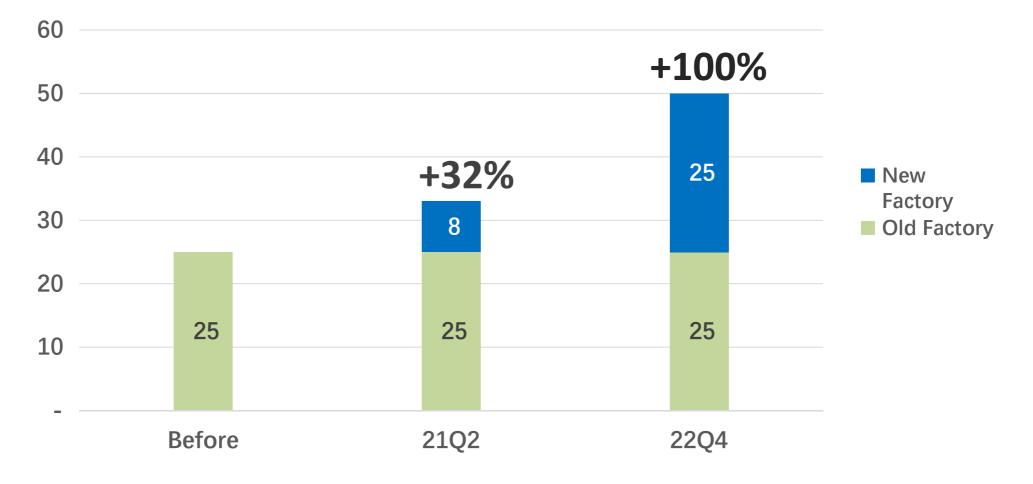




Core Advantage — Capacity Expansion

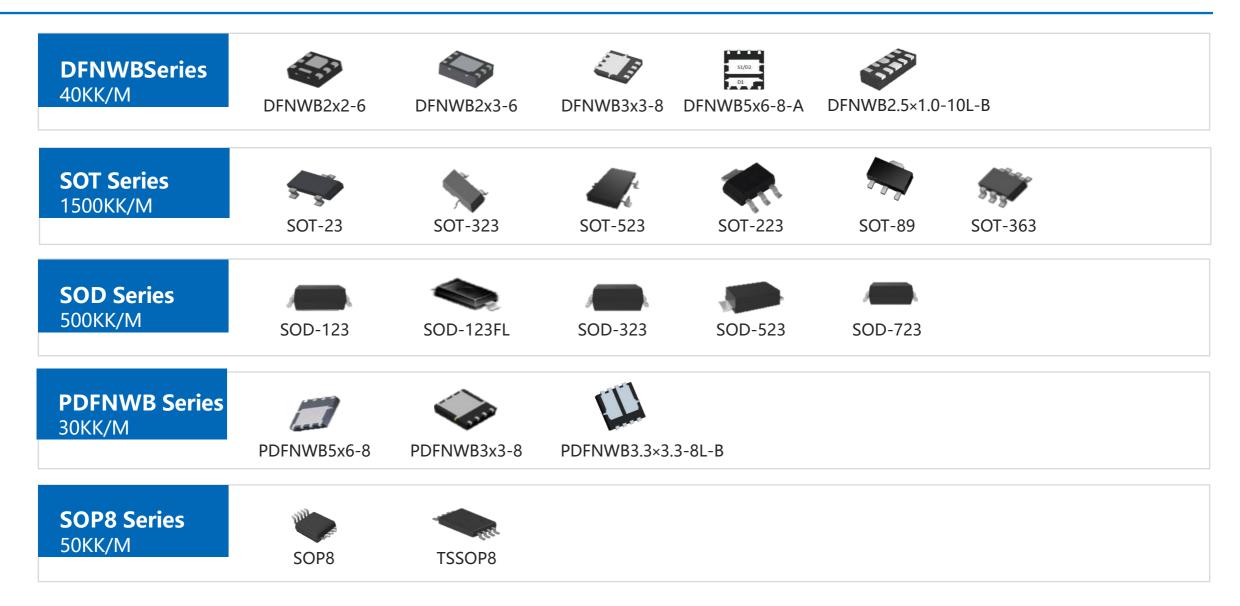


Capacity(0.1BPCS/M)









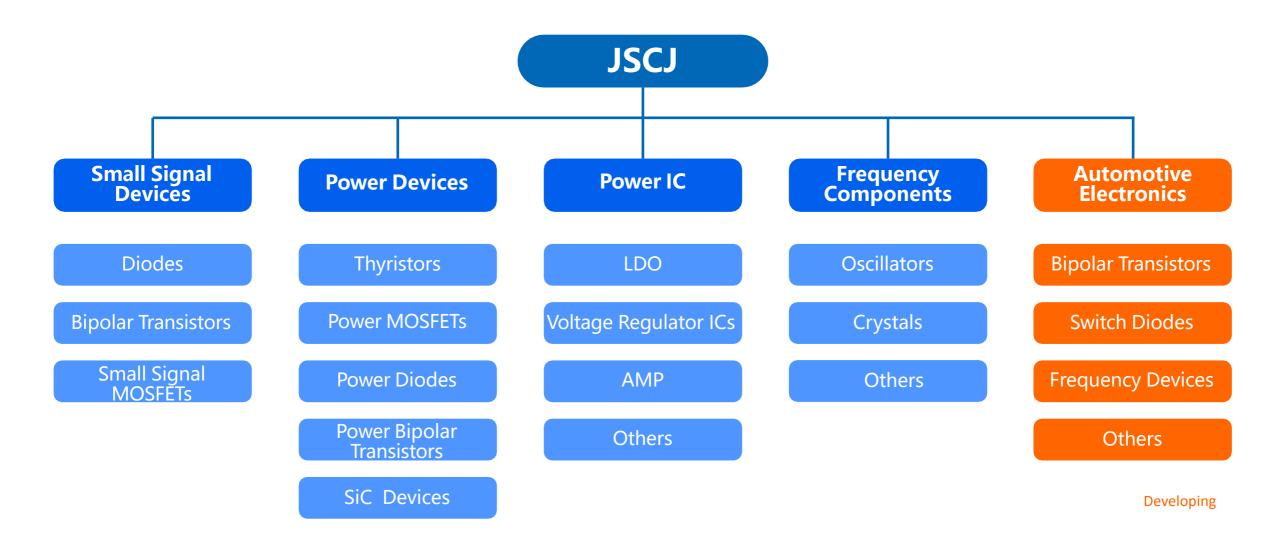






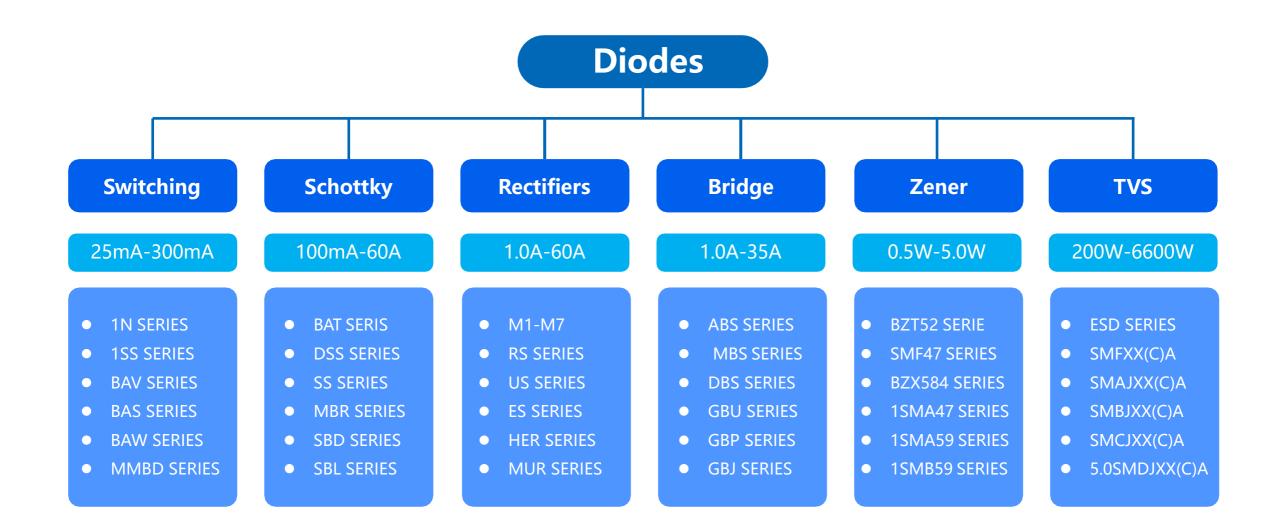






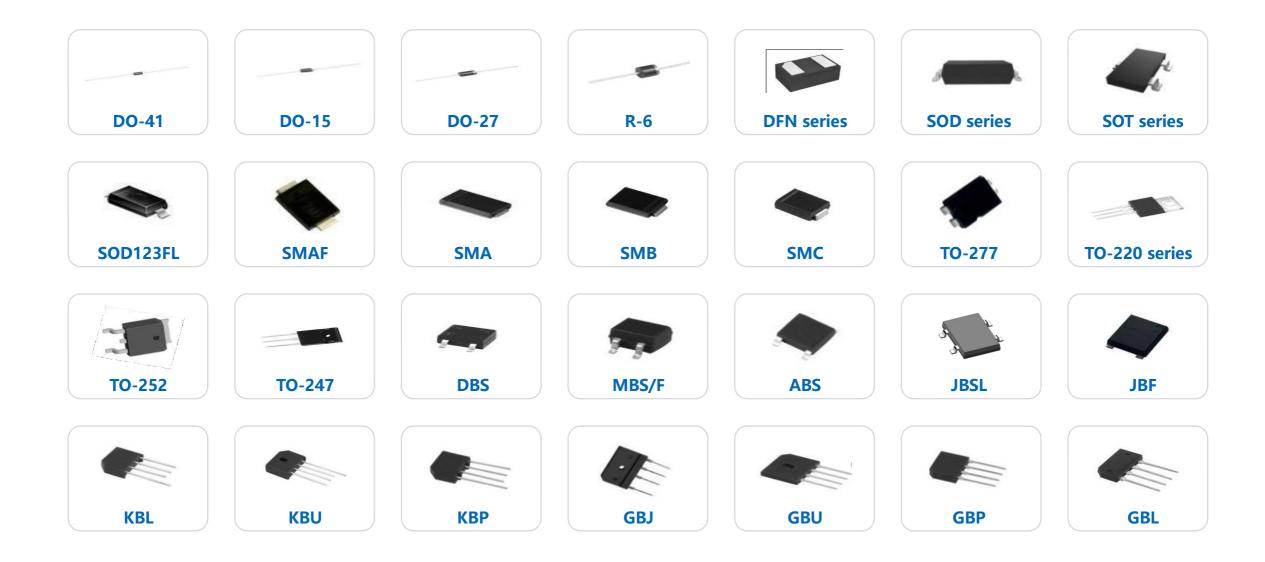






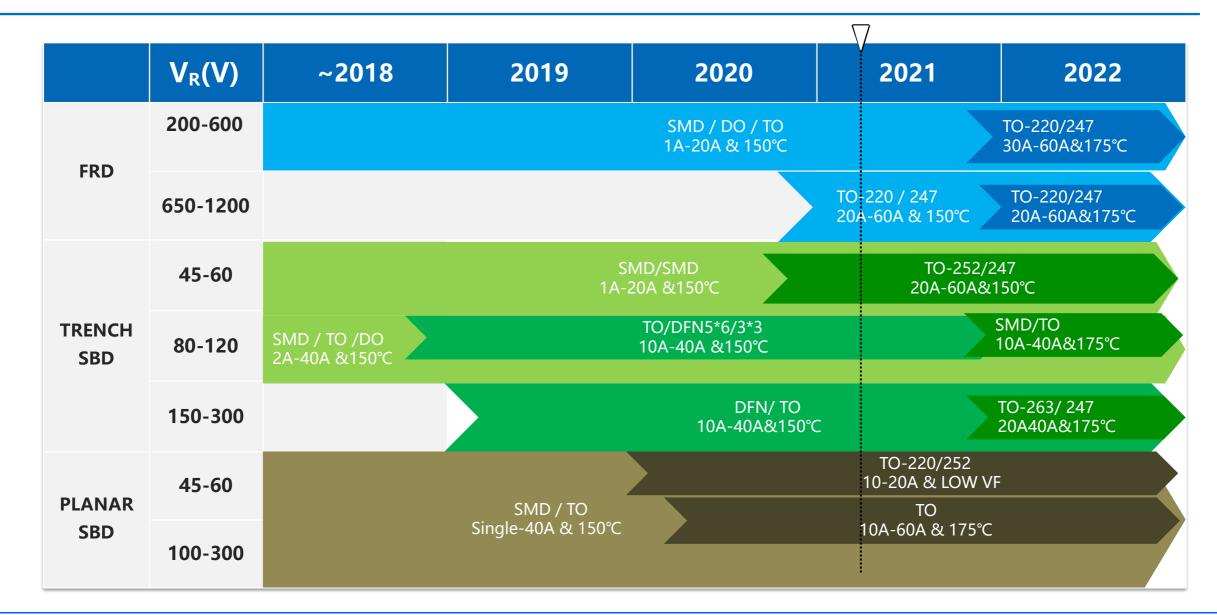


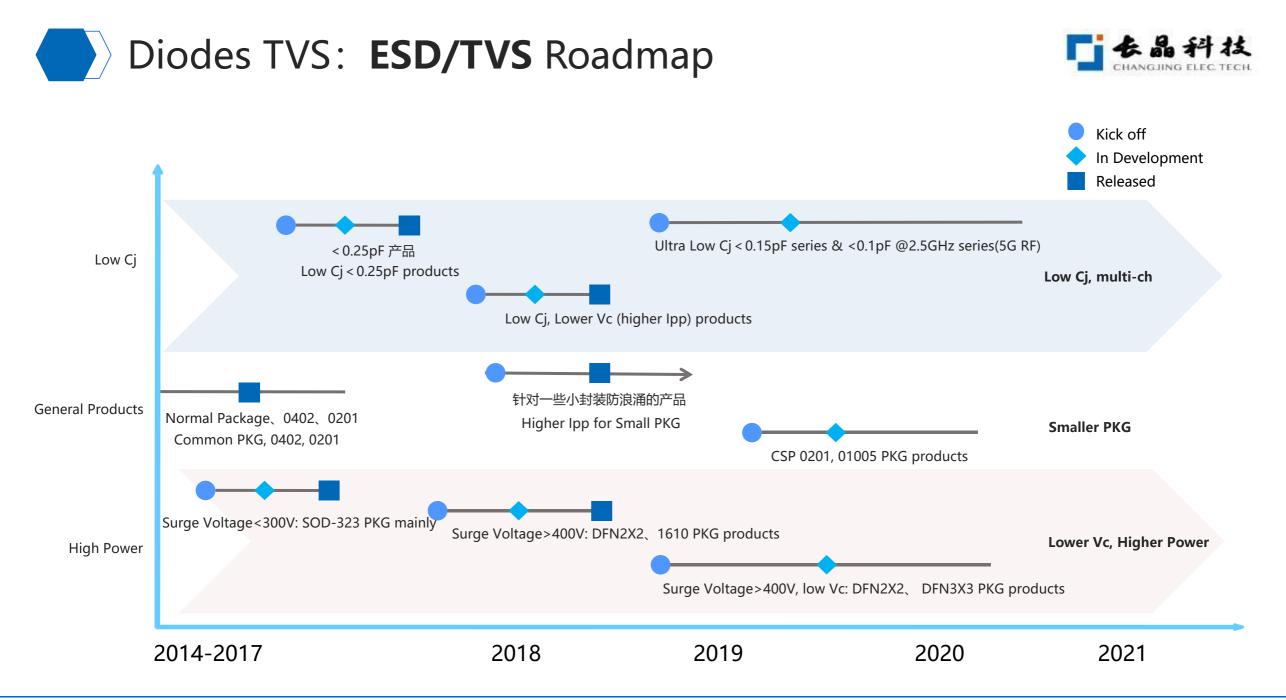












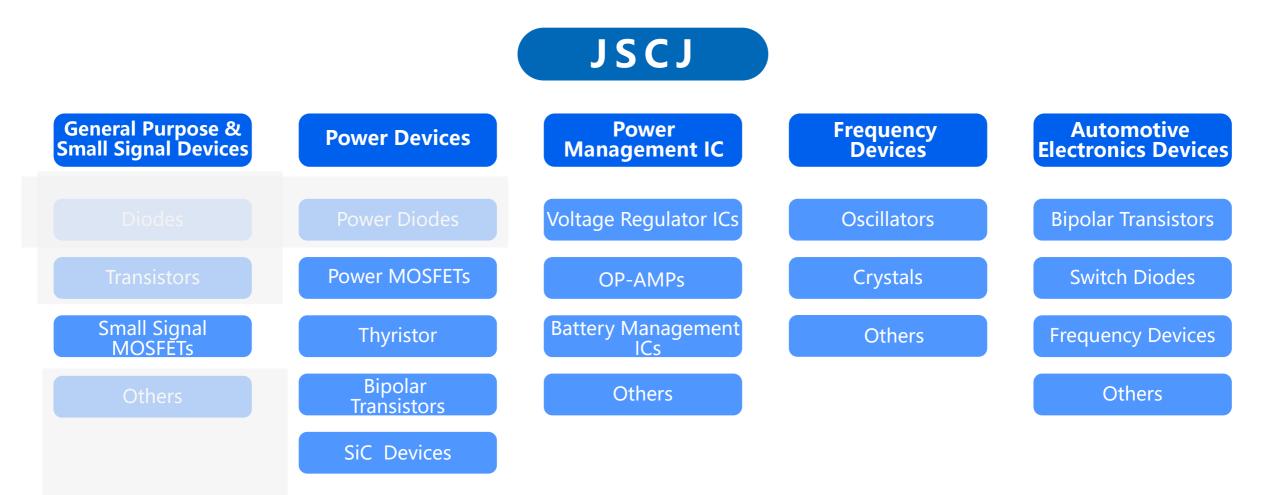




Ррр	200W	400W	600W	1.5kW	3kW	5kW	6.6kw
VRWM	5v~440v	5v~440v	5v~440v	5v~440v	5v~440v	5v~440v	20v~48v
Polarity	Ui/Bi	Ui/Bi	Ui/Bi	Ui/Bi	Ui/Bi	Ui/Bi	Ui
Series	SMF	SMAJ, P4SMA, P4KE	SMBJ, P6SMB, P6KE	SMCJ, 1.5SMC, 1.5KE	SMDJ, 3KP	5.0SMDJ 5KP	SMEJ











 $oldsymbol{\nabla}$ *New Generation will provide better FOM

产品 Products	封装 Package	2018	2019	2020	202	:1	2022		
		12V/24V Gen 2.0		12V/24V (Gen 3.0				
TRENCH LVMOS	🍬 🧼	15V-200V Gen 3.0		Gen 4.0					
		PMOS 30V-100V Gen		PMDS 30-100V Gen 3.0					
	00	30V Gen1.0	40V Gen1.0		·	40	30V Gen 2.0 V Gen2.0		
		60-6	5V Gen1.0		60V Gen2.0				
SGT		80V Gen			80V G				
LVMOS			100V Gen1.0	100V 0	Gen 2.0	100V Gen 2.5			
	THE REAL PROPERTY AND A DECEMBER OF A DECEMBER		120V Gen1.0	120V Gen2.0					
			150V Gen1.0)			150V Gen2.0		
							200V Gen2.0 250V Gen2.0		
HVMOS		Planar 600V-800V Gen	2.0						
							SJ 650V Gen 1.0		





Company	Part Number	Package	BVDSS (V)	VGS (V)	EAS⁺¹ (mJ)	Ron Typ@1 0V (mOhm)	Qg @10V (nC)	Ciss (pF)	Coss (pF)	Crss (pF)	FOM*² (mOhm -nC)
JSCJ	CJAC100SN08 U	PDFN506 0	80	+/-20	500	3.0	60	3780	1800	25	180
DIODES	DMTH8003SPS	PDFN506 0	80	+/-20	375	3.1	124	8952	533	26	384
NCE Power	NCEP055N80G	PDFN506 0	80	+/-20	423	4.6	51	3197	598	24	234
TOSHIBA	TPH4R008NH	SOP Adv	80	+/-20	340	3.3	59	4100	890	32	195





Company	Part Number	Package	BVDSS (V)	VGS (V)	EAS ^{∗1} (mJ)	Ron Typ@1 0V (mOhm)	Qg @10V (nC)	Ciss (pF)	Coss (pF)	Crss (pF)	FOM*² (mOhm −nC)
JSCJ	CJAC13TH06	PDFN506 0	60	+/-20	250	2.2	63.7	5298	1635	74.8	140
Diodes	DMTH62M8SP S	PowerDI 5060-8	60	+/-20	207	2.2	95.4	4556	1383	105	210
NCE Power	NCEP60T15AG	PDFN506 0	60	+/-20	819	2.7	88	5500	955	25	237
TOSHIBA	TPH2R306NH	SOP Adv	60	+/-20	453	1.9	72	4700	1500	55	136.8





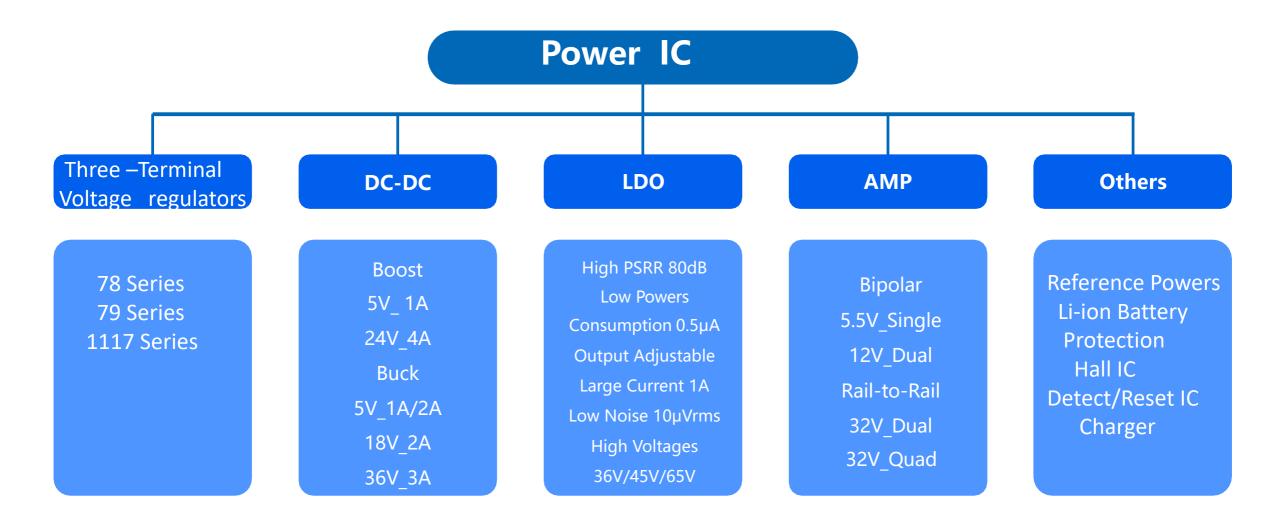
Company	Part Number	Package	BVDSS (V)	VGS (V)	EAS⁺¹ (mJ)	Ron Typ@1 0V (mOhm)	Qg @10V (nC)	Ciss (pF)	Coss (pF)	Crss (pF)	FOM*² (mOhm -nC)
JSCJ	CJAC200SN04	PDFN506 0	40	+/-20	400	0.88	120	7450	220	3.5	105
Diodes	DMTH4001SPS	PowerDI 5060-8	40	+/-20	440	0.73	144	10787	3929	156	105
NCE Power	NCEP40T20GU	PDFN506 0	40	+/-20	1800	0.85	137	8085	2123	121	116
TOSHIBA	TPH1R204PL	SOP Adv	40	+/-20	127	1.0	74	5500	1300	93	74



Products	2019	2020	2021	2022	2023	2024	2025				
	Battery CSP 12/24V Consumer series PC 30V SGT Smart Phone 30V SGT DFN2*2/3*3										
LVMOS	Power Supply	PD Fast Charge	ast Charge - 30/100V SGT AC/DC Mining Machine/Server 30 - 200V SGT DCDC/ Base 60 - 200V SGT Qn Hot Plug 150/200V SOA								
	Industrial Series		Electric Tool/ UAVCleaner 30-100V SGT BMS/ Stored Energy 85/100V SGT								
HVMOS	Power Supply Power Supply Power Supply PC/Server 650V/15-60A TO220/247 SJ/w-FRD Charging Pile 650V/60-100A TO247 SJ/w-FRD										
SiC SBD	Power Supply PD Fast Charge/PC/Server 650V/4-12A TO220/247 Industrial Series DC Charging Pile 1200V 5/10/15A TO247										
D-IGBT	Home Appliances			AC 650V/5A TO252 PFC/Air Conditioner H/S 650V/30A-50A TO247 C/R Industrial Souring Machine 650V/15A TO220 Induction Cooker/ Cooker 1350V/20A TO247 V/R Photovolataic/UPS 1200V/40A TO247							

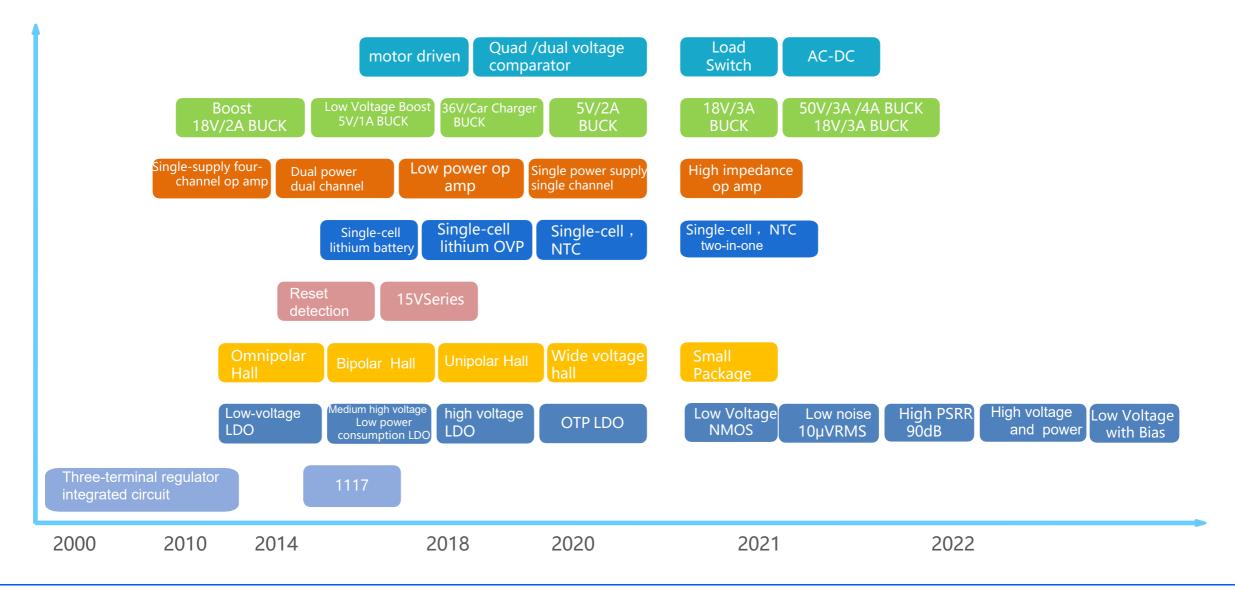






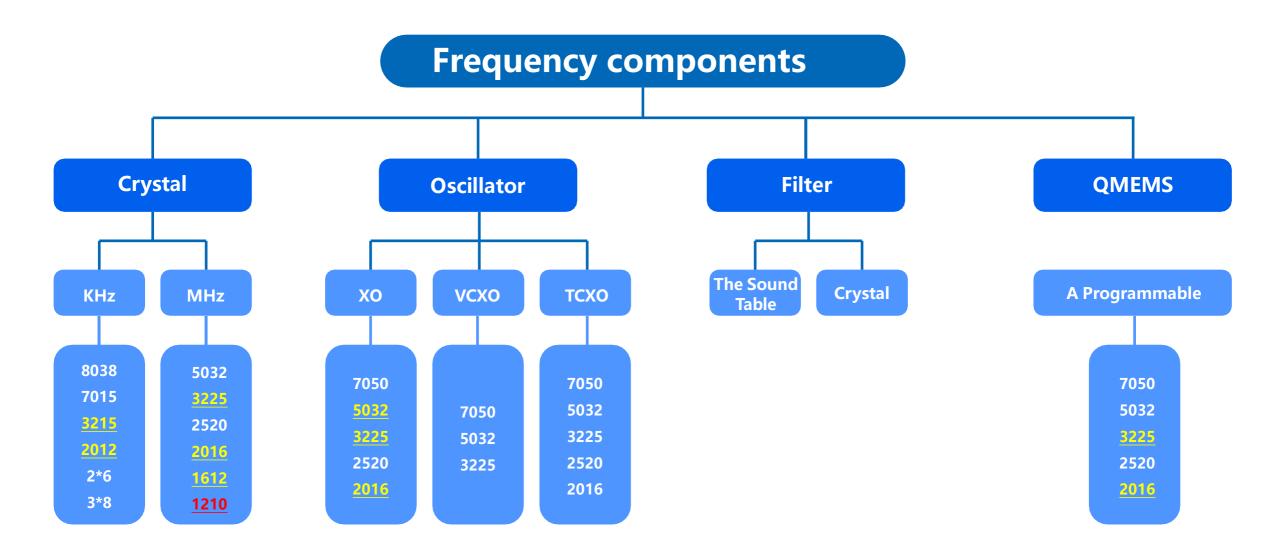




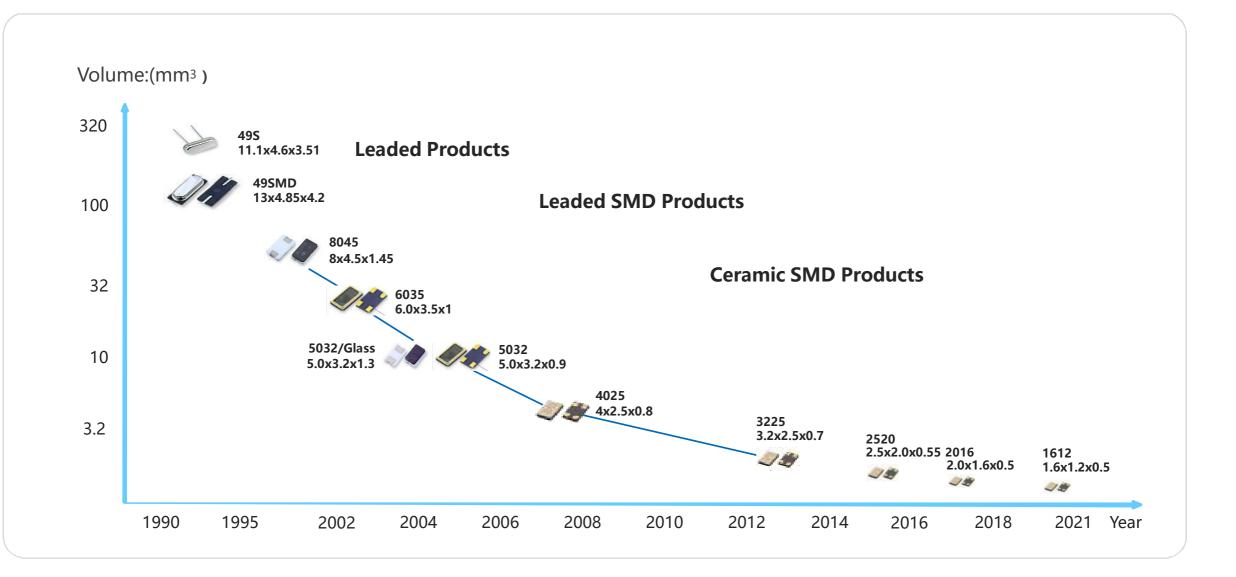




























ITEMS	STANDARD	GOAL
PRE	JESD22-A113F	Simulated placement products are affected by environmental changes such as temperature and humidity during transportation, storage and reflow soldering. This test shall be performed prior to the reliability test and represents only the package level of the product.
MSL	IPC/JEDEC J-STD-020	Identify the classification of non-hermetic solid surface mount components that are moisture sensitive so that they can be properly packaged, stored and handled to prevent damage to components during reflow and repair.
тнт	GB/T2423.3 JESD22-A101	The ability of the product to apply humidity and temperature stress over a long period of time is assessed.
тст	JESD22-A104 GB/T 2423.22	Evaluate the ability of the product package to withstand extreme high temperatures and extreme low temperatures, as well as the effects of extreme high temperatures and extreme low temperatures.
HTST	GB/T 2423.2 JESD22-A103	Assess the ability of the product to withstand long-term high temperature stresses.
LTST	GB/T 2423.1 JESD22-A119	Assess the ability of the product to withstand long periods of low temperature stress.
PCT	JESD22-A102	Assess the moisture resistance of the product package.
HAST	JESD22-A110 JESD22-A118	The non-hermetic package is evaluated for its resistance to moisture under (none) bias conditions.
Reflow	JESD22-A113	Evaluate the thermal resistance and effects of the product during reflow soldering.
BURN-IN	GB/T 4587	The ability of the device to apply electrical stress (voltage, current) and temperature stress (product temperature rise due to load) over a long period of time is assessed.
HTRB	GB/T 4587 JESD22-A108	The ability of the device to withstand long-term electrical stress (voltage) and temperature stress is assessed.
SHT	GB/T 2423.28 JESD22-B106	Assess the heat resistance of the product during its welding.
Solderability	GB/T 2423.28 EIA/IPC/JEDEC J- STD-002	Assess the weldability of the product.
Tin Whisker Test	JESD201 JESD22-A121	Assess the growth of tin whiskers under long-term application of temperature and humidity stress.
Electrical Test	GB/T 4589.1 GB/T 4587 GB/T 4586 GB/T 4023 GB/T 6571	Assess the electrical capacity of the product. Mainly for discrete device product testing.





ITEMS	STANDARD	GOAL
Optical Microscopy Test		Observe the appearance of the sample, surface shape, chip cracks, stains, scratches, oxide layer defects and metal layer corrosion, etc., and measure the size and observation function.
X-RAY Test		Observe the welding wire, load, hollow, etc.
*Ultrasonic Scanning Microscopy	JEDEC J-STD-035-1999	Used to detect interface delamination, voids in plastic bodies, chip cracks, etc.
JUNO Test		Electrical testing of semiconductor devices such as diodes, transistors, digital transistors, and Zener diodes.
*Semiconductor Characteristic Diagram Tester	GB/T 13973-2012	Confirm the failure mode and the failure pin positioning, identify the partial failure mechanism, and any difference between the failure tube and the same batch quality curve needs attention.
Package Unsealing Detection		LASER Opening: used to reduce the thickness of the plastic body, keep the pins Acid-opening: open the inner chip, inner leads and nips with a wet open cap
Chip Probe Station Detection		Probe test chip, observe the electrical parameters or characteristic curves of the chip.
Package Crater Test		Remove the wire and nip metal layer and observe the nip condition
Package Section Analysis Test - Ion Grinding System		Obtain the appropriate observation surface for the sample to observe the joint of the solder joint, layering, void, etc.
	JY-T 010-1996	Observing the short circuit, open circuit, electromigration, pinholes and corrosion of the oxide layer on the surface of the chip can also be used to observe the stacking faults, dislocations, and dimensional measurements of the pattern lines.
*Scanning Electron Microscopy		EDX confirms the surface composition of the sample.
Chip De-layering (RIE) Detection		It is mainly used to solve the observability and testability of the underlying layers of the chip multilayer structure.

