CMT826X High-Speed, Six-Channel Enhanced Digital Isolator

1 Features

- Safety-related certifications
  - DIN VDE V 0884-11: 2017-01
  - UL 1577 component recognition program
  - CSA certification according to IEC 60950-1, IEC 62368-1, IEC 61010-1 and IEC 60601-1 end equipment standards
  - CQC approval per GB4943.1-2022
  - TUV certification according to EN 60950-1, EN 62368-1 and EN 61010-1
- Robust electromagnetic compatibility
  - System-level ESD, EFT, and surge immunity
  - ±8 kV IEC 61000-4-2 contact discharge protection across isolation barrier
  - Low emissions
- Data rate: up to 150 Mbps
- Wide supply range: 2.5 to 5.5 V
- Operation temperature: -40°C to 125°C
- Robust isolation barrier
  - More than 40-year projected lifetime
  - Up to 5 kV_{RMS} isolation rating
  - Up to 8 kV surge capability
  - ±250 kV/μs typical CMTI
- Default output high and low options
- Low power consumption, typical 1.5 mA per channel at 1 Mbps
- Low propagation delay: 9 ns typical (5V supplies)
- SOIC 16 package (wide body and narrow body)

2 Applications

- Industrial automatic control
- New energy vehicles
- Solar inverters
- Motor control
- Isolated SPI
- General purpose multichannel isolation

3 Description

The CMT826X series devices are high-performance, six channel digital isolators with as high as 5 kV_{rms} isolation voltage by means of silicon-dioxide (SiO2) insulation barrier.

The digital isolator is used for communication between two different power supply domains while prevents noise currents on a data bus or other circuits from entering the local ground and interfering with or damaging sensitive circuitry.

CMT826X device has six forward and up to three reverse-direction channels. If the input power or signal is lost, the default output is high for the CMT826X1 device and low for the CMT826X0 device. See the Device Functional Modes section for further details.

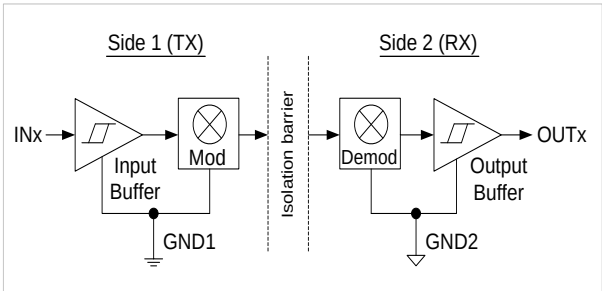
The isolator provides high electromagnetic immunity and low emissions at low-power consumption. Through innovative chip design and layout techniques, electromagnetic compatibility of the CMT826X device has been significantly enhanced to ease system-level ESD, EFT, surge, and emissions compliance.

The CMT826X series device is available in both narrow-body (NB) and wide-body (WB) 16-pin SOIC packages.

Device Information

Part No.	Package	Body Size (mm x mm)
CMT826X	NB(N) SOIC-16	9.9 x 3.9
	WB(W) SOIC-16	10.3 x 7.5
Refer to section 14 for ordering information.		

Simplified Schematic



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4 Absolute Maximum Ratings

Table 1. Absolute Maximum Ratings[1]

Parameters	Symbol	Condition	Min.	Max.	Unit
Power supply voltage[2]	VDD1, VDD2		-0.5	6	V
Maximum input voltage	INx	x = A, B, C, D	-0.4	VDD+0.4	V
Maximum output voltage	OUTx	x = A, B, C, D	-0.4	VDD+0.4	V
Maximum Input / output pulse voltage	-	Pulse width should be less than 100 ns, and duty cycle should be less than 10%	-0.8	VDD+0.8	V
Common-mode transient immunity	CMTI			±250	kV/us
Output current	I_O		-15	15	mA
Maximum surge immunity	-			8	kV
Operating temperature	T_A		-40	125	℃
Storage temperature	T_{STG}		-40	150	℃

Notes:

[1]. Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

[2]. All voltage values except differential I/O bus voltages are with respect to the local ground terminal (GND1 or GND2) and are peak voltage values.

5 Recommended Operating Conditions

Table 2. Recommended Operating Conditions

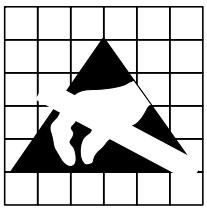
Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Power supply voltage	VDD1, VDD2		2.5	5	5.5	V
High level input voltage	V_{IH}	VDDI: input side VDD	2		VDDI	V
Low level input voltage	V_{IL}	VDDI: input side VDD	0		0.8	V
Data rate	DR		0		150	Mbps
Operating temperature	T_A		-40	25	125	℃
Junction temperature	T_J		-40		150	℃

6 ESD Ratings

Table 3. ESD Ratings

Parameter	Symbol	Condition	Max.	Unit
Electrostatic discharge	V_{ESD}	Human-body model (HBM)	±8000	V
		Charged-device model (CDM)	± 2000	

Notes:
1. IEC ESD strike is applied across the barrier with all pins on each side tied together creating a two-terminal device.
2. Testing is carried out in air or oil to determine the intrinsic contact discharge capability of the device.



Caution! ESD sensitive device. Precaution should be used when handling the device in order to prevent performance degradation or loss of functionality.

7 Pin Description

Both narrow-body (N) and wide-body (W) 16-pin SOIC packages are available for the series part numberCMT8260, CMT8261, CMT8262 and CMT8263. The pin lists are shown as below.

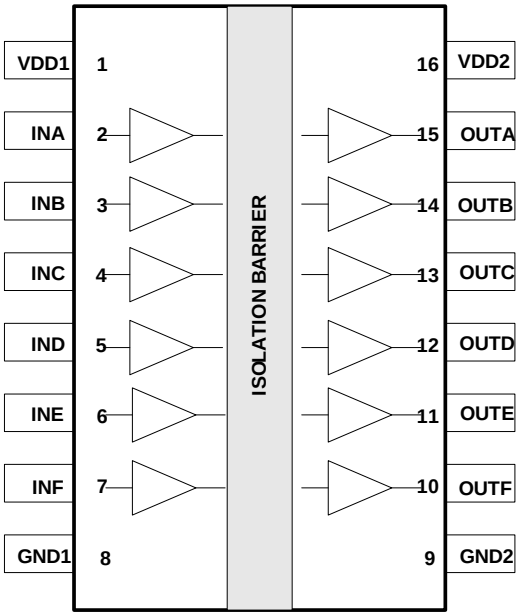


Figure 1. CMT8260 Pin List

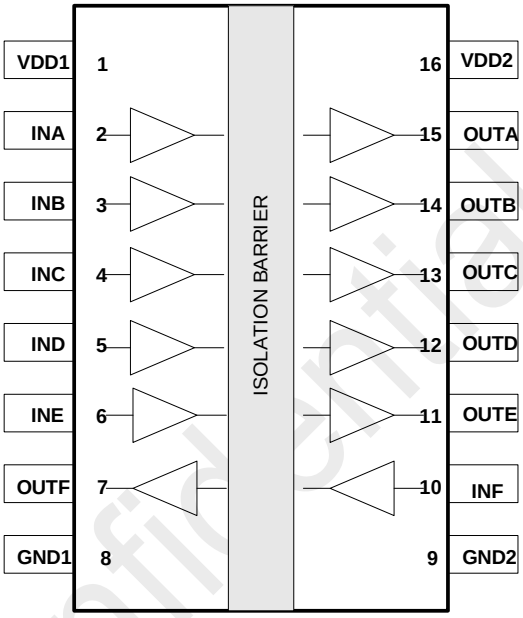


Figure 2. CMT8261 Pin List

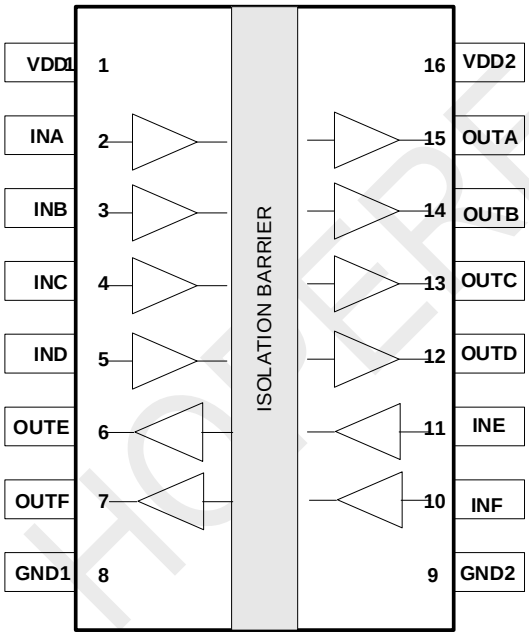


Figure 3. CMT8262 Pin List

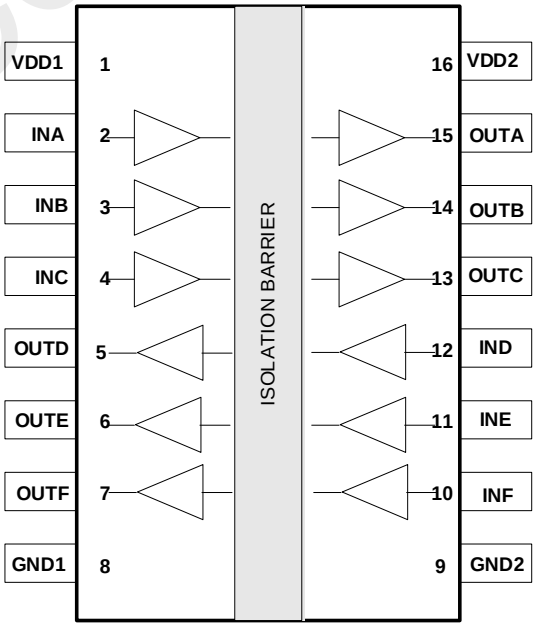


Figure 4. CMT8263 Pin List

Table 4. CMT8260/61/62/63 Pin Description

Pin Name	Pin Number				Description
	CMT8260	CMT8261	CMT8262	CMT8263	
VDD1	1	1	1	1	Power supply for isolator side 1
INA	2	2	2	2	Input, channel A
INB	3	3	3	3	Input, channel B
INC	4	4	4	4	Input, channel C
IND	5	5	5	12	Input, channel D
INE	6	6	11	11	Input, channel E
INF	7	10	10	10	Input, channel F
GND1	8	8	8	8	Ground 1, the ground reference for isolator side 1
GND2	9	9	9	9	Ground 2, the ground reference for isolator side 2
OUTF	10	7	7	7	Output, channel F
OUTE	11	11	6	6	Output, channel E
OUTD	12	12	5	5	Output, channel D
OUTC	13	13	13	13	Output, channel C
OUTB	14	14	14	14	Output, channel B
OUTA	15	15	15	15	Output, channel A
VDD2	16	16	16	16	Power supply for isolator side 2

8 Typical Application

8.1 Typical Application Schematic

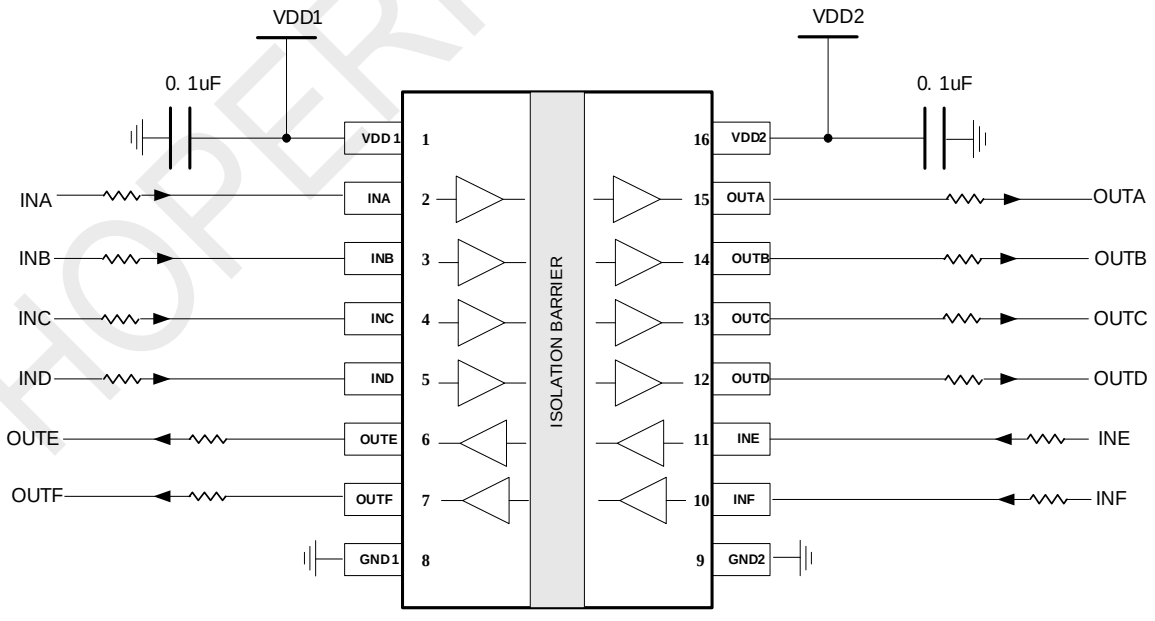


Figure 1. Typical Application Schematic (Take the CMT8262 as an example)

Note: *users should be careful not to connect ground and VDD reversely.*

8.2 PCB Layout Guidelines

The CMT826X requires a 0.1 μF bypass capacitor in both input side and output side. The capacitor should be placed as close as possible to the package pin of VDD1 and VDD2 respectively. The figures below show the recommended PCB layout. Please make sure the space under the chip keeps free from planes, traces, pads and via. To enhance the robustness of design, users may also include resistors (50 ~ 300 Ω) in series with the inputs and outputs if the system is excessively noisy. The series resistors also improve the system reliability such as latch-up immunity.

The typical output impedance of an isolator driver channel is approximately 50 Ω ± 40%. When driving loads where transmission line effects will be a factor, output pins should be appropriately terminated with controlled impedance PCB traces.

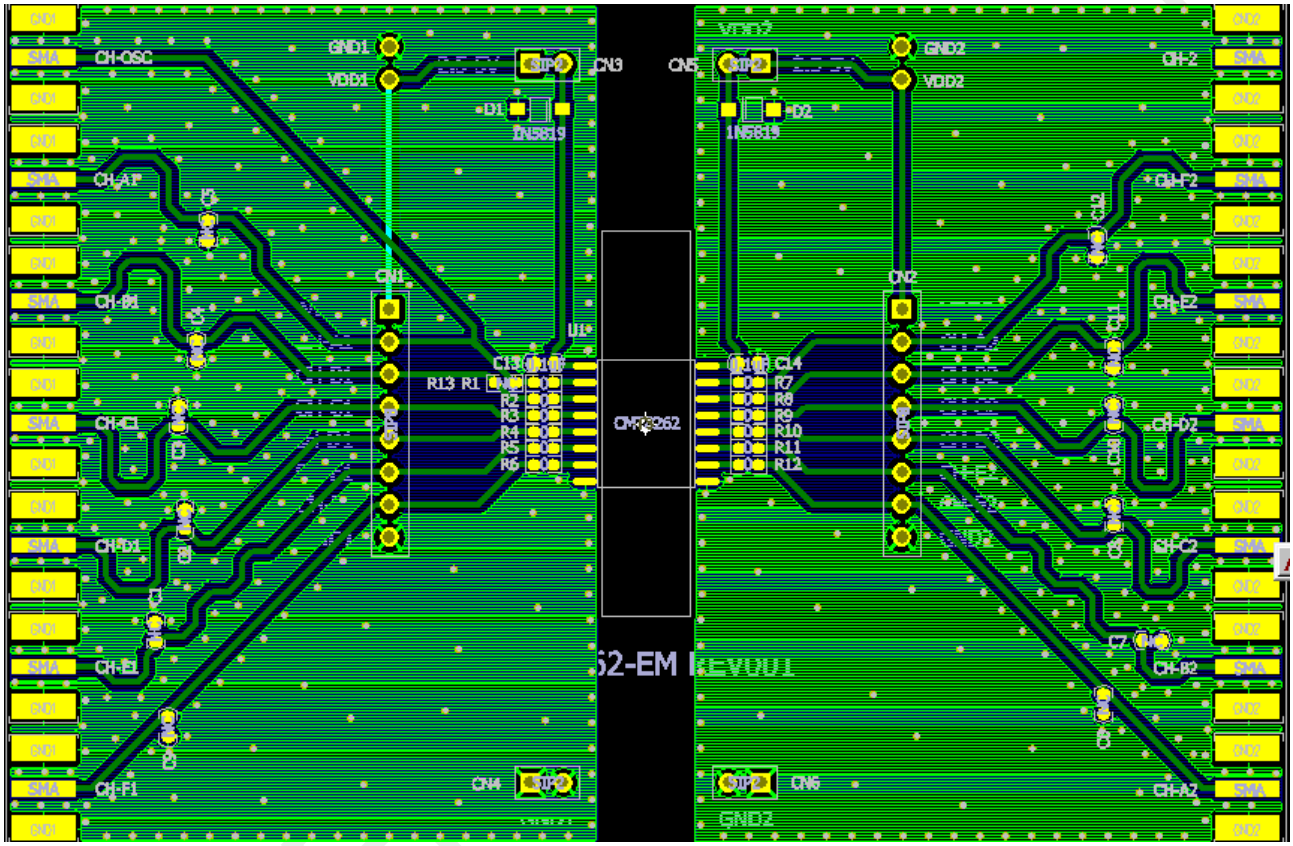


Figure 2. Recommended PCB Layout

9 Parameter Measurement Circuit Setup

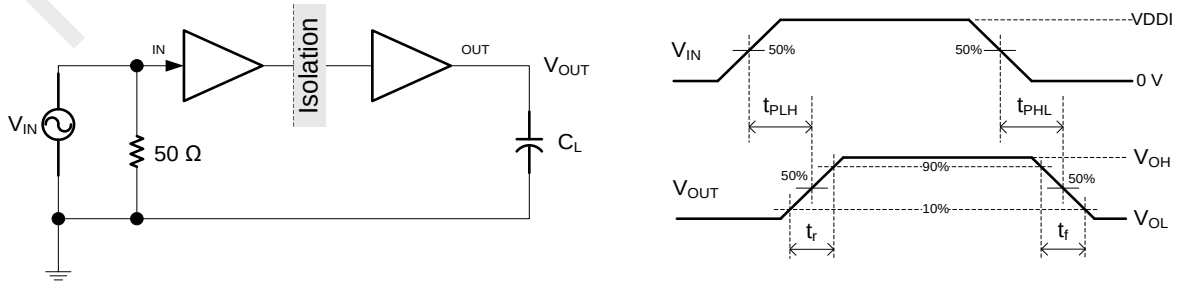


Figure 3. Switching Characteristics Test Circuit and Voltage Waveforms

Notes:

1. The input pulse is supplied by a generator, V_{IN} has the following characteristics: f_{PULSE} ≤ 100 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input side, 50 Ω resistor is required to terminate input generator signal. It is not needed in actual application.
2. Load capacitance influences the measurement results quite a lot, including instrumentation and fixture capacitance, totally no more than 15 pF loading is preferred.

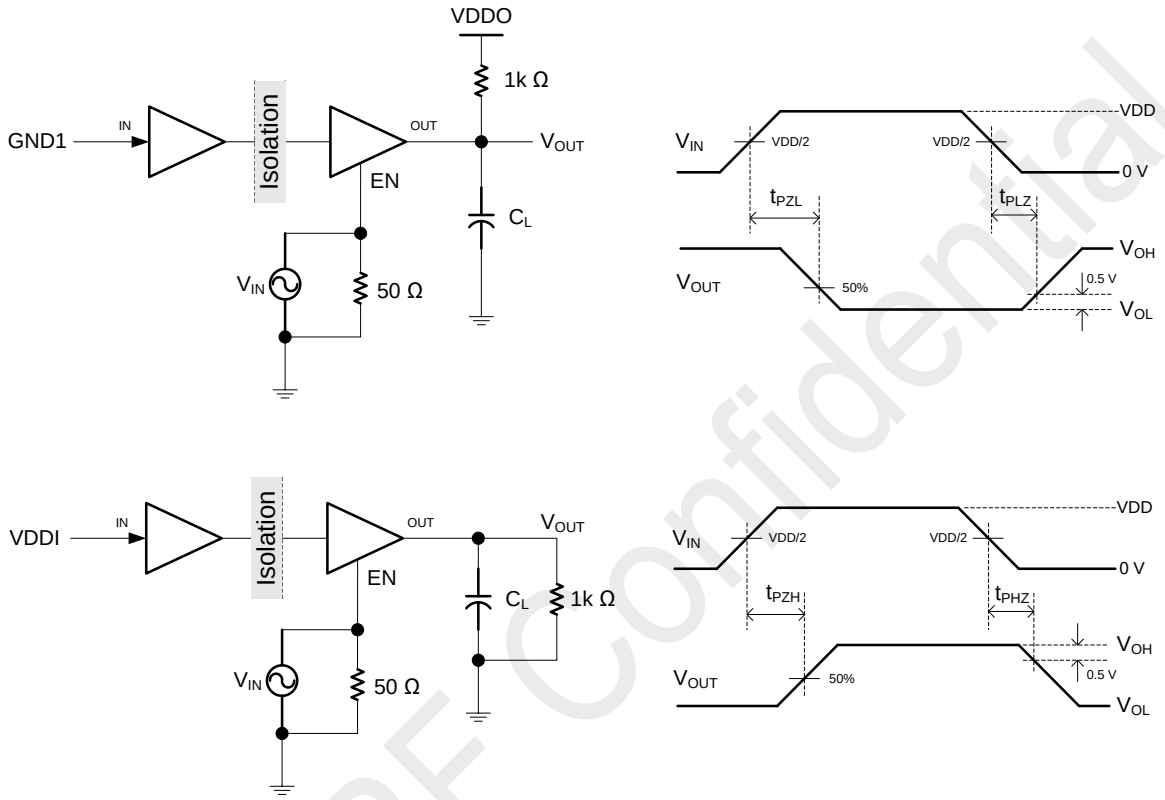


Figure 4. Enable/Disable Propagation Delay Time Test Circuit and Waveform

Notes:

1. The input pulse is supplied by a generator having the following characteristics: f_{PULSE} ≤ 10 kHz, 50% duty cycle, tr ≤ 3 ns, tf ≤ 3 ns, Z_O = 50 Ω.
2. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

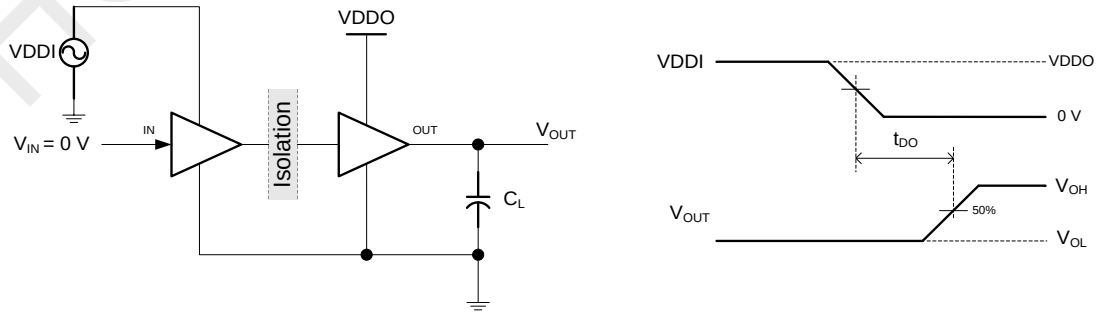


Figure 5. Default Output Delay Time Test Circuit and Voltage Waveforms

Notes:

1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.
2. Power supply ramp rate = 10 mV/ns.

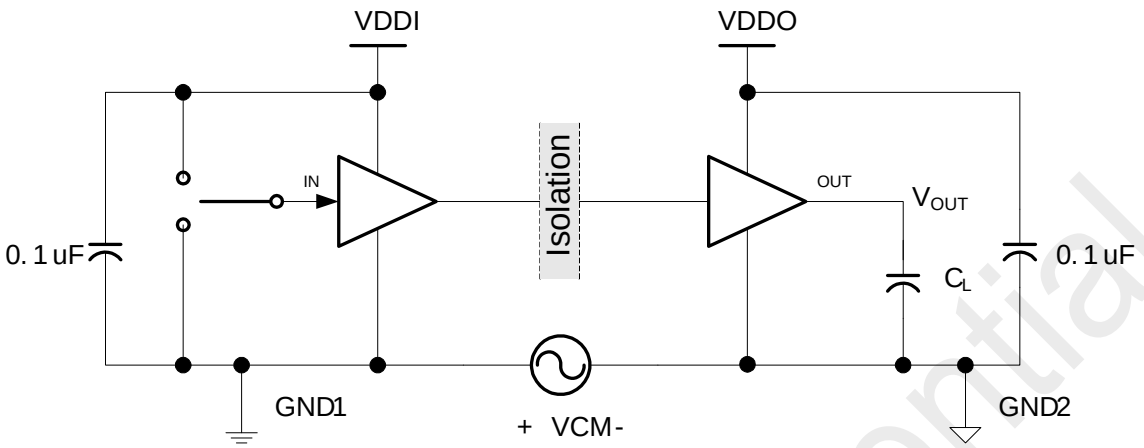


Figure 6. Common-Mode Transient Immunity Test Circuit

Notes:

1. C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

10 Electrical Specifications

10.1 Electrical Characteristics with 5 V Supply

VDD1 =VDD2= 5V, T_A= -40 to 125 ℃.

Table 5. Electrical Characteristics with 5 V Supply

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Power on reset	V_{POR}	POR threshold as during power- up		2.3		V
	V_{HYS}	POR threshold hysteresis		0.1		V
Input threshold	V_{IT}	Input threshold at rising edge		1.6		V
	V_{ITHYS}	Input threshold hysteresis		0.4		V
High level input voltage	V_{IH}		2			V
Low level input voltage	V_{IL}				0.8	V
High level output voltage	V_{OH}	I_{OH} =-4mA	VDD- 0.3			V
Low level output voltage	V_{OL}	I_{OL} = 4mA			0.3	V
Output impedance	R_O			50		Ω
Input pull high or low current	Ipull			13		uA
Start-up time after POR	trbs			30		us
Common mode transient Immunity	CMTI		150	250	270	kV/us

10.2 Supply Current Characteristics with 5 V Supply

VDD1 = VDD2 = 5V, T_A= -40 to 125 ℃.

Table 6. Supply Current Characteristics with 5 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8260				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.34		mA
	I_{DD2}	3.09		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	10.56		mA
	I_{DD2}	3.24		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.88		mA
	I_{DD2}	3.28		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.94		mA
	I_{DD2}	4.47		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	8.22		mA
	I_{DD2}	28.96		mA
CMT8261				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	1.69		mA
	I_{DD2}	3.36		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	9.25		mA
	I_{DD2}	4.98		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.50		mA
	I_{DD2}	4.39		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.84		mA
	I_{DD2}	6.42		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	9.68		mA
	I_{DD2}	27.68		mA
CMT8262				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	2.13		mA
	I_{DD2}	2.99		mA
Supply current: device is disabled. EN = VDDI, V_{IN} =VDDI,	I_{DD1}	8.27		mA
	I_{DD2}	6.12		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.26		mA
	I_{DD2}	4.74		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.97		mA
	I_{DD2}	6.32		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	13.87		mA
	I_{DD2}	22.16		mA
CMT8263				
Supply current	I_{DD1}	2.56		mA

Parameter	Symbol	Typ.	Max.	Unit
EN = VDDI, V_{IN} =0 V	I_{DD2}	2.51		mA
Supply current: device is disabled. EN = VDDI, VIN =VDDI,	I_{DD1}	7.31		mA
	I_{DD2}	7.13		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, CL = 15 pF	I_{DD1}	5.04		mA
	I_{DD2}	4.99		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	6.20		mA
	I_{DD2}	6.29		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	18.30		mA
	I_{DD2}	19.04		mA

Table 7-1. Supply Current with 5 V Supply- Characteristics of CMT826X

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, CL = 15 pF		5		ns
Propagation delay rising	t_{PLH}	See figure 6, CL = 15 pF		7.53		ns
Propagation delay falling	t_{PHL}	See figure 6, CL = 15 pF		8.43		ns
Pulse width distortion |t PHL – t PLH |	PWD	See figure 6, CL = 15 pF		0.9		ns
Rising time	tr	See figure 6, CL = 15 pF		0.8		ns
Falling time	tf	See figure 6, CL = 15 pF		0.85		ns
Peak eye diagram Jitter	t_{JIT}(PK)			400		ps
Channel-to-channel delay Skew	t_{SK}(c2c)			0.3		ns
Part-to-part delay skew	t_{SK}(p2p)					ns

10.3 Supply Current Characteristics with 3.3 V Supply

VDD1 = VDD2 = 3.3V, T_A= -40 to 125 ℃.

Table 8. Supply Current Characteristics with 3.3 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8260				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.34		mA
	I_{DD2}	3.08		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	10.46		mA
	I_{DD2}	3.23		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.89		mA
	I_{DD2}	3.33		mA
Supply current: 10 Mbps square wave clock input AC signal.	I_{DD1}	5.95		mA

Parameter	Symbol	Typ.	Max.	Unit
All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD2}	4.88		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	7.10		mA
	I_{DD2}	21.12		mA
CMT8261				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	1.73		mA
	I_{DD2}	3.28		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	9.43		mA
	I_{DD2}	4.89		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.59		mA
	I_{DD2}	4.23		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.78		mA
	I_{DD2}	5.58		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	9.61		mA
	I_{DD2}	19.86		mA
CMT8262				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	2.11		mA
	I_{DD2}	2.97		mA
Supply current: device is disabled. EN = VDDI, V_{IN} =VDDI,	I_{DD1}	8.22		mA
	I_{DD2}	6.09		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.20		mA
	I_{DD2}	4.66		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.63		mA
	I_{DD2}	5.71		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	11.92		mA
	I_{DD2}	16.61		mA
CMT8263				
Supply current EN = VDDI, V_{IN} =0 V	IDD1	2.54		mA
	IDD2	2.50		mA
Supply current: device is disabled. EN = VDDI, VIN =VDDI,	IDD1	7.27		mA
	IDD2	7.10		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	IDD1	4.97		mA
	IDD2	4.91		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	IDD1	5.70		mA
	IDD2	5.78		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	IDD1	14.70		mA
	IDD2	14.74		mA

Table 9-1. Supply Current with 3.3 V Supply - Characteristics of CMT826X

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, C_L = 15 pF		5		ns
Propagation delay rising	t_{PLH}	See figure 6, C_L = 15 pF		8		ns
Propagation delay falling	t_{PHL}	See figure 6, C_L = 15 pF		8.7		ns
Pulse width distortion |t PHL – t PLH |	PWD	See figure 6, C_L = 15 pF		0.7		ns
Rising time	t_r	See figure 6, C_L = 15 pF		1		ns
Falling time	t_f	See figure 6, C_L = 15 pF		0.9		ns
Peak eye diagram Jitter	t_{JIT}(PK)			400		ps
Channel-to-channel Delay Skew	t_{SK}(c2c)			0.5		ns
Part-to-part delay skew	t_{SK}(p2p)					ns

10.4 Supply Current Characteristics with 2.5 V Supply

VDD1 = VDD2 = 2.5 V, T_A= -40 to 125 ℃.

Table 10. Supply Current Characteristics with 2.5 V Supply

Parameter	Symbol	Typ.	Max.	Unit
CMT8260				
Supply current EN = VDDI,V_{IN} =0 V	I_{DD1}	1.33		mA
	I_{DD2}	3.16		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	10.46		mA
	I_{DD2}	3.30		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.87		mA
	I_{DD2}	3.37		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	6.00		mA
	I_{DD2}	5.80		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.44		mA
	I_{DD2}	16.83		mA
CMT8261				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	1.67		mA
	I_{DD2}	3.34		mA
Supply current: device is disabled. EN = VDDI,V_{IN} =VDDI,	I_{DD1}	9.16		mA
	I_{DD2}	4.95		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.42		mA
	I_{DD2}	4.26		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.55		mA
	I_{DD2}	5.29		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	7.30		mA
	I_{DD2}	16.00		mA
CMT8262				
Supply current EN = VDDI, V_{IN} =0 V	I_{DD1}	2.16		mA
	I_{DD2}	2.95		mA
Supply current: device is disabled. EN = VDDI, V_{IN} =VDDI,	I_{DD1}	8.33		mA
	I_{DD2}	6.04		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.26		mA
	I_{DD2}	4.59		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	I_{DD1}	5.56		mA
	I_{DD2}	5.40		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	I_{DD1}	9.37		mA
	I_{DD2}	13.51		mA
CMT8263				
Supply current	IDD1	2.54		mA

Parameter	Symbol	Typ.	Max.	Unit
EN = VDDI, V_{IN} =0 V	IDD2	2.49		mA
Supply current: device is disabled. EN = VDDI, VIN =VDDI,	IDD1	7.24		mA
	IDD2	7.08		mA
Supply current: 1 Mbps square wave clock input AC signal. All channels switching with 1 Mbps square wave input, C_L = 15 pF	IDD1	4.94		mA
	IDD2	4.88		mA
Supply current: 10 Mbps square wave clock input AC signal. All channels switching with 10 Mbps square wave input, C_L = 15 pF	IDD1	5.47		mA
	IDD2	5.53		mA
Supply current: 100 Mbps square wave clock input AC signal. All channels switching with 100 Mbps square wave input, C_L = 15 pF	IDD1	11.47		mA
	IDD2	11.91		mA

Table 11-1. Supply Current with 2.5 V Supply - Characteristics of CMT826X

Parameters	Symbol	Condition	Min.	Typ.	Max.	Unit
Data rate	DR		0	150		Mbps
Minimum pulse width	PW	See figure 6, C_L = 15 pF		5		ns
Propagation delay rising	t_{PLH}	See figure 6, C_L = 15 pF		8.63		ns
Propagation delay falling	t_{PHL}	See figure 6, C_L = 15 pF		9.11		ns
Pulse width distortion |t PHL – t PLH |	PWD	See figure 6, C_L = 15 pF		0.48		ns
Rising time	t_r	See figure 6, C_L = 15 pF		1.04		ns
Falling time	t_f	See figure 6, C_L = 15 pF		1.23		ns
Peak eye diagram Jitter	t_{JIT}(PK)			400		ps
Channel-to-channel Delay Skew	t_{SK}(c2c)			0.7		ns
Part-to-part delay skew	t_{SK}(p2p)			0		ns

10.5 Typical Characteristics

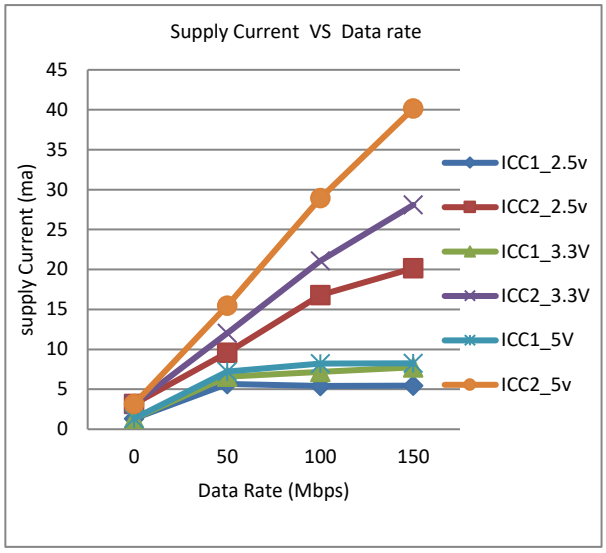


Figure 9-1. Supply Current vs. Data Rate (with 15-pF Load) T_A=25℃ C_L=15pF

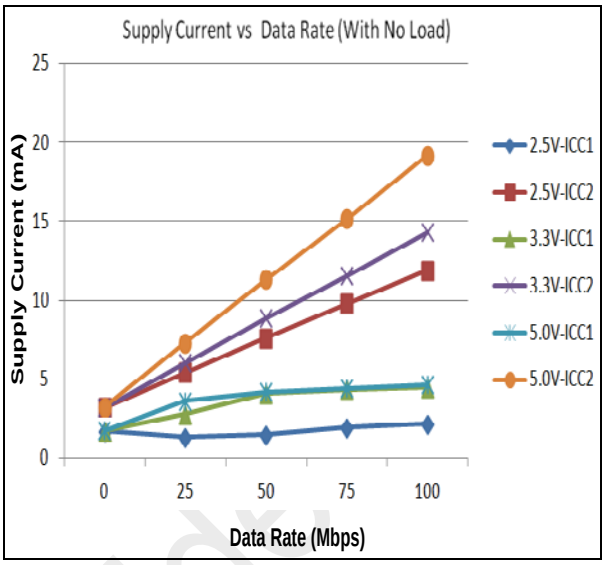


Figure 9-2. Supply Current vs. Data Rate (with No Load) T_A=25℃ C_L=No Load

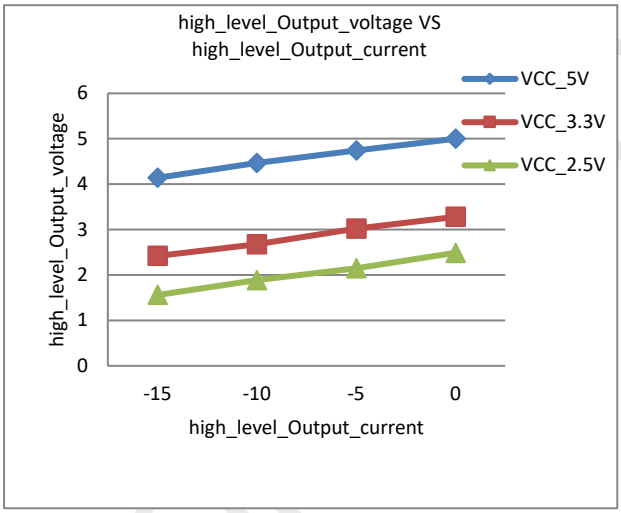


Figure 9-3. High-Level Output Voltage vs. High-Level Output Current (T_A=25℃)

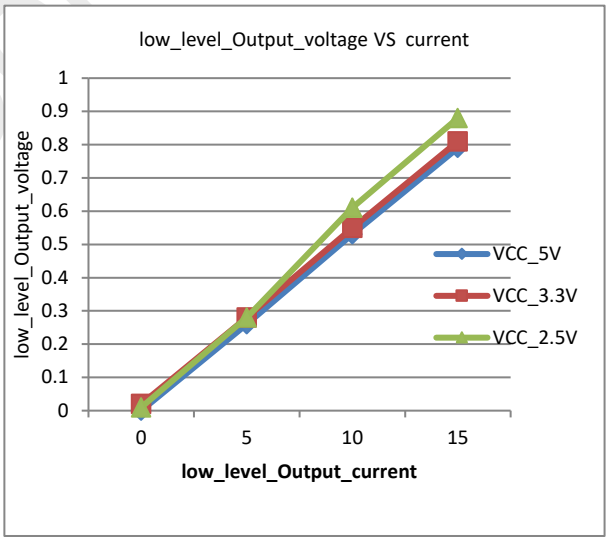


Figure 9-4. Low-Level Output Voltage vs. Low-Level Output Current (T_A=25℃)

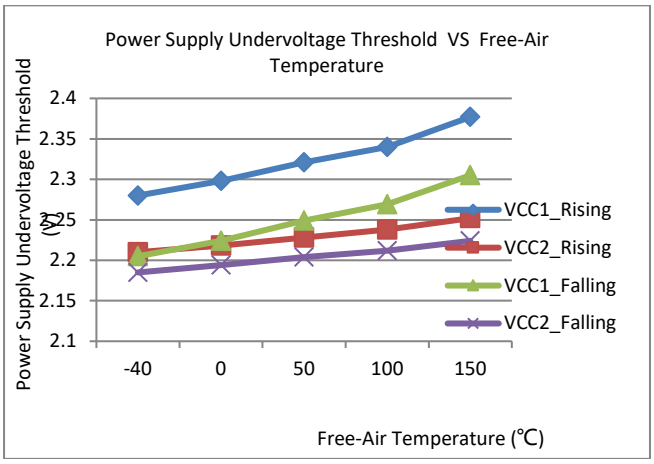


Figure 9-5. Power Supply Under-voltage Threshold vs. Free-Air Temperature

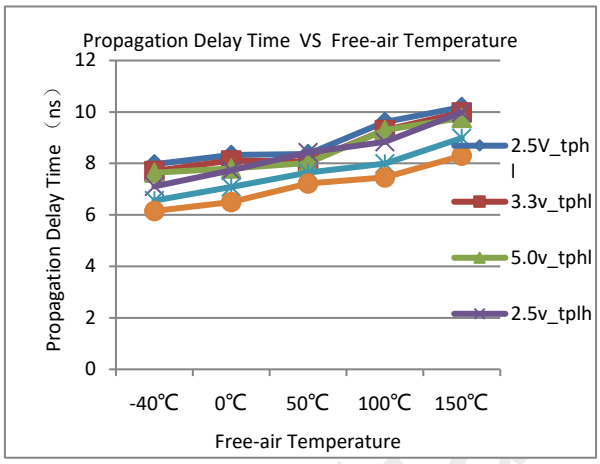


Figure 9-6. Propagation Delay Time vs. Free-Air Temperature

10.6 Insulation Specifications

Table 12. Insulation Specifications

Parameters	Sym.	Condition	Value		Unit
			NB SOIC-16	WB SOIC-16	
External clearance[1]	CLR	The shortest terminal-to-terminal distance through air	4.0	8.0	mm
External creepage[1]	CRP	The shortest terminal-to-terminal distance across the package surface	4.0	8.0	mm
Distance through insulation	DTI	Minimum internal gap	32	32	um
Comparative tracking index	CTI	DIN EN 60112 (VDE 0303-11);IEC 60112	> 400	> 600	V
Material group	-		1	1	-
Overvoltage category per IEC 60664-1	-	Rated mains voltage ≤ 300 V_{RMS}	I	I	-
		Rated mains voltage ≤ 600 V_{RMS}	I-IV	I-IV	-
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	I-III	-
DIN VDE V 0884-11:2017-01[2]					
Maximum peak isolation voltage	V_{IORM}		565	2121	V_{pk}
Maximum isolation working voltage	V_{IOWM}	AC voltage (sine wave); Time dependent dielectric breakdown (TDDB) test	400	1500	V_{RMS}
		DC voltage		2121	V_{DC}
Maximum transient isolation voltage	V_{IOTM}	V_{TEST} = V_{IOTM},t = 60 s (qualification); t = 1 s (100% production)	5300	8000	V_{pk}
Maximum surge isolation voltage[3]	V_{IOSM}	Test method per IEC60065, 1.2/50 us waveform, V_{TEST} = 1.6 x V_{IOSM} (qualification)	5300	8000	V_{pk}
Apparent charge[4]	q_{pd}	Method a: After I/O safety test subgroup 2/3, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.2 × V_{IORM}, t_m = 10 s		<5	≤5pC
		Method a: After environmental tests subgroup 1, V_{ini} = V_{IOTM}, t_{ini} = 60 s; $V_{pd(m)}$ = 1.6 × V_{IORM}, t_m = 10 s		<5	

		Method b1: At routine test (100% production) and preconditioning (type test) $V_{ini} = V_{IOTM}$, t_{ini} = 1 s; $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s		<5	
Isolation capacitance, input to output[5]	C_{IO}	V_{IO} = 0.4 x sin (2πft), f = 1 MHz	1.2	1.2	pF
Isolation resistance, input to output[5]	R_{IO}	V_{IO} = 500 V	$>10^{10}$	$>10^{10}$	Ω
UL 1577					
Withstand isolation voltage	V_{ISO}	$V_{TEST} = V_{ISO}$, t = 60 s (qualification); $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production)	3750	5000	V_{RMS}

Notes:

[1]. Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance. Creepage and clearance on a printed-circuit board are equal in certain cases. Techniques such as inserting grooves and ribs on printed-circuit board can help to improve the specifications.

[2]. This coupler is suitable for safe electrical insulation only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.

[3]. Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

[4]. Apparent charge is electrical discharge caused by a partial discharge (pd).

[5]. All pins on each side of the barrier are tied together creating a two-terminal device.

10.7 Safety-related Certifications

Table 13. Safety-related Certifications

VDE	CSA	UL	CQC	TUV
DIN VDE V0884-11:2017-01 （Patents pending）	IEC 60950-1, IEC 62368-1 and IEC 61010-1 （Patents pending）	Recognized under UL 1577 Component Recognition Program （Patents pending）	GB 4943.1-2011 （Patents pending）	EN 61010-1:2010 (3rd Ed) and EN 60950-1:2006/A2: 2013 （Patents pending）
Certificate number: pending	Master contract number: pending	File number: pending	Certificate number: pending	Client ID number: pending

10.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier potentially leading to secondary system failures

Table 14. Safety Limiting Values

Parameters	Symbol	Test Condition	Value		Unit
			NB SOIC-16	WB SOIC-16	
Safety input, output, or supply current	Is	$R_{\theta JA}$ = 140 °C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C	160		mA
		$R_{\theta JA}$ = 84 °C/W, V_I = 5.5 V, T_J = 125 °C, T_A = 25 °C		237	mA
Total power dissipation at 25℃	Ps			1499	W
Case temperature	Ts		125	125	℃

10.9 Thermal Information

Table 15. Thermal Information

Parameter	Symbol	Value		Unit
		NB SOIC-16	WB SOIC-16	
Junction-to-ambient thermal resistance	θ_{JA}	78.9	78.9	°C/W
Junction-to-case (top) thermal resistance	$\theta_{JC(top)}$	41.1	41.6	°C/W
Junction-to-board thermal resistance	θ_{JB}	49.5	43.6	°C/W

11 Function Description

11.1 Function Overview

The CMT826X device is a high-performance, quad-channel digital isolator with 5000 V_{RMS} isolation ratings. CMT826X has an On-Off keying (OOK) modulation scheme to transmit the digital data across a silicon dioxide based isolation barrier. The transmitter sends a high-frequency carrier across the barrier to represent one digital state and sends no signal to represent the other digital state. The receiver demodulates the signal after advanced signal conditioning and produces the output through a buffer stage. If the ENx pin is low then the output goes to high impedance. The CMT826X also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions due to the high frequency carrier and IO buffer switching. The figure below shows a conceptual detail of how the On-Off keying scheme works.

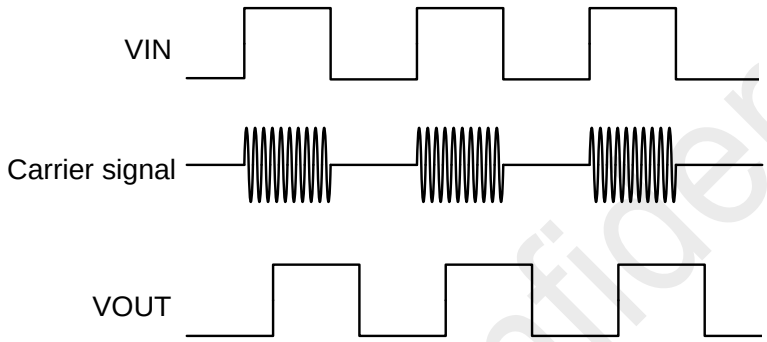


Figure 7. On-Off Keying Based Modulation Scheme

11.2 Functional Modes

The table below lists the functional modes of CMT826X.

Table 16. Function Table[1]

V_{DD1}	V_{DD2}	Input (INx)[2]	Output Enable (ENx)	Output (OUTx)	Comment
PU	PU	H	H or open	H	Normal operation: The channel output assumes the logic state of its input
		L	H or open	L	
		Open	H or open	Default	Default mode: when INx is open, the corresponding channel output goes to its default logic state
X	PU	X	L	Z	A low value of output enabling will output the high impedance
PD	PU	X	H or open	Default	Default mode: when VDDI is unpowered, a channel output assumes the logic state based on the selected default option. When VDD1 transitions from unpowered to powered-up, a channel output assumes the logic state of the input. When VDD1 transitions from powered-up to unpowered, channel output assumes the selected default state
X	PD	X	X	Undetermined	When VDD2 is unpowered, a channel output is undetermined[3]. When VDD2 transitions from unpowered to powered-up, a channel output assumes the logic state of the input

Notes:

[1]. VDDI = Input-side VDD; VDD2 = output-side VDD; PU = Powered up (VDD ≥ 2.6 V); PD = Powered down (VDD ≤ 1.7 V); X = Irrelevant; H= High level; L = Low level; Z = High Impedance.

[2]. A strongly driven input signal can weakly power the floating VDD through an internal protection diode and cause undetermined output.

[3]. The outputs are in undetermined state when 1.7 V < VDD1, VDD2< 2.5V.

11.3 Insulation Lifetime

Insulation lifetime projection data is collected by using industry-standard Time Dependent Dielectric Breakdown (TDDB) test method. In this test, all pins on each side of the barrier are tied together creating a two-terminal device and high voltage applied between the two sides; See the figure below for TDDB test setup. The insulation breakdown data is collected at various high voltages switching at 60 Hz over temperature. For reinforced insulation, VDE standard requires the use of TDDB projection line with failure rate of less than 1 part per million (ppm). Even though the expected minimum insulation lifetime is 20 years at the specified working isolation voltage, VDE reinforced certification requires additional safety margin of 20% for working voltage and 87.5% for lifetime which translates into minimum required insulation lifetime of 37.5 years at a working voltage that's 20% higher than the specified value.

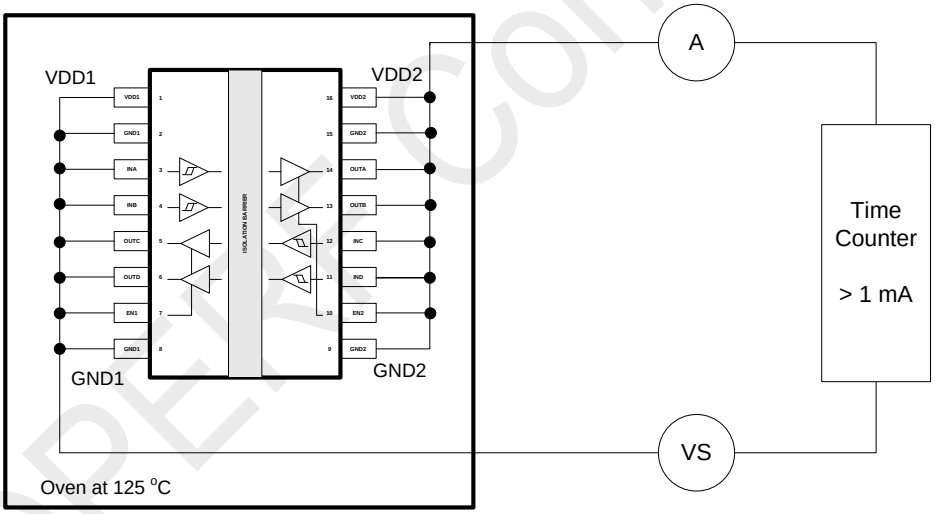


Figure 8. Test Setup for Insulation Lifetime Measurement

12 Packaging Information

The packaging information of the CMT826X SOIC16 is shown in the figures below.

12.1 CMT826X Narrow Body SOIC-16 Packaging

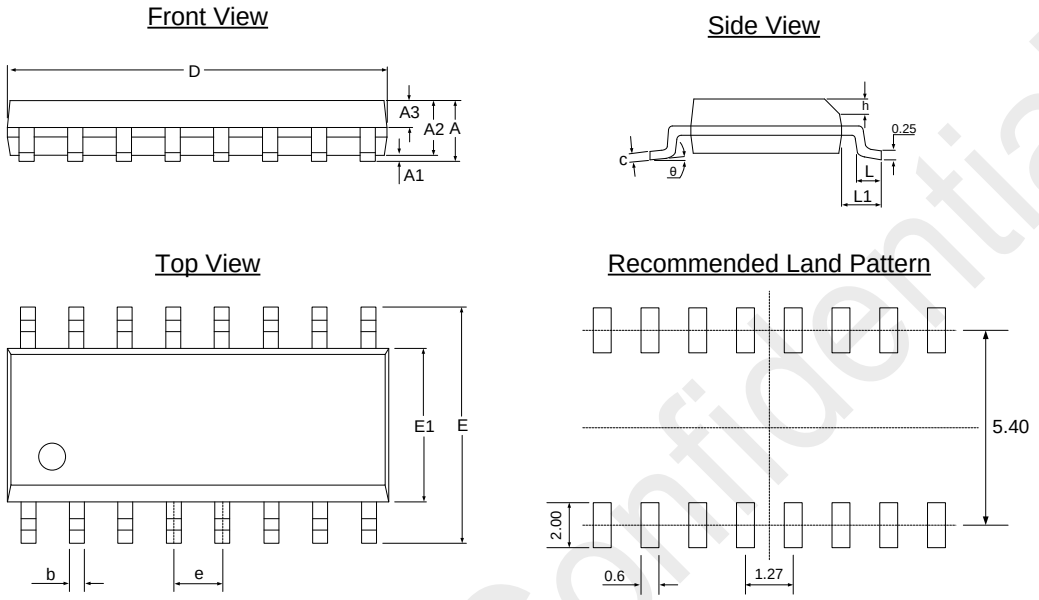


Figure 9. Narrow Body SOIC-16 Packaging

Table 17.Narrow Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	1.75
A1	0.10	-	0.25
b	0.36	-	0.49
c	0.19	-	0.25
D	9.80	9.90	10.0
E	5.80	-	6.20
E1	3.80	3.90	4.00
e	1.27		
L	0.40	-	1.00
L1	1.05		
θ	0	-	8°

12.2 CMT826X Wide Body SOIC-16 Packaging

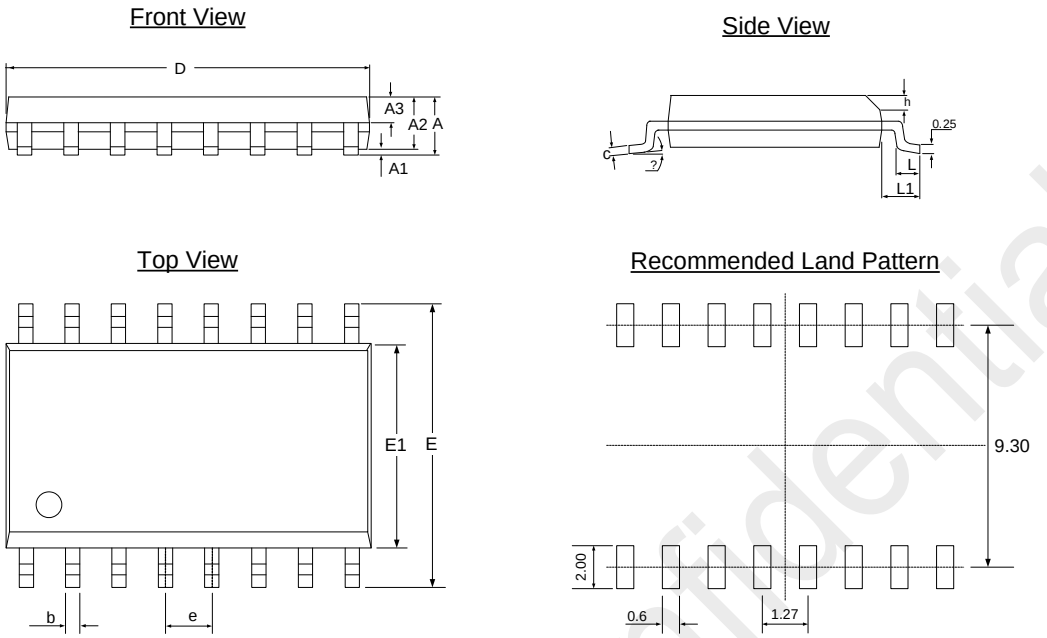


Figure 10. Wide Body SOIC-16 Packaging

Table 18. Wide Body SOIC-16 Packaging Scale

Symbol	Scale (mm)		
	Min.	Typ.	Max.
A	-	-	2.65
A1	0.10	0.20	0.30
A2	2.25	2.30	2.35
A3	1.00	1.05	1.10
b	0.35	0.37	0.43
c	0.15	0.20	0.30
D	10.30	10.40	10.50
E	10.10	10.30	10.50
E1	7.40	7.50	7.60
e	1.14	1.27	1.40
L	0.65	0.70	0.85
L1	1.40		
θ	0	-	8°

13 Top Marking

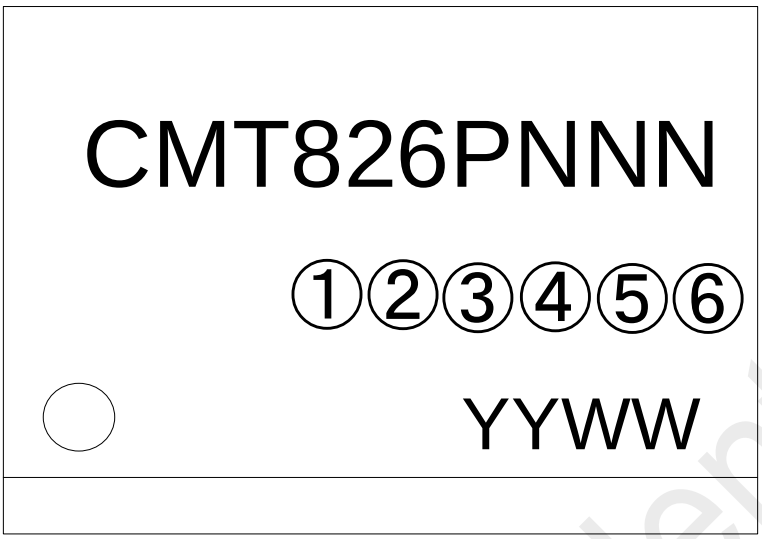


Figure 11. CMT826X Top Marking

Table 19. CMT826X Top Marking Information

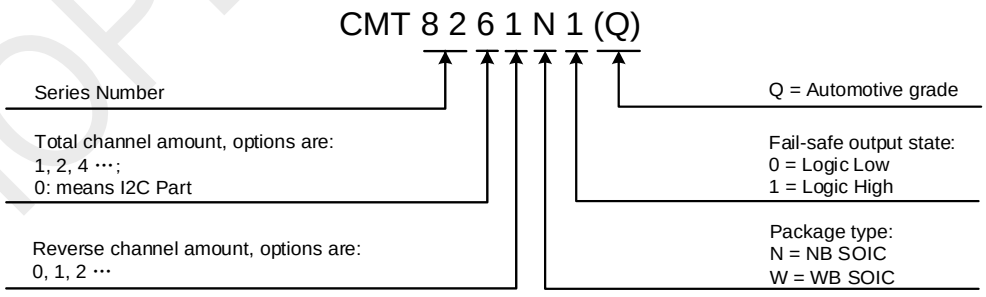
Marking Method	Laser
Pin 1 Mark	Diameter of the circle = 1 mm
Font Size	0.5 mm, align right
Line 1 Marking	P = 0 / 1 / 2, refers to part number CMT8260x/ CMT8261x/ CMT826X/CMT8263x respectively. NNN is the last characters following CMT826X in part number naming. See Chapter 14 Part number naming rule for details
Line 2 Marking	①②③④⑤⑥ is internal trace code
Line 3 Marking	YYWW is the package date number while YY is the last 2 digits of the year and WW is the working week.

14 Ordering Information

Table 20. Part Number List

Part Number	MOQ	Isolation Voltage (kV)	Numbers of total channel	Nmubers of forward channels	Nmubers of reverse channels	Max Data Rate (Mbps)	Default Output Level	Automotive Grade	Package
CMT8260W0	1000	5	6	6	0	150	Low	No	WB SOIC-16
CMT8260W1	1000	5	6	6	0	150	High	No	WB SOIC-16
CMT8261W0	1000	5	6	5	1	150	Low	No	WB SOIC-16
CMT8261W1	1000	5	6	5	1	150	High	No	WB SOIC-16
CMT8262W0	1000	5	6	4	2	150	Low	No	WB SOIC-16
CMT8262W1	1000	5	6	4	2	150	High	No	WB SOIC-16
CMT8263W0	1000	5	6	3	3	150	Low	No	WB SOIC-16
CMT8263W1	1000	5	6	3	3	150	High	No	WB SOIC-16
CMT8260N0	3000	3.75	6	6	0	150	Low	No	NB SOIC-16
CMT8260N1	3000	3.75	6	6	0	150	High	No	NB SOIC-16
CMT8261N0	3000	3.75	6	5	1	150	Low	No	NB SOIC-16
CMT8261N1	3000	3.75	6	5	1	150	High	No	NB SOIC-16
CMT8262N0	3000	3.75	6	4	2	150	Low	No	NB SOIC-16
CMT8262N1	3000	3.75	6	4	2	150	High	No	NB SOIC-16
CMT8263N0	3000	3.75	6	3	3	150	Low	No	NB SOIC-16
CMT8263N1	3000	3.75	6	3	3	150	High	No	NB SOIC-16

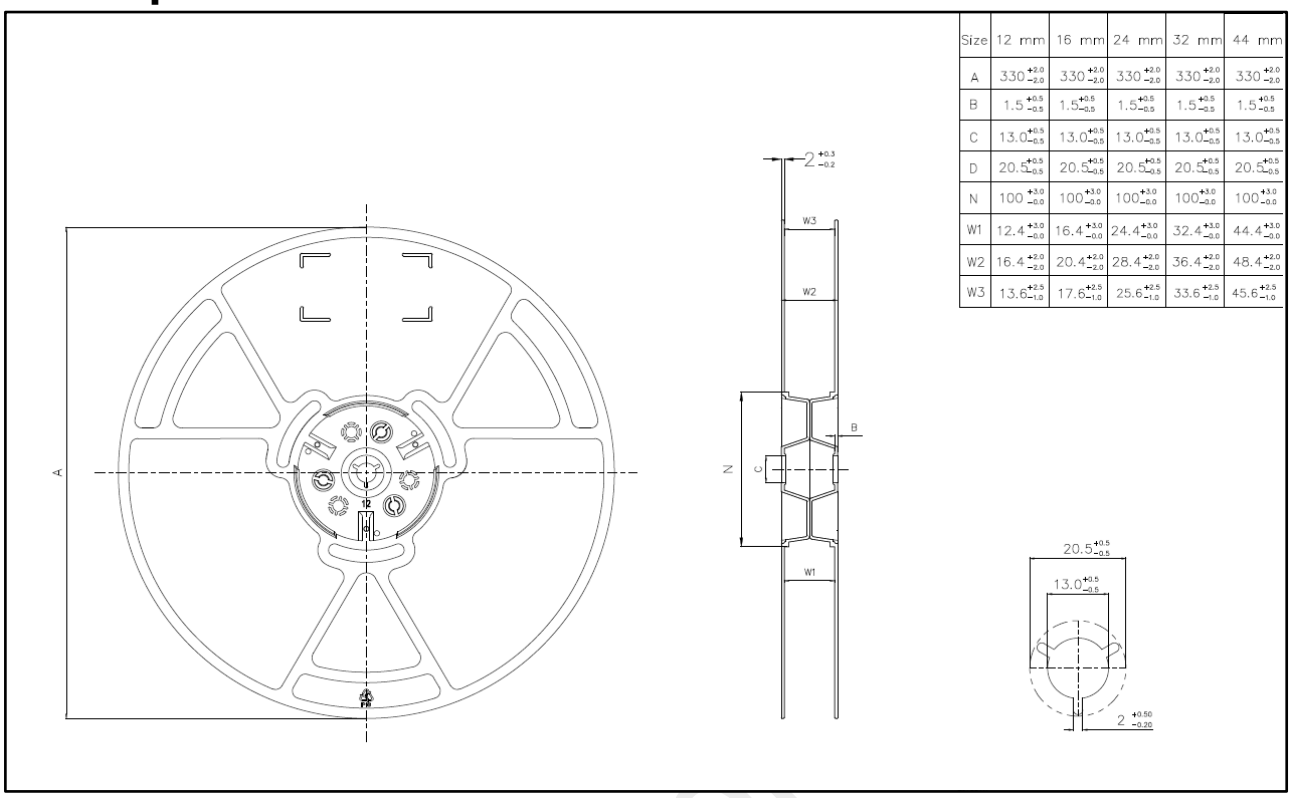
Part Number Naming Rule:



Please visit www.hoperf.com for more product/product line information.

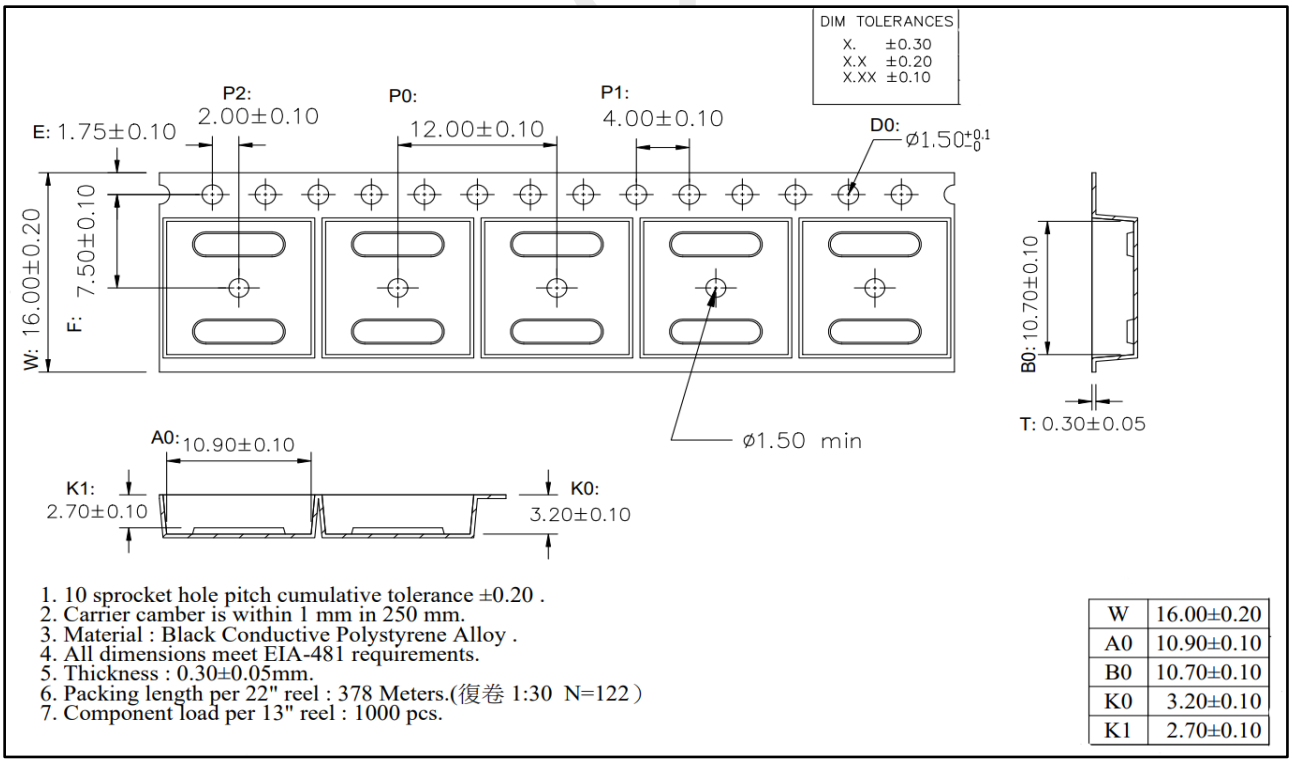
Please contact sales@hoperf.com or your local sales representative for sales or pricing requirements.

15 Tape and Reel Information



Size	12 mm	16 mm	24 mm	32 mm	44 mm
A	330 +2.0 -2.0	330 +2.0 -2.0	330 +2.0 -2.0	330 +2.0 -2.0	330 +2.0 -2.0
B	1.5 +0.5 -0.5	1.5 +0.5 -0.5	1.5 +0.5 -0.5	1.5 +0.5 -0.5	1.5 +0.5 -0.5
C	13.0 +0.5 -0.5	13.0 +0.5 -0.5	13.0 +0.5 -0.5	13.0 +0.5 -0.5	13.0 +0.5 -0.5
D	20.5 +0.5 -0.5	20.5 +0.5 -0.5	20.5 +0.5 -0.5	20.5 +0.5 -0.5	20.5 +0.5 -0.5
N	100 +3.0 -0.0	100 +3.0 -0.0	100 +3.0 -0.0	100 +3.0 -0.0	100 +3.0 -0.0
W1	12.4 +3.0 -0.0	16.4 +3.0 -0.0	24.4 +3.0 -0.0	32.4 +3.0 -0.0	44.4 +3.0 -0.0
W2	16.4 +2.0 -2.0	20.4 +2.0 -2.0	28.4 +2.0 -2.0	36.4 +2.0 -2.0	48.4 +2.0 -2.0
W3	13.6 +2.5 -1.0	17.6 +2.5 -1.0	25.6 +2.5 -1.0	33.6 +2.5 -1.0	45.6 +2.5 -1.0

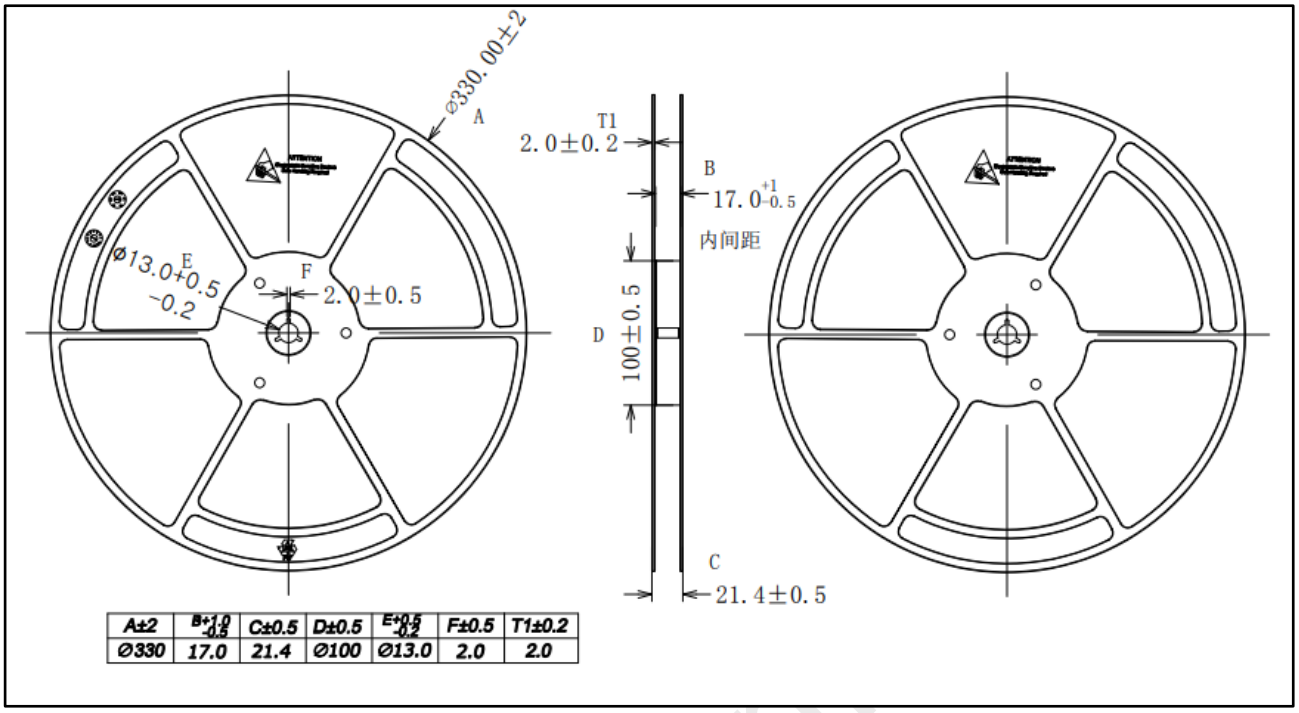
Figure 15. CMT826X WB SOIC-16 Tape and Reel Information



1. 10 sprocket hole pitch cumulative tolerance ±0.20 .
2. Carrier camber is within 1 mm in 250 mm.
3. Material : Black Conductive Polystyrene Alloy .
4. All dimensions meet EIA-481 requirements.
5. Thickness : 0.30±0.05mm.
6. Packing length per 22" reel : 378 Meters.(復卷 1:30 N=122）
7. Component load per 13" reel : 1000 pcs.

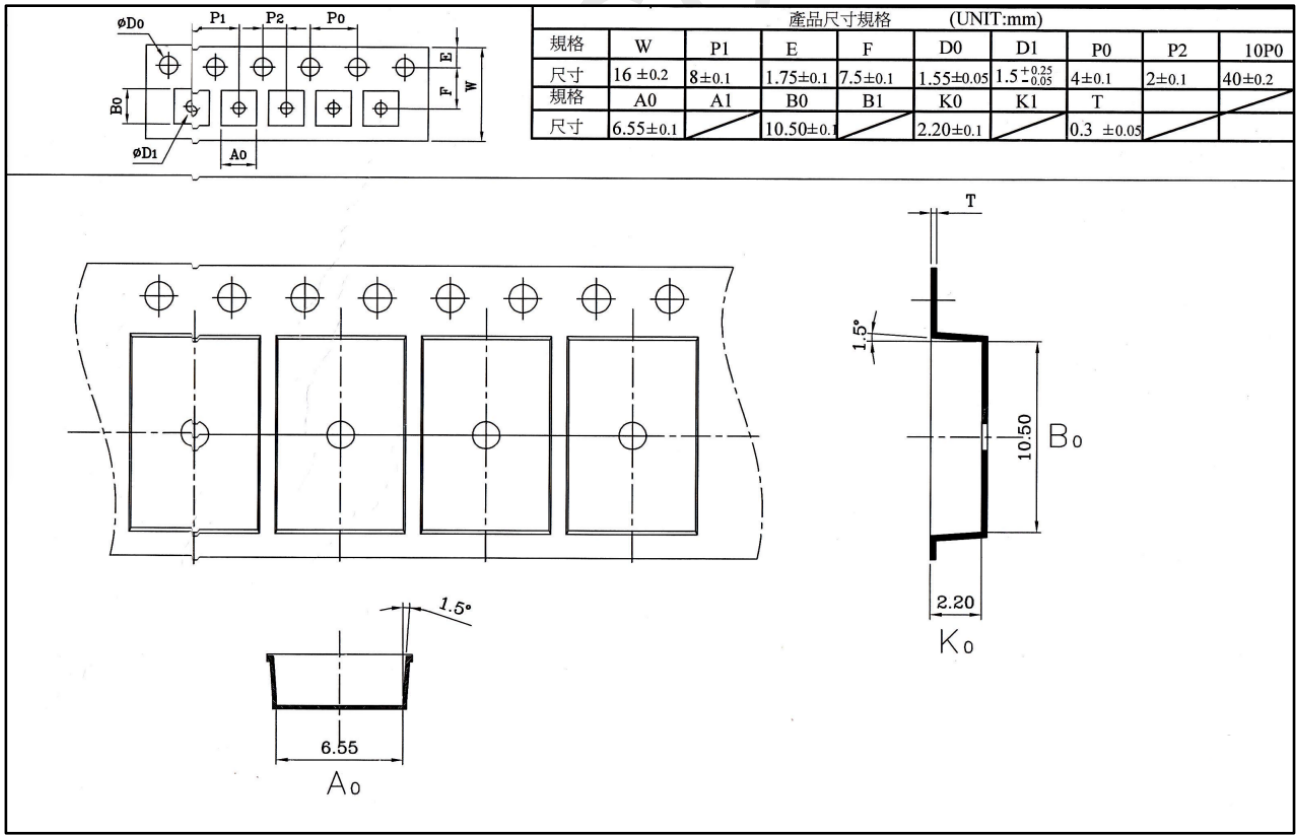
W	16.00±0.20
A0	10.90±0.10
B0	10.70±0.10
K0	3.20±0.10
K1	2.70±0.10

Figure16. CMT826X WB SOIC-16 Tape and Reel Information



A±2	B+1.0 -0.5	C±0.5	D±0.5	E+0.5 -0.2	F±0.5	T1±0.2
Ø330	17.0	21.4	Ø100	Ø13.0	2.0	2.0

Figure 17. CMT826X NB SOIC-16 Tape and Reel Information



產品尺寸規格 (UNIT:mm)

規格	W	P1	E	F	D0	D1	P0	P2	10P0
尺寸	16 ±0.2	8±0.1	1.75±0.1	7.5±0.1	1.55±0.05	1.5 +0.25 -0.05	4±0.1	2±0.1	40±0.2
規格	A0	A1	B0	B1	K0	K1	T		
尺寸	6.55±0.1		10.50±0.1		2.20±0.1		0.3 ±0.05		

Figure 18. CMT826X NB SOIC-16 Tape and Reel Information

16 Revise History

Table 21. Revise Records

Version No.	Chapter	Description	Date
0.1	All	Initial version	2023/02/07
0.2	13	Update silver print information	2023/3/29
	15	Added tape information	

17 Contacts

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