

1Gb F-die NAND Flash

Single-Level-Cell (1bit/Cell)

datasheet

SAMSUNG ELECTRONICS RESERVES THE RIGHT TO CHANGE PRODUCTS, INFORMATION AND SPECIFICATIONS WITHOUT NOTICE.

Products and specifications discussed herein are for reference purposes only. All information discussed herein is provided on an "AS IS" basis, without warranties of any kind.

This document and all information discussed herein remain the sole and exclusive property of Samsung Electronics. No license of any patent, copyright, mask work, trademark or any other intellectual property right is granted by one party to the other party under this document, by implication, estoppel or otherwise.

Samsung products are not intended for use in life support, critical care, medical, safety equipment, or similar applications where product failure could result in loss of life or personal or physical harm, or any military or defense application, or any governmental procurement to which special terms or provisions may apply.

For updates or additional information about Samsung products, contact your nearest Samsung office.

All brand names, trademarks and registered trademarks belong to their respective owners.

© 2016 Samsung Electronics Co., Ltd. All rights reserved.

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Date</u>	<u>Remark</u>	<u>Edited by</u>	<u>Reviewed by</u>
0.0	1. Initial issue	Feb. 24, 2016	Target	H.K.Kim	T.E.Kim
0.5	1. Read ID revised.	Mar. 28, 2016	Preliminary	S.M.Lee	T.E.Kim
1.0	1. Figure 7. AC Waveform for Power Transition revised	Jul. 26. 2016	Final	T.Y.Kim	S.J.Kim

Table Of Contents

1.0 INTRODUCTION	4
1.1 General Description	4
1.2 Features	4
1.3 Product List	4
1.4 Pin Configuration (TSOP1)	5
1.4.1 Package Dimensions	5
1.5 Pin Configuration (FBGA)	6
1.6 Package Dimensions	6
1.7 Pin Descriptions	7
2.0 PRODUCT INTRODUCTION	9
2.1 Valid Block	10
2.2 Absolute Maximum DC Ratings	10
2.3 Recommended Operating Conditions	10
2.4 DC Operating Characteristics	11
2.5 Input / Output Capacitance ($T_A=25^{\circ}\text{C}$, $V_{CC}=3.3\text{V}$, $f=1.0\text{Mhz}$)	11
2.6 AC Test Condition	11
2.7 Read / Program / Erase Characteristics	12
2.8 AC Timing Parameters Table	12
3.0 NAND FLASH TECHNICAL NOTES	13
3.1 Initial Invalid Block(s)	13
3.2 Identifying Initial Invalid Block(s)	13
3.3 Error in Write or Read Operation	14
3.4 Addressing for Program Operation	16
3.5 System Interface Using $\overline{\text{CE}}$ Don't-Care	17
4.0 FUNCTION DESCRIPTION	18
4.1 Data Protection & Power Up Sequence	18
4.2 Mode Selection	18
4.3 General Timing	19
4.3.1 Command Latch Cycle	19
4.3.2 Address Latch Cycle	19
4.3.3 Input Data Latch Cycle	20
4.3.4 Serial Access Cycle after Read ($\text{CLE}=\text{L}$, $\overline{\text{WE}}=\text{H}$, $\text{ALE}=\text{L}$)	20
4.4 Read Status Cycle	21
4.5 ECC Read Status Cycle	21
4.6 Read Operation	22
4.7 Read Operation (Intercepted by $\overline{\text{CE}}$)	22
4.8 Random Data Output In a Page Operation	23
4.9 Page Program Operation	23
4.10 Page Program Operation with Random Data Input Operation	24
4.11 Copy-Back Program Operation	25
4.12 Copy-Back Program Operation with Random Data Input Operation	26
4.13 Block Erase Operation	27
4.14 Read ID Operation	27
5.0 DEVICE OPERATION	28
5.1 Page Read Operation	28
5.2 Page Program Operation	29
5.3 Copy-Back Program Operation	30
5.4 Block Erase Operation	31
5.5 Read Status	31
5.6 ECC Read Status	32
5.7 ECC Sector Information	32
5.8 Partial Page Program Information	33
5.9 Read ID	34
5.9.1 00h Address ID Definition	34
5.9.1.1 00h Address ID Cycle	34
5.10 Reset Operation	35
5.11 Ready/Busy	36

1.0 INTRODUCTION

1.1 General Description

Offered in 128Mx8bit, the K9F1G08U0F is a 1G-bit NAND Flash Memory with spare 32M-bit. The device is offered in 3.3V V_{CC} . Its NAND cell provides the most cost-effective solution for the solid state application market. A program operation can be performed in typical 400 μ s on the (2K+64)Byte page and an erase operation can be performed in typical 4.5ms on a (128K+4K)Byte block. Data in the data register can be read out at 25ns cycle time per Byte. The I/O pins serve as the ports for address and data input/output as well as command input. The on-chip write controller automates all program and erase functions including pulse repetition, where required, and internal verification and margining of data. The K9F1G08U0F is an optimum solution for large nonvolatile storage applications such as solid state file storage and other portable applications requiring non-volatility.

1.2 Features

- Voltage Supply
 - V_{CC} : 3.3V (2.7V ~ 3.6V)
- Organization
 - Memory Cell Array : (128M + 4M) x 8bit
 - Page Size : (2K + 64)Byte
 - Data Register : (2K + 64) x 8bit
 - Block Erase : (128K + 4K)Byte
- Automatic Program and Erase
 - Page Program : (2K + 64)Byte
- Page Read Operation
 - Random Read : 25 μ s(Max.)
 - Serial Access : 25ns(Min.)
 - Data Transfer Rate : SDR 20Mhz(40Mbps)
- Fast Write Cycle Time
 - Page Program time : 400 μ s(Typ.)
 - Block Erase Time : 4.5ms(Typ.)
- Command/Address/Data Multiplexed I/O Port
- Hardware Data Protection
 - Program/Erase Lockout During Power Transitions
- Command Driven Operation
- Unique ID for Copyright Protection
- Package :
 - K9F1G08U0F-Sx¹B0 : Pb-Free, Halogen-Free Package
48 - Pin TSOP1 (12 x 20/0.5 mm pitch)
 - K9F1G08U0F-5x¹B0 : Pb-Free, Halogen-Free Package
63 - FBGA (9 x 11 / 0.8 mm pitch)

NOTE :

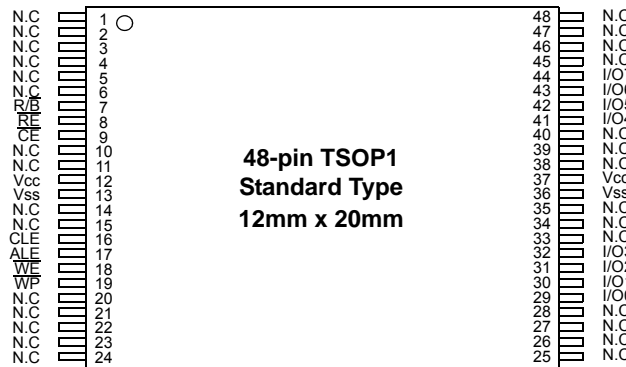
- 1) C : Commercial
I : Industrial
F : Automotive - Grade3
H : Automotive - Grade2

1.3 Product List

Part Number	Density	Organization	V_{CC} Range	PKG Type
K9F1G08U0F	1Gb	x8	2.7V ~ 3.6V	TSOP1
K9F1G08U0F	1Gb	x8	2.7V ~ 3.6V	63 FBGA

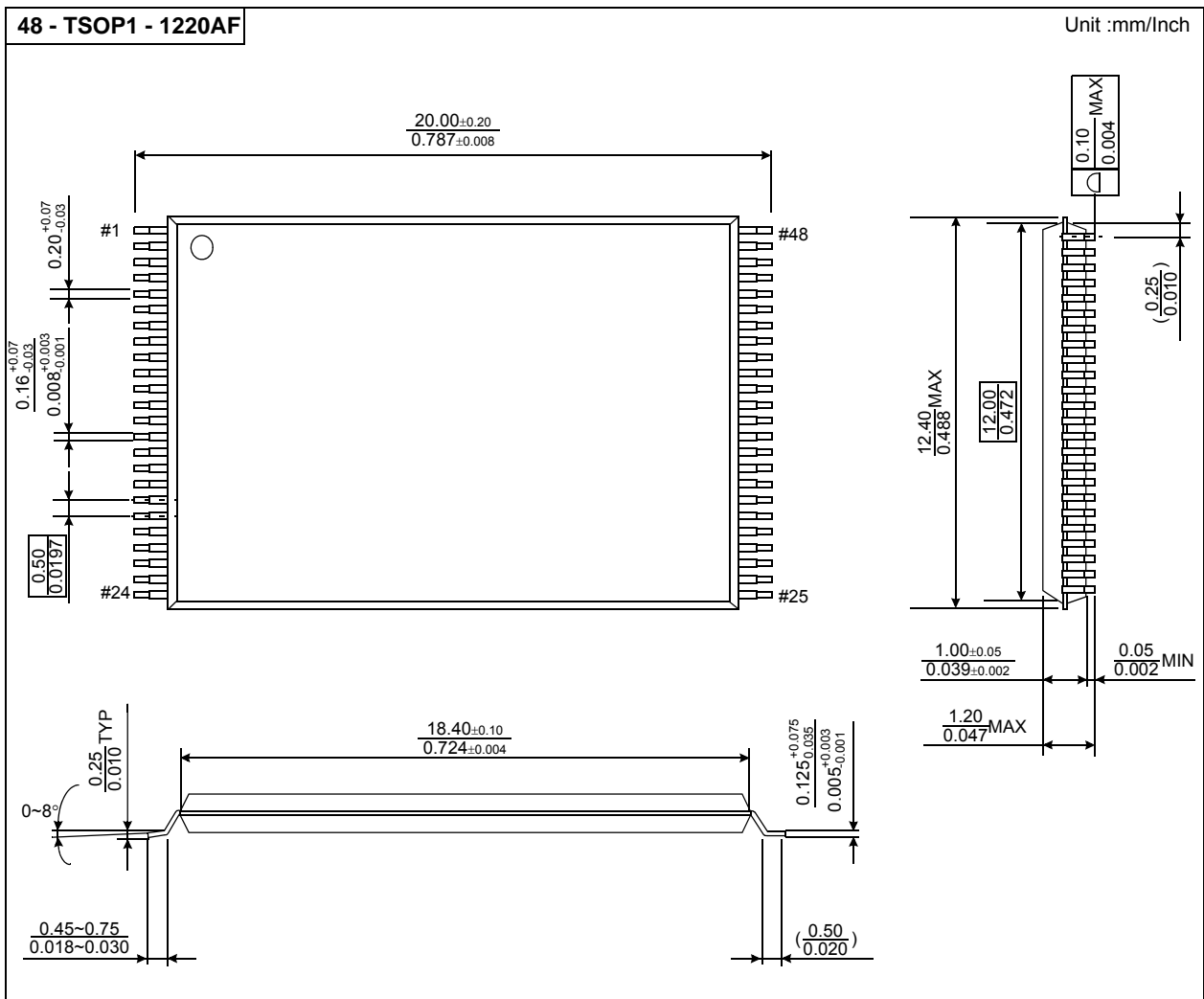
1.4 Pin Configuration (TSOP1)

K9F1G08U0F-SxB0



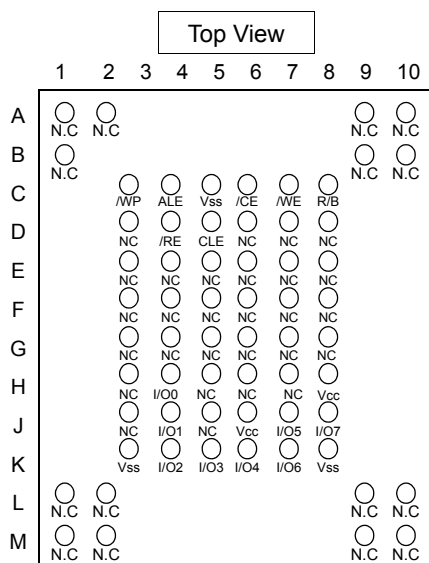
1.4.1 Package Dimensions

48-PIN LEAD FREE PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE(I)

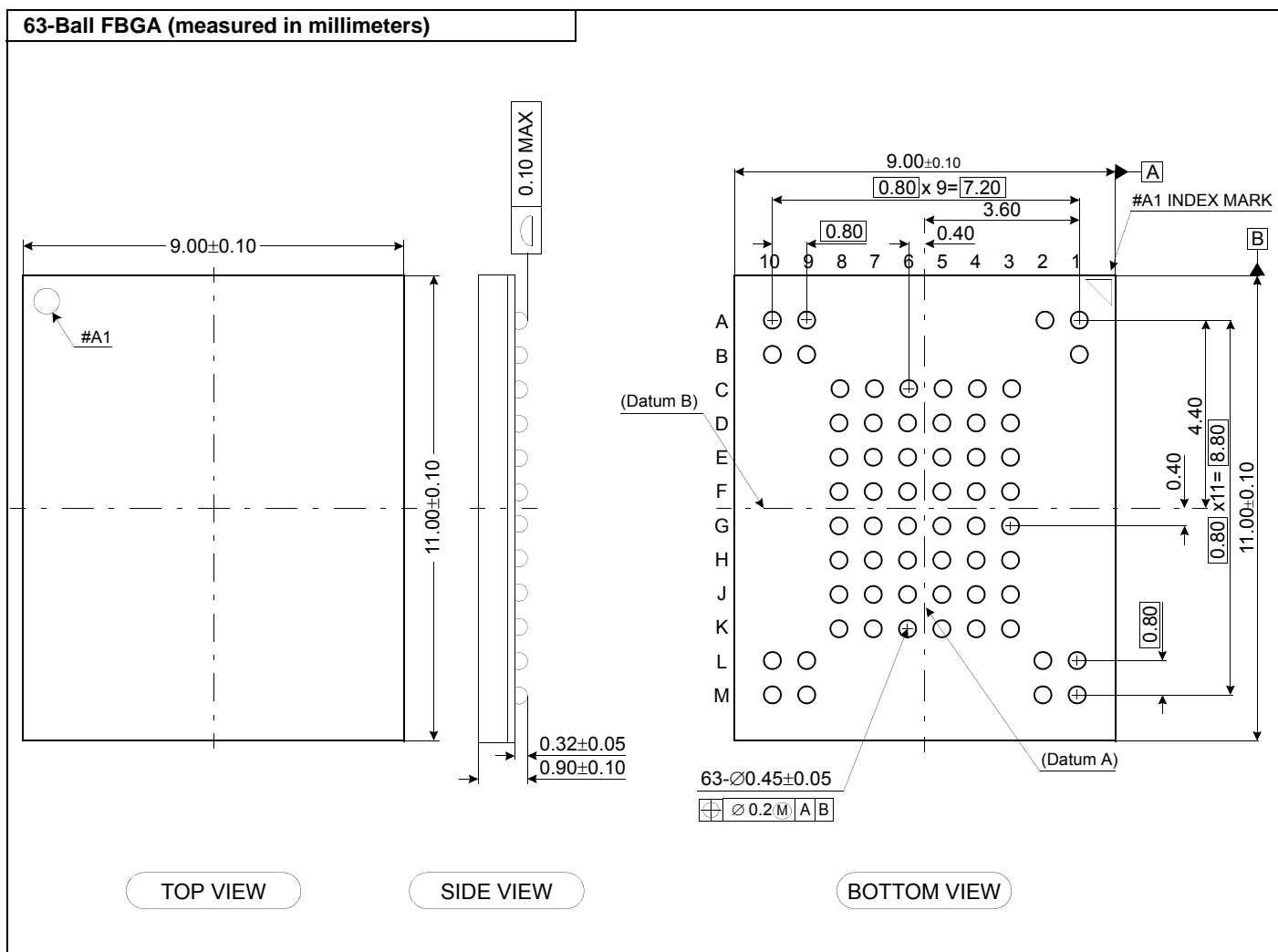


1.5 Pin Configuration (FBGA)

K9F1G08U0F-5xB0



1.6 Package Dimensions



1.7 Pin Descriptions

[Table 1] Pin Descriptions

Pin Name	Pin Function
I/O ₀ ~ I/O ₇	DATA INPUTS/OUTPUTS The I/O pins are used to input command, address and data, and to output data during read operations. The I/O pins float to high-z when the chip is deselected or when the outputs are disabled.
CLE	COMMAND LATCH ENABLE The CLE input controls the activating path for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the WE signal.
ALE	ADDRESS LATCH ENABLE The ALE input controls the activating path for address to the internal address registers. Addresses are latched on the rising edge of WE with ALE high.
$\overline{\text{CE}}$	CHIP ENABLE The $\overline{\text{CE}}$ input is the device selection control. When the device is in the Busy state, $\overline{\text{CE}}$ high is ignored, and the device does not return to standby mode in program or erase operation.
$\overline{\text{RE}}$	READ ENABLE The $\overline{\text{RE}}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid t _{REA} after the falling edge of $\overline{\text{RE}}$ which also increments the internal column address counter by one.
$\overline{\text{WE}}$	WRITE ENABLE The $\overline{\text{WE}}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{\text{WE}}$ pulse.
$\overline{\text{WP}}$	WRITE PROTECT The $\overline{\text{WP}}$ pin provides inadvertent program/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{\text{WP}}$ pin is active low.
R/ $\overline{\text{B}}$	READY/BUSY OUTPUT The R/ $\overline{\text{B}}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and returns to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or when outputs are disabled.
V _{CC}	POWER V _{CC} is the power supply for device.
V _{SS}	GROUND
N/C	NO CONNECTION

NOTE :

Connect all V_{CC} and V_{SS} pins of each device to common power supply outputs.

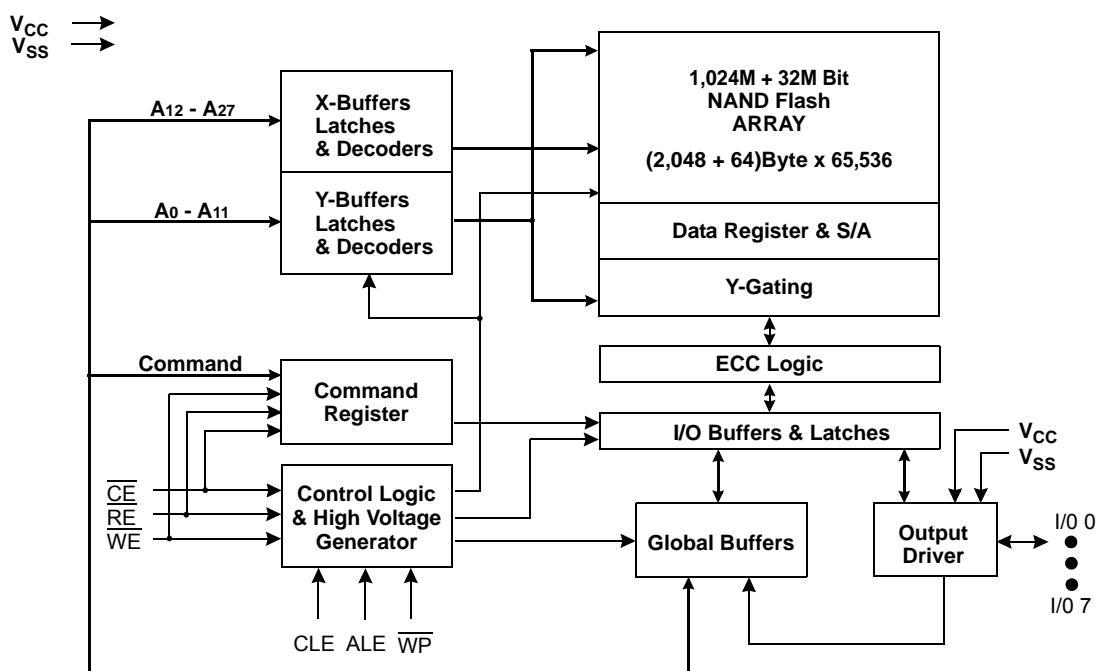


Figure 1. K9F1G08U0F Functional Block Diagram

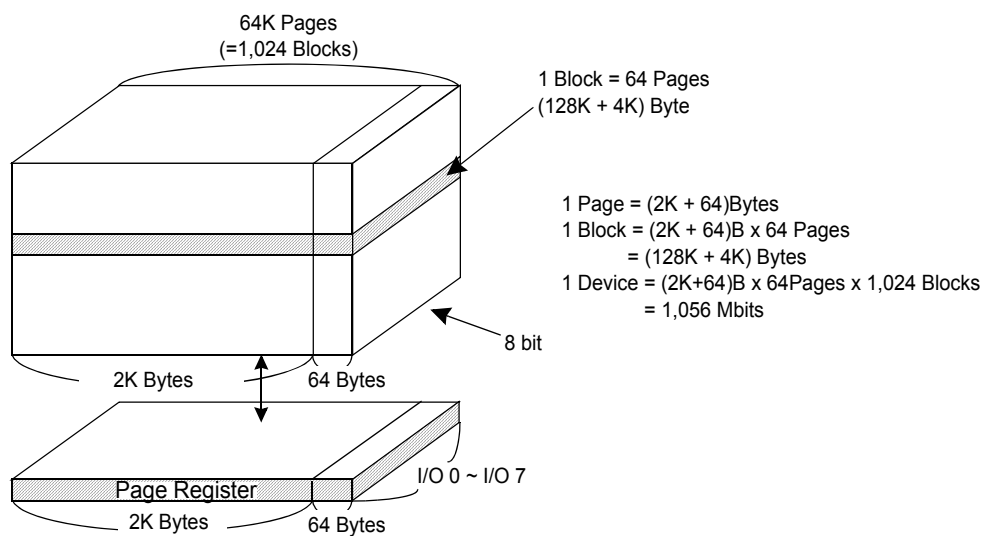


Figure 2. K9F1G08U0F Array Organization

	I/O 0	I/O 1	I/O 2	I/O 3	I/O 4	I/O 5	I/O 6	I/O 7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	Column Address
2nd Cycle	A8	A9	A10	A11	*L	*L	*L	*L	
3rd Cycle	A12	A13	A14	A15	A16	A17	A18	A19	Row Address
4th Cycle	A20	A21	A22	A23	A24	A25	A26	A27	

NOTE :

Column Address : Starting Address of the Register.

* L must be set to "Low".

* The device ignores any additional input of address cycles than required.

2.0 PRODUCT INTRODUCTION

NAND Flash Memory has addresses multiplexed into 8 I/Os. This scheme dramatically reduces pin counts and allows system upgrades to future densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing \overline{WE} to low while \overline{CE} is low. Those are latched on the rising edge of \overline{WE} . Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. Some commands require one bus cycle. For example, Reset Command, Status Read Command, etc. require just one cycle bus. Some other commands, like page read and block erase and page program, require two cycles: one cycle for setup and the other cycle for execution.- Page Read and Page Program need the same four address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table 2 defines the specific commands of the K9F1G08U0F.

[Table 2] Command Sets

Function	1st Cycle	2nd Cycle	Acceptable Command during Busy
Read	00h	30h	
Read for Copy Back	00h	35h	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	80h	10h	
Copy-Back Program	85h	10h	
Block Erase	60h	D0h	
Random Data Input ¹⁾	85h	-	
Random Data Output ¹⁾	05h	E0h	
Read Status	70h	-	O
ECC Read Status	7Ah		

NOTE :

1) Random Data Input/Output can be executed in a page.

Caution :

Any undefined command inputs are prohibited except for above command set of Table 2.

2.1 Valid Block

[Table 3] The Number of Valid Block per a $\overline{\text{CE}}$

Parameter	Symbol	Min	Typ.	Max	Unit
K9F1G08U0F	NvB	1,004	-	1,024	Blocks

NOTE :

- 1) The device may include initial invalid blocks when first shipped. Additional invalid blocks may develop while being used. The number of valid blocks is presented with both cases of invalid blocks considered. Invalid blocks are defined as blocks that contain one or more bad bits. Do not erase or program factory-marked bad blocks. Refer to the attached technical notes for appropriate management of invalid blocks.

2.2 Absolute Maximum DC Ratings

[Table 4] Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_{CC}	-0.6 to + 4.6	V
	V_{IN}	-0.6 to + 4.6	
	$V_{I/O}$	-0.6 to $V_{CC} + 0.3$ (< 4.6V)	
Temperature Under Bias	K9F1G08U0F-SCB0	T_{BIAS}	°C
	K9F1G08U0F-SxB0		
Storage Temperature	T_{STG}	-65 to +150	°C
Short Circuit Current	I_{OS}	5	mA

NOTE :

- 1) Minimum DC voltage is -0.6V on input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is $V_{CC}+0.3V$ which, during transitions, may overshoot to $V_{CC}+2.0V$ for periods <20ns.
- 2) Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2.3 Recommended Operating Conditions

[Table 5] Recommended Operating Conditions

Parameter	Symbol	K9F1G08U0F			Unit
		Min	Typ.	Max	
Power Supply Voltage	V_{CC}	2.7	3.3	3.6	V
Ground Supply Voltage	V_{SS}	0	0	0	V

NOTE :

Voltage reference to GND,

K9F1G08U0F-xCB0: $T_A = 0$ to 70°C , K9F1G08U0F-xIB0: $T_A = -40$ to 85°C , K9F1G08U0F-xFB0: $T_A = -40$ to $85^\circ\text{C}^{(1)}$, K9F1G08U0F-xHB0 : $T_A = -40$ to $105^\circ\text{C}^{(1)}$

- 1) Refer to AEC Q100 spec for detailed information regarding temperature measurement.

2.4 DC Operating Characteristics

[Table 6] DC & Operating Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Page Read Access Operation Current	I_{CC1}	$t_{RC}=25ns$ $\overline{CE}=V_{IL}, I_{OUT}=0mA$	-	15	30	mA
Program Operation Current	I_{CC2}	-	-	-	-	
Erase Operation Current	I_{CC3}	-	-	-	-	
Stand-by Current (TTL)	I_{SB1}	$\overline{CE}=V_{IH}, \overline{WP}=0V/V_{CC}$	-	-	1	mA
Stand-by Current (CMOS)	I_{SB2}	$\overline{CE}=V_{CC}-0.2, \overline{WP}=0V/V_{CC}$	-	10	70	
Input Leakage Current	I_{LI}	$V_{IN}=0$ to $V_{CC}(max)$	-	-	± 10	μA
Output Leakage Current	I_{LO}	$V_{OUT}=0$ to $V_{CC}(max)$	-	-	± 10	
Input High Voltage	$V_{IH}^{1)}$	-	$0.8xV_{CC}$	-	$V_{CC}+0.3$	V
Input Low Voltage, All inputs	$V_{IL}^{1)}$	-	-0.3	-	$0.2xV_{CC}$	
Output High Voltage Level	V_{OH}	$I_{OH}=-400\mu A$	2.4	-	-	
Output Low Voltage Level	V_{OL}	$I_{OL}=2.1mA$	-	-	0.4	
Output Low Current (R/ \overline{B})	$I_{OL}(R/\overline{B})$	$V_{OL}=0.4V$	8	10	-	mA

NOTE :

1) V_{IL} can undershoot to -0.4V and V_{IH} can overshoot to $V_{CC} + 0.4V$ for durations of 20ns or less.

2) Typical value is measured at $V_{CC}=3.3V, T_A=25^\circ C$. Not 100% tested.

2.5 Input / Output Capacitance ($T_A=25^\circ C, V_{CC}=3.3V, f=1.0MHz$)

[Table 7] Input / Output Capacitance

Item	Symbol	Test Condition	Min	Max	Unit
Input/Output Capacitance	$C_{I/O}$	$V_{IL}=0V$	-	8	pF
Input Capacitance	C_{IN}	$V_{IN}=0V$	-	8	pF

NOTE :

Capacitance is periodically sampled and not 100% tested.

2.6 AC Test Condition

[Table 8] AC Test Condition

Parameter	K9F1G08U0F
Input Pulse Levels	0V to V_{CC}
Input Rise and Fall Times	5ns
Input and Output Timing Levels	$V_{CC}/2$
Output Load	1 TTL GATE and $C_L=50pF$

MOTE :

K9F1G08U0F-xCB0: $T_A=0$ to $70^\circ C$, K9F1G08U0F-xIB0: $T_A=-40$ to $85^\circ C$, K9F1G08U0F-xFB0: $T_A=-40$ to $85^\circ C^{1)}$, K9F1G08U0F-xHB0: $T_A=-40$ to $105^\circ C^{1)}$,
K9F1G08U0F : $V_{CC}=2.7V\sim 3.6V$ unless otherwise noted.

1) Refer to AEC_Q100 spec for detailed information regarding temperature measurement.

2.7 Read / Program / Erase Characteristics

[Table 9] NAND Read / Program / Erase Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
Data Transfer from Cell to Register	t _R	-		25	μs
Program Time	t _{PROG}	-	400	900	μs
Number of Partial Program Cycles	N _{op}	-	-	4	cycles
Block Erase Time	t _{BERS}	-	4.5	16	ms

NOTE :

- 1) Typical value is measured at V_{CC}=3.3V, T_A=25°C. Not 100% tested.
- 2) Typical program time is defined as the time within which more than 50% of the whole pages are programmed at 3.3V V_{CC} and 25°C temperature.

2.8 AC Timing Parameters Table

[Table 10] AC Timing Characteristics

Parameter	Symbol	Min	Max	Unit
CLE Setup Time	t _{CLS} ¹⁾	12	-	ns
CLE Hold Time	t _{CLH}	5	-	ns
$\overline{\text{CE}}$ Setup Time	t _{CS} ¹⁾	20	-	ns
$\overline{\text{CE}}$ Hold Time	t _{CH}	5	-	ns
$\overline{\text{WE}}$ Pulse Width	t _{WP}	12	-	ns
ALE Setup Time	t _{ALS} ¹⁾	12	-	ns
ALE Hold Time	t _{ALH}	5	-	ns
Data Setup Time	t _{DS} ¹⁾	12	-	ns
Data Hold Time	t _{DH}	5	-	ns
Write Cycle Time	t _{WC}	25	-	ns
$\overline{\text{WE}}$ High Hold Time	t _{WH}	10	-	ns
Address to Data Loading Time	t _{ADL} ²⁾	100	-	ns
ALE to $\overline{\text{RE}}$ Delay	t _{AR}	10	-	ns
CLE to $\overline{\text{RE}}$ Delay	t _{CLR}	10	-	ns
Ready to $\overline{\text{RE}}$ Low	t _{RR}	20	-	ns
$\overline{\text{RE}}$ Pulse Width	t _{RP}	12	-	ns
$\overline{\text{WE}}$ High to Busy	t _{WB}	-	100	ns
Read Cycle Time	t _{RC}	25	-	ns
$\overline{\text{RE}}$ Access Time	t _{REA}	-	20	ns
$\overline{\text{CE}}$ Access Time	t _{CEA}	-	25	ns
$\overline{\text{RE}}$ High to Output Hi-Z	t _{RHZ}	-	100	ns
$\overline{\text{CE}}$ High to Output Hi-Z	t _{CHZ}	-	30	ns
$\overline{\text{CE}}$ High to ALE or CLE Don't Care	t _{CSD}	0	-	ns
$\overline{\text{RE}}$ High to Output Hold	t _{RHOH}	15	-	ns
Data Hold Time after $\overline{\text{CE}}$ Disable	t _{COH}	15	-	ns
$\overline{\text{RE}}$ High Hold Time	t _{REH}	10	-	ns
Output Hi-Z to $\overline{\text{RE}}$ Low	t _{IR}	0	-	ns
$\overline{\text{RE}}$ High to $\overline{\text{WE}}$ Low	t _{RHW}	100	-	ns
$\overline{\text{WE}}$ High to $\overline{\text{RE}}$ Low	t _{WHR}	60	-	ns
Device Resetting Time (Read/Program/Erase)	t _{RST}	-	5/10/500 ¹⁾	μs

NOTE :

- 1) The transition of the corresponding control pins must occur only once while $\overline{\text{WE}}$ is held low.
- 2) t_{ADL} is the time from the $\overline{\text{WE}}$ rising edge of final address cycle to the $\overline{\text{WE}}$ rising edge of first data cycle.
- 3) If reset command(FFh) is written at Ready state, the device goes into Busy for maximum 5μs.

3.0 NAND FLASH TECHNICAL NOTES

3.1 Initial Invalid Block(s)

Initial invalid blocks are defined as blocks that contain one or more initial invalid bits whose reliability is not guaranteed by Samsung. The information regarding the initial invalid block(s) is called the initial invalid block information. Devices with initial invalid block(s) have the same quality level as devices with all valid blocks and have the same AC and DC characteristics. An initial invalid block(s) does not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor. The system design must be able to mask out the initial invalid block(s) via address mapping.

3.2 Identifying Initial Invalid Block(s)

All device locations are erased(FFh) except locations where the initial invalid block(s) information is written prior to shipping. The initial invalid block(s) status is defined by the 1st byte in the spare area. Samsung makes sure that either the 1st or 2nd page of every initial invalid block has non-FFh data at the column address of 2048. Since the initial invalid block information is also erasable in most cases, it is impossible to recover the information once it has been erased. Therefore, the system must be able to recognize the initial invalid block(s) based on the original initial invalid block information and create the initial invalid block table via the following suggested flow chart(Figure 3). Any intentional erasure of the original initial invalid block information is prohibited.

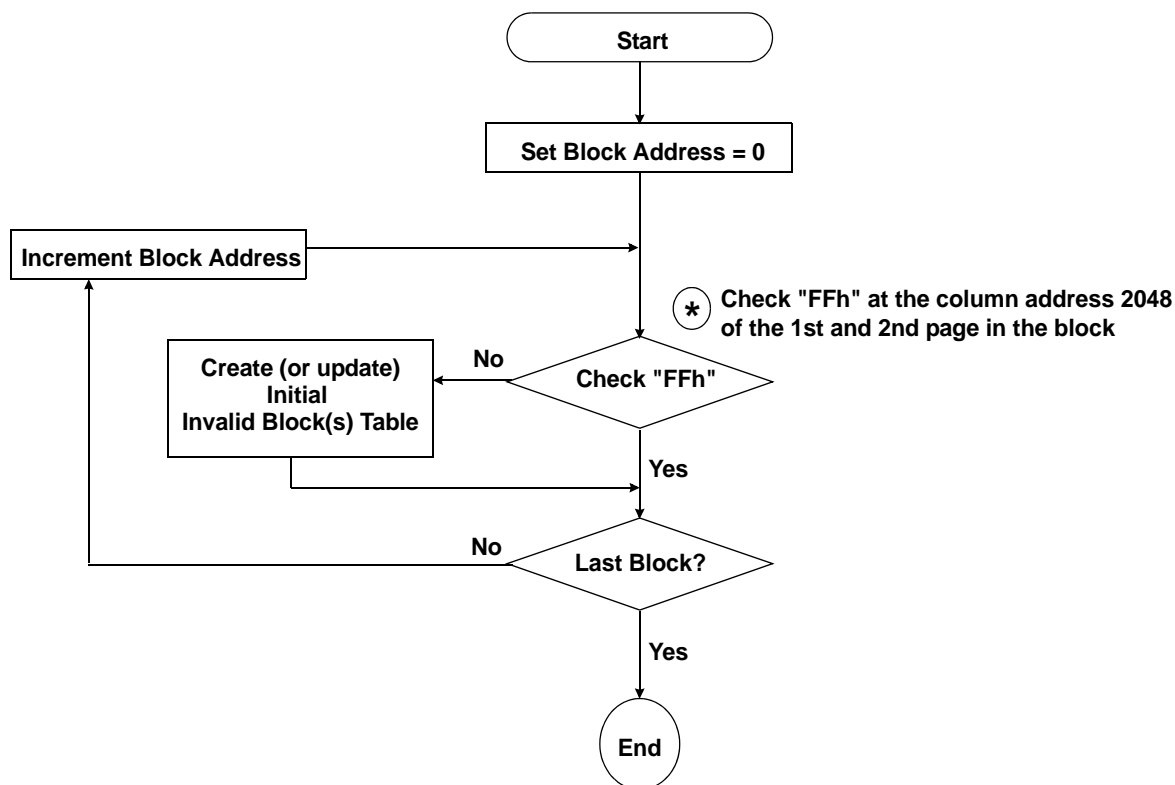


Figure 3. Flow Chart to Create Initial Invalid Block Table

3.3 Error in Write or Read Operation

Within its life time, additional invalid blocks may develop with NAND Flash memory. Refer to the qualification report for the actual data. The following possible failure modes should be considered to implement a highly reliable system. In the case of status read failure after erase or program, block replacement should be done. Because program status fail during a page program does not affect the data of the other pages in the same block, block replacement can be executed with a page-sized buffer by finding an erased empty block and reprogramming the current target data and copying the rest of the replaced block. In case of Read, ECC must be employed. To improve the efficiency of memory space, it is recommended that the read or verification failure due to single bit error be reclaimed by ECC without any block replacement. The said additional block failure rate does not include those reclaimed blocks.

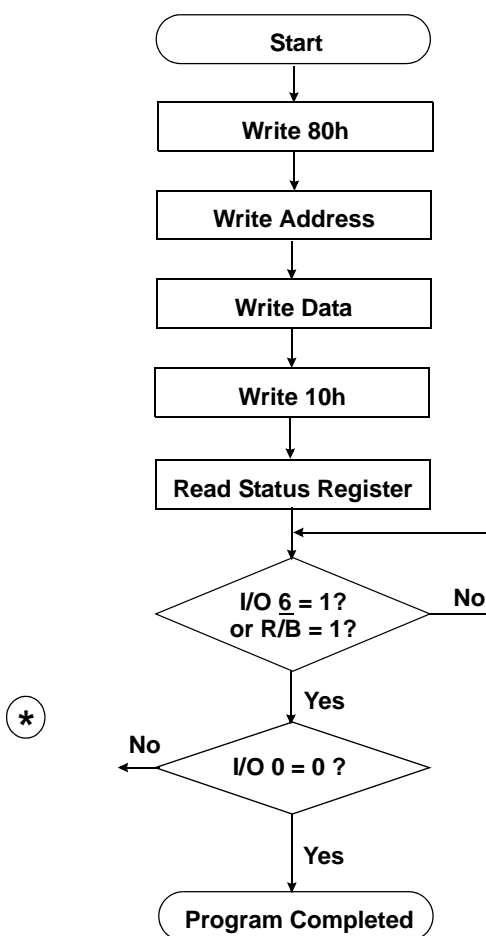
[Table 11] Failure Cases

Failure Mode		Detection and Countermeasure Sequence
Write	Erase Failure	Read Status after Erase --> Block Replacement
	Program Failure	Read Status after Program --> Block Replacement
Read	Single bit Failure	Verify ECC -> ECC Correction

ECC

: Error Correcting Code --> Hamming Code etc.

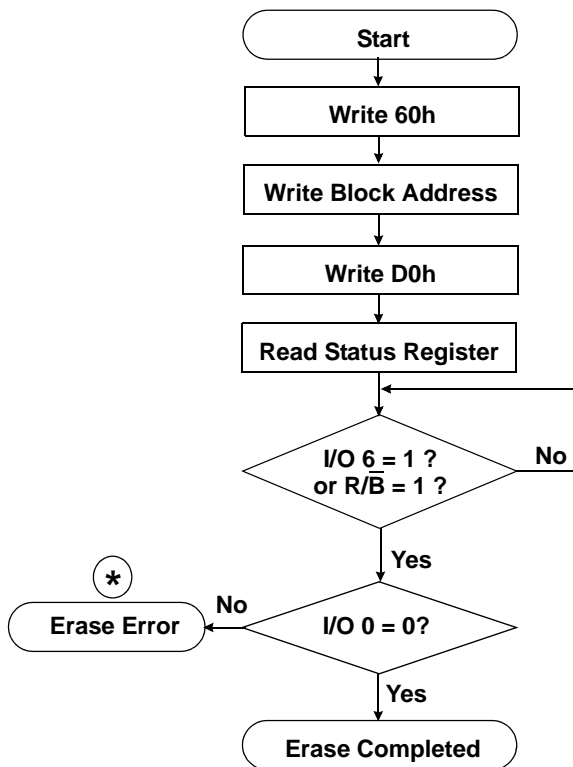
Example) 1bit correction & 2bit detection



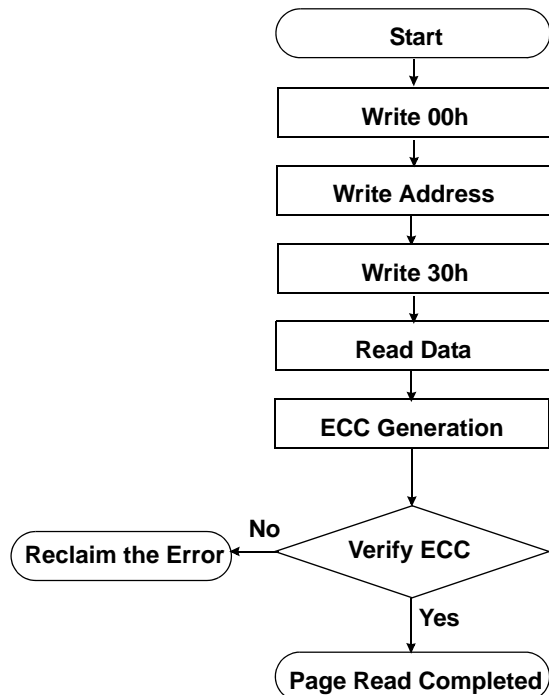
* : If program operation results in an error, map out the block including the page in error and copy the target data to another block.

Figure 4. Program Flow Chart

Erase Flow Chart

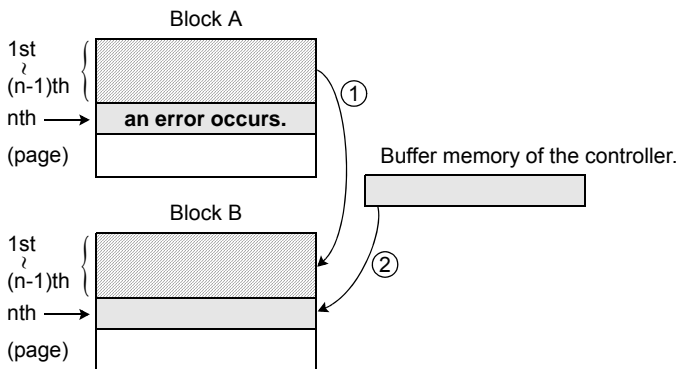


Read Flow Chart



* : If erase operation results in an error, map out the failing block and replace it with another block.

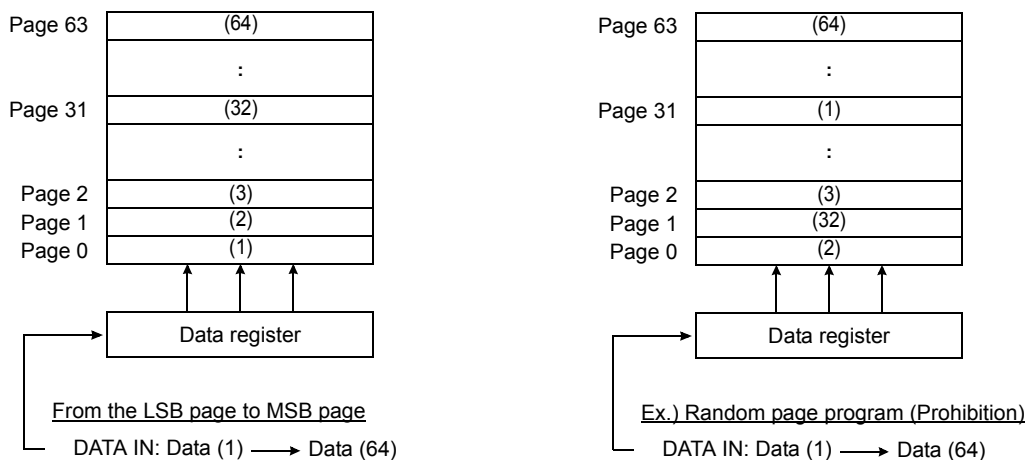
Block Replacement



- * Step1
When an error happens in the nth page of the Block 'A' during erase or program operation.
- * Step2
Copy the data in the 1st ~ (n-1)th page to the same location of another free block. (Block 'B')
- * Step3
Then, copy the nth page data of the Block 'A' in the buffer memory to the nth page of the Block 'B'.
- * Step4
Do not erase or program to Block 'A' by creating an 'invalid block' table or other appropriate scheme.

3.4 Addressing for Program Operation

Within a block, the pages must be programmed consecutively from the LSB(least significant bit) page of the block to the MSB(most significant bit) pages of the block. Random page address programming is prohibited. In this case, the definition of LSB page is the LSB among the pages to be programmed. Therefore, LSB doesn't need to be page 0.



[Table 12] Address Information

Device	I/O	DATA	ADDRESS			
	I/Ox	Data In/Out	Col. Add1	Col. Add2	Row Add1	Row Add2
K9F1G08U0F	I/O 0 ~ I/O 7	2112Byte	A0~A7	A8~A11	A12~A19	A20~A27

3.5 System Interface Using \overline{CE} Don't-Care

For an easier system interface, \overline{CE} may be inactive during the data-loading or serial access as shown below. The internal 2,112byte data registers are utilized as separate buffers for this operation and the system design gets more flexible. In addition, for voice or audio applications which use slow cycle time on the order of μ -seconds, de-activating \overline{CE} during the data-loading and serial access would provide significant savings in power consumption.

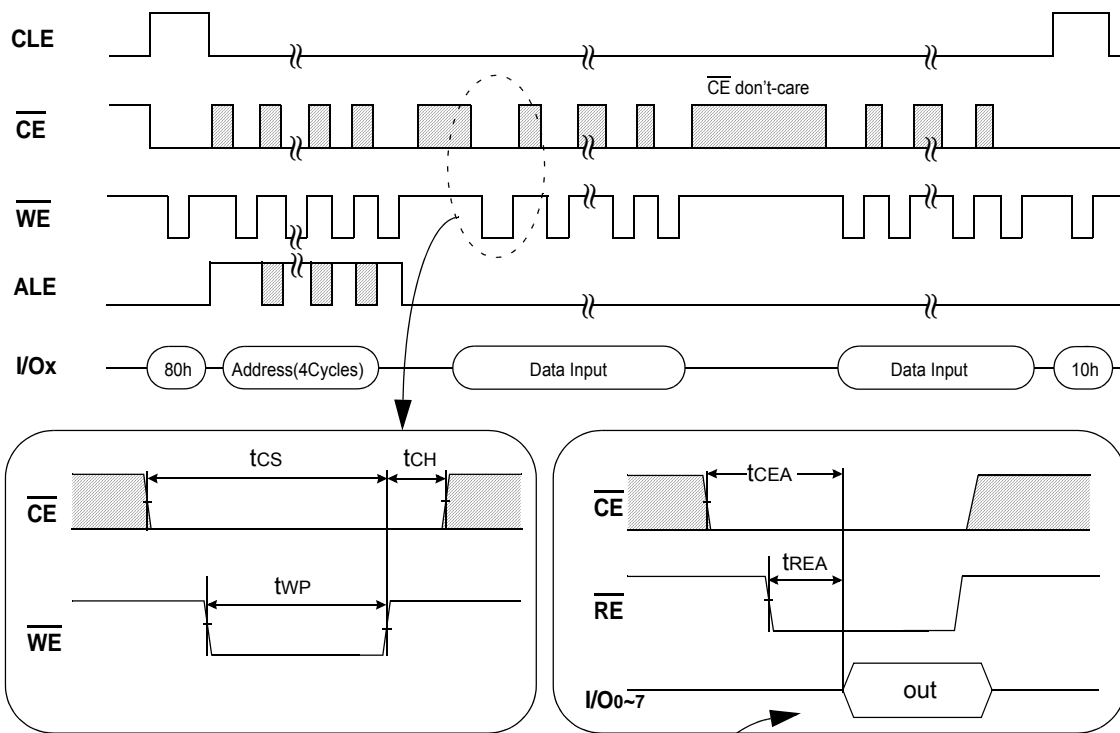


Figure 5. Program Operation with \overline{CE} don't-care

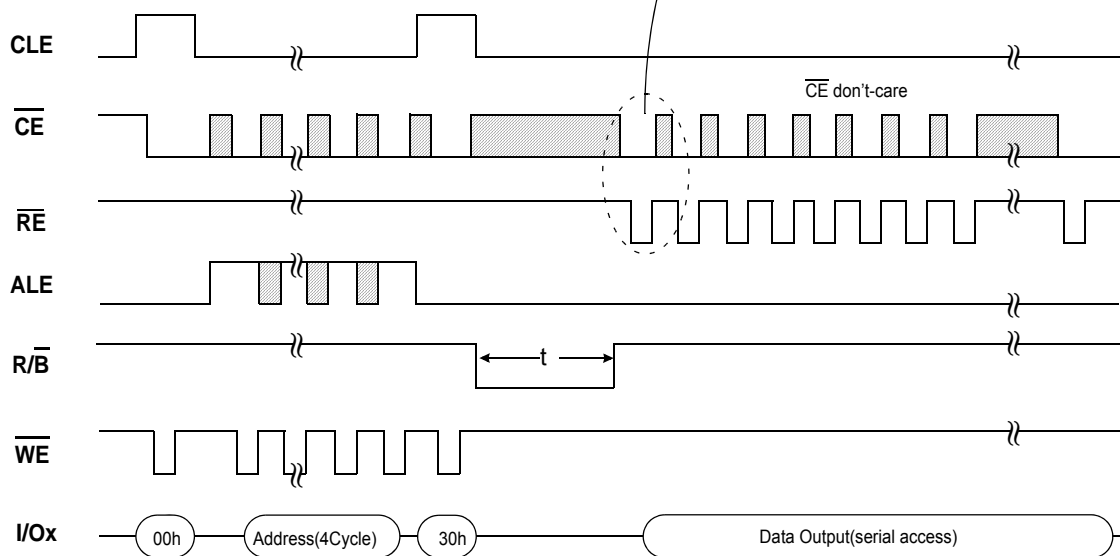


Figure 6. Read Operation with \overline{CE} don't-care

4.0 FUNCTION DESCRIPTION

4.1 Data Protection & Power Up Sequence

The device is designed to offer protection from any involuntary program/erase during power-transitions. An internal voltage detector disables all functions whenever V_{CC} is below about 2V(3.3V device). \overline{WP} pin provides hardware protection and is recommended to be kept at V_{IL} during power-up and power-down. A recovery time of minimum 1ms is required before internal circuit gets ready for any command sequences as shown in Figure 7. The two step command sequence for program/erase provides additional software protection.

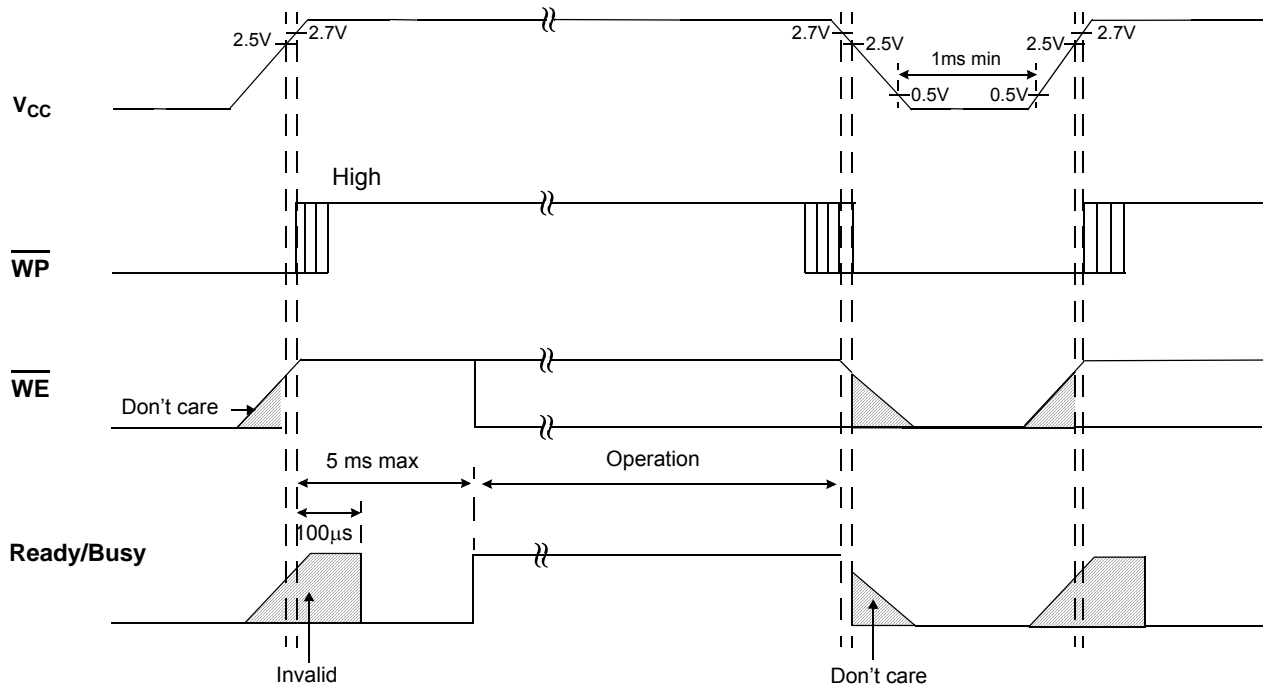


Figure 7. AC Waveforms for Power Transition

NOTE :

- 1) During the initialization, the device consumes a maximum current of 30mA ($ICC1$).
- 2) Once V_{CC} drops under 2.5V, V_{CC} is recommended that it should be driven down to 0.5V and stay low under 0.5V for at least 1ms before V_{CC} power up.

4.2 Mode Selection

[Table 13] Mode Selection

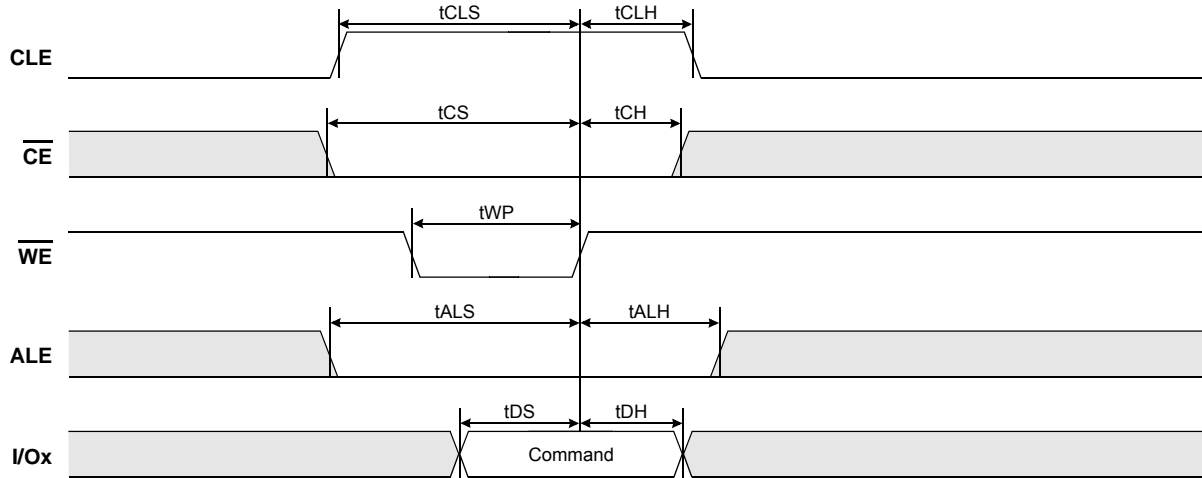
CLE	ALE	CE	WE	RE	WP	Mode	
H	L	L		H	X	Read Mode	Command Input
L	H	L		H	X		Address Input(4cycles)
H	L	L		H	H	Write Mode	Command Input
L	H	L		H	H		Address Input(4cycles)
L	L	L		H	H	Data Input	
L	L	L	H		X	Data Output	
X	X	X	X	H	X	During Read(Busy)	
X	X	X	X	X	H	During Program(Busy)	
X	X	X	X	X	H	During Erase(Busy)	
X	X ¹⁾	X	X	X	L	Write Protect	
X	X	H	X	X	0V/ V_{CC} ²⁾	Stand-by	

NOTE :

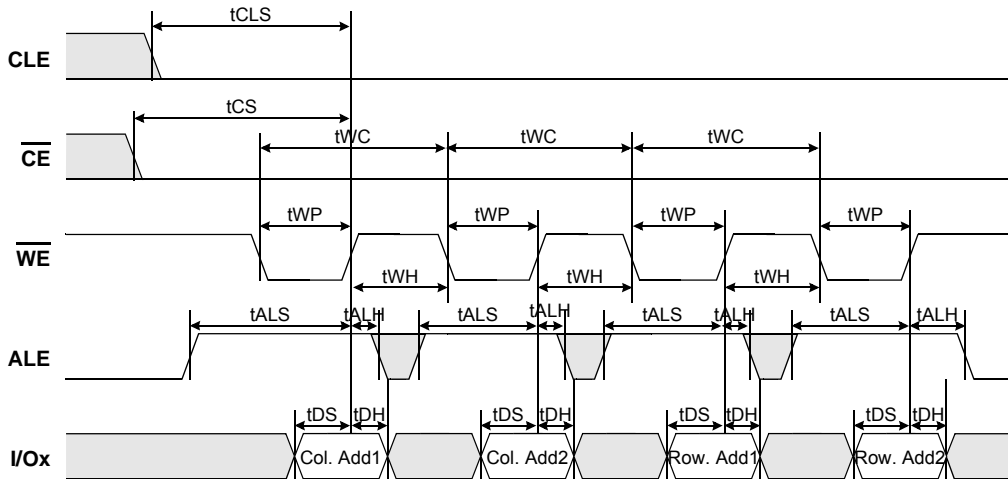
- 1) X can be V_{IL} or V_{IH} .
- 2) \overline{WP} should be biased to CMOS high or CMOS low for standby.

4.3 General Timing

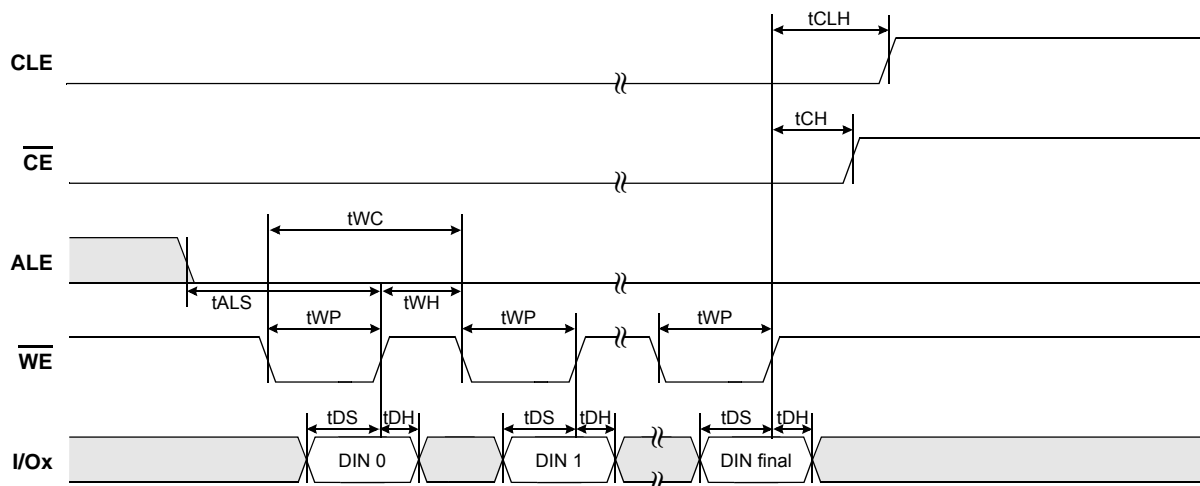
4.3.1 Command Latch Cycle



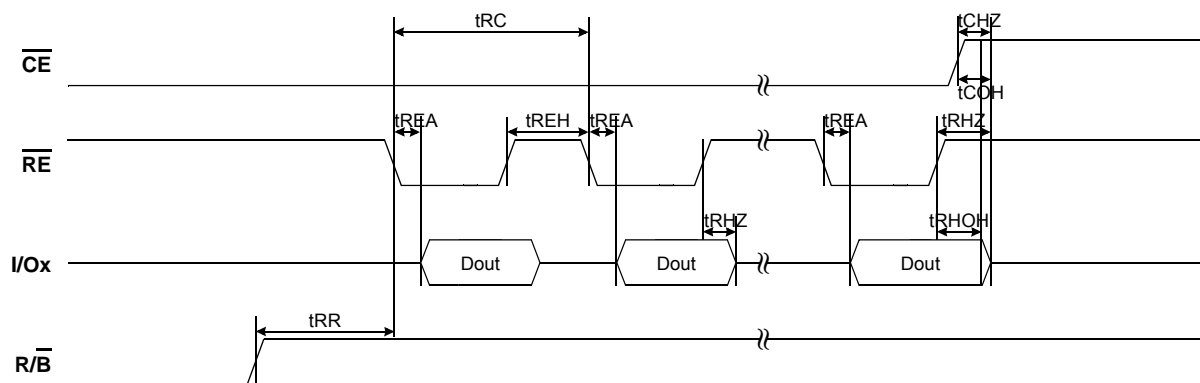
4.3.2 Address Latch Cycle



4.3.3 Input Data Latch Cycle

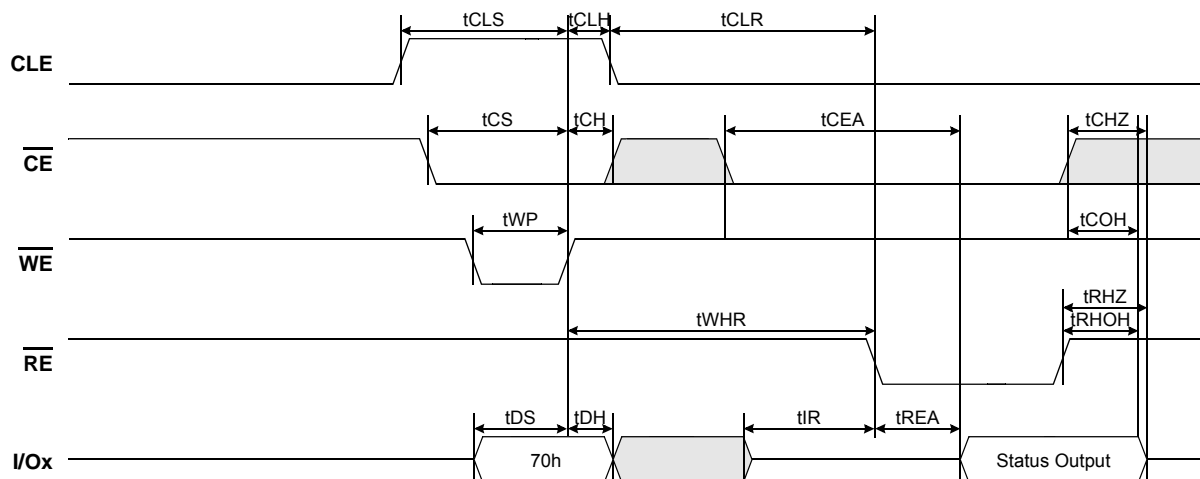


4.3.4 Serial Access Cycle after Read (CLE=L, WE=H, ALE=L)

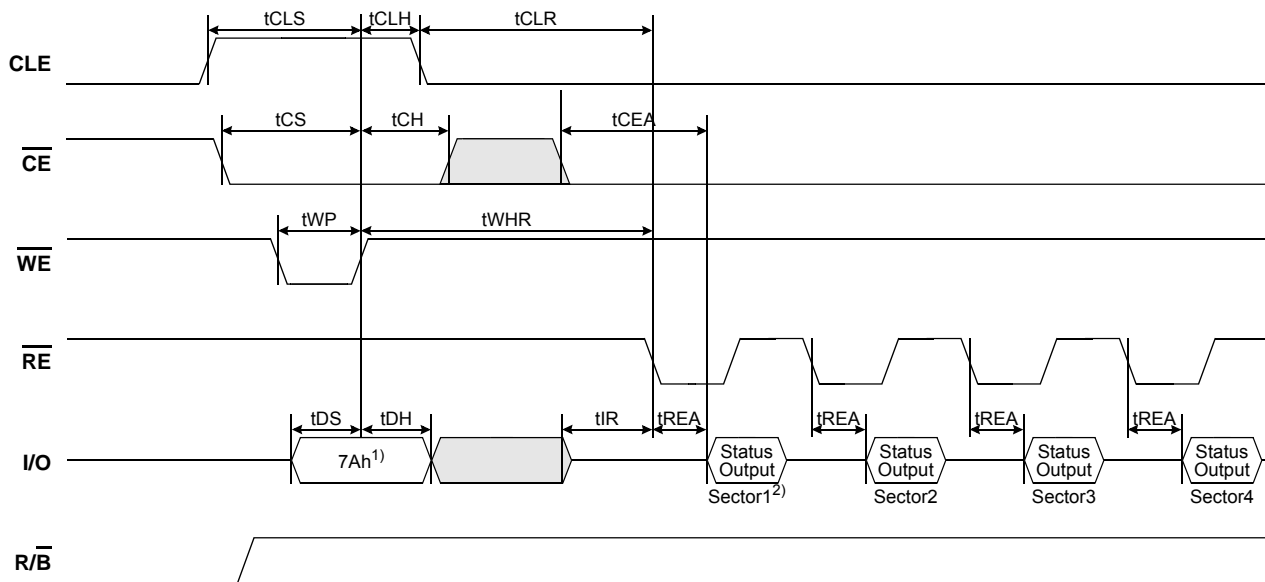


NOTE :
 1) Transition is measured at ±200mV from steady state voltage with load.
 This parameter is sampled and not 100% tested.
 2) tRHOH starts to be valid when frequency is lower than 20Mhz.

4.4 Read Status Cycle

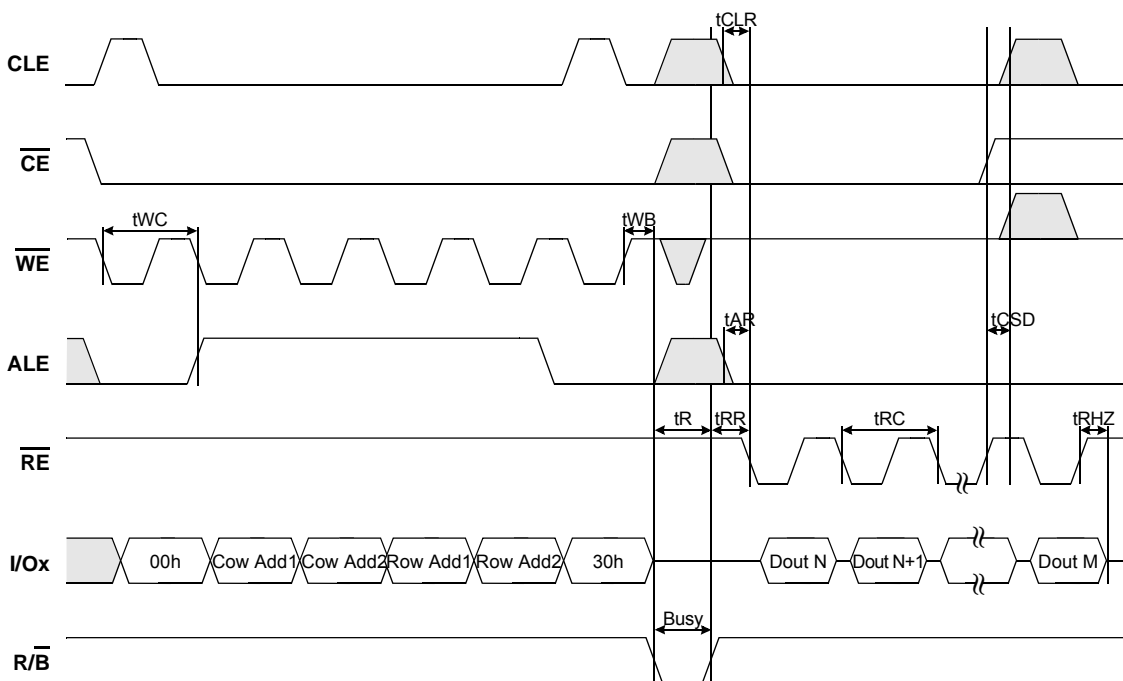


4.5 ECC Read Status Cycle

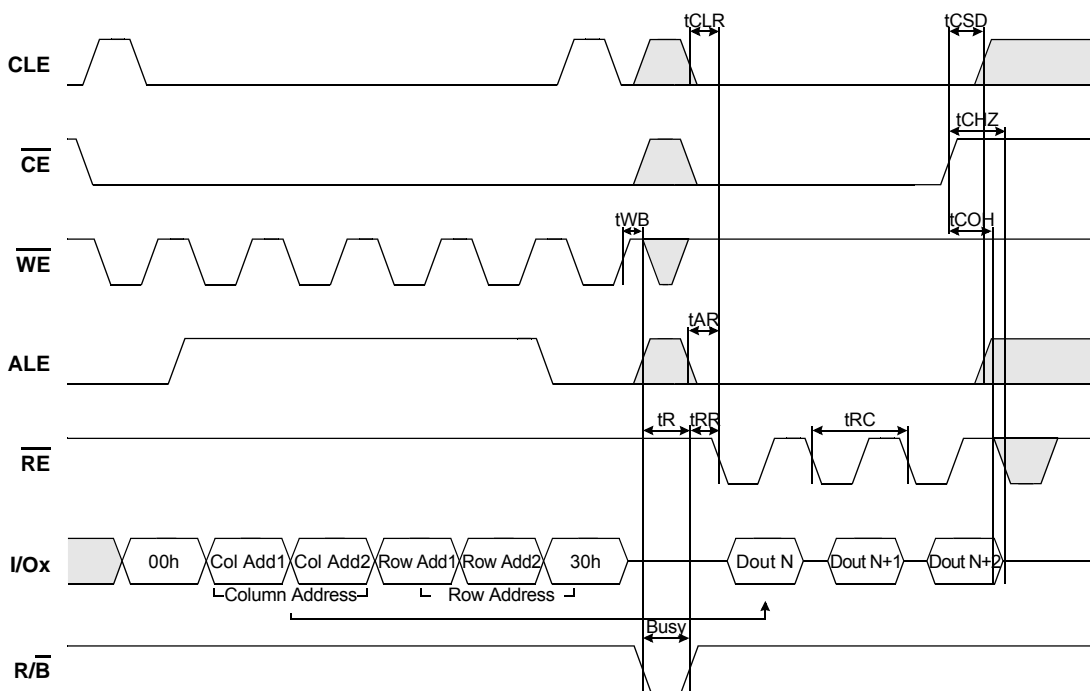


NOTE :
 1) ECC Read Status output should include all 4 sector information.

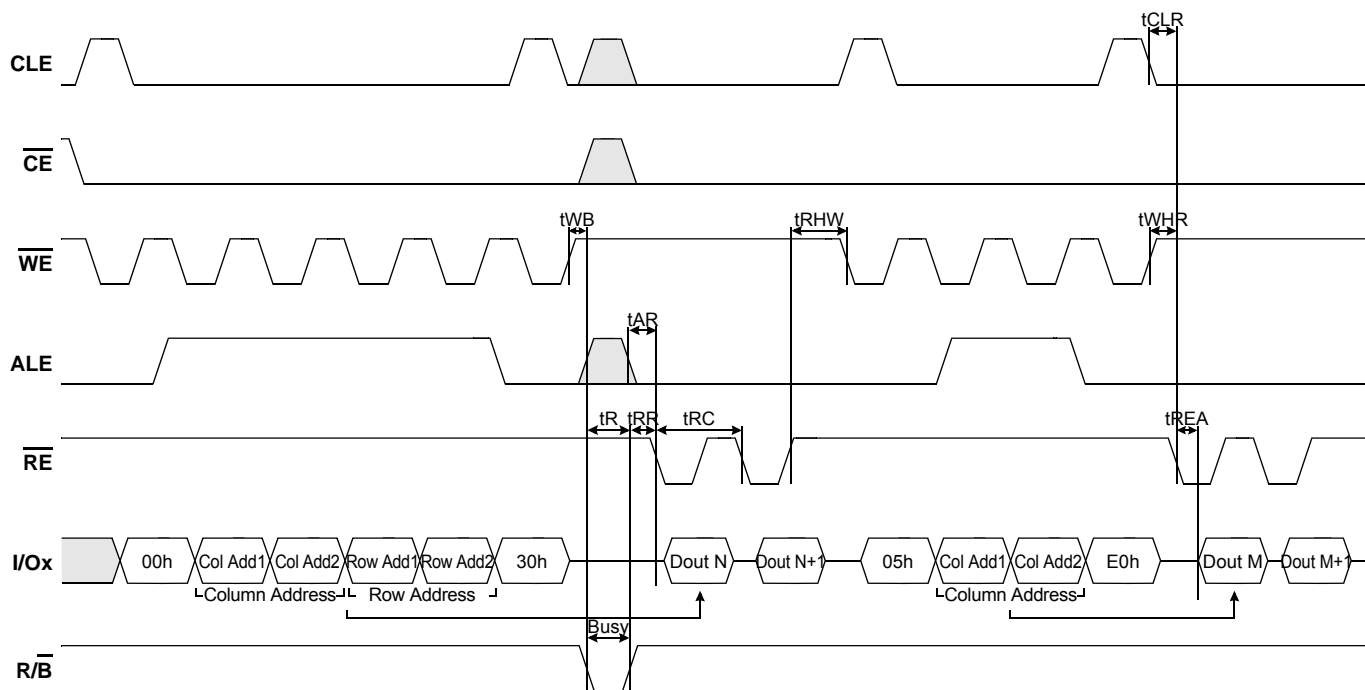
4.6 Read Operation



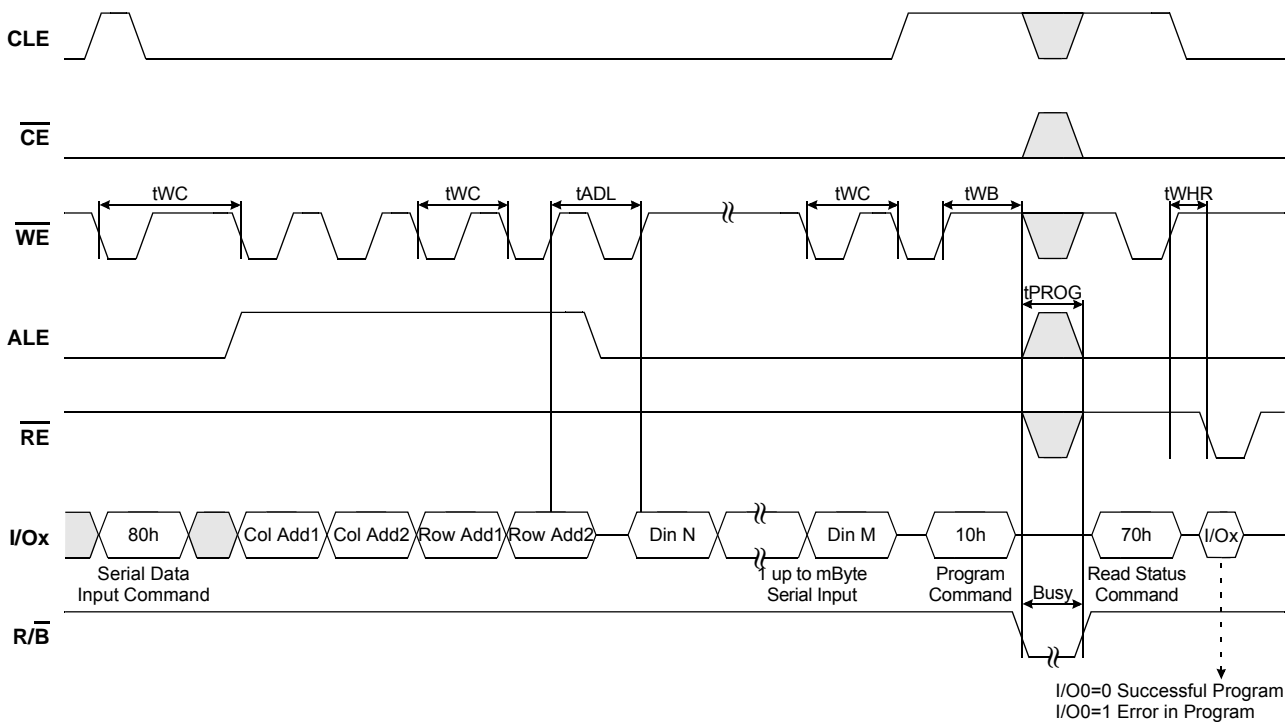
4.7 Read Operation (Intercepted by CE)



4.8 Random Data Output In a Page Operation

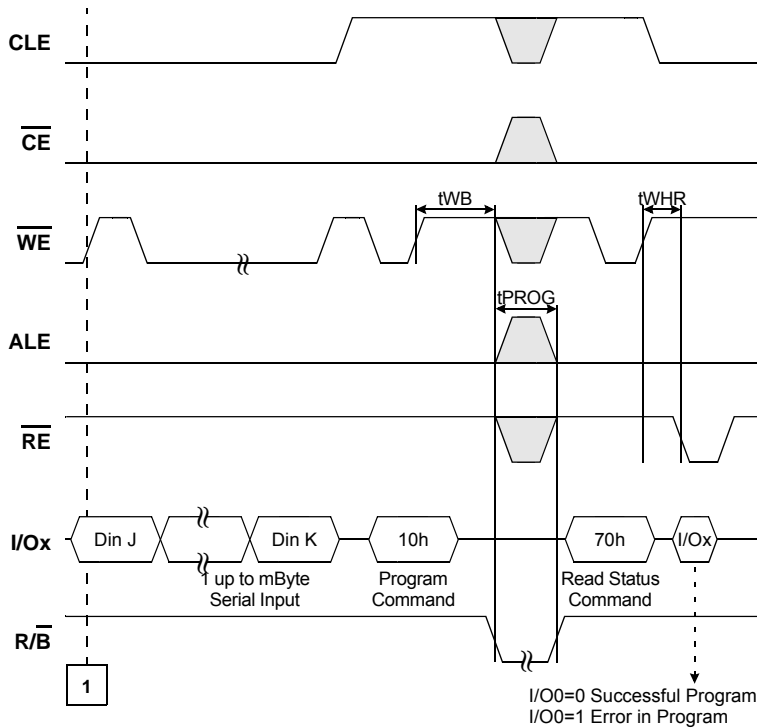
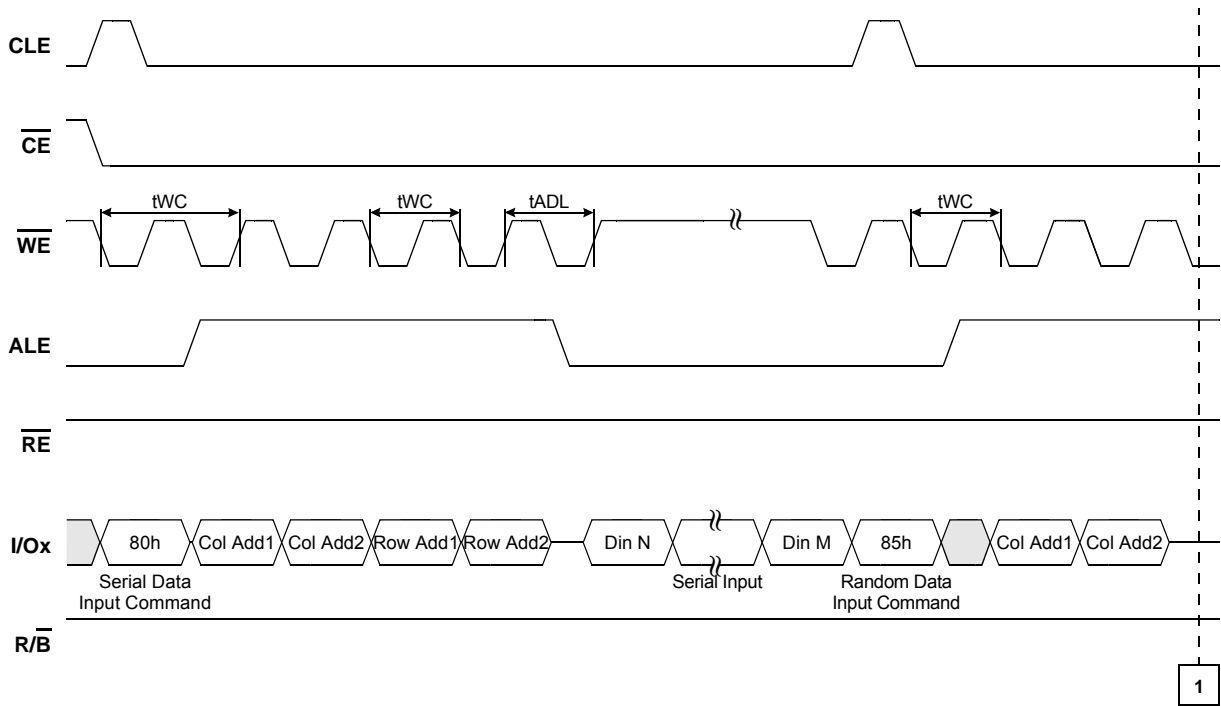


4.9 Page Program Operation

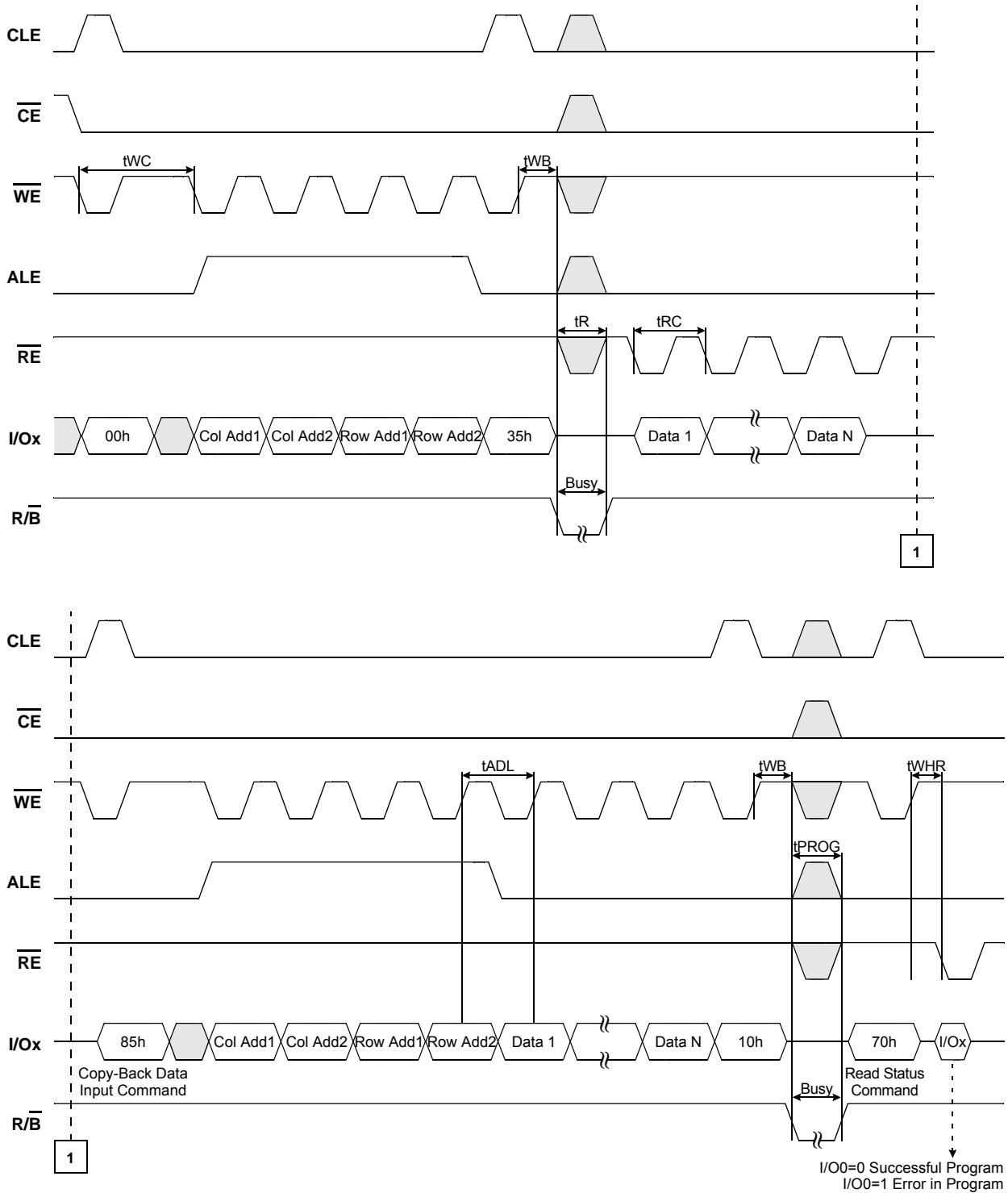


NOTE :
 tADL is the time from the \overline{WE} rising edge of final address cycle to the \overline{WE} rising edge of first data cycle.

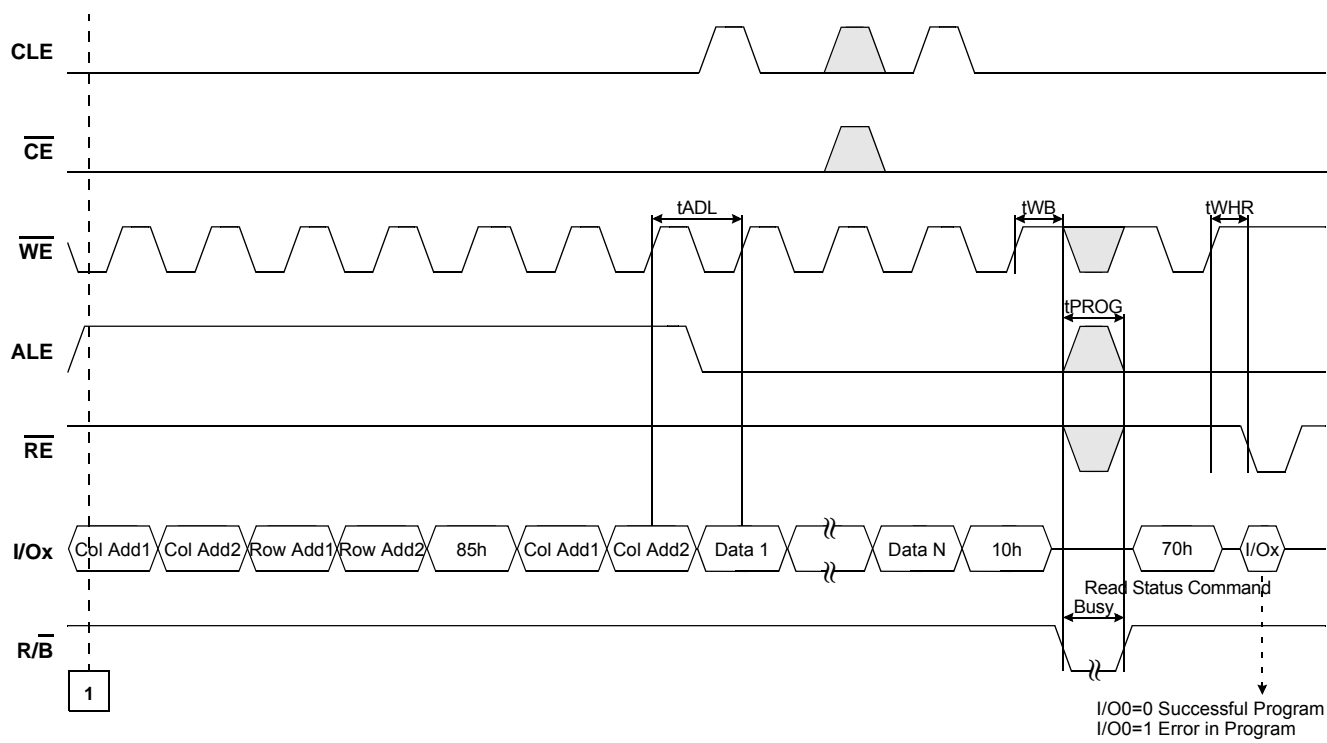
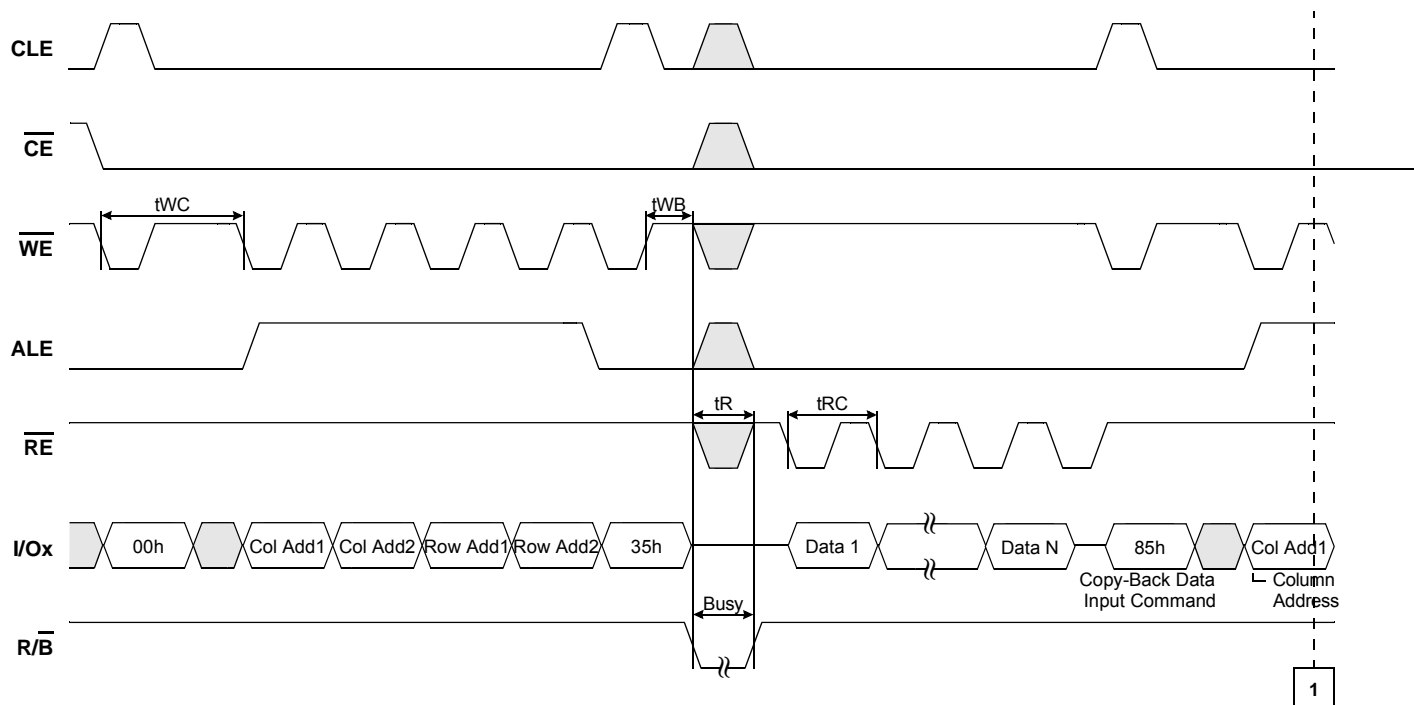
4.10 Page Program Operation with Random Data Input Operation



4.11 Copy-Back Program Operation

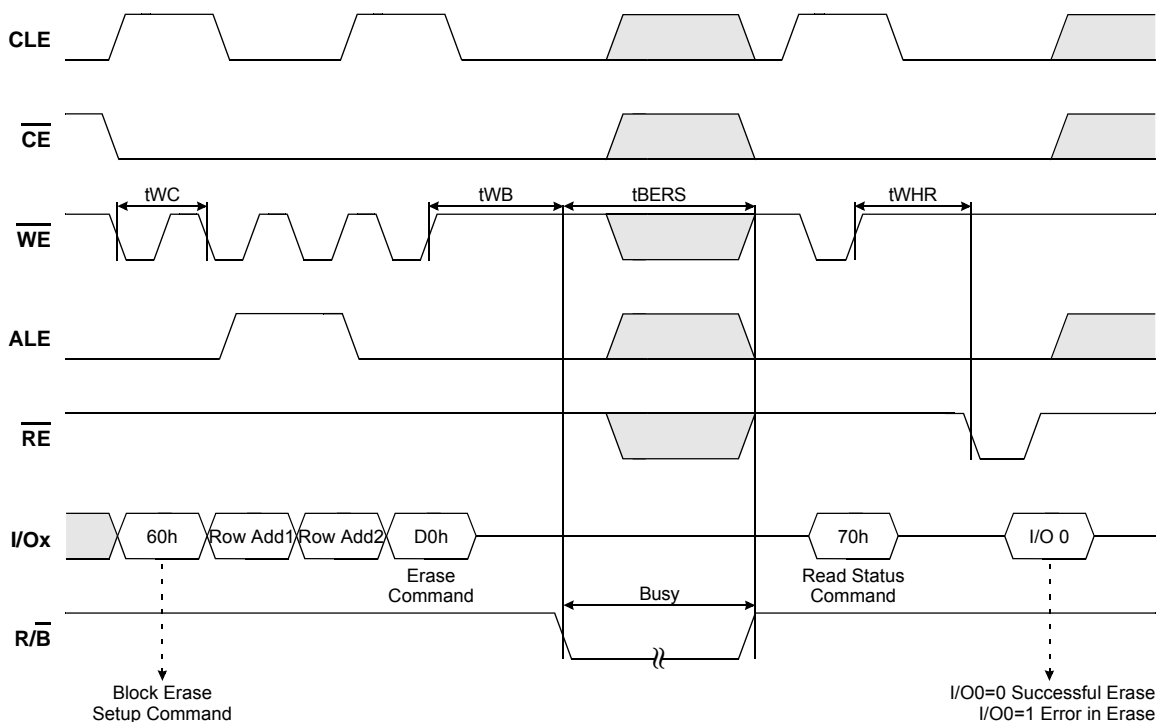


4.12 Copy-Back Program Operation with Random Data Input Operation

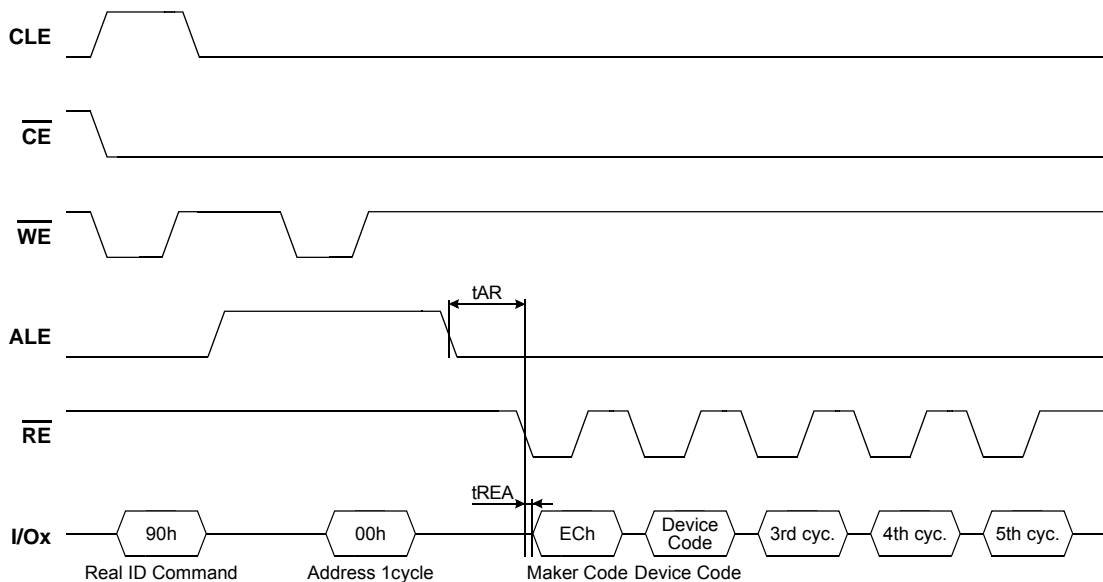


NOTE :
 1) tADL is the time from the \overline{WE} rising edge of final address cycle to the \overline{WE} rising edge of first data cycle.
 2) Copy-Back Program operation is allowed only within the same memory plane.

4.13 Block Erase Operation



4.14 Read ID Operation



5.0 DEVICE OPERATION

5.1 Page Read Operation

Page read is initiated by writing 00h-30h to the command register along with four address cycles. After initial power up, 00h command is latched. Therefore only four address cycles and 30h command initiates that operation after initial power up. The 2,112 bytes of data within the selected page are transferred to the data registers in less than $25\mu\text{s}(t_R)$. The system controller can detect the completion of this data transfer (t_R) by analyzing the output of R/B pin. Once the data in a page is loaded into the data registers, they may be read out in 25ns cycle time by sequentially pulsing $\overline{\text{RE}}$. The repetitive high to low transitions of the $\overline{\text{RE}}$ clock make the device output the data starting from the selected column address up to the last column address.

The device may output random data in a page instead of the consecutive sequential data by writing random data output command. The column address of next data, which is going to be out, may be changed to the address which follows random data output command. Random data output can be operated multiple times regardless of how many times it is done in a page.

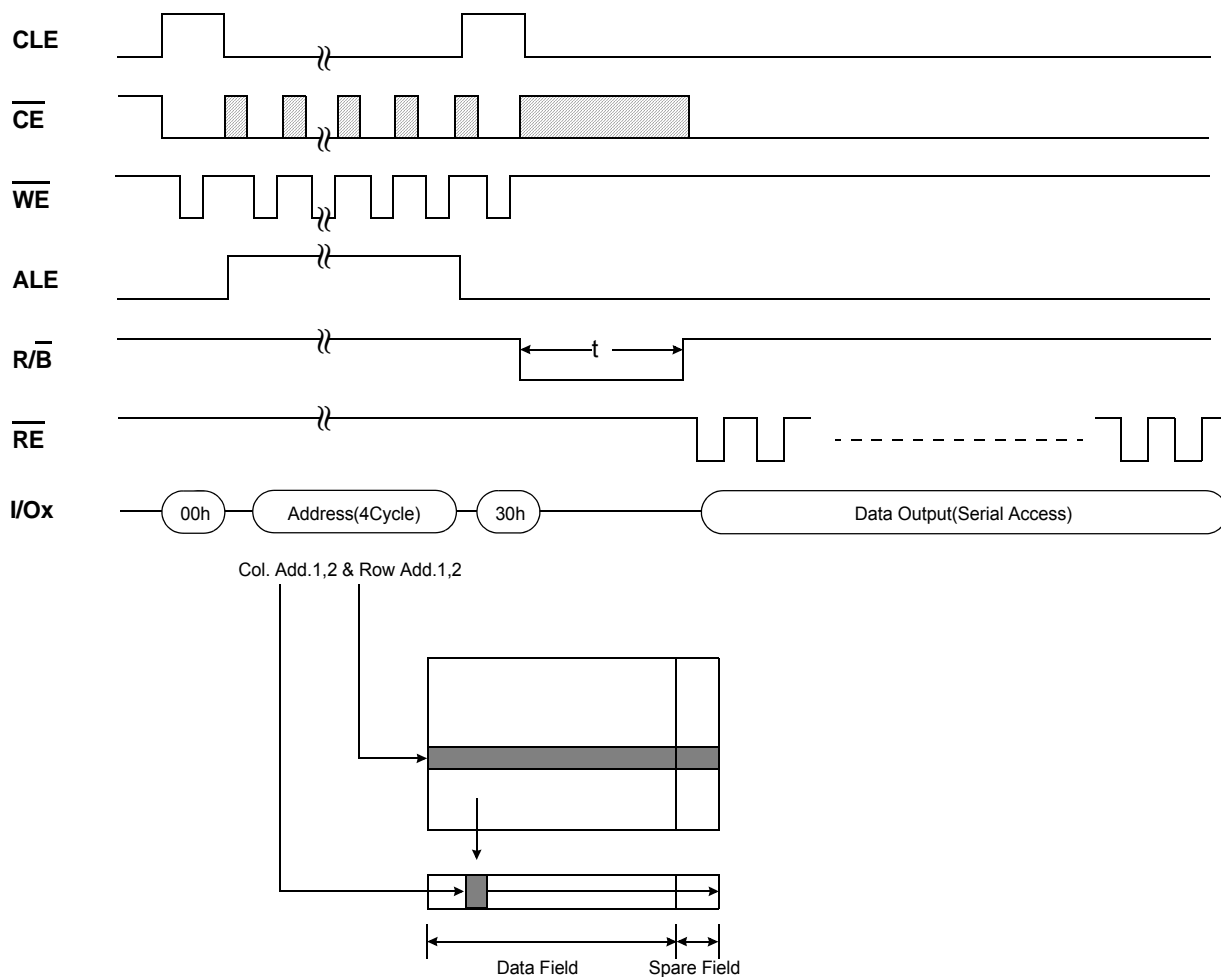


Figure 8. Page Read Sequence

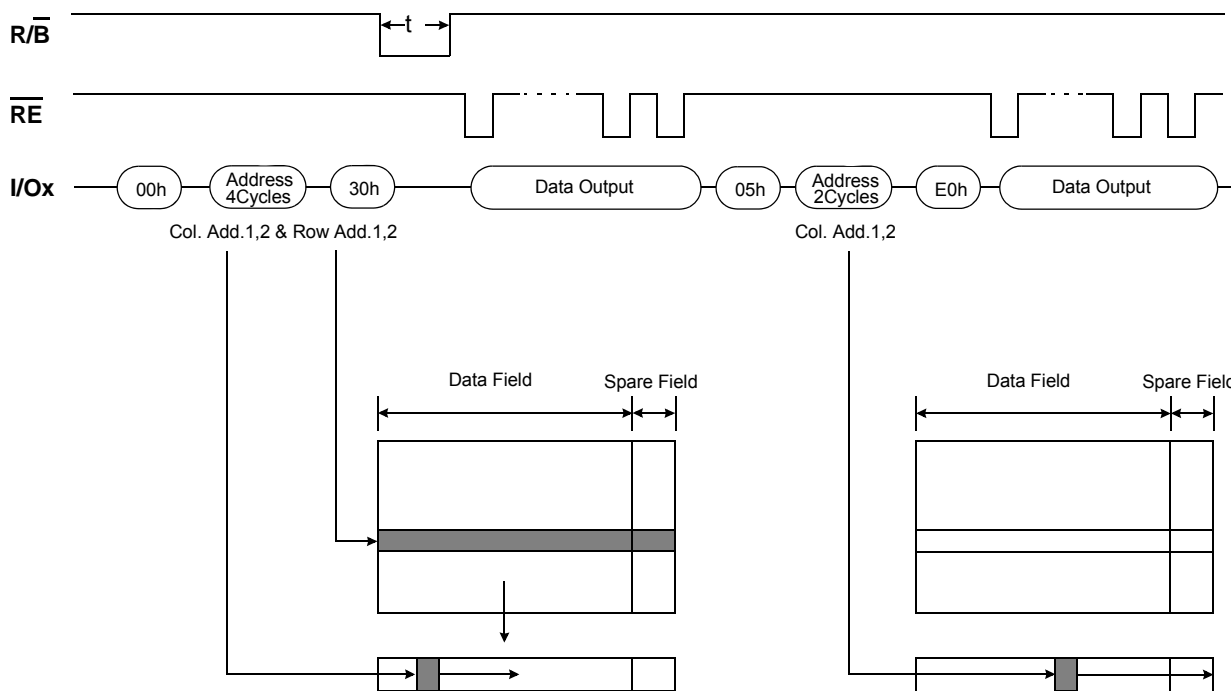


Figure 9. Page Read with Random Data Output Sequence

5.2 Page Program Operation

The device is programmed basically on a page basis, and each page shall be programmed only once before being erased. The addressing should be done in sequential order in a block. A page program cycle consists of a serial data loading period in which up to 2,112bytes of data may be loaded into the data register, followed by a non-volatile programming period where the loaded data is programmed into the appropriate cell. The serial data loading period begins by inputting the Serial Data Input command(80h), followed by the four cycle address inputs and then serial data loading. The words other than those to be programmed do not need to be loaded. The device supports random data input in a page. The column address for the next data, which will be entered, may be changed to the address which follows random data input command(85h). Random data input may be operated multiple times regardless of how many times it is done in a page. The Page Program confirm command(10h) initiates the programming process. Writing 10h alone without previously entering the serial data will not initiate the programming process. The internal write state controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the system controller for other tasks. Once the program process starts, the Read Status Register command may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 10). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

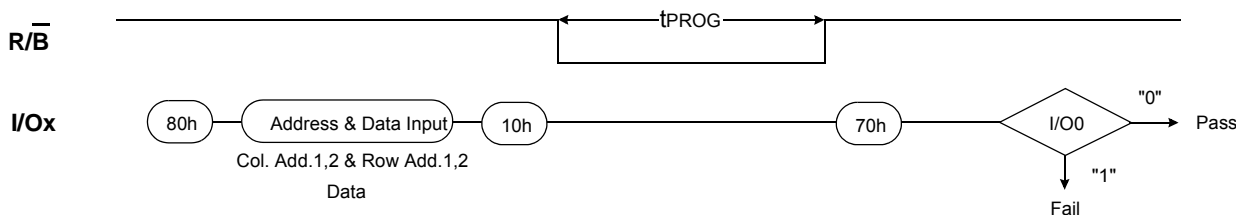


Figure 10. Page Program Sequence

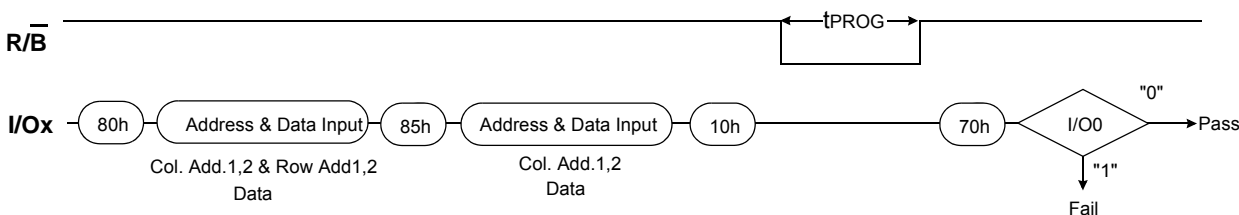
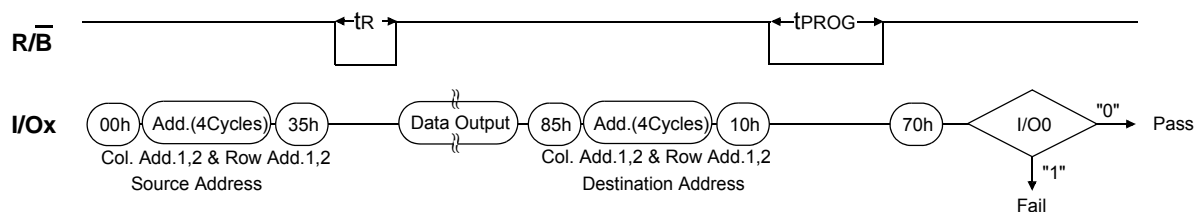


Figure 11. Program Operation with Random Data Input Sequence

5.3 Copy-Back Program Operation

Copy-Back program with Read for Copy-Back is configured to quickly and efficiently rewrite data stored in one page. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly assigned free block. Copy-Back operation is a sequential execution of Read for Copy-Back and of copy-back program with the destination page address. A read operation with "35h" command and the address of the source page moves the whole 2,112-byte data into the internal data buffer. A bit error is checked by sequential reading the data output. In the case where there is no bit error, the data do not need to be reloaded. Therefore Copy-Back program operation is initiated by issuing Page-Copy Data-Input command (85h) with destination page address. Actual programming operation begins after Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the R/B output, or the Status bit(I/O 6) of the Status Register. When the Copy-Back Program is complete, the Write Status Bit(I/O 0) may be checked(Figure 11). The command register remains in Read Status command mode until another valid command is written to the command register.

During copy-back program, data modification is possible using random data input command (85h) as shown in Figure 12.



NOTE :
Copy-Back Program operation is allowed only within the same memory plane.

Figure 12. Copy-Back Program Sequence

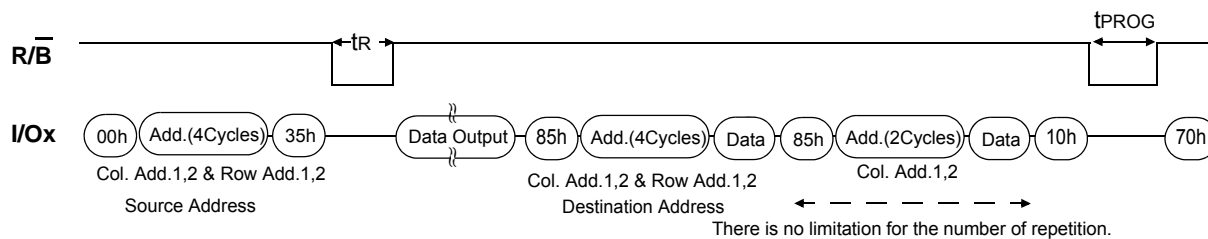


Figure 13. Copy-Back Program with Random Data Input Sequence

5.4 Block Erase Operation

The Erase operation is done on a block basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60h). Only address A18 to A27 is valid while A12 to A17 is ignored. The Erase Confirm command(D0h) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution command ensures that memory contents are not accidentally erased due to external noise conditions.

At the rising edge of \overline{WE} after the erase confirm command input, the internal write controller handles erase and erase-verify. When the erase operation is completed, the Write Status Bit(I/O 0) may be checked. Figure 14 details the sequence.

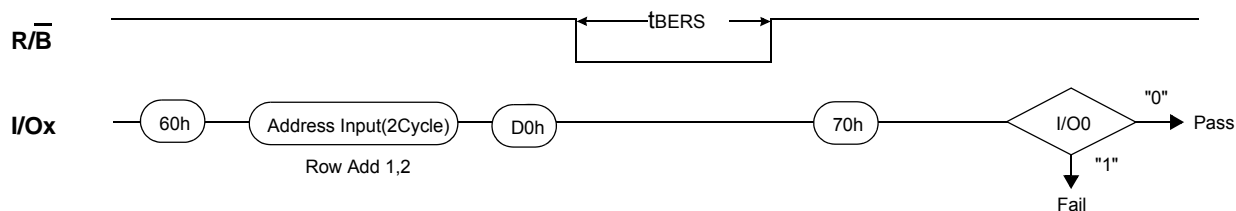


Figure 14. Block Erase Sequence

5.5 Read Status

The device contains a Status Register which may be read to find out whether program or erase operation is completed, and whether the program or erase operation is completed successfully. After writing 70h command to the command register, a read cycle outputs the content of the Status Register to the I/O pins on the falling edge of \overline{CE} or \overline{RE} , whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/B pins are common-wired. \overline{RE} or \overline{CE} does not need to be toggled for updated status. Refer to Table 14 for specific Status Register definitions. The command register remains in Read Status mode until further commands are issued to it. Therefore, if the status register is read during a random read cycle, the read command(00h) should be given before starting read cycles.

[Table 14] Status Register Definition for 70h Command

I/O	Page Program	Block Erase	Read	Definition
I/O 0	Pass/Fail	Pass/Fail	Not use	Pass : "0" Fail : "1"
I/O 1	Not use	Not use	Not use	Don't -cared
I/O 2	Not use	Not use	Not use	Don't -cared
I/O 3	Not use	Not use	Normal or uncorrectable / Recommended to rewrite	Chip Read Status Normal or uncorrectable : 0 Recommended to rewrite : 1
I/O 4	Not Use	Not Use	Not Use	Don't -cared
I/O 5	Not Use	Not Use	Not Use	Don't -cared
I/O 6	Ready/Busy	Ready/Busy	Ready/Busy	Busy : "0" Ready : "1"
I/O 7	Write Protect	Write Protect	Write Protect	Protected : "0" Not Protected : "1"

NOTE :

1) I/Os defined 'Not use' are recommended to be masked out when Read Status is being executed.

5.6 ECC Read Status

Using the ECC Read Status function, the Error Correction Status can be identified.

ECC is performed on the NAND Flash main and spare areas.

The ECC Read Status function also shows the number of errors in a sector as identified from a ECC check during a read operation.

7	6	5	4	3	2	1	I/O0
Sector Information				ECC Status			

[Table 15] ECC Status

I/O3 to I/O0	ECC Status
0000	No Error
0001	1bit error (Correctable)
0010	2bit error (Correctable)
0011	3bit error (Correctable)
0100	4bit error (Correctable)
Others	Reserved

[Table 16] Sector Information

I/O7 to I/O4	Sector Information
0000	1st Sector (Main and Spare area)
0001	2nd Sector (Main and Spare area)
0010	3rd Sector (Main and Spare area)
0011	4th Sector (Main and Spare area)
Others	Reserved

5.7 ECC Sector Information

ECC is generated by internal ECC logic during program operation.

During Read operation, the device automatically executes ECC. After read operation is executed, read status command can be issued to identify the read status the read status remains unmodified until other valid commands are executed.

[Table 17] 2KByte Page Assignment

1'st Main	2'nd Main	3'rd Main	4'th Main	1'st Spare	2'nd Spare	3'rd Spare	4'th Spare
512B	512B	512B	512B	16B	16B	16B	16B

[Table 18] Definition of 528Byte Sector

Sector	Column Address (Byte)	
	Main Field	Spare Field
1'st Sector	0 ~ 511	2,048 ~ 2,063
2'nd Sector	512 ~ 1,023	2,064 ~ 2,079
3'rd Sector	1,024 ~ 1,535	2,080 ~ 2,095
4'th Sector	1,536 ~ 2,047	2,096 ~ 2,111

NOTE :

1) The Internal ECC manages all data of Main area and Spare area.

2) A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

5.8 Partial Page Program Information

Each Sector can be programmed individually as defined Figure 15.

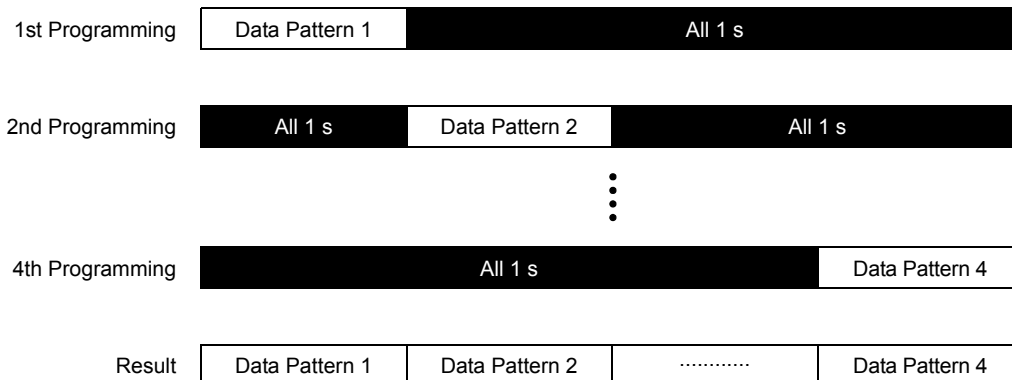


Figure 15. Partial Page Program Guide

NOTE :

1) A sector is the minimum unit for program operation and the number of program per page must not exceed 4.

5.9 Read ID

5.9.1 00h Address ID Definition

The device contains a product identification mode, initiated by writing 90h to the command register, followed by an address input of 00h. Five read cycles sequentially output the manufacturer code (ECh), and the device code and 3rd, 4th, 5th cycle ID respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 16 shows the operation sequence.

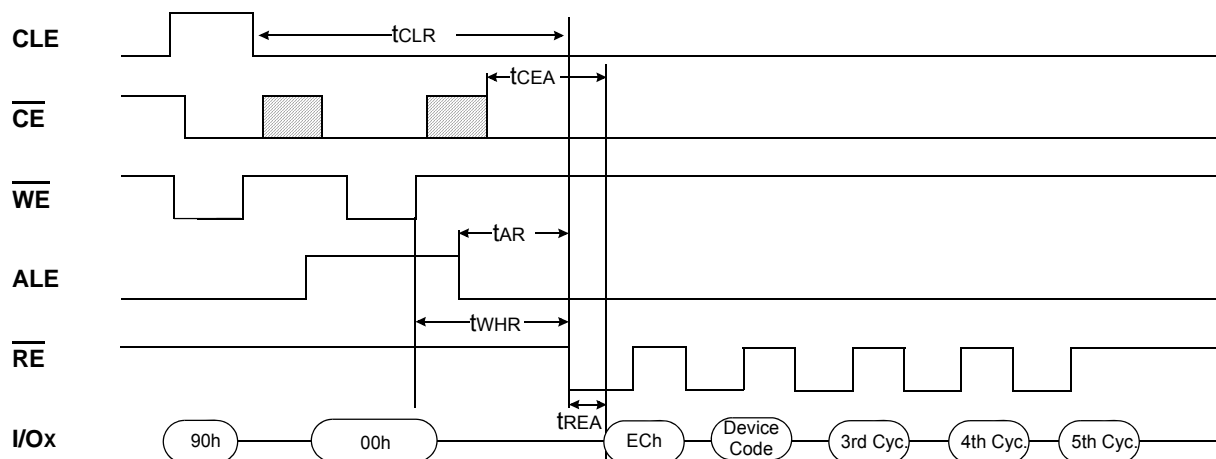


Figure 16. Read ID Sequence

5.9.1.1 00h Address ID Cycle

[Table 19] 00h Address ID cycle

Device	Device Code (2nd Cycle)	3rd Cycle	4th Cycle	5th Cycle
K9F1G08U0F	F1h	00h	95h	42h

[Table 20] 00 Address ID Definition Table

	Description
1 st Byte	Maker Code
2 nd Byte	Device Code
3 rd Byte	Internal Chip Number, Cell Type, Number of Simultaneously Programmed Pages, Etc
4 th Byte	Page Size, Block Size, Redundant Area Size, Organization, Serial Access Minimum
5 th Byte	Plane Number, Plane Size

[Table 21] 3rd ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Internal Chip Number	1							0	0
	2							0	1
	4							1	0
	8							1	1
Cell Type	2 Level Cell					0	0		
	4 Level Cell					0	1		
	8 Level Cell					1	0		
	16 Level Cell					1	1		
Number of Simultaneously Programmed Pages	1			0	0				
	2			0	1				
	4			1	0				
	8			1	1				
Interleave Program Between multiple chips	Not Support		0						
	Support		1						
Cache Program	Not Support	0							
	Support	1							

[Table 22] 4th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Page Size (w/o redundant area)	1KB							0	0
	2KB							0	1
	4KB							1	0
	8KB							1	1
Block Size (w/o redundant area)	64KB			0	0				
	128KB			0	1				
	256KB			1	0				
	512KB			1	1				
Redundant Area Size (byte/512byte)	8						0		
	16						1		
Organization	x8		0						
	x16		1						
Serial Access Minimum	50ns/30ns	0				0			
	25ns	1				0			
	Reserved	0				1			
	Reserved	1				1			

[Table 23] 5th ID Data

	Description	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
Plane Number	1					0	0		
	2					0	1		
	4					1	0		
	8					1	1		
Plane Size (w/o redundant Area)	64Mb		0	0	0				
	128Mb		0	0	1				
	256Mb		0	1	0				
	512Mb		0	1	1				
	1Gb		1	0	0				
	2Gb		1	0	1				
	4Gb		1	1	0				
	8Gb		1	1	1				
Proccess	21nm							0	1
	1ynm							1	0
	reserved							0	0
	reserved							1	1
Reserved		0						0	0

5.10 Reset Operation

The device offers a reset feature, executed by writing FFh to the command register. When the device is in Busy state during random read, program or erase mode, the reset operation will abort these operations. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0h when \overline{WP} is high. If the device is already in reset state a new reset command will be accepted by the command register. The $\overline{R/B}$ pin changes to low for t_{RST} after the Reset command is written. Refer to Figure 17 below

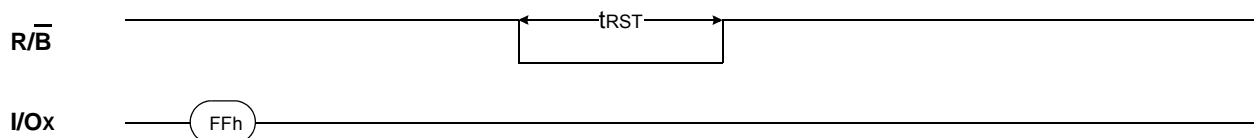


Figure 17. Reset Sequence

[Table 24] Device Status

	After Power-up	After Reset
Operation mode Mode	00h Command is latched	Waiting for next command

5.11 Ready/Busy

The device has a R/B output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/B pin is normally high but transitions to low after program or erase command is written to the command register or random read is started after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more R/B outputs to be Or-tied. Because pull-up resistor value is related to tr(R/B) and current drain during busy(ibusy), an appropriate value can be obtained with the following reference chart.(Figure 18). Its value can be determined by the following guidance.

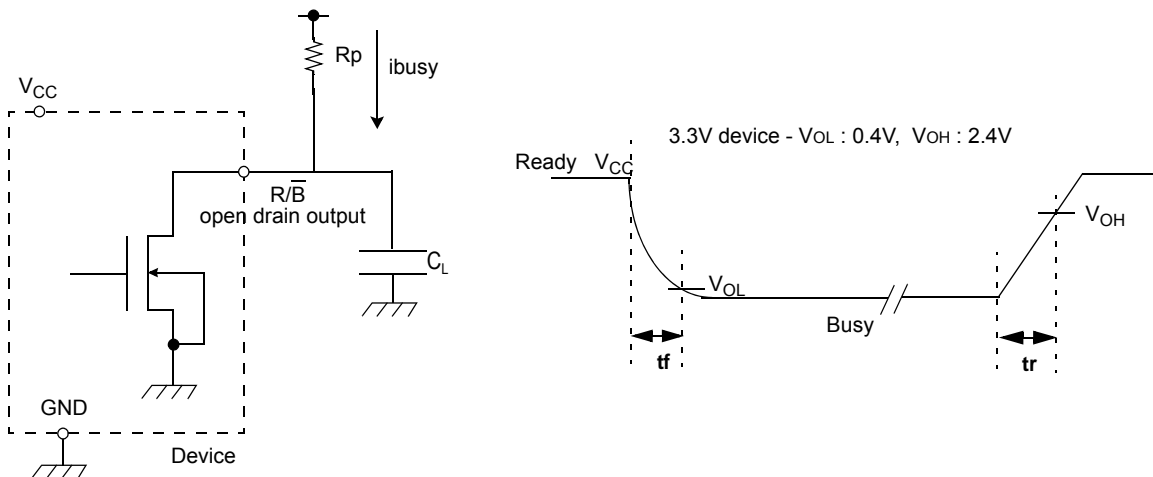
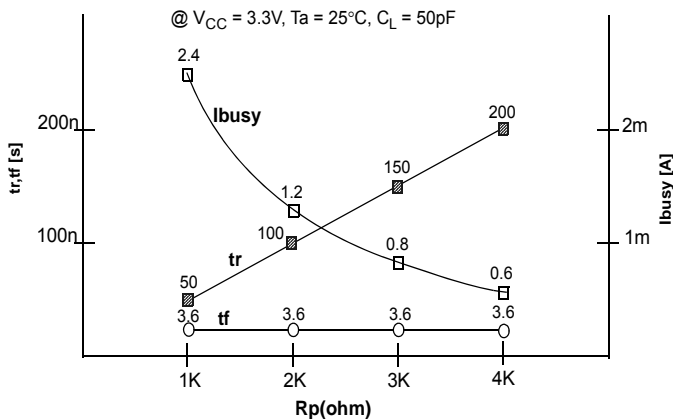


Figure 18. Rp vs tr, tf & Rp vs ibusy



Rp value guidance

$$Rp(\text{min, 3.3V part}) = \frac{V_{CC}(\text{Max.}) - V_{OL}(\text{Max.})}{I_{OL} + \sum I_L} = \frac{3.2V}{8\text{mA} + \sum I_L}$$

where IL is the sum of the input currents of all devices tied to the R/B pin.

Rp(max) is determined by maximum permissible limit of tr