Datasheet

Ultra-Low Power Serial Persistent SRAM Memory

Revision E

Ultra-Low Power Serial Persistent SRAM Memory

(AS1001101, AS1004101, AS1008101, AS1016101, AS1032101, AS3001101, AS3004101, AS3008101, AS3016101, AS3032101)

Features

- Interface
  - Serial Peripheral Interface SPI (1-1-1)
- Technology
  - 40nm pMTJ STT-MRAM
  - Data Endurance: 10^{16} write cycles
  - Data Retention: 20 years @ 85°C
- Density
  - 1Mb, 4Mb, 8Mb, 16Mb, 32Mb
- Operating Voltage Range
  - V_{CC}: 1.71V – 2.00V
  - V_{CC}: 2.70V – 3.60V
- Operating Temperature Range
  - Commercial: 0°C to 70°C
  - Industrial: -40°C to 85°C
  - Industrial Plus: -40°C to 105°C
- Packages
  - 8-pad WSON (5.0mm x 6.0mm)
  - 8-pin SOIC (5.2mm x 5.2mm)
- Data Protection
  - Hardware Based
    - Write Protect Pin (WP#)
  - Software Based
    - Address Range Selectable through Configuration bits (Top/Bottom, Block Protect[2:0])
- Identification
  - 64-bit Unique ID
  - 64-bit User Programmable Serial Number
- Augmented Storage Array (Reflow Protected)
  - 256-byte User Programmable and Lockable
- Supports HOLD# Functionality - Pause

Performance

Device Operation	Typical Values	Units
Frequency of Operation	10.0 (maximum)	MHz
Standby Current (Commercial)	1.3 (typical)	µA
Active Current (Commercial)	1.8 (typical)	mA

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General Description

ASxxxx101 is a magneto-resistive random-access memory (MRAM). It is offered in density ranging from 1Mbit to 32Mbit. MRAM technology is analogous to Flash technology with SRAM compatible read/write timings (Persistent SRAM, P-SRAM). Data is always non-volatile with unlimited endurance and greater than 20-year retention.

Figure 1: Technology Comparison

	SRAM	Flash	EEPROM	MRAM
Non-Volatility	–	√	√	√
Write Performance	√	–	–	√
Read Performance	√	–	–	√
Endurance	√	–	–	√
Power	–	–	–	√

MRAM is a true random-access memory; allowing both reads and writes to occur randomly in memory. MRAM is ideal for applications that must store and retrieve data without incurring large latency penalties. It offers low latency, low power, infinite endurance and scalable non-volatile memory technology.

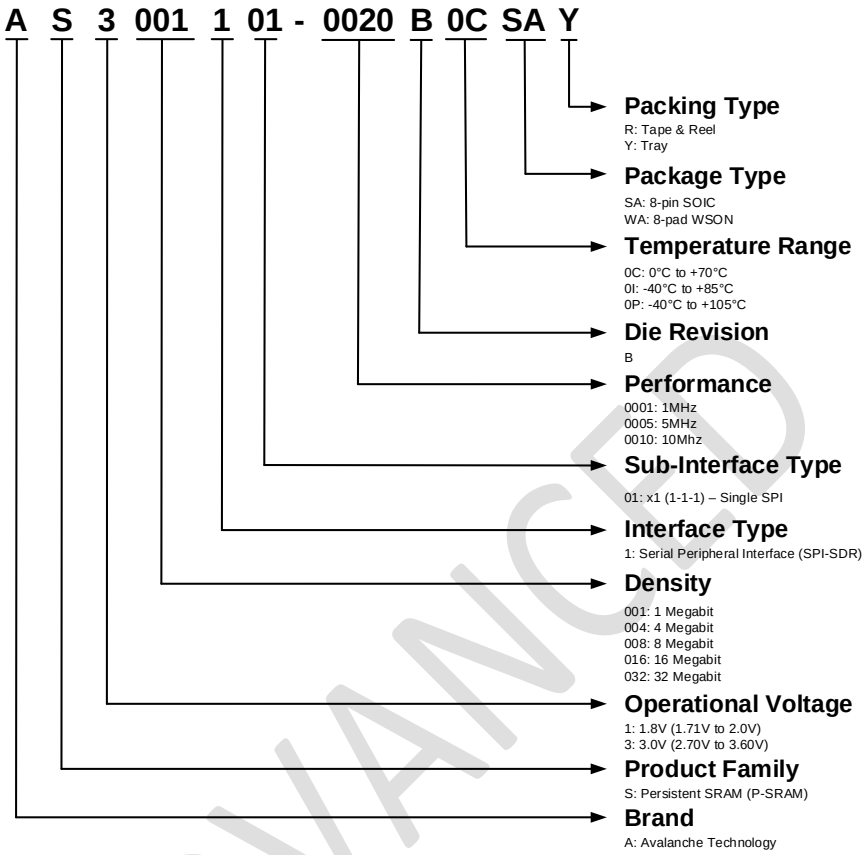
ASxxxx101 has a Serial Peripheral Interface (SPI). SPI is a synchronous interface which uses separate lines for data and clock to help keep the host and slave in perfect synchronization. The clock tells the receiver exactly when to sample the bits on the data line. This can be either the rising (Low to High) or falling (High to Low) edge of the clock signal; please consult the instruction sequences in this datasheet for more details. When the receiver detects that correct edge, it can latch in the data.

ASxxxx101 is available in small footprint 8-pad WSON and 8-pin SOIC packages. These packages are compatible with similar low-power volatile and non-volatile products.

ASxxxx101 is offered with commercial (0°C to 70°C), industrial (-40°C to 85°C) and industrial plus (-40°C to 105°C) operating temperature ranges.

Ordering Options

The ordering part numbers are firmed by a valid combination of the following options:



Valid Combinations — Standard

Valid Combinations list includes device configurations currently available. Contact your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1: Valid Combinations List

Valid Combinations – 1MHz				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS1001101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS1001101-0001B0CSAR
				AS1001101-0001B0CSAY
				AS1001101-0001B0ISAR
				AS1001101-0001B0ISAY
				AS1001101-0001B0PSAR
				AS1001101-0001B0PSAY
				AS1001101-0001B0CWAR
				AS1001101-0001B0CWAY
				AS1001101-0001B0IWAR

				AS1001101-0001B0IWAY
				AS1001101-0001B0PWAR
				AS1001101-0001B0PWAY
AS1004101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS1004101-0001B0CSAR
				AS1004101-0001B0CSAY
				AS1004101-0001B0ISAR
				AS1004101-0001B0ISAY
				AS1004101-0001B0PSAR
				AS1004101-0001B0PSAY
				AS1004101-0001B0CWAR
				AS1004101-0001B0CWAY
				AS1004101-0001B0IWAR
				AS1004101-0001B0IWAY
				AS1004101-0001B0PWAR
				AS1004101-0001B0PWAY
AS1008101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS1008101-0001B0CSAR
				AS1008101-0001B0CSAY
				AS1008101-0001B0ISAR
				AS1008101-0001B0ISAY
				AS1008101-0001B0PSAR
				AS1008101-0001B0PSAY
				AS1008101-0001B0CWAR
				AS1008101-0001B0CWAY
				AS1008101-0001B0IWAR
				AS1008101-0001B0IWAY
				AS1008101-0001B0PWAR
				AS1008101-0001B0PWAY
AS1016101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS1016101-0001B0CSAR
				AS1016101-0001B0CSAY
				AS1016101-0001B0ISAR
				AS1016101-0001B0ISAY
				AS1016101-0001B0PSAR
				AS1016101-0001B0PSAY
				AS1016101-0001B0CWAR
				AS1016101-0001B0CWAY
				AS1016101-0001B0IWAR
				AS1016101-0001B0IWAY
				AS1016101-0001B0PWAR
				AS1016101-0001B0PWAY
AS1032101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS1032101-0001B0CSAR
				AS1032101-0001B0CSAY

				AS1032101-0001B0ISAR
				AS1032101-0001B0ISAY
				AS1032101-0001B0PSAR
				AS1032101-0001B0PSAY
				AS1032101-0001B0CWAR
				AS1032101-0001B0CWAY
				AS1032101-0001B0IWAR
				AS1032101-0001B0IWAY
				AS1032101-0001B0PWAR
				AS1032101-0001B0PWAY
AS3001101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS3001101-0001B0CSAR
				AS3001101-0001B0CSAY
				AS3001101-0001B0ISAR
				AS3001101-0001B0ISAY
				AS3001101-0001B0PSAR
				AS3001101-0001B0PSAY
				AS3001101-0001B0CWAR
				AS3001101-0001B0CWAY
				AS3001101-0001B0IWAR
				AS3001101-0001B0IWAY
				AS3001101-0001B0PWAR
				AS3001101-0001B0PWAY
AS3004101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS3004101-0001B0CSAR
				AS3004101-0001B0CSAY
				AS3004101-0001B0ISAR
				AS3004101-0001B0ISAY
				AS3004101-0001B0PSAR
				AS3004101-0001B0PSAY
				AS3004101-0001B0CWAR
				AS3004101-0001B0CWAY
				AS3004101-0001B0IWAR
				AS3004101-0001B0IWAY
				AS3004101-0001B0PWAR
				AS3004101-0001B0PWAY
AS3008101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS3008101-0001B0CSAR
				AS3008101-0001B0CSAY
				AS3008101-0001B0ISAR
				AS3008101-0001B0ISAY
				AS3008101-0001B0PSAR
				AS3008101-0001B0PSAY
				AS3008101-0001B0CWAR
				AS3008101-0001B0CWAY
				AS3008101-0001B0IWAR

				AS3008101-0001B0IWAY
				AS3008101-0001B0PWAR
				AS3008101-0001B0PWAY
AS3016101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS3016101-0001B0CSAR
				AS3016101-0001B0CSAY
				AS3016101-0001B0ISAR
				AS3016101-0001B0ISAY
				AS3016101-0001B0PSAR
				AS3016101-0001B0PSAY
				AS3016101-0001B0CWAR
				AS3016101-0001B0CWAY
				AS3016101-0001B0IWAR
				AS3016101-0001B0IWAY
				AS3016101-0001B0PWAR
				AS3016101-0001B0PWAY
AS3032101-0001B	0C, 0I, 0P	SA, WA	R, Y	AS3032101-0001B0CSAR
				AS3032101-0001B0CSAY
				AS3032101-0001B0ISAR
				AS3032101-0001B0ISAY
				AS3032101-0001B0PSAR
				AS3032101-0001B0PSAY
				AS3032101-0001B0CWAR
				AS3032101-0001B0CWAY
				AS3032101-0001B0IWAR
				AS3032101-0001B0IWAY
				AS3032101-0001B0PWAR
				AS3032101-0001B0PWAY
Valid Combinations – 5Mhz				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS1001101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS1001101-0005B0CSAR
				AS1001101-0005B0CSAY
				AS1001101-0005B0ISAR
				AS1001101-0005B0ISAY
				AS1001101-0005B0PSAR
				AS1001101-0005B0PSAY
				AS1001101-0005B0CWAR
				AS1001101-0005B0CWAY
				AS1001101-0005B0IWAR
				AS1001101-0005B0IWAY
				AS1001101-0005B0PWAR
				AS1001101-0005B0PWAY
AS1004101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS1004101-0005B0CSAR

				AS1004101-0005B0CSAY
				AS1004101-0005B0ISAR
				AS1004101-0005B0ISAY
				AS1004101-0005B0PSAR
				AS1004101-0005B0PSAY
				AS1004101-0005B0CWAR
				AS1004101-0005B0CWAY
				AS1004101-0005B0IWAR
				AS1004101-0005B0IWAY
				AS1004101-0005B0PWAR
				AS1004101-0005B0PWAY
AS1008101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS1008101-0005B0CSAR
				AS1008101-0005B0CSAY
				AS1008101-0005B0ISAR
				AS1008101-0005B0ISAY
				AS1008101-0005B0PSAR
				AS1008101-0005B0PSAY
				AS1008101-0005B0CWAR
				AS1008101-0005B0CWAY
				AS1008101-0005B0IWAR
				AS1008101-0005B0IWAY
				AS1008101-0005B0PWAR
				AS1008101-0005B0PWAY
AS1016101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS1016101-0005B0CSAR
				AS1016101-0005B0CSAY
				AS1016101-0005B0ISAR
				AS1016101-0005B0ISAY
				AS1016101-0005B0PSAR
				AS1016101-0005B0PSAY
				AS1016101-0005B0CWAR
				AS1016101-0005B0CWAY
				AS1016101-0005B0IWAR
				AS1016101-0005B0IWAY
				AS1016101-0005B0PWAR
				AS1016101-0005B0PWAY
AS1032101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS1032101-0005B0CSAR
				AS1032101-0005B0CSAY
				AS1032101-0005B0ISAR
				AS1032101-0005B0ISAY
				AS1032101-0005B0PSAR
				AS1032101-0005B0PSAY

				AS1032101-0005B0CWAR
				AS1032101-0005B0CWAY
				AS1032101-0005B0IWAR
				AS1032101-0005B0IWAY
				AS1032101-0005B0PWAR
				AS1032101-0005B0PWAY
AS3001101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS3001101-0005B0CSAR
				AS3001101-0005B0CSAY
				AS3001101-0005B0ISAR
				AS3001101-0005B0ISAY
				AS3001101-0005B0PSAR
				AS3001101-0005B0PSAY
				AS3001101-0005B0CWAR
				AS3001101-0005B0CWAY
				AS3001101-0005B0IWAR
				AS3001101-0005B0IWAY
				AS3001101-0005B0PWAR
				AS3001101-0005B0PWAY
AS3004101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS3004101-0005B0CSAR
				AS3004101-0005B0CSAY
				AS3004101-0005B0ISAR
				AS3004101-0005B0ISAY
				AS3004101-0005B0PSAR
				AS3004101-0005B0PSAY
				AS3004101-0005B0CWAR
				AS3004101-0005B0CWAY
				AS3004101-0005B0IWAR
				AS3004101-0005B0IWAY
				AS3004101-0005B0PWAR
				AS3004101-0005B0PWAY
AS3008101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS3008101-0005B0CSAR
				AS3008101-0005B0CSAY
				AS3008101-0005B0ISAR
				AS3008101-0005B0ISAY
				AS3008101-0005B0PSAR
				AS3008101-0005B0PSAY
				AS3008101-0005B0CWAR
				AS3008101-0005B0CWAY
				AS3008101-0005B0IWAR
				AS3008101-0005B0IWAY
				AS3008101-0005B0PWAR
				AS3008101-0005B0PWAY
AS3016101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS3016101-0005B0CSAR
				AS3016101-0005B0CSAY

				AS3016101-0005B0ISAR
				AS3016101-0005B0ISAY
				AS3016101-0005B0PSAR
				AS3016101-0005B0PSAY
				AS3016101-0005B0CWAR
				AS3016101-0005B0CWAY
				AS3016101-0005B0IWAR
				AS3016101-0005B0IWAY
				AS3016101-0005B0PWAR
				AS3016101-0005B0PWAY
AS3032101-0005B	0C, 0I, 0P	SA, WA	R, Y	AS3032101-0005B0CSAR
				AS3032101-0005B0CSAY
				AS3032101-0005B0ISAR
				AS3032101-0005B0ISAY
				AS3032101-0005B0PSAR
				AS3032101-0005B0PSAY
				AS3032101-0005B0CWAR
				AS3032101-0005B0CWAY
				AS3032101-0005B0IWAR
				AS3032101-0005B0IWAY
				AS3032101-0005B0PWAR
				AS3032101-0005B0PWAY
Valid Combinations – 10Mhz				
Base Part Number	**Temperature Range**	**Package Type**	**Packing Type**	**Part Number**
AS1001101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS1001101-0010B0CSAR
				AS1001101-0010B0CSAY
				AS1001101-0010B0ISAR
				AS1001101-0010B0ISAY
				AS1001101-0010B0PSAR
				AS1001101-0010B0PSAY
				AS1001101-0010B0CWAR
				AS1001101-0010B0CWAY
				AS1001101-0010B0IWAR
				AS1001101-0010B0IWAY
				AS1001101-0010B0PWAR
				AS1001101-0010B0PWAY
AS1004101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS1004101-0010B0CSAR
				AS1004101-0010B0CSAY
				AS1004101-0010B0ISAR
				AS1004101-0010B0ISAY
				AS1004101-0010B0PSAR
				AS1004101-0010B0PSAY

				AS1004101-0010B0CWAR
				AS1004101-0010B0CWAY
				AS1004101-0010B0IWAR
				AS1004101-0010B0IWAY
				AS1004101-0010B0PWAR
				AS1004101-0010B0PWAY
AS1008101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS1008101-0010B0CSAR
				AS1008101-0010B0CSAY
				AS1008101-0010B0ISAR
				AS1008101-0010B0ISAY
				AS1008101-0010B0PSAR
				AS1008101-0010B0PSAY
				AS1008101-0010B0CWAR
				AS1008101-0010B0CWAY
				AS1008101-0010B0IWAR
				AS1008101-0010B0IWAY
				AS1008101-0010B0PWAR
				AS1008101-0010B0PWAY
AS1016101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS1016101-0010B0CSAR
				AS1016101-0010B0CSAY
				AS1016101-0010B0ISAR
				AS1016101-0010B0ISAY
				AS1016101-0010B0PSAR
				AS1016101-0010B0PSAY
				AS1016101-0010B0CWAR
				AS1016101-0010B0CWAY
				AS1016101-0010B0IWAR
				AS1016101-0010B0IWAY
				AS1016101-0010B0PWAR
				AS1016101-0010B0PWAY
AS1032101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS1032101-0010B0CSAR
				AS1032101-0010B0CSAY
				AS1032101-0010B0ISAR
				AS1032101-0010B0ISAY
				AS1032101-0010B0PSAR
				AS1032101-0010B0PSAY
				AS1032101-0010B0CWAR
				AS1032101-0010B0CWAY
				AS1032101-0010B0IWAR
				AS1032101-0010B0IWAY
				AS1032101-0010B0PWAR

				AS1032101-0010B0PWAY
AS3001101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS3001101-0010B0CSAR
				AS3001101-0010B0CSAY
				AS3001101-0010B0ISAR
				AS3001101-0010B0ISAY
				AS3001101-0010B0PSAR
				AS3001101-0010B0PSAY
				AS3001101-0010B0CWAR
				AS3001101-0010B0CWAY
				AS3001101-0010B0IWAR
				AS3001101-0010B0IWAY
				AS3001101-0010B0PWAR
				AS3001101-0010B0PWAY
AS3004101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS3004101-0010B0CSAR
				AS3004101-0010B0CSAY
				AS3004101-0010B0ISAR
				AS3004101-0010B0ISAY
				AS3004101-0010B0PSAR
				AS3004101-0010B0PSAY
				AS3004101-0010B0CWAR
				AS3004101-0010B0CWAY
				AS3004101-0010B0IWAR
				AS3004101-0010B0IWAY
				AS3004101-0010B0PWAR
				AS3004101-0010B0PWAY
AS3008101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS3008101-0010B0CSAR
				AS3008101-0010B0CSAY
				AS3008101-0010B0ISAR
				AS3008101-0010B0ISAY
				AS3008101-0010B0PSAR
				AS3008101-0010B0PSAY
				AS3008101-0010B0CWAR
				AS3008101-0010B0CWAY
				AS3008101-0010B0IWAR
				AS3008101-0010B0IWAY
				AS3008101-0010B0PWAR
				AS3008101-0010B0PWAY
AS3016101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS3016101-0010B0CSAR
				AS3016101-0010B0CSAY
				AS3016101-0010B0ISAR
				AS3016101-0010B0ISAY
				AS3016101-0010B0PSAR
				AS3016101-0010B0PSAY
				AS3016101-0010B0CWAR

				AS3016101-0010B0CWAY
				AS3016101-0010B0IWAR
				AS3016101-0010B0IWAY
				AS3016101-0010B0PWAR
				AS3016101-0010B0PWAY
AS3032101-0010B	0C, 0I, 0P	SA, WA	R, Y	AS3032101-0010B0CSAR
				AS3032101-0010B0CSAY
				AS3032101-0010B0ISAR
				AS3032101-0010B0ISAY
				AS3032101-0010B0PSAR
				AS3032101-0010B0PSAY
				AS3032101-0010B0CWAR
				AS3032101-0010B0CWAY
				AS3032101-0010B0IWAR
				AS3032101-0010B0IWAY
				AS3032101-0010B0PWAR
				AS3032101-0010B0PWAY

Signal Description and Assignment

Figure 2: Device Pinout

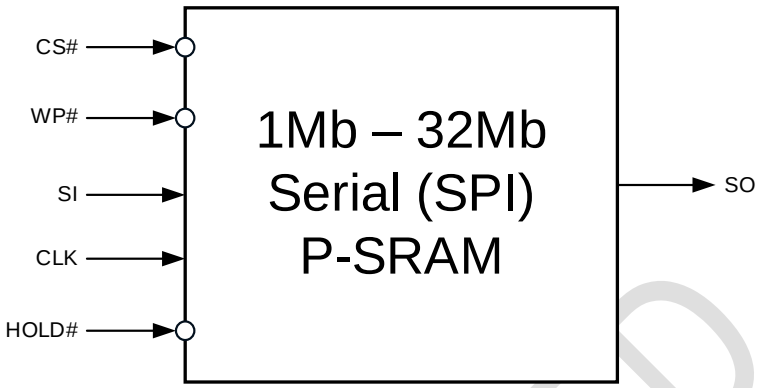


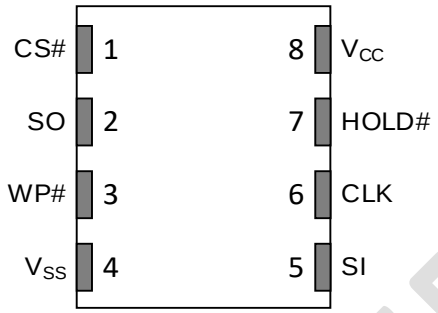
Table 2: Signal Description

Signal	Type	Description
CS#	Input	**Chip Select:** When CS# is driven High, the device will enter standby mode. All other input pins are ignored and the output pin is tri-stated. Driving CS# Low enables the device, placing it in the active mode. After power-up, a falling edge on CS# is required prior to the start of any instructions.
WP#	Input	**Write Protect:** Write protects the status register in conjunction with the enable/disable bit of the status register. This is important since other write protection features are controlled through the Status Register. When the enable/disable bit of the status register is set to 1 and the WP# signal is driven Low, the status register becomes read-only and the WRITE STATUS REGISTER operation will not execute. This signal does not have internal pull-ups, it cannot be left floating and must be driven.
CLK	Input	**Clock:** Provides the timing of the serial interface. Command, address and data inputs are latched on the rising edge of the clock. Data is output on the falling edge of the clock. The following two SPI clock modes are supported. • SPI Mode 0 (CPOL = 0, CPHA = 0) • SPI Mode 3 (CPOL = 1, CPHA = 1)
HOLD#	Input	**Hold:** Pauses serial communications with the device without deselecting or resetting the device. Outputs are tri-stated and inputs are ignored.
SI	Input	**Serial Data Input:** The unidirectional I/O transfers data into the device on the rising edge of the clock.
SO	Output	**Serial Data Output:** The unidirectional I/O transfers data out of the device on the falling edge of the clock.
V_{CC}	Supply	**V_{CC}:** Core and I/O power supply.
V_{SS}	Supply	**V_{SS}:** Core and I/O ground supply.

Package Options

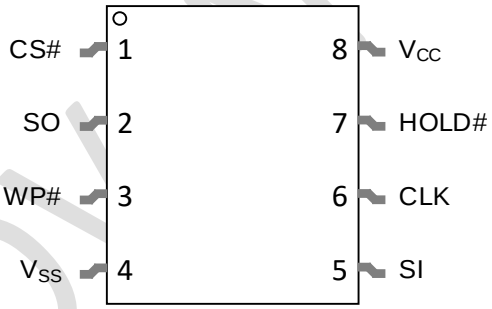
8-Pad WSON (Top View)

Figure 3: 8-Pad WSON



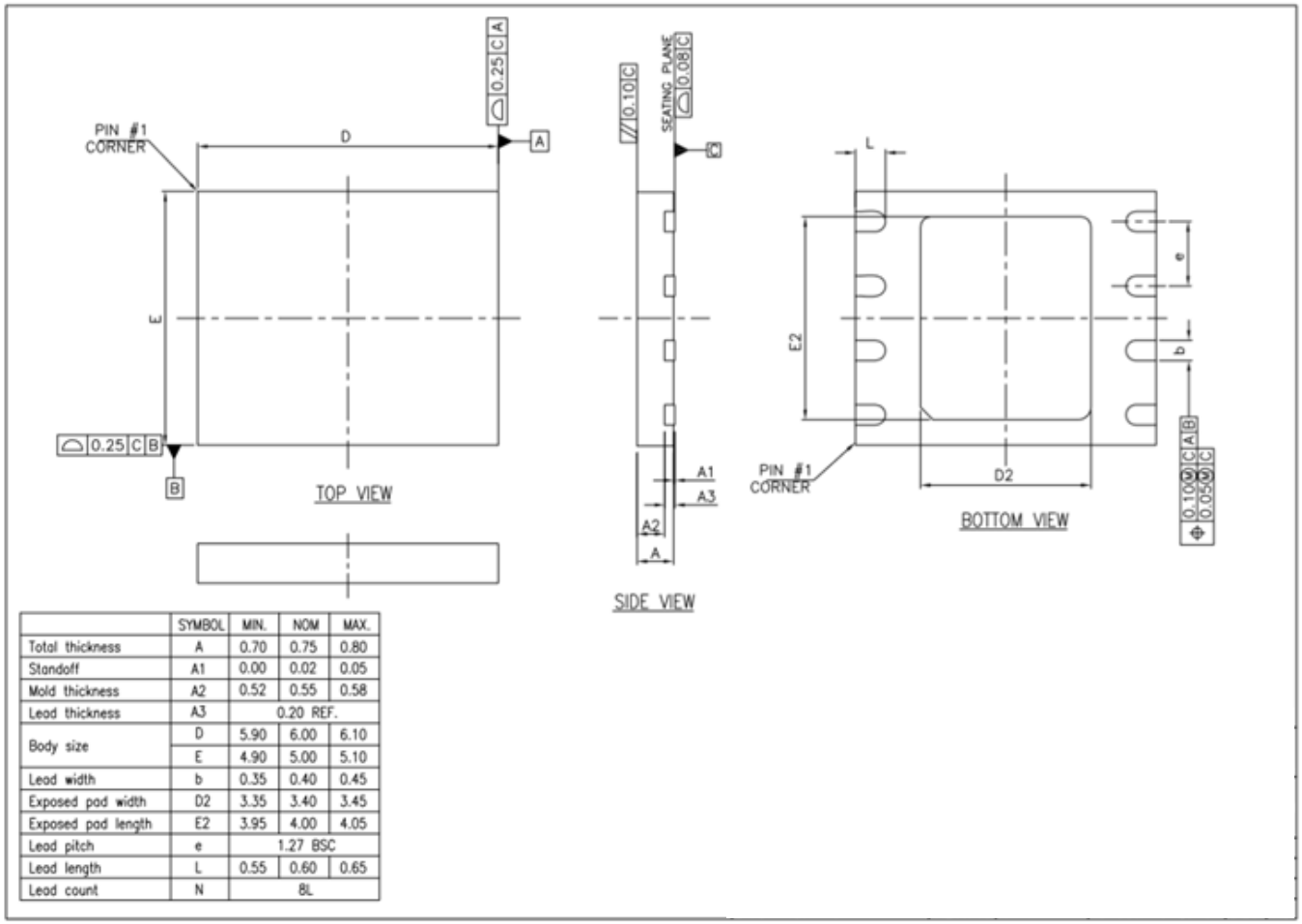
8-Pin SOIC (Top View)

Figure 4: 8-Pin SOIC



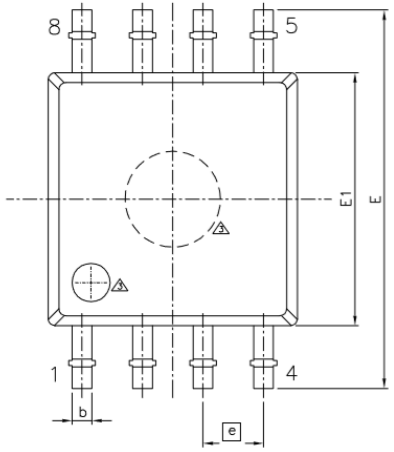
Package Drawings

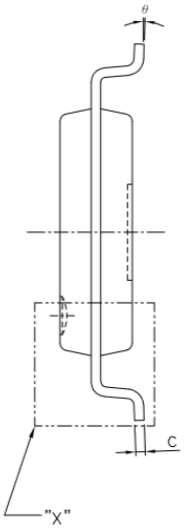
8-Pad WSON



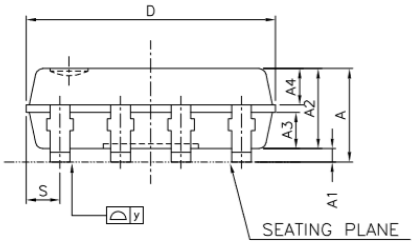
	SYMBOL	MIN.	NOM	MAX.
Total thickness	A	0.70	0.75	0.80
Standoff	A1	0.00	0.02	0.05
Mold thickness	A2	0.52	0.55	0.58
Lead thickness	A3		0.20 REF.	
Body size	D	5.90	6.00	6.10
	E	4.90	5.00	5.10
Lead width	b	0.35	0.40	0.45
Exposed pad width	D2	3.35	3.40	3.45
Exposed pad length	E2	3.95	4.00	4.05
Lead pitch	e		1.27 BSC	
Lead length	L	0.55	0.60	0.65
Lead count	N		8L	

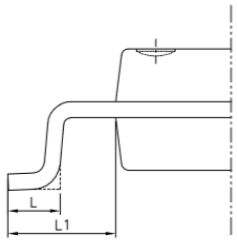
8-Pin SOIC





SYMBOL	DIMENSION (MM)			DIMENSION (MIL)		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	———	———	2.16	———	———	85.04
A1	0.05	0.15	0.25	1.97	5.91	9.84
A2	1.70	1.80	1.91	66.93	70.87	75.20
A3	0.773	0.798	0.823	30.43	31.42	32.40
A4	0.773	0.798	0.823	30.43	31.42	32.40
b	0.36	0.41	0.51	14.17	16.14	20.08
C	0.19	0.20	0.25	7.48	7.87	9.84
D	5.13	5.23	5.33	201.97	205.91	209.84
E	7.70	7.90	8.10	303.15	311.02	318.90
E1	5.18	5.28	5.38	203.94	207.87	211.81
e		1.27 BSC			50 BSC	
L	0.50	0.65	0.80	19.69	25.59	31.50
L1	1.27	1.37	1.47	50.00	53.94	57.87
S	0.62	0.74	0.88	24.41	29.13	34.65
ϕ	0°	5°	8°	0°	5°	8°
y	———	———	0.075	———	———	2.95





DETAIL "X"

NOTE:

1. DIMENSION "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm (6mil) PER SIDE.
2. DIMENSION "E" DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUS SHALL NOT EXCEED 0.25mm (10 mil) PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETER

Architecture

ASxxxx101 is an ultra-low power serial STT-MRAM device. It features a SPI-compatible bus interface, execute-in-place (XIP) functionality, and hardware/software based data protection mechanisms.

When CS# is Low, the device is selected and in active power mode. When CS# is High, the device is deselected but can remain in active power mode until ongoing internal operations are completed. Then the device goes into standby power mode and device current consumption drops to I_{SB}.

ASxxxx101 contains an 8-bit instruction register. All functionality is controlled through the values loaded into this instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of CLK - CS# pin must be Low and the HOLD# pin must be High for the entire operation. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD# input and place ASxxxx101 in 'HOLD' state. After releasing the HOLD# pin, operation will resume from the point when the HOLD# was asserted.

ASxxxx101 has a 256-byte Augmented Storage Array which is independent from the main memory array. The Augmented Storage is reflow protected. It is user programmable and can be locked against inadvertent writes.

The device offers both hardware and software based data protection schemes. Hardware protection is through WP# pin. Software protection is controlled by configuration bits in the Status register. Both schemes inhibit writing to the memory array.

Figure 5: Functional Block Diagram

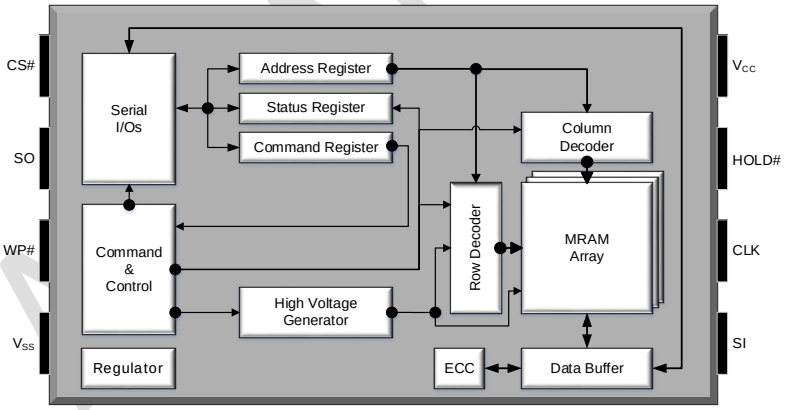


Table 3: Modes of Operation

Mode	CS#	Current	SI	SO	HOLD#
Standby	H	I_{SB}	Gated	Hi-Z	Gated
Active - Read	L	I_{READ}	Instruction	Dataout	H
Active - Write	L	I_{WRITE}	Instruction, Datain	Hi-Z	H
Hold	L	I_{READ}, I_{WRITE}	Not Gated	FD	L

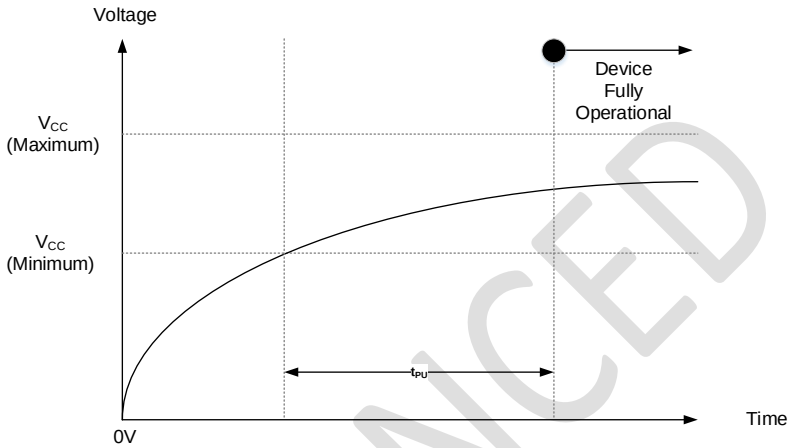
Notes:
H: High (Logic '1')
L: Low (Logic '0')
Hi-Z: High Impedance

Device Initialization

When powering up, the following procedure is required to initialize the device correctly:

- Ramp up V_{CC} (R_{VR})
- CS# must follow V_{CC} during power-up (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- Upon Power-up, the device is in Standby mode

Figure 6: Power-Up Behavior



When powering down, the following procedure is required to turn off the device correctly:

- Ramp down V_{CC} (R_{VF})
- CS# must follow V_{CC} during power-down (a 10KΩ pull-up Resistor to V_{CC} is recommended)
- It is recommended that no instructions are sent to the device when V_{CC} is below V_{CC} (minimum)
- V_{CC} dropping below $V_{CC\text{-}CUTOFF}$ requires it to stay below V_{CC_CUTOFF} for t_{PD}

Figure 7: Power-Down Behavior

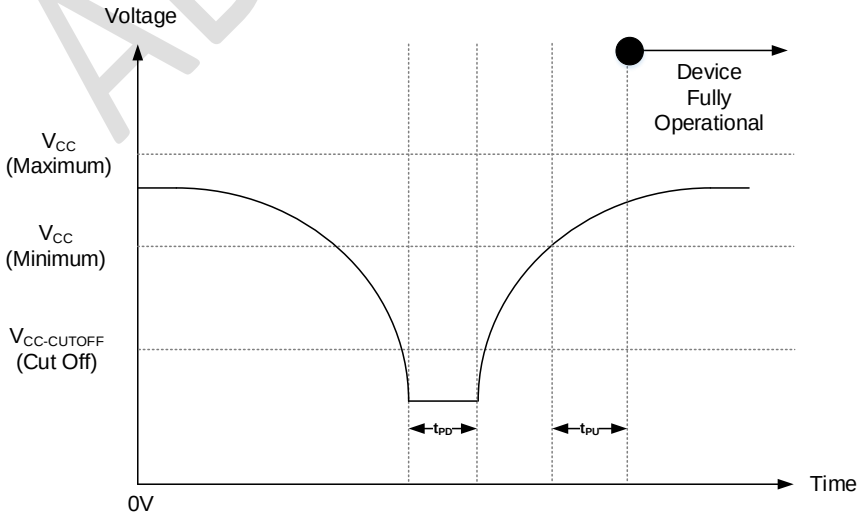


Table 4: Device Initialization Timing

Parameter	Symbol	Test Conditions	3.0V			
			Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	2.7	-	3.6	V
V_{CC} Ramp Up Time	R_{VR}	All operating voltages and temperatures	30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}	All operating voltages and temperatures	20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}	All operating voltages and temperatures	-	-	250	µs
V_{CC} Low Time when V_{CC} at $V_{CC-CUTOFF}$	t_{PD1}	All operating voltages and temperatures	130	-	-	µs
V_{CC} Low Time when V_{CC} at V_{SS}	t_{PD2}	All operating voltages and temperatures	70	-	-	µs
V_{CC} Cutoff – Must Initialize Device	$V_{CC-CUTOFF}$	All operating voltages and temperatures	1.6	-	-	V

Table 5: Device Initialization Timing – 1.8V

Parameter	Symbol	Test Conditions	1.8V			
			Minimum	Typical	Maximum	Units
V_{CC} Range		All operating voltages and temperatures	1.71	-	2.0	V
V_{CC} Ramp Up Time	R_{VR}	All operating voltages and temperatures	30	-	-	µs/V
V_{CC} Ramp Down Time	R_{VF}	All operating voltages and temperatures	20	-	-	µs/V
V_{CC} Power Up to First Instruction	t_{PU}	All operating voltages and temperatures	-	-	250	µs
V_{CC} Low Time when V_{CC} at $V_{CC-CUTOFF}$	t_{PD1}	All operating voltages and temperatures	130	-	-	µs
V_{CC} Low Time when V_{CC} at V_{SS}	t_{PD2}	All operating voltages and temperatures	70	-	-	µs
V_{CC} Cutoff – Must Initialize Device	$V_{CC-CUTOFF}$	All operating voltages and temperatures	1.6	-	-	V

Memory Map

Table 6: Memory Map

Density	Address Range	24-bit Address [23:0]	
1Mb	000000h – 01FFFFh	[23:17] – Logic '0'	[16:0] - Addressable
4Mb	000000h – 07FFFFh	[23:19] – Logic '0'	[18:0] - Addressable
8Mb	000000h – 0FFFFFh	[23:20] – Logic '0'	[19:0] - Addressable
16Mb	000000h – 1FFFFFh	[23:21] – Logic '0'	[20:0] - Addressable
32Mb	000000h – 3FFFFFh	[23:22] – Logic '0'	[21:0] - Addressable

Augmented Storage Array Map

Table 7: Augmented Storage Array Map

Density	Address Range	24-bit Address [23:0]	
1Mb	002000h – 0020FFh [1]	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
4Mb	002000h – 0020FFh [1]	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
8Mb	002000h – 0020FFh [1]	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
16Mb	002000h – 0020FFh [1]	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable
32Mb	002000h – 0020FFh [1]	[23:14] – Logic '0', [13] – Logic '1', [12:8] – Logic '0'	[7:0] - Addressable

Register Map

Status Register / Device Protection Register (Read/Write)

Status register is a legacy SPI register and contains options for enabling/disabling data protection.

Table 8: Status Register

Bits	Name	Description	Read / Write	Default State	Selection Options
SR[7]	WP#EN	Hardware Based WP# Protection Enable/Disable	R/W	0	1: Protection Enabled – write protects when WP# is Low 0: Protection Disabled – Doesn't write protect when WP# is Low
SR[6]	SNPEN	Serial Number Protection Enable/Disable	R/W	0	1: S/N Write protected - protection enabled 0: S/N Writable - protection disabled
SR[5]	TBPSEL	Software Top/Bottom Memory Array Protection Selection	R/W	0	1: Bottom Protection Enabled (Lower Address Range) 0: Top Protection Enabled (Higher Address Range)
SR[4]	BPSEL[2]	Block Protect Selection Bit 2	R/W	0	Block Protection Bits
SR[3]	BPSEL[1]	Block Protect Selection Bit 1	R/W	0	
SR[2]	BPSEL[0]	Block Protect Selection Bit 0	R/W	0	
SR[1]	WREN	Write Operation Enable/Disable	R	0	1: Write Operation Enabled 0: Write Operation Disabled
SR[0]	RSVD	Reserved	R	0	Reserved for future use

Table 9: Top Block Protection Address Range Selection (TBPSEL=0)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb	32Mb
0	**0**	**0**	None	None	None	None	None	None
0	**0**	**1**	Upper 1/64	01F800h – 01FFFFh	07E000h – 07FFFFh	0FC000h – 0FFFFFh	1F8000h – 1FFFFFh	3F8000h – 3FFFFFh
0	**1**	**0**	Upper 1/32	01F000h – 01FFFFh	07C000h – 07FFFFh	0F8000h – 0FFFFFh	1F0000h – 1FFFFFh	3F0000h – 3FFFFFh
0	**1**	**1**	Upper 1/16	01E000h – 01FFFFh	078000h – 07FFFFh	0F0000h – 0FFFFFh	1E0000h – 1FFFFFh	3E0000h – 3FFFFFh
1	**0**	**0**	Upper 1/8	01C000h – 01FFFFh	070000h – 07FFFFh	0E0000h – 0FFFFFh	1C0000h – 1FFFFFh	3C0000h – 3FFFFFh
1	**0**	**1**	Upper 1/4	018000h – 01FFFFh	060000h – 07FFFFh	0C0000h – 0FFFFFh	180000h – 1FFFFFh	380000h – 3FFFFFh
1	**1**	**0**	Upper 1/2	010000h – 01FFFFh	040000h – 07FFFFh	080000h – 0FFFFFh	1F0000h – 1FFFFFh	3F0000h – 3FFFFFh
1	**1**	**1**	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh	000000h – 3FFFFFh

Table 10: Bottom Block Protection Address Range Selection (TBPSEL=1)

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb	32Mb
0	**0**	**0**	None	None	None	None	None	None
0	**0**	**1**	Lower 1/64	000000h – 0007FFh	000000h – 001FFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh
0	**1**	**0**	Lower 1/32	000000h – 00FFFh	000000h – 003FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh

BPSEL [2]	BPSEL [1]	BPSEL [0]	Protected Portion	1Mb	4Mb	8Mb	16Mb	32Mb
0	**1**	**1**	Lower 1/16	000000h – 001FFFh	000000h – 007FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh
1	**0**	**0**	Lower 1/8	000000h – 003FFFh	000000h – 00FFFFh	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh
1	**0**	**1**	Lower 1/4	000000h – 007FFFh	000000h – 01FFFFh	000000h – 03FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh
1	**1**	**0**	Lower 1/2	000000h – 00FFFFh	000000h – 03FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh
1	**1**	**1**	All	000000h – 01FFFFh	000000h – 07FFFFh	000000h – 0FFFFFh	000000h – 1FFFFFh	000000h – 3FFFFFh

Table 11: Write Protection Modes

WREN (Status Register)	WP#EN (Status Register)	WP# (Pin)	Status Register	Memory[1] Array Protected Area	Memory[1] Array Unprotected Area
0	**X**	**X**	Protected	Protected	Protected
1	**0**	**X**	Unprotected	Protected	Unprotected
1	**1**	**Low**	Protected	Protected	Unprotected
1	**1**	**High**	Unprotected	Protected	Unprotected

Notes:
High: Logic '1'
Low: Logic '0'
X: Don't Care – Can be Logic '0' or '1'
Protected: Write protected
Unprotected: Writable
1: Memory address range protection based on Block Protection Bits

Device Identification Register (Read Only)

Device identification register contains Avalanche's Manufacturing ID along with device configuration information.

Table 12: Device Identification Register – Read Only

Size	Avalanche Manufacturer's ID	Device Configuration	Device Density	Device Revision
ID[32:0]	ID[31:24]	ID[23:8]	ID[7:4]	ID[3:0]

Serial Number Register (Read/Write)

Serial Number register is user writable.

Table 13: Serial Number Register – Read and Write

Bits	Name	Description	Read / Write	Default State [1]	Selection Options
SN[63:0]	SN	Serial Number Value	R/W	0000000000000000h	Value stored is based on the customer

Unique Identification Register (Read Only)

Unique Identification register contains a number unique to every device.

Table 14: Unique ID Register – Read Only

Bits	Name	Description	Read / Write	Selection Options
UID[63:0]	UID	Unique Identification Number Value	R	Value stored is written in the factory and is device specific

Instruction Set

Table 15: Instruction Set

#	Instruction Name	Command (Opcode)	1-0-0	1-0-1	1-1-1	Latency Cycles	Data Bytes	Address Bytes	Max. Frequency	Prerequisite
	Control Instructions									
1	**No Operation**	NOOP - 00h	•					0	10MHz	
2	**Write Enable**	WREN- 06h	•					0	10MHz	
3	**Write Disable**	WRDI - 04h	•					0	10MHz	
4	**Software Reset Enable**	SRTE - 66h	•					0	10MHz	
5	**Software Reset**	SRST - 99h	•					0	10MHz	SRTE
	Read Register Instructions									
6	**Read Status Register** [3]	RDSR - 05h		•			1	0	10MHz	
7	**Read Device ID** [3]	RDID - 9Fh		•			4	0	10MHz	
8	**Read Unique ID** [3]	RUID - 4Ch		•			8	0	10MHz	
9	**Read Serial Number Register** [3]	RDSN - C3h		•			8	0	10MHz	
	Write Register Instructions									
10	**Write Status Register**	WRSR - 01h		•			1	0	10MHz	WREN
11	**Write Serial Number Register**	WRSN - C2h		•			8	0	10MHz	WREN
	Read Memory Array Instructions									
12	**Read Memory Array**	READ - 03h			•		1 to ∞	3	10MHz	
13	**Fast Read Memory Array** [4]	RDFT - 0Bh			•	•	1 to ∞	3	10MHz	
	Write Memory Array Instructions									
14	**Write Memory Array**	WRTE - 02h			•		1 to ∞	3	10MHz	WREN
	Augmented Storage Array Instructions									
15	**Read Augmented Storage Array**	RDAS - 4Bh			•		1 to 256	3^2	10MHz	
16	**Write Augmented Storage Array**	WRAS - 42h			•		1 to 256	3^2	10MHz	WREN

Notes:

1: The command code for an instruction is always transmitted on SI according to the SPI standard. However, an instruction may transmit address and data (send or receive) as well. The command-address-data column shows which of these three components the instruction contains. As an example, READ instruction has command, address, and data information: 1-1-1. On the other hand, SRST instruction only has command information: 1-0-0.

2: The augmented storage array is 256-Bytes in size.

3: Registers do not wrap data during reads. Reading beyond the specified number of bytes will yield indeterminate data.

4: Fast Read instruction requires 8 dummy CLK cycles after the address is entered and before the beginning of the read data. SI can be driven High or Low or left floating during the dummy CLK cycles.

Instruction Description and Structures

All communication between a host and ASxxxx101 is in the form of instructions. Instructions define the operation that must be executed. Instructions consist of a command followed by an optional address modifier and data transfer to or from ASxxxx101. All command, address and data information is transferred sequentially. Instructions are structured as follows:

- Each instruction begins with CS# going Low (logic '0') and ends with CS# returning High (Logic'1').
- CLK marks the transfer of each bit.
- Each instructions starts out with an 8-bit command. The command selects the type of operation ASxxxx101 must perform. The command is transferred on the rising edges of CLK.
- The command can be stand alone or followed by address to select a memory location. The address is always 24-bits wide. The address is transferred on the rising edges of CLK.
- The address bits are followed by data bits. Write data bits to ASxxxx101 are transferred on the rising edges of CLK. Read data bits from ASxxxx101 are transferred on the falling edges of CLK.
- Fast Read instruction (RDFT) requires 8 dummy CLK cycles after the address is entered and before the beginning of the read data. The dummy clock cycles are latency cycles. SI is ignored by ASxxxx101 during these dummy cycles.
- Write instructions must be preceded by the WREN instruction. WREN instruction sets the WREN bit in the Status register. WREN bit is reset at the end of every write instruction. WREN bit can also be reset by executing the WRDI instruction.
- The entire memory array can be read from or written to using a single read or write instruction. After the staring address is entered, subsequent address are internally incremented as long as CS# is Low and CLK continues to cycle.
- All commands, address and data are shifted with the most significant bit first.

Figure 8 to Figure 11 shows the description of instruction types supported.

Figure 8: Description of (1-0-0) Instruction Type

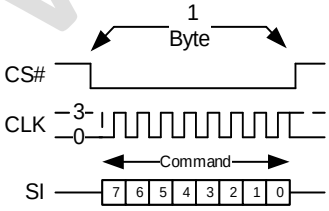


Figure 9: Description of (1-0-1) Instruction Type

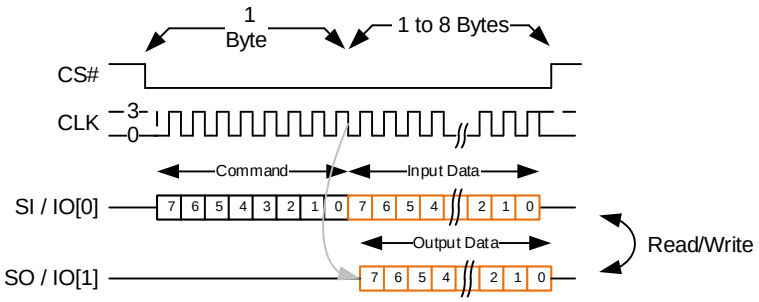


Figure 10: Description of (1-1-1) Instruction Type (No Latency)

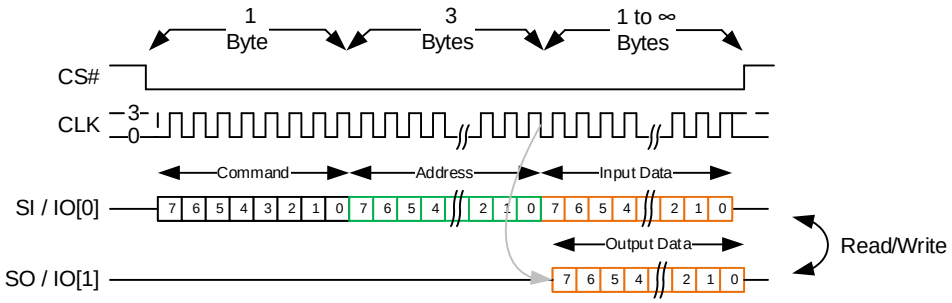
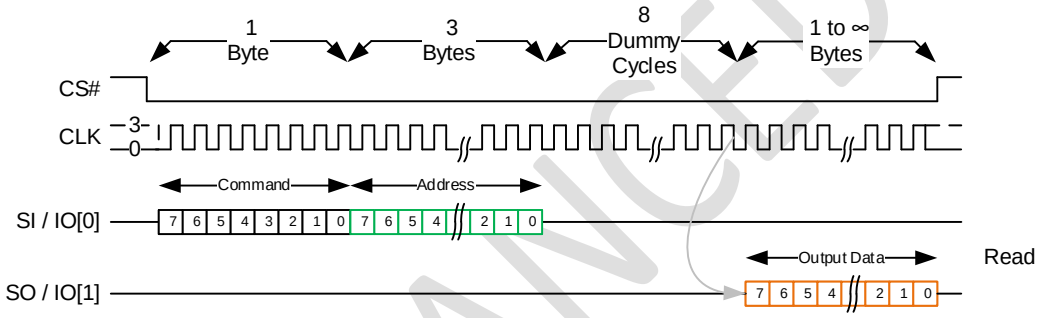


Figure 11: Description of (1-1-1) Instruction Type (With Latency)



Electrical Specifications

Table 16: Recommended Operating Conditions

Parameter / Condition		Minimum	Typical	Maximum	Units
Operating Temperature	Commercial	0.0	-	70.0	°C
	Industrial	-40.0	-	85.0	°C
	Industrial Plus	-40.0	-	105.0	°C
V_{CC} Supply Voltage (1.8V)	1.8V	1.71	1.8	2.0	V
V_{CC} Supply Voltage (3.0V)	3.3V	2.7	3.0	3.6	V
V_{SS} Supply Voltage		0.0	0.0	0.0	V

Table 17: Pin Capacitance

Parameter	Test Conditions	Symbol	Maximum	Units
Input Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{IN}	6.0	pF
Output Pin Capacitance	TEMP = 25°C; f = 1 MHz; V_{IN} = 3.0V	C_{INOUT}	8.0	pF

Table 18: Endurance & Retention

Parameter	Symbol	Test Conditions	Minimum	Units
Write Endurance	END	-	10^{16}	cycles
Data Retention	RET	85°C	20.0	years

Table 19: DC Characteristics

Parameter	Symbol	Test Conditions	3.0V Device (2.7V-3.6V)			
			Minimum	Typical	Maximum	Units
Read Current	I_{READ}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=10MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}	-	1.8	3.0	mA
Write Current	I_{WRITE}	V_{CC} = 3.6V, I_{OUT}=0mA, CLK=10MHz (V_{IL} / V_{IH}), CS#= V_{IL}, SI= V_{IL} or V_{IH}	-	1.8	3.0	mA
Standby Current (CMOS) Commercial (0°C to 70°C)	I_{SB1}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}, Temperature=25°C	-	1.3	-	µA
Standby Current (CMOS) Industrial (-40°C to 85°C)	I_{SB2}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}, Temperature=85°C	-	-	17.0	µA
Standby Current (CMOS) Industrial Plus (-40°C to 105°C)	I_{SB3}	V_{CC} = 3.6V, CLK=V_{CC}, CS#=V_{CC}, SI=V_{CC}, Temperature=105°C	-	-	TBD	µA
Input Leakage Current	I_{LI}	V_{IN}=0 to V_{CC} (max)	-	-	±5.0	µA
Output Leakage Current	I_{LO}	V_{OUT}=0 to V_{CC} (max)	-	-	±5.0	µA

Parameter	Symbol	Test Conditions	3.0V Device (2.7V-3.6V)			
			Minimum	Typical	Maximum	Units
Input High Voltage	V_{IH}		0.7xV_{CC}	-	V_{CC}+0.3	V
Input Low Voltage	V_{IL}		-0.3	-	0.3xV_{CC}	V
Output High Voltage Level	V_{OH}	I_{OH} = -100µA	V_{CC}-0.2	-	-	V
		I_{OH} = -1mA	2.4	-	-	V

Table 20: AC Test Conditions

Parameter	Value
Input pulse levels	0.0V to V_{CC}
Input rise and fall times	3.0ns
Input and output measurement timing levels	V_{CC}/2
Output Load	CL = 30.0pF

CS# Operation & Timing

Figure 12: CS# Operation & Timing

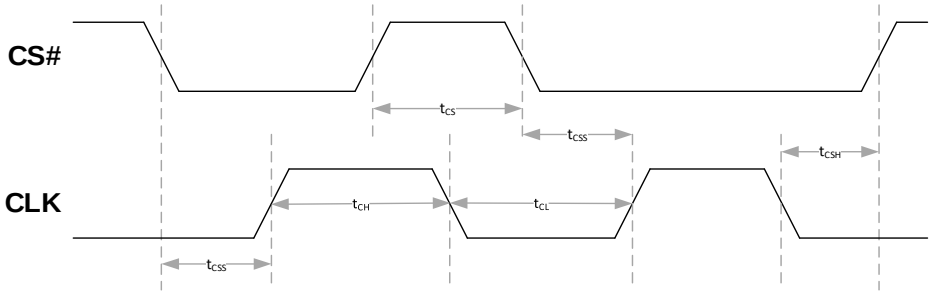


Table 21: CS# Operation

Parameter	Symbol	Minimum	Maximum	Units
Clock Frequency	f_{CLK}	1.0	10.0	MHz
Clock Low Time	t_{CL}	11.0	-	ns
Clock High Time	t_{CH}	11.0	-	ns
CS# High Time (End of Status Register Write)	t_{CS1}	3.0	-	µs
CS# High Time (End of Serial Number Register Write)	t_{CS2}	10.0	-	µs
CS# High Time (End of Memory Array Read / Write)	t_{CS3}	40.0	-	ns
CS# Setup Time (w.r.t CLK)	t_{CSS}	5.0	-	ns
CS# Hold Time (w.r.t CLK)	t_{CSH}	5.0	-	ns

Notes:
Power supplies must be stable

Command, Address and Data Input Operation & Timing

Figure 13: Command, Address and Data Input Operation & Timing

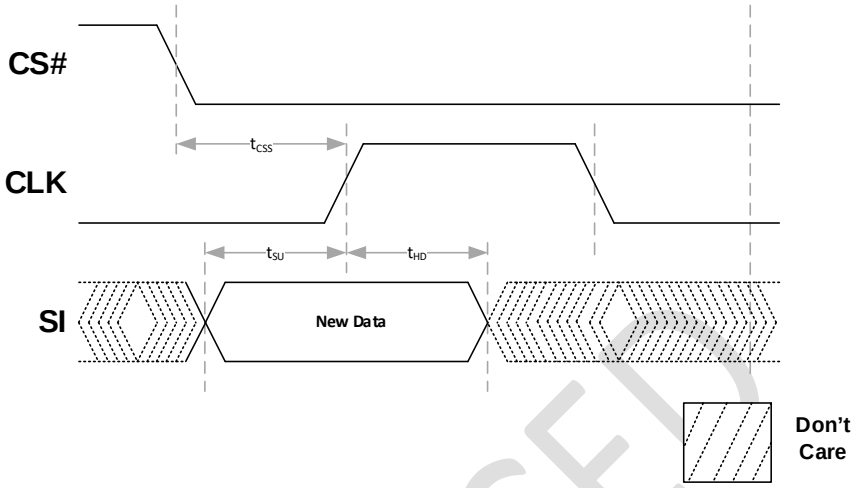


Table 22: Command, Address and Data Input Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
Data Setup Time (w.r.t CLK)	t_{SU}	5.0	-	ns
Data Hold Time (w.r.t CLK)	t_{HD}	5.0	-	ns

Notes:
Power supplies must be stable

Data Output Operation & Timing

Figure 14: Data Output Operation & Timing

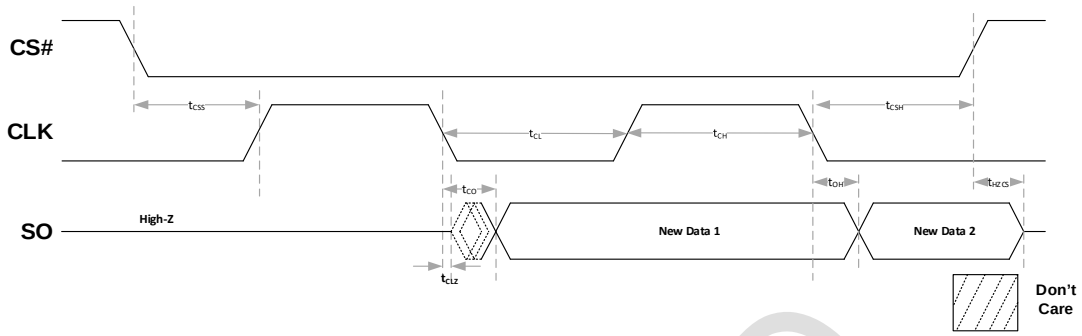


Table 23: Data Output Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
CLK Low to Output Low Z (Active)	t_{CLZ}	0	-	ns
Output Valid (w.r.t CLK)	t_{CO}	-	9.0	ns
Output Hold Time (w.r.t CLK)	t_{OH}	1.0	-	ns
Output Disable Time (w.r.t CS#)	t_{HZCS}	-	12	ns

Notes:
Power supplies must be stable

WP# Operation & Timing

Figure 15: WP# Operation & Timing

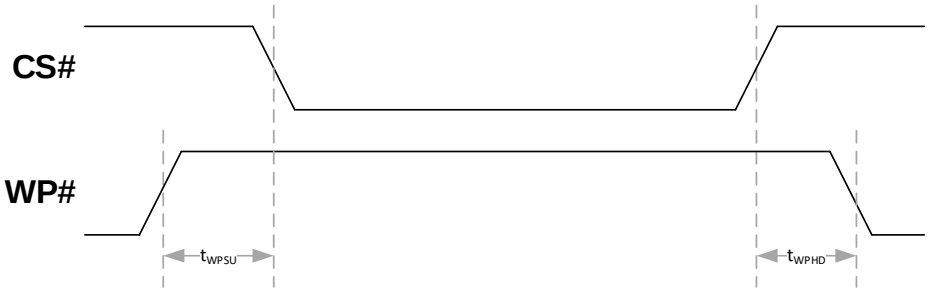


Table 24: WP# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
WP# Setup Time (w.r.t CS#)	t_{WPSU}	20	-	ns
WP# Hold Time (w.r.t CS#)	t_{WPHD}	20	-	ns

Notes:
Power supplies must be stable

HOLD# Operation & Timing

Figure 16: HOLD# Operation & Timing

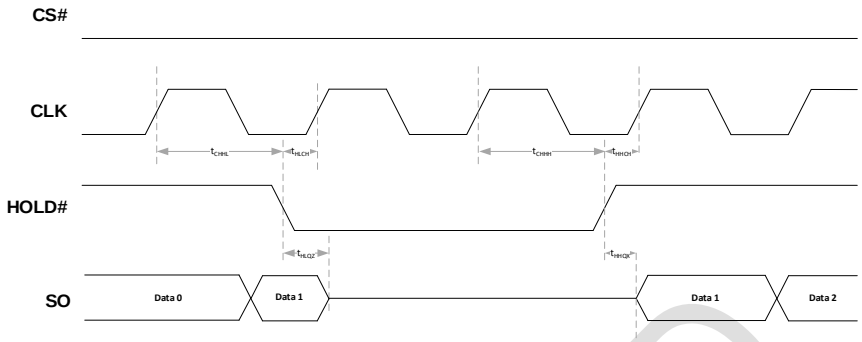


Table 25: HOLD# Operation & Timing

Parameter	Symbol	Minimum	Maximum	Units
HOLD# Active Setup Time (w.r.t CLK)	t_{CHHL}	10	-	ns
HOLD# Active Hold Time (w.r.t CLK)	t_{HLCH}	10	-	ns
HOLD# Inactive Setup Time (w.r.t CLK)	t_{CHHH}	10	-	ns
HOLD# Inactive Hold Time (w.r.t CLK)	t_{HHCH}	10	-	ns
HOLD# to Output Low-Z (Active)	t_{HHQX}	-	20	ns
HOLD# to Output High-Z	t_{HLQZ}	-	20	ns

Notes:
Power supplies must be stable

Revision History

Revision	Date	Change Summary
REV A	03/12/2019	Initial release
REV B	03/14/2019	Package Drawings Updated Added 1.8V support
REV C	05/01/2019	Updated 8-pad WSON drawing
REV D	06/03/2019	Updated 8-pin SOIC drawing Updated address range for Augmented Storage Array Updated figures 8-11 (extra clock cycles representation only) Added 10Mhz ordering options – 10Mhz part numbers Removed JEDEC Reset
REV E	06/24/3019	Added 1MHz and 5MHz ordering options Removed 20MHz ordering option Removed Cost per Bit Analysis Updated Instruction Set Table – Table 15