

ALLWINNER[®]

High-performance quad-core 64-bit intelligent cockpit processor T5 Series

Overview

T5 series (T507/T517) is a high-performance quad-core Cortex - A53 platform SoC for the new generation of automotive markets. T5 series is qualified to Automotive AEC-Q100 testing. The chip family integrates Cortex-A53 quad-core CPU, G31 MP2 GPU, 32-bit DDR3/LPDDR3/DDR4/LPDDR4 DRAM, multi video output interfaces (RGB/2*LVDS/ HDMI/CVBS OUT), and multi video input interfaces(MIPI CSI/BT656/BT1120). The chip family supports 4K@60fps H.265 decoder, 4K@25fps H.264 encoder, DI, 3D noise reduction, SmartColor system, and keystone correction module, which provides smooth user experience and professional visual effect. T5 series can be used in IVI, digital cluster, HD AVM, HUD and other intelligent cockpit products.

Highlights

- Automotive grade: AEC-Q100 certified.
- High performance: T5 series integrates 1.5GHz 4*A53 CPU, G31 MP2 GPU, and 4GB DDR3/DDR4/LPDDR3/LPDDR4 at maximum frequency of 800MHz, which provides smooth user experience and professional visual effect.
- Video multimedia: Supports full format video playback, 4K@60fps H.265 video decoder, and 4K@25fps H.264 video encoder.
- Video output: Supports multi video output interfaces such as RGB888, dual link LVDS, HDMI, CVBS OUT, to achieve different display in dual screen.
- Video input: Integrated MIPI CSI and parallel CSI can support maximum 8-ch HD camera inputs (maximum processing 6-ch of data at the same time) to achieve 360° AVM, DVR functions.
- Rich interfaces: Supports 4xUSB, 2xEthernet MAC, 6xUART, 6xTWI, 4xGPADC, greatly facilitating product expansion.

Features

CPU	• Quad-core ARM Cortex [™] - A53@1.5GHz
GPU	 G31 MP2 Supports OpenGL ES 3.2/2.0/1.0, Vulkan 1.1, OpenCL 2.0

Memory	 32-bit DDR4/DDR3/DDR3L/LPDDR3/LPDDR4 interface, supporting maximum capacity of 4GB SD3.0/eMMC5.0 interface 8-bit Nand flash interface with maximum 80-bit/1KB ECC
Video Engine	 Video decoder H.265 MP decoder up to 4K@60fps H.264 BL/MP/HP decoder up to 4K@30fps VP9 decoder up to 4K@60fps AVS2 decoder up to 4K@60fps Multi-format 1080p@60fps video playback, including VP8, MPEG1/2 SP/MP, MPEG4 SP/ASP, AVS+/AVS JIZHUN, VC1 SP/MP Video encoder H.264 encoder up to 4K@25fps MJPEG encoder up to 4K@15fps JPEG encoder up to 8K x 8K resolution
Video Input	 Supports one 8-/10-/12-/16-bit digital camera(DC) interface Maximum pixel clock of 148.5MHz for each DC interface BT656, BT1120 video input for multichannel YUV Four-lane MIPI CSI, up to 1Gbps per lane in HS transmission, compliant with MIPI-CSI2 V1.00 and MIPI DPHY V1.00 Maximum video capture resolution of 8M@30fps or 4x 1080p@25fps for MIPI CSI Supports formats: YUV422, YUV420, RAW-8, RAW-10, RAW-12
Audio	 Two DAC channels Supports 1 audio output interface (differential LINEOUTP/N or single-end LINEOUTL/LINEOUTR) One Audio HUB, supporting internal mixing function Embedded 3 I2S/PCM for connecting the external devices (I2S0 for extended audio codec, I2S2 for BT, I2S3 for digital power amplifier) Supports Left-justified, Right-justified, Standard I2S mode, PCM mode, and TDM mode I2S mode supports 8 channels, and 32-bit/192kbit sample rate I2S and TDM modes support maximum 16 channels, and 32-bit/96kbit sample rate One OWA OUT interface, supporting 16-/20-/24-bit outputs Integrated digital microphone, supporting maximum 8 digital PDM microphones
Display Output	 HDMI 2.0a up to 4K@60fps (only forT50 7) TV CVBS output, supporting PAL/NTSC LVDS interface with dual link, up to 1080p@60fps RGB interface with DE/SYNC mode, up to 1080p@60fps
Security Engine	 Supports Full Disk Encryption AES, DES, 3DES, and XTS encryption and decryption algorithms MD5, SHA, and HMAC tamper proofing RSA, ECC signature and verification algorithms Supports 160-bit hardware pseudo random number generator(PRNG) with 175-bit seed Supports 256-bit hardware true random number generator(TRNG) Integrated 2K-bit EFUSE for chip ID and security application

Connectivity	 3 x USB2.0 Host, 1 x USB2.0 OTG 2 x Ethernet MAC (one 10/100 Mbps Ethernet port with RMII interface, one 10/100/1000 Mbps Ethernet port with RGMII and RMII interfaces) SDIO 3.0, TSC, SCR, CIR Receiver 6 x TWI, 2 x SPI, 6 x UART 6-ch PWM, 4-ch GPADC, 1-ch LRADC
PMIC	Companion Allwinner Power Management IC
Package	 TFBGA 421balls 15 mm x 15 mm size,0.65 mm ball pitch,0.35 mm ball size
Process	• 28nm HPC

Block Diagram



Note: Only T507 supports HDMI

Application Diagram



Note: Only T507 supports HDMI

Product Diagram

IVI + HD 360°



IVI + SD 360° + DVR



HD AVM Box



Digital Cluster



ABOUT ALLWINNER

Allwinner Technology is a leading fabless design company dedicated to smart application processor SoCs and smart analog ICs. Its product line includes multi-core application processors for smart devices and smart power management ICs used by brands worldwide.

With its focus on cutting edge UHD video processing, high performance multi-core CPU/GPU integration, and ultra-low power consumption, Allwinner Technology is a mainstream solution provider for the global tablet, internet TV, smart home device, automotive in-dash device, smart power management, and mobile connected device markets. Allwinner Technology is headquartered in Zhuhai, China.

CONTACT US

For more product info, please contact service@allwinnertech.com, or scan the QR code to follow us on Wechat.

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