Rockchip RK3399Pro Datasheet

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Revision History

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Chapter 1 Introduction

1.1 Overview

RK3399Pro is a low power, high performance processor for computing, personal mobile internet devices and other smart device applications. Based on Big.Little architecture, it integrates dual-core Cortex-A72 and quad-core Cortex-A53 with separate NEON coprocessor. Equipped with one powerful neural network process unit(NPU), it supports mainstream platforms in the market, such as caffe, tensor flow, and so on.
Many embedded powerful hardware engines provide optimized performance for high-end application. RK3399Pro supports multi-format video decoders and encoders.
Embedded 3D GPU makes RK3399Pro completely compatible with OpenGL ES1.1/2.0/3.0/3.1, OpenCL and DirectX 11.1. Special 2D hardware engine with MMU will maximize display performance and provide very smooth operation.

1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

1.2.1 Microprocessor

- Dual-core ARM Cortex-A72 MPCore processor and Quad-core ARM Cortex-A53 MPCore processor, both are high-performance, low-power and cached application processors
- Two CPU clusters. Big cluster with dual-coreCortex-A72 is optimized for high-performance and little cluster with quad-core Cortex-A53 is optimized for low power.
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerating media and signal processing
- ARMv8 Cryptography Extensions
- CCI500 ensures the memory coherency between the two clusters
- Each Cortex-A72 integrates 48KB L1 instruction cache and 32KB L1 data cache with 4-way set associative. Each Cortex A53 integrates 32KB L1 instruction cache and 32kB L1 data cache separately with 4-way set associative
- 1MB unified L2 Cache for Big cluster, 512KB unified L2 Cache for Little cluster
- TrustZone technology support
- Full CoreSight debug solution
  - Debug and trace visibility of whole systems
  - ETM trace support
  - Invasive and non-invasive debug
- Eight separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A72_B0: 1st Cortex-A72 + Neon + FPU + L1 I/D cache of big cluster
  - PD_A72_B1: 2nd Cortex-A72+ Neon + FPU + L1 I/D cache of big cluster
  - PD_SCU_B: SCU + L2 Cache controller, and including PD_A72_B0, PD_A72_B1, debug logic of big cluster
  - PD_A53_L0: 1st Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L1: 2nd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_A53_L3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache of little cluster
  - PD_SCU_L: SCU + L2 Cache controller, and including PD_A53_L0, PD_A53_L1, PD_A53_L2, PD_A53_L3, debug logic of little cluster
- Two isolated voltage domain to support DVFS for big cluster and little cluster separately.

1.2.2 Neural Process Unit

- Support 1920 Int8 MAC operations per cycle
- Support 64 FP16 MAC operations per cycle

- Support 192 Int16 MAC operations per cycle
- 512KB internal buffer
- One isolated voltage domain to support DVFS

1.2.3 Boot

- Support system boot from the following device :
  - SPI interface
  - eMMC interface
  - SD/MMC interface
- Support system code download by the following interface:
  - USB OTG interface

1.2.4 Internal Memory

- Internal BootROM
  - Size : 32KB
- Internal SRAM
  - Size : 200KB
  - Support security and non-security access
  - Security or non-security space is software programmable
  - Security space can be 0KB,4KB,8KB,12KB,16KB,… up to 64KB by 4KB step

1.2.5 External Memory or Storage device

- NPU Dedicated Dynamic Memory Interface (DDR3/DDR3L/LPDDR2/LPDDR3)
  - Compatible with JEDEC standards
  - Compatible with DDR3-1600/DDR3L-1600/ LPDDR2-1066 /LPDDR3-1600
    - Support 32-bit data width, 2 ranks (chip selects), max 2GB addressing space per rank, total addressing space is 2GB(max)
- Dual-Channel Dynamic Memory Interface (DDR3/DDR3L/LPDDR3/LPDDR4) ①
  - Compatible with JEDEC standard DDR3-1866 /DDR3L-1866 /LPDDR3-1866 / LPDDR4 SDRAM
  - Support 2 channels, each channel is 16 or 32bits data width
  - Support up to 2 ranks (chip selects) for each channel; totally 4GB(max) address space. Maximum address space of one rank in a channel is also 4GB, which is software-configurable
- eMMC Interface
  - Fully compliant with JEDEC eMMC 5.1and eMMC 5.0 specification
  - There is only one eMMC interface
  - It is backward compliant with eMMC 4.51 and earlier versions specification.
  - Supports HS400, HS200, DDR50 and legacy operating modes.
- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - There are 2 MMC interfaces which can be configured as SD/MMC or SDIO
  - Data bus width is 4bits

1.2.6 System Component

- Cortex-M0
  - Two Cortex-M0 inside RK3399Pro to cooperate with Cortex-A72/Cortex-A53
  - Fast code execution permits slower processor clock or increases sleep mode time
  - Deterministic, high-performance interrupt handling for time-critical applications
- CRU (clock & reset unit)
  - Support clock gating control for individual components inside RK3399Pro
  - One oscillator with 24MHz clock input and 8 embedded PLLs
  - Support global soft-reset control for whole SOC, also individual soft-reset for every components
- PMU (power management unit)
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control

- Lots of wakeup sources in different mode
- 6 separate voltage domains
- 30 separate power domains, which can be power up/down by software based on different application scenes

- Timer
  - 14 on-chip 64-bit Timers in SoC with interrupt-based operation for non-secure application
  - 12 on-chip 64-bit Timers in SoC with interrupt-based operation for secure application
  - Provide two operation modes: free-running and user-defined count
  - Support timer work state checkable
  - Fixed 24MHz clock input
- PWM
  - Four on-chip PWMs with interrupt-based operation
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
- Watchdog
  - Three Watchdogs in SoC with 32-bit counter width
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period
- Mailbox
  - Two Mailboxes in SoC to service multi-core communication
  - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
  - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- Bus Architecture
  - 128-bit/64-bit/32-bit multi-layer AXI/AHB/APB composite bus architecture
  - CCI500 embedded to support two clusters cache coherency
- Interrupt Controller
  - Support 8 PPI interrupt source and 148 SPI interrupt sources input from different components inside RK3399Pro
  - Support 16 software-triggered interrupts
  - Input interrupt level is fixed, high-level sensitive for SPI and low-level sensitive for PPI
  - Support Locality-specific Peripheral Interrupts (LPIs). These interrupts are generated by a peripheral writing to a memory-mapped register in the controller
  - Two AXI stream interrupt interfaces separately for each cluster
  - Support different interrupt priority for each interrupt source, and they are always software-programmable
- DMAC
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
  - Signals the occurrence of various DMA events using the interrupt output signals
  - Mapping relationship between each channel and different interrupt outputs is software-programmable
  - Two embedded DMA controller, BUS_DMAC is for bus system, PERI_DMAC is for peripheral system
  - DMAC0 features:
    - 6 channels totally
    - 10 hardware request from peripherals
    - 2 interrupt output

- Support TrustZone technology and programmable secure state for each DMA channel
- DMAC1 features:
  - 8 channels totally
  - 20 hardware request from peripherals
  - 2 interrupt output
  - Support TrustZone technology and programmable secure state for each DMA channel

- Security system
  - Support TrustZone technology for the following components inside RK3399Pro
    - Cortex-A72, support security and non-security mode, switch by software
    - Cortex-A53, support security and non-security mode, switch by software
    - Except Cortex-A72 and Cortex-A53, the other masters in the SoC can also support security and non-security mode by software-programmable
    - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
    - Internal memory, part of space is addressed only in security mode, detailed size is software-programmable together with TZMA (TrustZone memory adapter)
    - External DDR space can be divided into eight parts; each part can be software-programmable to be addressed in security mode or non-security mode
  - Embedded dual-channel encryption and decryption engine
    - Support AES 128/192/256-bit key mode, ECB/CBC/CTR/XTS chain mode, Slave/FIFO mode
    - Support DES/3DES (ECB and CBC chain mode), 3DES (EDE/EEE key mode), Slave/FIFO mode
    - Support SHA1/SHA256/MD5(with hardware padding) HASH function, FIFO mode only
    - Support 160-bit Pseudo Random Number Generator (PRNG)
    - Support 256-bit True Random Number Generator (TRNG)
    - Support PKA 512/1024/2048-bit Exp Modulator
  - Support security boot
  - Support security debug

1.2.7 Video CODEC

- Video Decoder
  - H.264/AVC, Base/Main/High/High10 profile @ level 5.1; up to 4Kx2K @ 30fps
  - H.265/HEVC, Main/Main10 profile @ level 5.1 High-tier; up to 4Kx2K @ 60fps
  - VP9, profile 0, up to 4Kx2K @ 60fps
  - MPEG-1, ISO/IEC 11172-2, up to 1080P @ 60fps
  - MPEG-2, ISO/IEC 13818-2, SP@ML, MP@HL, up to 1080P @ 60fps
  - MPEG-4, ISO/IEC 14496-2, SP@L0-3, ASP@L0-5, up to 1080P @ 60fps
  - VC-1, SP@ML, MP@HL, AP@L0-3, up to 1080P @ 60fps
  - MVC is supported based on H.264 or H.265, up to 1080P @ 60fps
  - Output data format YUV420 semi-planar, YUV400(monochrome), YUV422 is supported by H.264
  - For MPEG-4, GMC (global motion compensation) not supported
  - For VC-1, up-scaling and range mapping are supported in image post-processor
- Video Encoder
  - Support video encoder for H.264 UP to HP@level4.1, MVC and VP8
  - Only support I and P slices, not B slices
  - Input data format:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444

- RGB555 and BGR555
- RGB565 and BGR565
- RGB888 and BRG888
- RGB101010 and BRG101010

- Image size is from 96x96 to 1920x1080(Full HD)
- Maximum frame rate is up to 1920x1080@30FPS[②]

1.2.8 JPEG CODEC

- JPEG Decoder
  - Input JPEG file: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 sampling formats
  - Output raw image: YCbCr 4:0:0, 4:2:0, 4:2:2, 4:4:0, 4:1:1 and 4:4:4 semi-planar
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI (region of image) decode
  - Maximum data rate[③] is up to 76million pixels per second
  - Embedded memory management unit(MMU)
- JPEG Encoder
  - Input raw image:
    - YCbCr 4:2:0 planar
    - YCbCr 4:2:0 semi-planar
    - YCbYCr 4:2:2
    - CbYCrY 4:2:2 interleaved
    - RGB444 and BGR444
    - RGB555 and BGR555
    - RGB565 and BGR565
    - RGB888 and BRG888
    - RGB101010 and BRG101010
  - Output JPEG file: JFIF file format 1.02 or Non-progressive JPEG
  - Encoder image size up to 8192x8192(64million pixels) from 96x32
  - Maximum data rate[③] up to 90million pixels per second

1.2.9 Image Enhancement-Processor (IEP)

- Image format
  - Input data: XRGB/RGB565/YUV420/YUV422
  - Output data: ARGB/RGB565/YUV420/YUV422
  - Max resolution for dynamic image
    - De-interlace: 1920x1080
    - Sampling noise reduction: 1920x1080
    - Compression noise reduction: 4096x2304
    - Enhancement: 4096x2304
- Enhancement
  - Gamma adjustment with programmable mapping table
  - Hue/Saturation/Brightness/Contrast enhancement
  - Programmable distance table for detail and edge enhancement
- Noise reduction
  - Spatial sampling noise reduction
  - Temporal sampling noise reduction
- De-interlace
  - Input 4 fields, output 2 frames mode
  - Input 4 fields, output 1 frames mode
  - Input 2 fields, output 1 frames mode

1.2.10 Graphics Engine

- 3D Graphics Engine:
  - ARM Mali-T860MP4 GPU, support OpenGL ES1.1/2.0/3.0, OpenCL1.2, DirectX11.1 etc.
  - Embedded 4 shader cores with shared hierarchical tiler

- Provide MMU and L2 Cache with 256KB size
- 2D Graphics Engine:
  - Data format
    - Support input of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Support input of YUV422SP(10-bit)/YUV420SP(10-bit)
    - Support output of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Support output of YVYU422/420
    - Max resolution: 8192x8192 source, 4096x4096 destination
  - Scaling
    - Support scaling up and down
    - Arbitrary non-integer scaling ratio，from 1/16 to 16
  - Rotation
    - 0, 90, 180, 270 degree rotation
    - x-mirror, y-mirror& rotation operation
  - BitBLT
  - Alpha Blending

1.2.11 Video IN/OUT

- Camera Interface
  - One or two MIPI-CSI input interface
- Image Signal Processer
  - Input interface
    - DVP interface
      - ITU-R BT601/656 with raw8/raw10/raw12
    - MIPI interface
      - Support x1/x2/x4 DPHY RX data lanes
      - Support RAW8, RAW10, RAW12
    - Maximum input resolution is 4416x3312
  - ISP process
    - Support Black level compensation
    - Support 4 channels of Lens shade correction
    - Support AF/AWB/AE/Hist
  - Output interface
    - Support output format :
      - YUV422sp/YUV420sp, with UV swap
      - RGB888/RGB666/RGB565
      - RAW8/RAW12
  - Display Interface
    - Embedded two VOP, output from the following display interface.
      - Two MIPI-DSI port, and one of which can be configured with MIPI-CSI2
      - One eDP port
      - One DP port
      - One HDMI port
    - Support AFBC function co-operation with GPU
- Video Output Processor(VOP_BIG)
  - Display interface
    - HDMI interface
      - Support 480p/480i/576p/576i/720p/1080p/1080i/4k
      - Support RGB/YUV420(up to 10-bit) format
    - DP interface
      - Support progressive/interlace
      - Support RGB/YUV420/YUV422/YUV444(up to 10-bit) format
    - MIPI interface
      - MIPI DCS command mode
      - Dual-MIPI
    - EDP interface
    - Max resolution

        - Max input resolution：4096x2304
        - Max output resolution：4096x2160
      - Scanning timing 8192x4096
      - Support configurable polarity of DCLK/HSYNC/VSYNC/DEN
  - Display process
    - GAMMA
    - X-MIRROR, Y-MIRROR
    - Post scale down for TV over scan
  - Layer process
    - Background layer
      - programmable 30-bit color
    - Afbcd
      - format: ARGB8888/RGB888/RGB565
      - win_sel(win0/win1/win2/win3)
    - Win0/Win1 layer
      - Support data format
        - RGB888, ARGB888, RGB565,
        - YCbCr420SP, YCbCr422SP, CbCr444SP, YUYV420, YUYV422, YVYU420, YVYU422
        - RGB(8-bit), YUV(8-bit/10-bit), YVYU/YUYV(8-bit)
      - Support 1/8 to 8 scaling-down and scaling-up engine
    - Win2/Win3 layer
      - Support data format
        - RGB888, ARGB888, RGB565
        - 8BPP
      - 4 display regions
        - only one region at one scanning line
    - Hardware Cursor layer
      - Support data format
        - RGB888, ARGB888, RGB565
        - 8BPP
    - Overlay
      - support RGB and YUV domain overlay
      - Support 6 layers, background/win0/win1/win2/win3/hwc
      - Alpha blending
  - Write back
    - Support format
      - RGB565(8-bit), RGB888P(8-bit)
      - YUV420(8-bit)
    - Support scale
      - horizontal scale down, 0.25~1.0
      - vertical throw odd/even line
- Video Output Processor(VOP_LIT)
  - Display interface
    - HDMI interface
      - Support 480p/480i/576p/576i/720p/1080p/1080i
      - Support RGB format
    - DP interface
      - Support progressive/interlace
      - Support RGB/YUV420/YUV422/YUV444format
    - MIPI interface
      - MIPI DCS command mode
      - Dual-MIPI
    - EDP interface
    - Max resolution
      - Max input resolution：4096x2304
      - Max output resolution：2560x1600

- Scanning timing 8192x4096
- Support configurable polarity of DCLK/HSYNC/VSYNC/DEN

- Display process
  - GAMMA
  - X-MIRROR, Y-MIRROR
  - Post scale down for TV overscan
- Layer process
  - Background layer
    - Programmable 30-bit color
  - Win0 layer
    - Support data format
      - RGB888, ARGB888, RGB565,
      - YCbCr420SP, YCbCr422SP, CbCr444SP, YUYV420, YUYV422, YVYU420, YVYU422
      - RGB(8-bit), YUV(8-bit), YVYU/YUYV(8-bit)
    - Support 1/8 to 8 scaling-down and scaling-up engine
  - Win2 layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
    - 4 display regions
      - only one region at one scanning line
  - Hardware Cursor layer
    - Support data format
      - RGB888, ARGB888, RGB565
      - 8BPP
    - Support four hwc size: 32x32,64x64,96x96,128x128
  - Overlay
    - support RGB and YUV domain overlay
    - Support 4 layers, background/win0/win2/hwc
    - Alpha blending

1.2.12 HDMI

- Single Physical Layer PHY with support for HDMI 1.4 and 2.0 operation
- Support HDCP 1.4/2.2

1.2.13 MIPI PHY

- Embedded 3 MIPI PHY, MIPI0 only for DSI, MIPI1 for DSI or CSI, MIPI2 only for CSI
- Lane operation ranging from 80 Mbps to 1.5 Gbps in forward direction
- Each port has 4 data lane, providing up to 6.0 Gbps data rate

1.2.14 eDP PHY

- Compliant with eDP™ Specification, version 1.3
- Up to 4 physical lanes of 2.7/1.62 Gbps/lane
- Hot plug and unplug detection and link status monitor
- Support Panel Self Refresh(PSR)

1.2.15 DisplayPort

- Compliant with DisplayPort Specification, version 1.2
- Compliant with HDCP2.2 (and compatible with HDCP1.3)
- There is only one DisplayPort controller built-in RK3399Pro which is shared by Type-C interface
- Supports up to 4kx2k @60fps resolution
- Variety of audio formats–PCM and compressed, over I2S or SPDIF interfaces
- 1Mbps AUX channel

1.2.16 TYPE-C Interface

- Embedded 1 Type-C PHY
- Compliant with USB Type-C Specification, revision 1.1
- Compliant with USB Power Delivery Specification, revision 2.0
- Attach/detach detection and signaling as DFP, UFP and DRP
- Plug orientation/cable twist detection
- Enable/disable VBUS as DFP and DRP (when operating as DFP)
- VBUS detection as UFP and DRP (when operating as UFP)
- USB Power Delivery communication across the CC wire
- Support USB3.0 Type-C and DisplayPort 1.2 Alt Mode on USB Type-C. Two PMA TX-only lanes and two PMA half-duplex TX/RX lanes (can be configured as TX-only or RX-only)
- Up to 5Gbps data rate for USB3.0
- Up to 5.4Gbps(HBR2) data rate for DP1.2, can support 1/2/4lane mode
- Support DisplayPort AUX channel

1.2.17 Audio Interface

- I2S/PCM
  - Three I2S/PCM in SoC
  - I2S0/I2S2 support up to 8 channels TX and 8 channels RX. I2S1 supports up to 2 channels TX and 2 channels RX
  - I2S2 is connected to HDMI and DisplayPort internally. I2S0 and I2S1 are exposed for peripherals.
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - I2S and PCM mode cannot be used at the same time
- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31-bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24-bit audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

1.2.18 Connectivity

- SDIO interface
  - Compatible with SDIO 3.0 protocol
  - 4bits data bus width
  - There are 2 total MMC interfaces which may be configured as SD/MMC or SDIO
- GMAC 10/100/1000M ethernet controller
  - Supports 10/100/1000-Mbps RGMII interfaces and 10/100-Mbps RMII interface
  - Supports both full-duplex and half-duplex operation
    - Supports CSMA/CD Protocol for half-duplex operation
    - Supports packet bursting and frame extension in 1000 Mbps half-duplex operation
    - Supports IEEE 802.3x flow control for full-duplex operation
  - Preamble and start-of-frame data (SFD) insertion in Transmit, and deletion in receive paths
  - Automatic CRC and pad generation controllable on a per-frame basis
  - Options for Automatic Pad/CRC Stripping on receive frames
  - Programmable fame length to support Standard Ethernet frames
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - MDIO Master interface for PHY device configuration and management
  - Support detection of LAN wake-up frames and AMD Magic Packet frames

- SPI Controller
  - 5 on-chip SPI controllers are inside
  - Support serial-master and serial-slave mode, software-configurable
  - DMA-based or interrupt-based operation
- UART Controller
  - 5 on-chip UART controllers inside RK3399Pro
  - DMA-based or interrupt-based operation
  - Support 5bits,6bits,7bits,8bits serial data transmit or receive
  - Standard asynchronous communication bits such as start,stop and parity
  - Support different input clock for UART operation to get up to 4Mbps or other special baud rate
  - Support non-integer clock divides for baud clock generation
  - Support auto flow control mode for UART0 and UART3
- I2C controller
  - 9 on-chip I2C controllers
  - Multi-master I2C operation
  - Support 7bits and 10bits address mode
  - Serial 8bits oriented and bidirectional data transfers can be made
  - Software programmable clock frequency
  - Data on the I2C-bus can be transferred at rates of up to 100KHz in the Standard-mode, up to 400KHz in the Fast-mode or up to 1MHz in Fast-mode Plus.
- GPIO
  - 5 groups of GPIO (GPIO0~GPIO4)
  - All of GPIOs can be used to generate interrupt to CPU
  - GPIO0 and GPIO1 can be used to wakeup system from low-power mode
  - The pull direction (pull-up or pull-down) for all of GPIOs are software-programmable
  - All of GPIOs are always in input direction in default after power-on-reset
  - The drive strength for all of GPIOs is software-programmable
- USB 3.0 DRD
  - Embedded 1 USB 3.0 interfaces
  - Compatible with USB3.0 Specification
    - Universal Serial Bus 3.0 Specification, Revision 1.0
    - Universal Serial Bus Specification, Revision 2.0
    - Extensible Host Controller Interface for Universal Serial Bus (xHCI), Revision 1.1
  - Support Control/Bulk (including stream)/Interrupt/Isochronous Transfer
  - Supports super-speed (5Gbps)
  - Descriptor Caching and Data Pre-fetching
  - USB 3.0 xHCI Host Features
    - Support up to 64 devices
    - Support 1 interrupter
    - Support 1 USB2.0 port and 1 Super-Speed port
    - Concurrent USB3.0/USB2.0 traffic, up to 8.48Gbps bandwidth
    - Support standard or open-source xHCI and class driver
    - Support xHCI Debug Capability
  - USB 3.0 Dual-Role Device (DRD) Features
    - Static Device operation
    - Static Host operation
    - USB3.0/USB2.0 OTG A device and B device basing on ID
    - UFP/DFP and Data Role Swap Defined in USB TypeC Specification
    - Not support USB3.0/USB2.0 OTG session request protocol(SRP), host negotiation protocol(HNP) and Role Swap Protocol(RSP)
- USB 2.0 Host
  - Embedded 2 USB 2.0 Host interfaces
  - Compatible with USB 2.0Host specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Provides 16 host mode channels
  - Support periodic out channel in host mode

- PCIe
  - One PCIe port in RK3399Pro
  - Compatible with PCI Express Base Specification Revision 2.1
  - Dual operation mode: Root Complex(RC)and End Point(EP)
  - Maximum link width is 4, single bi-directional Link interface
  - Support 2.5Gbps serial data transmission rate per lane per direction
  - Support Single Physical PCI Functions in Endpoint Mode
  - Support Legacy Interrupt and MSI and MSI-X interrupt

1.2.19 Others

- Temperature Sensor(TSADC)
  - Embedded 2 channel TSADC in RK3399Pro
  - TSADC clock must be less than 800KHz
  - 10-bit TSADC up to 50Ksps sampling rate
  - -40~125C temperature range and 5℃ temperature resolution
- Successive Approximation Register(SARADC)
  - 6-channel single-ended 10-bit SAR analog-to-digital converter
  - SARADC clock must be less than 13MHz
  - Conversion speed range is up to 1Msps sampling rate
- eFuse
  - Two 1024bits(32x32) high-density electrical Fuse are integrated in RK3399Pro
  - Support standby mode and power down mode
  - Embedded power-switch
  - Embedded four redundancy bits
- Package Type
  - FCBGA1372(body: 27mmx27mm; ball size: 0.35mm)

Notes : *① DDR3/DDR3L/LPDDR3/LPDDR4 could not be used simultaneously*

② Actual maximum frame rate will depend on the clock frequency and system bus performance

③ Actual maximum data rate will depend on the clock frequency and JPEG compression rate

1.3 Block Diagram

The following diagram shows the basic block diagram.

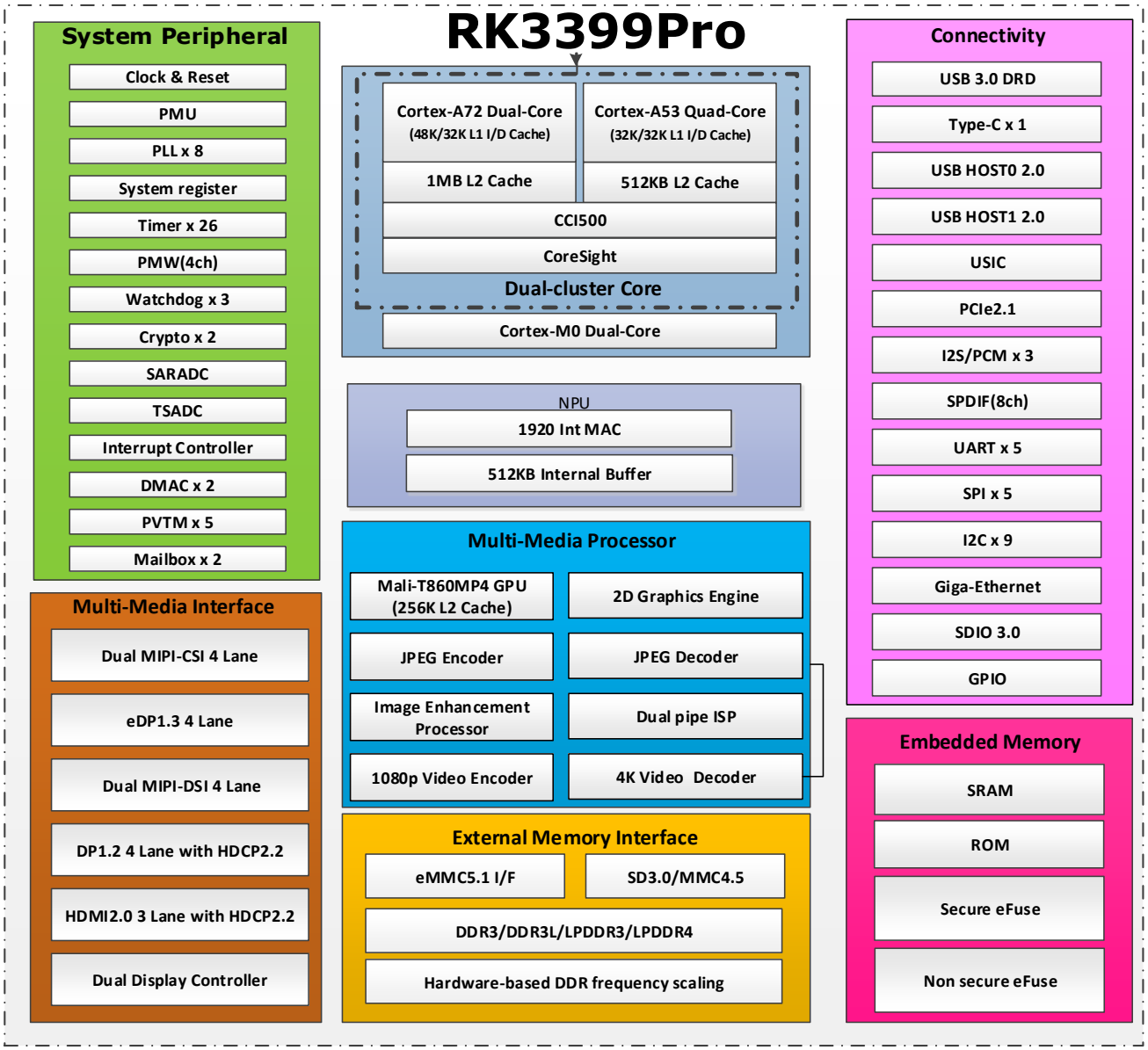


Fig. 1-1 Block Diagram

Notes :
USB3.0 DRD/USB HOST0 2.0 are only for internal use, could not be used by clients

Chapter 2 Package information

2.1 Ordering information

Orderable Device	RoHS status	Package	Package Qty	Device Feature
RK3399Pro	RoHS	FCBGA1372	400	1.8G A72 AP

2.2 Top Marking

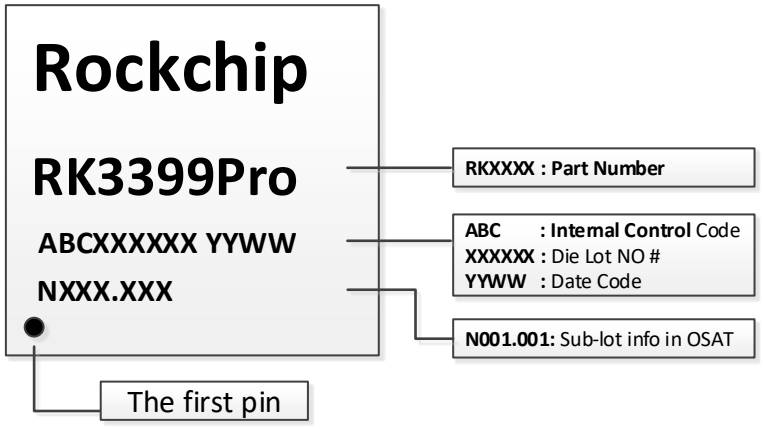


Fig. 2-1 RK3399Pro Top Marking

2.3 Dimension

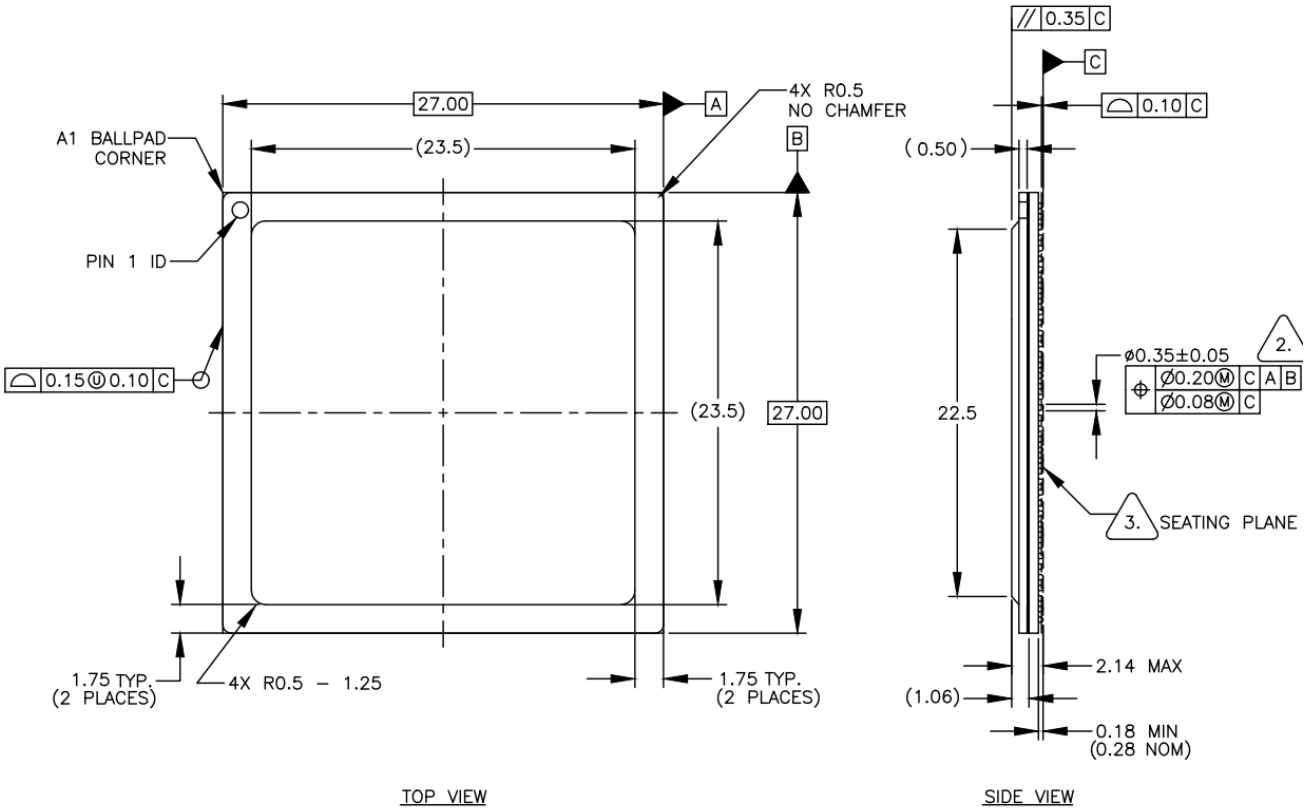


Fig. 2-2 Package Top and SideView

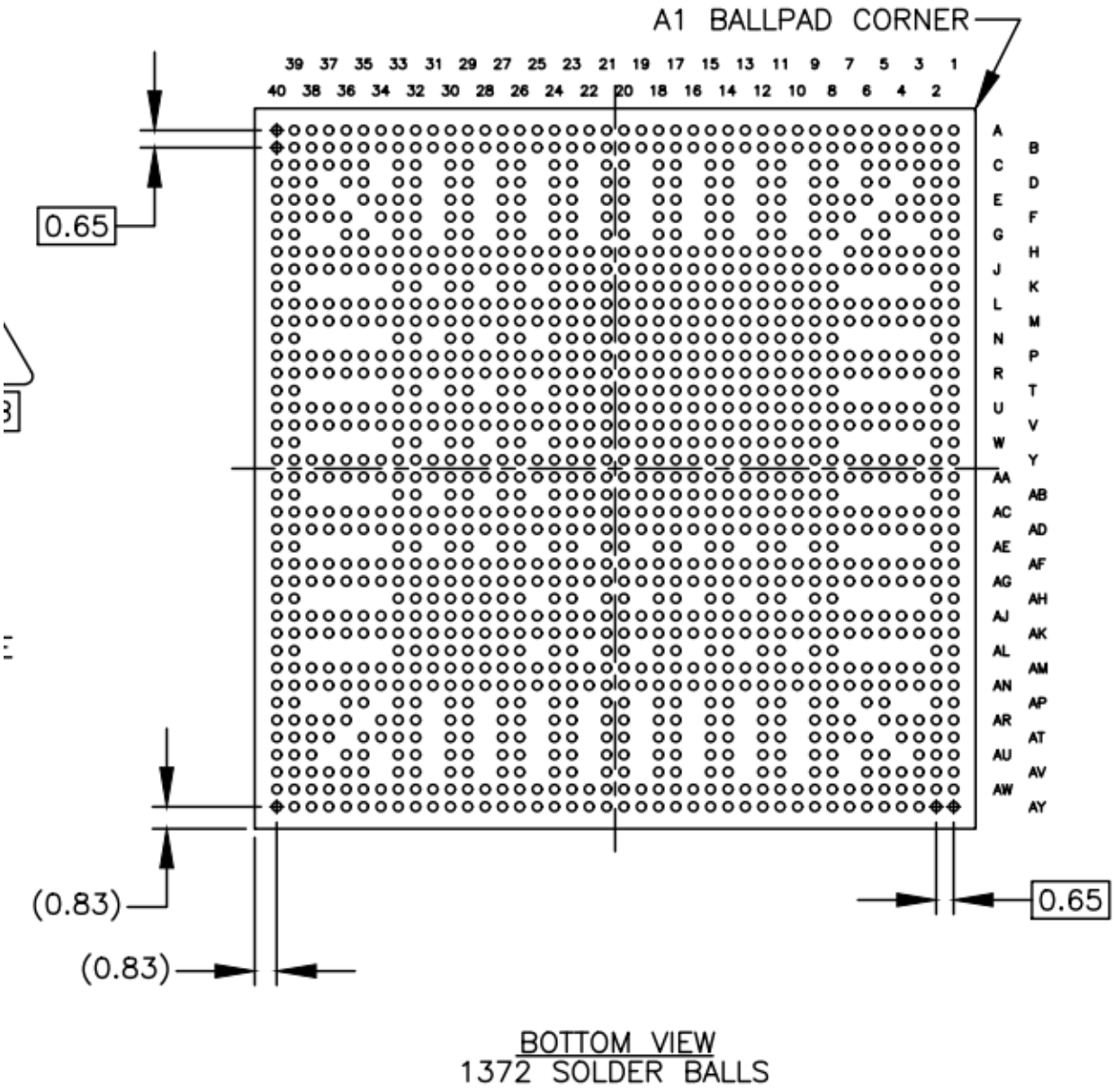
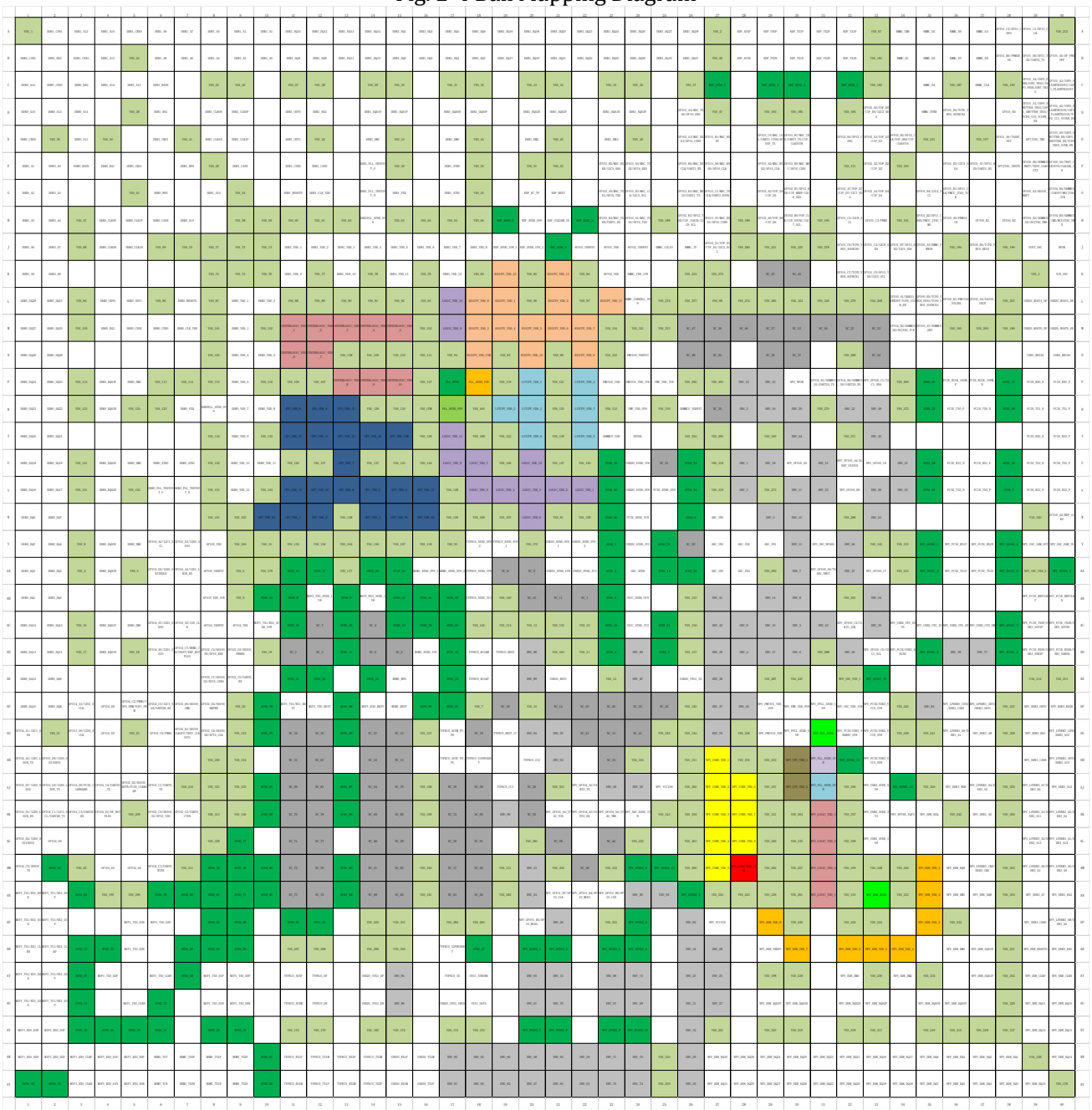


Fig. 2-3 Package Bottom View

2.4 Ball Map

Fig. 2-4 Ball Mapping Diagram



2.5 Ball Pin Number Order

Table 2-1 Ball Pin Number Order Information

Pin#	Pin name	Pin#	Pin name
A1	VSS_1	AY6	HDMI_TCN
A2	DDR1_CSN1	AY7	HDMI_TX0N
A3	DDR1_A12	AY8	HDMI_TX1N
A4	DDR1_A10	AY9	HDMI_TX2N
A5	DDR1_CKE0	AY10	AVSS_62
A6	DDR1_A9	AY11	TYPEC0_RX1M
A7	DDR1_A7	AY12	TYPEC0_TX1P
A8	DDR1_A5	AY13	TYPEC0_RX2M
A9	DDR1_A3	AY14	TYPEC0_TX2P
A10	DDR1_A1	AY15	USB30_RX1M
A11	DDR1_DQ10	AY16	USB30_TX1P
A12	DDR1_DQ12	AY17	DNU_91
A13	DDR1_DQ13	AY18	DNU_95
A14	DDR1_DQ14	AY19	DNU_62
A15	DDR1_DQ1	AY20	DNU_57
A16	DDR1_DQ3	AY21	DNU_64
A17	DDR1_DQ5	AY22	DNU_63
A18	DDR1_DQ6	AY23	DNU_75
A19	DDR1_DQ16	AY24	DNU_74
A20	DDR1_DQ18	AY25	VSS_200
A21	DDR1_DQ20	AY26	DNU_30
A22	DDR1_DQ23	AY27	NPU_DDR_DQ31
A23	DDR1_DQ24	AY28	NPU_DDR_DQ29
A24	DDR1_DQ26	AY29	NPU_DDR_DQ27
A25	DDR1_DQ27	AY30	NPU_DDR_DQ26
A26	DDR1_DQ29	AY31	NPU_DDR_DQ22
A27	VSS_2	AY32	NPU_DDR_DQ20
A28	EDP_AUXP	AY33	NPU_DDR_DQ19
A29	EDP_TX0P	AY34	NPU_DDR_DQ18
A30	EDP_TX1P	AY35	NPU_DDR_DQ7
A31	EDP_TX2P	AY36	NPU_DDR_DQ5
A32	EDP_TX3P	AY37	NPU_DDR_DQ3
A33	VSS_67	AY38	NPU_DDR_DQ0
A34	EMMC_CMD	AY39	NPU_DDR_DQ15
A35	EMMC_D2	AY40	VSS_178
A36	EMMC_D0	B1	DDR0_CSN1
A37	EMMC_D3	B2	DDR1_BA0
A38	GPIO1_C2/SPI3_CSN0	B3	DDR1_CSN3
A39	GPIO1_C1/SPI3_CLK	B4	DDR1_A13
A40	VSS_212	B5	VSS_24

Pin#	Pin name	Pin#	Pin name
AA1	DDR0_DQ3	B6	DDR1_A8
AA2	DDR0_DQ2	B7	DDR1_A6
AA3	VSS_4	B8	DDR1_A4
AA4	DDR0_DQS0N	B9	DDR1_A2
AA5	VSS_5	B10	DDR1_A0
AA6	GPIO3_D5/I2S0_SDI2SDO2	B11	DDR1_DQ8
AA7	GPIO4_A4/I2S1_LRCK_RX	B12	DDR1_DQ9
AA8	APIO5_VDDPST	B13	DDR1_DQ11
AA9	VSS_6	B14	DDR1_DQ15
AA10	VSS_179	B15	DDR1_DQ0
AA11	AVSS_13	B16	DDR1_DQ2
AA12	AVSS_17	B17	DDR1_DQ4
AA13	VSS_177	B18	DDR1_DQ7
AA14	AVSS_26	B19	DDR1_DQ17
AA15	AVSS_53	B20	DDR1_DQ19
AA16	HDMI_AVDD_0V9_1	B21	DDR1_DQ21
AA17	HDMI_AVDD_0V9_2	B22	DDR1_DQ22
AA18	TYPEC0_AVDD_1V8	B23	DDR1_DQ25
AA19	NC_8	B24	DDR1_DQ28
AA20	NC_9	B25	DDR1_DQ30
AA21	USB30_AVDD_1V8	B26	DDR1_DQ31
AA22	USB30_AVDD_3V3	B27	VSS_56
AA23	AVSS_4	B28	EDP_AUXN
AA24	ADC_AVDD	B29	EDP_TX0N
AA25	AVSS_14	B30	EDP_TX1N
AA26	AVSS_40	B31	EDP_TX2N
AA27	ADC_IN5	B32	EDP_TX3N
AA28	ADC_IN4	B33	VSS_181
AA29	VSS_290	B34	EMMC_D1
AA30	DNU_7	B35	EMMC_D5
AA31	NPU_GPIO0_A6/TSADC_SHUT	B36	EMMC_D7
AA32	DNU_47	B37	EMMC_D6
AA33	NPU_GPIO0_C7	B38	GPIO1_B6/PWM3B_IR
AA34	VSS_233	B39	GPIO1_B0/SPI1_TXD/UART4_TX
AA35	NPU_AVSS1_4	B40	GPIO1_A5/AP_PWROFF
AA36	NPU_PCIE_TX1P	C1	DDR0_A12
AA37	NPU_PCIE_TX1N	C2	DDR0_CSN3
AA38	NPU_AVSS1_5	C3	DDR0_BA0
AA39	NPU_OSC_VSS_2	C4	DDR1_A14
AA40	NPU_AVSS1_3	C5	DDR1_A11
AB1	DDR0_DQ1	C6	DDR1_RASN
AB2	DDR0_DQ0	C8	VSS_25
AB8	APIO3_VDD_1V8	C9	VSS_26

Pin#	Pin name	Pin#	Pin name
AB9	VSS_9	C11	VSS_27
AB10	AVSS_12	C12	VSS_28
AB11	AVSS_8	C14	VSS_29
AB12	MIPI_TX0_AVDD_1V8	C15	VSS_30
AB13	AVSS_9	C17	VSS_31
AB14	MIPI_RX0_AVDD_1V8	C18	VSS_32
AB15	AVSS_42	C20	VSS_33
AB16	AVSS_41	C21	VSS_34
AB17	AVSS_52	C23	VSS_35
AB18	TYPEC0_AVDD_3V3	C24	VSS_36
AB19	VSS_140	C26	VSS_37
AB20	NC_10	C27	EDP_AVSS_7
AB21	NC_11	C29	EDP_AVSS_3
AB22	NC_1	C30	EDP_AVSS_4
AB23	AVSS_5	C32	EDP_AVSS_1
AB24	USIC_AVDD_0V9	C33	VSS_182
AB26	VSS_315	C35	EMMC_D4
AB27	DNU_41	C36	VSS_187
AB29	DNU_14	C37	EMMC_CLK
AB30	DNU_8	C38	VSS_192
AB32	VSS_291	C39	GPIO1_A4/ISP0_PRELIGHT_TRIG/ISP1_PRELIGHT_TRIG
AB33	DNU_54	C40	GPIO1_A3/ISP0_FLASHTRIGOUT/ISP1_FLASHTRIGOUT
AB39	NPU_PCIE_REFCLKP	D1	DDR0_A10
AB40	NPU_PCIE_REFCLKN	D2	DDR0_A13
AC1	DDR0_DQ14	D3	DDR0_A14
AC2	DDR0_DQ15	D5	VSS_38
AC3	VSS_16	D6	DDR1_BA1
AC4	DDR0_DQS1P	D8	DDR1_CLK0N
AC5	DDR0_DM1	D9	DDR1_CLK0P
AC6	GPIO4_A7/I2S1_SDO0	D11	DDR1_ODT0
AC7	GPIO4_A0/I2S_CLK	D12	DDR1_BA2
AC8	APIO4_VDDPST	D14	DDR1_DQS1N
AC9	APIO4_VDD	D15	DDR1_DQS1P
AC10	MIPI_TX1/RX1_AVDD_1V8	D17	DDR1_DQS0N
AC11	AVSS_44	D18	DDR1_DQS0P
AC12	NC_7	D20	DDR1_DQS2N
AC13	AVSS_45	D21	DDR1_DQS2P
AC14	NC_4	D23	DDR1_DQS3N
AC15	AVSS_10	D24	DDR1_DQS3P
AC16	AVSS_18	D26	GPIO3_A4/MAC_TXD0/SPI0_RXD
AC17	AVSS_43	D27	VSS_47
AC18	VSS_145	D29	VSS_183

Pin#	Pin name	Pin#	Pin name
AC19	VSS_314	D30	VSS_185
AC20	VSS_13	D32	VSS_184
AC21	VSS_132	D33	GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA
AC22	VSS_12	D35	EMMC_STRB
AC23	AVSS_19	D36	GPIO1_D0/TCPD_VBUS_SOURCE2
AC24	USIC_AVDD_1V2	D38	GPIO1_B5
AC25	AVSS_51	D39	GPIO1_A1/ISP0_SHUTTER_TRIG/ISP1_SHUTTER_TRIG/ TCPD_CC0_VCONN_EN
AC26	VSS_316	D40	GPIO1_A2/ISP0_FLASHTRIGIN/ISP1_FLASHTRIGIN/TCP D_CC1_VCONN_EN
AC27	DNU_42	E1	DDR0_CKE0
AC28	DNU_9	E2	VSS_39
AC29	DNU_19	E3	DDR0_A11
AC30	DNU_5	E4	VSS_40
AC31	DNU_43	E6	DDR1_CKE1
AC32	NPU_GPIO0_C2/CLKIO_32K	E7	VSS_41
AC33	DNU_35	E8	DDR1_CLK1N
AC34	NPU_USB2_OTG_VBUS	E9	DDR1_CLK1P
AC35	NPU_USB2_OTG_ID	E11	DDR1_ODT1
AC36	NPU_USB2_OTG_DP	E12	VSS_42
AC37	NPU_USB2_OTG_DM	E14	DDR1_DM1
AC38	NPU_AVSS1_7	E15	VSS_43
AC39	NPU_PCIE_TX0P/USB3_SSTXP	E17	DDR1_DM0
AC40	NPU_PCIE_TX0N/USB3_SSTXN	E18	VSS_44
AD1	DDR0_DQ13	E20	DDR1_DM2
AD10	VSS_19	E21	VSS_45
AD11	NC_2	E23	DDR1_DM3
AD12	NC_3	E24	VSS_46
AD13	AVSS_11	E26	GPIO3_A3/MAC_RXD3/SPI4_CSN0
AD14	NC_5	E27	GPIO3_B1/MAC_RXDV
AD15	NC_6	E29	GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX
AD16	HDMI_AVDD_1V8	E30	GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB
AD17	AVSS_16	E32	GPIO2_B4/SPI2_CSN0
AD18	TYPEC0_RCLKM	E33	GPIO2_A3/VOP_D3/CIF_D3
AD19	TYPEC0_REXT	E34	GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUTA
AD2	DDR0_DQ11	E35	VSS_231
AD3	VSS_17	E37	VSS_197
AD4	DDR0_DQS1N	E38	GPIO1_A6/TSADC_INT
AD5	VSS_18	E39	DFTJTAG_TMS
AD6	GPIO4_A6/I2S1_SDI0	E40	GPIO1_A0/ISP0_SHUTTER_EN/ISP1_SHUTTER_EN/TCPD _VBUS_SINK_EN
AD7	GPIO4_C7/HDMI_CECINOUT/EDP_HOTPL UG	F1	DDR0_A1

Pin#	Pin name	Pin#	Pin name
AD8	GPIO2_C4/SDIO0_D0/SPI5_RXD	F2	DDR0_A0
AD9	GPIO2_D3/SDIO0_PWREN	F3	DDR0_RASN
AD20	DNU_88	F4	DDR0_BA1
AD21	VSS_163	F5	DDR0_CKE1
AD22	VSS_11	F7	DDR1_WEN
AD23	AVSS_2	F8	VSS_48
AD24	DNU_85	F9	DDR1_CASN
AD25	AVSS_3	F11	DDR1_CSN2
AD26	VSS_317	F12	DDR1_CSN0
AD27	DNU_39	F14	DDR1_PLL_TESTOUT_P
AD28	DNU_4	F15	VSS_49
AD29	DNU_17	F17	DDR1_ATB0
AD30	DNU_6	F18	VSS_50
AD31	VSS_288	F20	VSS_51
AD32	DNU_36	F21	VSS_52
AD33	NPU_GPIO0_C0/I2C1_SCL	F23	GPIO3_B2/MAC_RXER/I2C5_SDA
AD34	NPU_PCIE/USB3_RBIAS	F24	GPIO3_A0/MAC_TXD2/SPI4_RXD
AD35	NPU_AVSS1_8	F26	GPIO3_B6/MAC_RXCLK/UART3_RX
AD36	DNU_78	F27	GPIO3_A6/MAC_RXD0/SPI0_CLK
AD37	DNU_77	F29	GPIO3_A2/MAC_RXD2/SPI4_CLK
AD38	NPU_AVSS1_9	F30	GPIO3_B0/MAC_MDC/SPI0_CSN1
AD39	NPU_PCIE_RX0P/USB3_SSRXP	F32	VSS_171
AD40	NPU_PCIE_RX0N/USB3_SSRXN	F33	GPIO2_A2/VOP_D2/CIF_D2
AE1	DDR0_DQ12	F34	VSS_193
AE2	DDR0_DQ9	F36	GPIO1_B3/I2C4_SDA
AE8	GPIO2_C7/SDIO0_D3/SPI5_CSN0	F37	GPIO1_A7/SPI1_RXD/UART4_RX
AE9	GPIO2_C0/UART0_RX	F38	DFTJTAG_TRSTN
AE11	AVSS_21	F39	GPIO0_B0/SDMMC0_WRPT/TEST_CLKOUT2
AE12	AVSS_22	F40	GPIO0_A0/TEST_CLKOUT0/CLK32K_IN
AE14	AVSS_23	G1	DDR0_A2
AE15	HDMI_HPD	G2	DDR0_A3
AE17	AVSS_24	G5	VSS_53
AE18	TYPEC0_RCLKP	G6	DDR0_WEN
AE20	DNU_89	G8	DDR1_A15
AE21	USB30_REXT	G9	VSS_54
AE23	VSS_14	G11	DDR1_RESETN
AE24	DNU_87	G12	DDR1_CLK_VDD
AE26	USB20_OTG1_ID	G14	DDR1_PLL_TESTOUT_N
AE27	DNU_38	G15	DDR1_PZQ
AE29	VSS_287	G17	DDR1_ATB1
AE30	VSS_247	G18	VSS_55
AE32	NPU_OSC_VSS_1	G20	EDP_DC_TP
AE33	NPU_AVSS1_10	G21	EDP_REXT

Pin#	Pin name	Pin#	Pin name
AE39	VSS_214	G23	GPIO3_A5/MAC_TXD1/SPI0_TXD
AE40	VSS_213	G24	GPIO3_B3/MAC_CLK/I2C5_SCL
AF1	DDR0_DQ10	G26	GPIO3_B5/MAC_MDIO/UART1_TX
AF2	DDR0_DQ8	G27	GPIO3_C1/MAC_TXCLK/UART3_RTSN
AF3	GPIO4_A3/I2S1_SCLK	G29	GPIO2_A5/VOP_D5/CIF_D5
AF4	GPIO4_D6	G30	GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA
AF5	GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM	G32	GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA
AF6	GPIO4_C0/I2C3_SDA/UART2B_RX	G33	GPIO2_A4/VOP_D4/CIF_D4
AF7	GPIO2_D0/SDIO0_CMD	G35	GPIO1_B4/I2C4_SCL
AF8	GPIO2_D4/SDIO0_BKPWR	G36	GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK
AF9	VSS_20	G39	GPIO0_A3/SDIO0_WRPT
AF10	AVSS_78	G40	GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK
AF11	MIPI_TX1/RX1_REXT	H1	DDR0_A5
AF12	MIPI_TX0_REXT	H2	DDR0_A4
AF13	AVSS_88	H3	VSS_57
AF14	MIPI_RX0_REXT	H4	DDR0_CLK0P
AF15	HDMI_REXT	H5	DDR0_CLK1P
AF16	AVSS_90	H6	DDR0_CASN
AF17	AVSS_27	H7	DDR0_A15
AF18	VSS_7	H9	VSS_58
AF19	NC_18	H10	VSS_59
AF20	VSS_10	H11	VSS_60
AF21	NC_14	H12	VSS_61
AF22	NC_20	H13	VSS_62
AF23	NC_40	H14	DDR1PLL_AVDD_0V9
AF24	NC_25	H15	VSS_63
AF25	NC_42	H16	VSS_64
AF26	VSS_345	H17	VSS_65
AF27	DNU_37	H18	VSS_66
AF28	DNU_40	H19	EDP_AVSS_5
AF29	NPU_PMUIO1_VDD_1V8	H20	EDP_AVDD_0V9
AF30	NPU_PMU_VDD_0V8	H21	EDP_CLK24M_IN
AF31	NPU_PPLL_AVDD_1V8	H22	EDP_AVSS_2
AF32	NPU_OSC_VDD_1V8	H23	GPIO3_B4/MAC_TXEN/UART1_RX
AF33	NPU_PCIE/USB3_VCCA_1V8	H24	GPIO3_A1/MAC_TXD3/SPI4_TXD
AF34	VSS_240	H25	VSS_188
AF35	DNU_83	H26	GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL
AF36	NPU_LPDDR3_CSN1/DDR3_CSB1	H27	GPIO3_A7/MAC_RXD1/SPI0_CSN0
AF37	NPU_LPDDR3_ODT1/DDR3_ODT1	H28	VSS_189
AF38	VSS_207	H29	GPIO2_A6/VOP_D6/CIF_D6
AF39	NPU_DDR3_ODT0	H30	GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL
AF40	NPU_DDR3_RASB	H31	VSS_190
AG1	GPIO4_A1/I2C1_SDA	H32	GPIO1_C5/I2C8_SCL

Pin#	Pin name	Pin#	Pin name
AG2	VSS_21	H33	GPIO1_C3/PWM2
AG3	GPIO3_D0/I2S0_SCLK	H34	VSS_191
AG4	GPIO4_D2	H35	GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS
AG5	VSS_23	H36	GPIO0_A6/PWM3A_IR
AG6	GPIO4_C6/PWM1	H37	GPIO0_B3
AG7	GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1	H38	GPIO0_B2
AG8	GPIO2_C6/SDIO0_D2/SPI5_CLK	H39	GPIO4_B3/SDMMC0_D3/APJTAG_TMS
AG9	VSS_312	H40	GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS
AG10	AVSS_79	J1	DDR0_A6
AG11	NC_34	J2	DDR0_A7
AG12	NC_30	J3	VSS_68
AG13	AVSS_89	J4	DDR0_CLK0N
AG14	NC_27	J5	DDR0_CLK1N
AG15	NC_12	J6	VSS_69
AG16	VSS_337	J7	VSS_70
AG17	TYPEC0_AUXM_PU_PD	J8	VSS_71
AG18	NC_19	J9	VSS_72
AG19	TYPEC0_REXT_CC	J10	VSS_73
AG20	DNU_94	J11	DDR1_VDD_1
AG21	DNU_97	J12	DDR1_VDD_2
AG22	NC_21	J13	DDR1_VDD_3
AG23	NC_15	J14	DDR1_VDD_4
AG24	NC_41	J15	DDR1_VDD_5
AG25	VSS_255	J16	DDR1_VDD_6
AG26	VSS_344	J17	DDR1_VDD_7
AG27	DNU_79	J18	DDR1_VDD_8
AG28	VSS_259	J19	EDP_AVDD_1V8_1
AG29	NPU_PMUIO2_VDD	J20	EDP_AVDD_1V8_2
AG30	NPU_PPLL_AVDD_0V8	J21	EDP_AVSS_6
AG31	NPU_PLL_AVSS	J22	APIO1_VDDPST
AG32	NPU_PCIE/USB3_VDDREF_0V8	J23	APIO1_VDD
AG33	NPU_PCIE/USB3_VCCD_0V8	J24	APIO2_VDDPST
AG34	VSS_258	J25	EMMC_CALIO
AG35	VSS_241	J26	EMMC_TP
AG36	NPU_LPDDR3_A9/DDR3_A1	J27	GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL
AG37	NPU_DDR3_A8	J28	VSS_280
AG38	VSS_208	J29	VSS_251
AG39	NPU_DDR3_BA1	J30	VSS_325
AG40	NPU_LPDDR3_CSN0/DDR3_A10	J31	VSS_278
AH1	GPIO4_A5/I2S1_LRCK_TX	J32	GPIO1_C6/TCPD_VBUS_SOURCE0
AH2	GPIO3_D6/I2S0_SDI3SDO1	J33	GPIO1_C4/I2C8_SDA
AH8	VSS_256	J34	GPIO1_B7/SPI3_RXD/I2C0_SDA

Pin#	Pin name	Pin#	Pin name
AH9	VSS_334	J35	GPIO0_A5/EMMC_PWRON
AH11	NC_33	J36	VSS_194
AH12	NC_67	J37	GPIO0_B4/TCPD_VBUS_BDIS
AH14	NC_32	J38	VSS_196
AH15	NC_13	J39	XOUT_OSC
AH17	TYPEC0_AUXP_PD_PU	J40	NPOR
AH18	TYPEC0_U3VBUSDET	K1	DDR0_A9
AH20	TYPEC0_CC2	K2	DDR0_A8
AH21	DNU_93	K8	VSS_74
AH23	NC_16	K9	VSS_75
AH24	VSS_304	K10	VSS_76
AH26	VSS_311	K11	DDR1_VDD_9
AH27	NPU_CORE_VDD_1	K12	VSS_77
AH28	VSS_305	K13	DDR1_VDD_10
AH29	VSS_253	K14	VSS_78
AH30	NPU_CPU_VDD_1	K15	DDR1_VDD_11
AH31	NPU_PLL_AVDD_1V8	K16	VSS_79
AH32	NPU_AVSS1_11	K17	DDR1_VDD_12
AH33	NPU_PCIE/USB3_VCCA_0V8	K18	VSS_80
AH39	NPU_DDR3_CASB	K19	BIGCPU_VDD_12
AH40	NPU_LPDDR3_ODT0/DDR3_A15	K20	VSS_82
AJ1	GPIO3_D7/I2S0_SDO0	K21	BIGCPU_VDD_13
AJ2	GPIO3_D2/I2S0_LRCK_TX	K22	VSS_84
AJ3	GPIO4_D0/PCIE_CLKREQNB	K23	APIO2_VDD
AJ4	GPIO4_C4/UART2C_TX	K24	EMMC_VDD_1V8
AJ5	GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN	K26	VSS_224
AJ6	GPIO2_C1/UART0_TX	K27	VSS_275
AJ7	VSS_210	K29	NC_43
AJ8	VSS_327	K30	NC_45
AJ9	VSS_335	K32	GPIO1_C7/TCPD_VBUS_SOURCE1
AJ10	AVSS_91	K33	GPIO1_C0/SPI3_TXD/I2C0_SCL
AJ11	NC_69	K39	VSS_3
AJ12	NC_81	K40	XIN_OSC
AJ13	AVSS_87	L1	DDR0_DQ29
AJ14	NC_64	L2	DDR0_DQ31
AJ15	NC_79	L3	VSS_85
AJ16	VSS_338	L4	DDR0_ODT0
AJ17	NC_39	L5	DDR0_ODT1
AJ18	NC_59	L6	VSS_86
AJ19	TYPEC0_CC1	L7	DDR0_RESETN
AJ20	NC_26	L8	VSS_87
AJ21	VSS_303	L9	DDR0_VDD_1
AJ22	NPU_GPIO4_A2/UART2_TX	L10	DDR0_VDD_2

Pin#	Pin name	Pin#	Pin name
AJ23	DNU_49	L11	VSS_88
AJ24	DNU_50	L12	VSS_89
AJ25	NPU_VCCIO6	L13	VSS_90
AJ26	VSS_265	L14	VSS_91
AJ27	NPU_CORE_VDD_2	L15	VSS_92
AJ28	NPU_CORE_VDD_6	L16	VSS_93
AJ29	VSS_257	L17	LOGIC_VDD_10
AJ30	NPU_CPU_VDD_2	L18	BIGCPU_VDD_8
AJ31	NPU_PLL_AVDD_0V8	L19	BIGCPU_VDD_1
AJ32	VSS_306	L20	VSS_96
AJ33	NPU_USB2_AVDD_0V8	L21	BIGCPU_VDD_2
AJ34	NPU_AVSS1_12	L22	VSS_97
AJ35	VSS_250	L23	BIGCPU_VDD_11
AJ36	NPU_DDR3_WEB	L24	EMMC_COREDLL_0V9
AJ37	NPU_LPDDR3_A4/DDR3_A2	L25	VSS_276
AJ38	VSS_205	L26	VSS_277
AJ39	NPU_LPDDR3_A7/DDR3_A6	L27	VSS_99
AJ40	NPU_DDR3_A12	L28	VSS_274
AK1	GPIO3_D1/I2S0_LRCK_RX	L29	VSS_285
AK2	GPIO4_C1/I2C3_SCL/UART2B_TX	L30	VSS_324
AK3	GPIO4_C3/UART2C_RX	L31	VSS_326
AK4	GPIO4_D1/DP_HOTPLUG	L32	VSS_279
AK5	VSS_209	L33	VSS_268
AK6	GPIO2_C5/SDIO0_D1/SPI5_TXD	L34	GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN
AK7	GPIO2_C2/UART0_CTSN	L35	GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3
AK8	VSS_313	L36	GPIO0_B1/PMUIO2_VOLSEL
AK9	VSS_336	L37	GPIO0_A4/SDIO0_INTN
AK10	AVSS_92	L38	VSS_267
AK11	NC_70	L39	USB20_HOST1_DP
AK12	NC_78	L40	USB20_HOST1_DN
AK13	AVSS_86	M1	DDR0_DQ27
AK14	NC_65	M2	DDR0_DQ30
AK15	NC_80	M3	VSS_100
AK16	VSS_339	M4	DDR0_BA2
AK17	NC_74	M5	DDR0_CSN2
AK18	NC_60	M6	DDR0_CSN0
AK19	DNU_96	M7	DDR0_CLK_VDD
AK20	NC_55	M8	VSS_101
AK21	NPU_GPIO4_A4/JTAG_TCK	M9	DDR0_VDD_3
AK22	NPU_GPIO4_A3/UART2_RX	M10	VSS_102
AK23	NPU_GPIO4_A5/JTAG_TMS	M11	CENTERLOGIC_VDD_1
AK24	NPU_ADC_AVDD_1V8	M12	CENTERLOGIC_VDD_2
AK25	VSS_343	M13	CENTERLOGIC_VDD_3

Pin#	Pin name	Pin#	Pin name
AK26	VSS_254	M14	CENTERLOGIC_VDD_4
AK27	NPU_CORE_VDD_3	M15	CENTERLOGIC_VDD_5
AK28	NPU_CORE_VDD_7	M16	VSS_103
AK29	VSS_331	M17	LOGIC_VDD_9
AK30	VSS_264	M18	BIGCPU_VDD_3
AK31	NPU_LOGIC_VDD_3	M19	BIGCPU_VDD_4
AK32	VSS_307	M20	BIGCPU_VDD_5
AK33	NPU_USB2_AVDD_3V3	M21	BIGCPU_VDD_6
AK34	NPU_EFUSE_VQPS	M22	BIGCPU_VDD_7
AK35	NPU_DDR_RZQ	M23	VSS_104
AK36	VSS_242	M24	VSS_321
AK37	NPU_DDR3_A0	M25	VSS_323
AK38	VSS_206	M26	NC_47
AK39	NPU_LPDDR3_A3/DDR3_A11	M27	NC_49
AK40	NPU_LPDDR3_A5/DDR3_A4	M28	NC_46
AL1	GPIO3_D4/I2S0_SDI1SDO3	M29	NC_57
AL2	GPIO4_D5	M30	NC_53
AL8	VSS_328	M31	NC_54
AL9	AVSS_77	M32	NC_22
AL11	NC_71	M33	NC_23
AL12	NC_77	M34	GPIO4_B2/SDMMC0_D2/APJTAG_TCK
AL14	NC_66	M35	GPIO0_A7/SDMMC0_DET
AL15	NC_28	M36	VSS_195
AL17	NC_29	M37	VSS_266
AL18	NC_61	M38	VSS_186
AL20	VSS_281	M39	USB20_HOST0_DP
AL21	NC_58	M40	USB20_HOST0_DN
AL23	NC_44	N1	DDR0_DQ26
AL24	VSS_222	N2	DDR0_DQ28
AL26	VSS_263	N8	VSS_105
AL27	NPU_CORE_VDD_4	N9	DDR0_VDD_4
AL28	NPU_CORE_VDD_8	N10	DDR0_VDD_5
AL29	VSS_226	N11	CENTERLOGIC_VDD_6
AL30	VSS_330	N12	CENTERLOGIC_VDD_7
AL31	NPU_LOGIC_VDD_2	N13	VSS_108
AL32	VSS_308	N14	VSS_109
AL33	NPU_USB2_AVDD_1V8	N15	VSS_110
AL39	NPU_LPDDR3_A2/DDR3_A13	N16	VSS_111
AL40	NPU_LPDDR3_A1/DDR3_A14	N17	VSS_94
AM1	GPIO4_C5/SPDIF_TX	N18	BIGCPU_VDD_COM
AM2	AVSS_64	N19	VSS_83
AM3	VSS_22	N20	BIGCPU_VDD_10
AM4	GPIO4_D3	N21	VSS_98

Pin#	Pin name	Pin#	Pin name
AM5	GPIO4_D4	N22	BIGCPU_VDD_9
AM6	GPIO2_C3/UART0_RTSN	N23	VSS_322
AM7	VSS_211	N24	PMUIO2_VDDPST
AM8	AVSS_38	N26	NC_48
AM9	AVSS_39	N27	NC_50
AM10	AVSS_80	N29	NC_36
AM11	NC_72	N30	NC_37
AM12	NC_76	N32	VSS_289
AM13	AVSS_85	N33	NC_24
AM14	NC_31	N39	USB1_RBIAS
AM15	NC_82	N40	USB0_RBIAS
AM16	VSS_340	P1	DDR0_DQ24
AM17	NC_17	P2	DDR0_DQ25
AM18	NC_62	P3	VSS_112
AM19	VSS_131	P4	DDR0_DQS3P
AM20	DNU_33	P5	DDR0_DM3
AM21	VSS_302	P6	VSS_113
AM22	NC_38	P7	VSS_114
AM23	VSS_332	P8	VSS_115
AM24	NPU_AVSS1_6	P9	DDR0_VDD_6
AM25	NPU_AVSS1_13	P10	VSS_116
AM26	VSS_260	P11	VSS_106
AM27	NPU_CORE_VDD_5	P12	VSS_107
AM28	NPU_CORE_VDD_COM	P13	CENTERLOGIC_VDD_8
AM29	VSS_262	P14	CENTERLOGIC_VDD_9
AM30	VSS_227	P15	CENTERLOGIC_VDD_10
AM31	NPU_LOGIC_VDD_4	P16	VSS_117
AM32	VSS_309	P17	PLL_AVSS
AM33	VSS_248	P18	PLL_AVDD_1V8
AM34	VSS_246	P19	VSS_119
AM35	NPU_DDR_VDD_1	P20	LITCPU_VDD_1
AM36	NPU_DDR_DQ9	P21	VSS_121
AM37	NPU_LPDDR3_CKE/DDR3_CKE	P22	LITCPU_VDD_4
AM38	VSS_203	P23	PMUIO2_VDD
AM39	NPU_LPDDR3_A6/DDR3_A3	P24	PMUIO1_VDD_1V8
AM40	NPU_LPDDR3_A0/DDR3_A9	P25	PMU_VDD_1V8
AN1	MIPI_TX1/RX1_D0N	P26	VSS_292
AN2	MIPI_TX1/RX1_D0P	P27	VSS_293
AN3	AVSS_63	P28	DNU_15
AN4	VSS_199	P29	DNU_12
AN5	VSS_296	P30	NPU_NPOR
AN6	AVSS_70	P31	GPIO4_B1/SDMMC0_D1/UART2A_TX
AN7	AVSS_66	P32	GPIO4_B0/SDMMC0_D0/UART2A_RX

Pin#	Pin name	Pin#	Pin name
AN8	AVSS_67	P33	NPU_GPIO0_C1/I2C1_SDA
AN9	AVSS_71	P34	VSS_269
AN10	AVSS_81	P35	AVSS_20
AN11	NC_73	P36	PCIE_RCLK_100M_P
AN12	NC_75	P37	PCIE_RCLK_100M_N
AN13	AVSS_84	P38	AVSS_15
AN14	NC_68	P39	PCIE_RX0_N
AN15	NC_83	P40	PCIE_RX0_P
AN16	VSS_341	R1	DDR0_DQ23
AN17	NC_63	R2	DDR0_DQ22
AN18	NC_56	R3	VSS_123
AN19	VSS_282	R4	DDR0_DQS3N
AN20	DNU_24	R5	VSS_124
AN21	NPU_GPIO1_B7/SPI0_CLK	R6	VSS_125
AN22	NPU_GPIO1_B4/SPI0_MOSI	R7	DDR0_PZQ
AN23	NPU_GPIO1_B6/SPI0_CSN	R8	DDR0PLL_AVDD_0V9
AN24	DNU_80	R9	DDR0_VDD_7
AN25	DNU_81	R10	DDR0_VDD_8
AN26	NPU_AVSS2_3	R11	GPU_VDD_8
AN27	VSS_252	R12	GPU_VDD_9
AN28	VSS_243	R13	GPU_VDD_13
AN29	VSS_329	R14	VSS_129
AN30	VSS_261	R15	VSS_130
AN31	NPU_LOGIC_VDD_1	R16	VSS_COM
AN32	VSS_310	R17	PLL_AVDD_0V9
AN33	NPU_DDR_AVSS	R18	VSS_165
AN34	VSS_232	R19	LITCPU_VDD_2
AN35	NPU_DDR_VDD_2	R20	LITCPU_VDD_3
AN36	NPU_DDR_DM1	R21	VSS_120
AN37	NPU_DDR_DQ8	R22	LITCPU_VDD_7
AN38	VSS_204	R23	VSS_133
AN39	NPU_DDR3_A7	R24	PMU_VDD_0V9
AN40	NPU_DDR3_BA2	R25	VSS_150
AP1	MIPI_TX1/RX1_D1N	R26	SDMMC0_VDDPST
AP2	MIPI_TX1/RX1_D1P	R27	NC_35
AP5	MIPI_TX0_D3N	R28	DNU_2
AP6	MIPI_TX0_D3P	R29	DNU_16
AP8	AVSS_65	R30	DNU_20
AP9	AVSS_68	R31	VSS_270
AP11	AVSS_82	R32	DNU_22
AP12	AVSS_83	R33	DNU_48
AP14	VSS_225	R34	VSS_272
AP15	VSS_301	R35	AVSS_25

Pin#	Pin name	Pin#	Pin name
AP17	VSS_284	R36	PCIE_TX0_P
AP18	VSS_283	R37	PCIE_TX0_N
AP20	NPU_GPIO1_B5/SPI0_MISO	R38	AVSS_48
AP21	DNU_26	R39	PCIE_TX1_N
AP23	VSS_223	R40	PCIE_TX1_P
AP24	NPU_AVSS2_4	T1	DDR0_DQ20
AP26	DNU_82	T2	DDR0_DQ21
AP27	NPU_VCCIO5	T8	VSS_134
AP29	NPU_DDR_VDD_8	T9	DDR0_VDD_9
AP30	VSS_249	T10	VSS_135
AP32	VSS_245	T11	GPU_VDD_10
AP33	VSS_244	T12	GPU_VDD_11
AP35	NPU_DDR_VDD_3	T13	GPU_VDD_12
AP36	VSS_234	T14	GPU_VDD_14
AP39	NPU_DDR3_CSB0	T15	GPU_VDD_COM
AP40	NPU_LPDDR3_A8/DDR3_A5	T16	VSS_138
AR1	MIPI_TX1/RX1_CLKN	T17	LOGIC_VDD_11
AR2	MIPI_TX1/RX1_CLKP	T18	VSS_168
AR3	AVSS_33	T19	VSS_122
AR4	AVSS_72	T20	LITCPU_VDD_6
AR5	MIPI_TX0_D2N	T21	VSS_139
AR7	AVSS_59	T22	LITCPU_VDD_5
AR8	AVSS_60	T23	SDMMC0_VDD
AR9	AVSS_69	T24	EFUSE
AR11	VSS_297	T26	VSS_294
AR12	VSS_298	T27	VSS_295
AR14	VSS_299	T29	VSS_160
AR15	VSS_300	T30	DNU_44
AR17	TYPEC0_U2VBUSDET	T32	VSS_271
AR18	AVSS_47	T33	DNU_45
AR20	NPU_AVSS2_1	T39	PCIE_RX2_N
AR21	NPU_AVSS2_2	T40	PCIE_RX2_P
AR23	NPU_AVSS2_5	U1	DDR0_DQ18
AR24	NPU_AVSS2_6	U2	DDR0_DQ19
AR26	DNU_34	U3	VSS_141
AR27	DNU_28	U4	DDR0_DQS2P
AR29	NPU_DDR_VREFO	U5	DDR0_DM2
AR30	NPU_DDR_VDD_7	U6	DDR0_ATB0
AR32	NPU_DDR_VDD_6	U7	DDR0_ATB1
AR33	NPU_DDR_VDD_5	U8	VSS_142
AR34	NPU_DDR_VDD_4	U9	DDR0_VDD_10
AR36	NPU_DDR_DM0	U10	DDR0_VDD_11
AR37	NPU_DDR_DQS1N	U11	VSS_126

Pin#	Pin name	Pin#	Pin name
AR38	VSS_201	U12	VSS_127
AR39	NPU_DDR_RESETN	U13	GPU_VDD_7
AR40	NPU_DDR3_BA0	U14	VSS_137
AT1	MIPI_TX1/RX1_D2N	U15	VSS_143
AT2	MIPI_TX1/RX1_D2P	U16	VSS_144
AT3	AVSS_57	U17	LOGIC_VDD_8
AT4	MIPI_TX0_D2P	U18	LOGIC_VDD_7
AT6	MIPI_TX0_CLKP	U19	VSS_146
AT7	AVSS_58	U20	LOGIC_VDD_12
AT8	MIPI_TX0_D1P	U21	VSS_147
AT9	MIPI_TX0_D0P	U22	VSS_149
AT11	TYPEC0_AUXP	U23	AVSS_49
AT12	TYPEC0_DP	U24	USB20_AVDD_1V8
AT14	USB20_OTG1_DP	U25	NC_51
AT15	DNU_84	U26	AVSS_74
AT17	TYPEC0_ID	U27	VSS_318
AT18	USIC_STROBE	U28	DNU_1
AT20	DNU_65	U29	DNU_18
AT21	DNU_72	U30	NPU_GPIO0_A2
AT23	DNU_68	U31	DNU_51
AT24	DNU_73	U32	NPU_GPIO0_A4/SLEEP_STATUS
AT26	DNU_23	U33	NPU_GPIO0_C6
AT27	DNU_25	U34	DNU_21
AT29	VSS_198	U35	AVSS_28
AT30	VSS_239	U36	PCIE_RX1_N
AT32	NPU_DDR_DM3	U37	PCIE_RX1_P
AT33	VSS_236	U38	AVSS_30
AT34	NPU_DDR_DM2	U39	PCIE_TX3_N
AT35	VSS_235	U40	PCIE_TX3_P
AT37	NPU_DDR_DQS1P	V1	DDR0_DQ16
AT38	VSS_202	V2	DDR0_DQ17
AT39	NPU_DDR_CLKP	V3	VSS_151
AT40	NPU_DDR_CLKN	V4	DDR0_DQS2N
AU1	MIPI_TX1/RX1_D3N	V5	VSS_152
AU2	MIPI_TX1/RX1_D3P	V6	DDR0_PLL_TESTOUT_P
AU3	AVSS_34	V7	DDR0_PLL_TESTOUT_N
AU5	MIPI_TX0_CLKN	V8	VSS_153
AU6	AVSS_73	V9	DDR0_VDD_12
AU8	MIPI_TX0_D1N	V10	VSS_154
AU9	MIPI_TX0_D0N	V11	GPU_VDD_15
AU11	TYPEC0_AUXM	V12	GPU_VDD_16
AU12	TYPEC0_DN	V13	GPU_VDD_6
AU14	USB20_OTG1_DN	V14	GPU_VDD_5

Pin#	Pin name	Pin#	Pin name
AU15	DNU_86	V15	GPU_VDD_4
AU17	USB20_OTG1_VBUS	V16	GPU_VDD_17
AU18	USIC_DATA	V17	VSS_148
AU20	DNU_61	V18	LOGIC_VDD_5
AU21	DNU_76	V19	LOGIC_VDD_4
AU23	DNU_67	V20	LOGIC_VDD_3
AU24	DNU_69	V21	LOGIC_VDD_2
AU26	DNU_31	V22	LOGIC_VDD_1
AU27	DNU_27	V23	AVSS_50
AU29	NPU_DDR_DQS3P	V24	USB20_AVDD_0V9
AU30	NPU_DDR_DQS3N	V25	PCIE_AVDD_0V9
AU32	NPU_DDR_DQS2N	V26	AVSS_75
AU33	NPU_DDR_DQS2P	V27	VSS_319
AU35	NPU_DDR_DQS0N	V28	DNU_3
AU36	NPU_DDR_DQS0P	V29	VSS_273
AU38	VSS_229	V30	DNU_11
AU39	NPU_DDR_DQ11	V31	DNU_52
AU40	NPU_DDR_DQ10	V32	NPU_GPIO0_B0
AV1	MIPI_RX0_D3N	V33	DNU_56
AV2	MIPI_RX0_D3P	V34	DNU_55
AV3	AVSS_35	V35	AVSS_29
AV4	AVSS_56	V36	PCIE_TX2_N
AV5	AVSS_55	V37	PCIE_TX2_P
AV6	AVSS_31	V38	AVSS_7
AV8	AVSS_36	V39	PCIE_RX3_N
AV9	AVSS_37	V40	PCIE_RX3_P
AV11	VSS_175	W1	DDR0_DQ6
AV12	VSS_176	W2	DDR0_DQ7
AV14	VSS_180	W8	VSS_161
AV15	VSS_172	W9	VSS_162
AV17	VSS_173	W10	GPU_VDD_20
AV18	VSS_174	W11	GPU_VDD_1
AV20	NPU_AVSS2_7	W12	GPU_VDD_2
AV21	NPU_AVSS2_8	W13	VSS_128
AV23	NPU_AVSS2_9	W14	GPU_VDD_3
AV24	NPU_AVSS2_10	W15	GPU_VDD_19
AV26	DNU_32	W16	GPU_VDD_18
AV27	VSS_221	W17	VSS_159
AV29	VSS_220	W18	VSS_169
AV30	VSS_219	W19	VSS_167
AV32	VSS_218	W20	LOGIC_VDD_6
AV33	VSS_217	W21	VSS_81
AV35	VSS_216	W22	VSS_158

Pin#	Pin name	Pin#	Pin name
AV36	VSS_215	W23	AVSS_46
AV37	VSS_228	W24	PCIE_AVDD_1V8
AV38	VSS_237	W26	AVSS_6
AV39	NPU_DDR_DQ12	W27	ADC_IN0
AV40	NPU_DDR_DQ13	W29	DNU_0
AW1	MIPI_RX0_D2N	W30	DNU_10
AW2	MIPI_RX0_D2P	W32	VSS_286
AW3	MIPI_RX0_CLKP	W33	DNU_53
AW4	MIPI_RX0_D1P	W39	VSS_320
AW5	MIPI_RX0_D0P	W40	GPIO0_A2/REF_CLKO
AW6	HDMI_TCP	Y1	DDR0_DQ5
AW7	HDMI_TX0P	Y2	DDR0_DQ4
AW8	HDMI_TX1P	Y3	VSS_8
AW9	HDMI_TX2P	Y4	DDR0_DQS0P
AW10	AVSS_61	Y5	DDR0_DM0
AW11	TYPEC0_RX1P	Y6	GPIO4_A2/I2C1_SCL
AW12	TYPEC0_TX1M	Y7	GPIO3_D3/I2S0_SDI0
AW13	TYPEC0_RX2P	Y8	APIO5_VDD
AW14	TYPEC0_TX2M	Y9	VSS_166
AW15	USB30_RX1P	Y10	VSS_15
AW16	USB30_TX1M	Y11	VSS_155
AW17	DNU_90	Y12	VSS_136
AW18	DNU_92	Y13	VSS_164
AW19	DNU_66	Y14	VSS_156
AW20	DNU_58	Y15	VSS_157
AW21	DNU_60	Y16	VSS_118
AW22	DNU_59	Y17	VSS_95
AW23	DNU_71	Y18	TYPEC0_AVDD_0V9_2
AW24	DNU_70	Y19	TYPEC0_AVDD_0V9_1
AW25	VSS_230	Y20	VSS_170
AW26	DNU_29	Y21	USB30_AVDD_0V9_1
AW27	NPU_DDR_DQ30	Y22	USB30_AVDD_0V9_2
AW28	NPU_DDR_DQ28	Y23	AVSS_1
AW29	NPU_DDR_DQ24	Y24	USB20_AVDD_3V3
AW30	NPU_DDR_DQ25	Y25	AVSS_76
AW31	NPU_DDR_DQ23	Y26	NC_52
AW32	NPU_DDR_DQ21	Y27	ADC_IN3
AW33	NPU_DDR_DQ16	Y28	ADC_IN2
AW34	NPU_DDR_DQ17	Y29	ADC_IN1
AW35	NPU_DDR_DQ6	Y30	DNU_13
AW36	NPU_DDR_DQ4	Y31	NPU_OSC_BPASS
AW37	NPU_DDR_DQ2	Y32	DNU_46
AW38	NPU_DDR_DQ1	Y33	VSS_342

Pin#	Pin name	Pin#	Pin name
AW39	VSS_238	Y34	VSS_333
AW40	NPU_DDR_DQ14	Y35	NPU_AVSS1_1
AY1	AVSS_54	Y36	NPU_PCIE_RX1P
AY2	AVSS_32	Y37	NPU_PCIE_RX1N
AY3	MIPI_RX0_CLKN	Y38	NPU_AVSS1_2
AY4	MIPI_RX0_D1N	Y39	NPU_OSC_24M_OUT
AY5	MIPI_RX0_D0N	Y40	NPU_OSC_24M_IN

Notes :
NPU_PICE_XXX are only for internal use, could not be used by clients

2.6 Power/ground IO descriptions

Table 2-2 Power/Ground IO information

Group	Ball #	Descriptions
VSS	A1,A27,K39,AA3,AA5,AA9,AF18,Y3,AB9,AF20,AD22,AC22,AC20,AE23,Y10,AC3,AD3,AD5,AD10,AF9,AG2,AM3,AG5,B5,C8,C9,C11,C12,C14,C15,C17,C18,C20,C21,C23,C24,C26,D5,E2,E4,E7,E12,E15,E18,E21,E24,D27,F8,F15,F18,F20,F21,G5,G9,G18,B27,H3,H9,H10,H11,H12,H13,H15,H16,H17,H18,A33,J3,J6,J7,J8,J9,J10,K8,K9,K10,K12,K14,K16,K18,W21,K20,N19,K22,L3,L6,L8,L11,L12,L13,L14,L15,L16,N17,Y17,L20,L22,N21,L27,M3,M8,M10,M16,M23,N8,P11,P12,N13,N14,N15,N16,P3,P6,P7,P8,P10,P16,Y16,P19,R21,P21,T19,R3,R5,R6,U11,U12,W13,R14,R15,AM19,AC21,R23,T8,T10,Y12,U14,T16,T21,AB19,U3,U8,U15,U16,AC18,U19,U21,V17,U22,R25,V3,V5,V8,V10,Y11,Y14,Y15,W22,W17,T29,W8,W9,AD21,Y13,R18,Y9,W19,T18,W18,Y20,F32,AV15,AV17,AV18,AV11,AV12,AA13,AY40,AA10,AV14,B33,C33,D29,D32,D30,M38,C36,H25,H28,H31,H34,C38,F34,J36,M36,J38,E37,AT29,AN4,AY25,AR38,AT38,AM38,AN38,AJ38,AK38,AF38,AG38,AK5,AJ7,AM7,A40,AE40,AE39,AV36,AV35,AV33,AV32,AV30,AV29,AV27,AL24,AP23,K26,AP14,AL29,AM30,AV37,AU38,AW25,E35,AN34,AA34,AP36,AT35,AT33,AV38,AW39,AT30,AF34,AG35,AK36,AN28,AP33,AP32,AM34,AE30,AM33,AP30,AJ35,J29,AN27,AH29,AK26,AG25,AH8,AJ29,AG34,AG28,AM26,AN30,AM29,AL26,AK30,AJ26,M37,L38,L33,P34,R31,T32,R34,V29,L28,K27,L25,L26,J31,L32,J28,AL20,AN19,AP18,AP17,L29,W32,AE29,AD31,N32,AA29,AB32,P26,P27,T26,T27,AN5,AR11,AR12,AR14,AR15,AP15,AM21,AJ21,AH24,AH28,AJ32,AK32,AL32,AM32,AN32,AH26,AG9,AK8,AC19,AB26,AC26,AD26,U27,V27,W39,M24,N23,M25,L30,J30,L31,AJ8,AL8,AN29,AL30,AK29,AM23,Y34,AH9,AJ9,AK9,AG16,AJ16,AK16,AM16,AN16,Y33,AK25,AG26,AF26,R16	Internal Logic Ground and Digital IO Ground
AVSS	Y23,AD23,AD25,AA23,AB23,W26,V38,AB11,AB13,AC15,AD13,AB10,AA11,AA25,P38,AD17,AA12,AC16,AC23,P35,AE	Analog Ground

Group	Ball #	Descriptions
	11,AE12,AE14,AE17,R35,AA14,AF17,U35,V35,U38,AV6,AY2,AR3,AU3,AV3,AV8,AV9,AM8,AM9,AA26,AB16,AB15,AC17,AC11,AC13,W23,AR18,R38,U23,V23,AC25,AB17,AA15,AY1,AV5,AV4,AT3,AT7,AR7,AR8,AW10,AY10,AN3,AM2,AP8,AN7,AN8,AP9,AR9,AN6,AN9,AR4,AU6,U26,V26,Y25,AL9,AF10,AG10,AM10,AN10,AP11,AP12,AN13,AM13,AK13,AJ13,AF13,AG13,AF16,AJ10,AK10,A35,AA38,AA40,AC38,AD35,AD38,AE33,AH32,AJ34,AN26,AP24,AR20,AR21,AR23,AR24,AV20,AV21,AV23,AV24,Y35,Y38	
BIGCPU_VDD	K19,K21,L18,L19,L21,L23,M18,M19,M20,M21,M22,N18,N20,N22	Internal BIG CPU A72 Power
LITCPU_VDD	P20,P22,R19,R20,R22,T20,T22	Internal LITTLE CPU A53 Power
GPU_VDD	R11,R12,R13,T11,T12,T13,T14,T15,U13,V11,V12,V13,V14,V15,V16,W10,W11,W12,W14,W15,W16	Internal GPU power
LOGIC_VDD	L17,M17,T17,U17,U18,U20,V18,V19,V20,V21,V22,W20	Internal Logic Power
CENTERLOGIC_VDD	M11,M12,M13,M14,M15,N11,N12,P13,P14,P15	Internal center logic power
DDR0_VDD	L9,L10,M9,N9,N10,P9,R9,R10,T9,U9,U10,V9	DDR0 Digital IO Power
DDR0_CLK_VDD	M7	DDR0Clock IO Power
DDR0PLL_AVDD_0V9	R8	DDR0 PHY PLL power
DDR1_VDD	J11,J12,J13,J14,J15,J16,J17,J18,K11,K13,K15,K17	DDR1 Digital IO Power
DDR1_CLK_VDD	G12	DDR1 Clock IO Power
DDR1PLL_AVDD_0V9	H14	DDR1 PHY PLL power
PMU_VDD_0V9	T24	Internal PMU Domain Power
PMU_VDD_1V8	U25	
PMUIO1_VDD	R24	PMUIO1 Domain IO Power
PMUIO2_VDD	P23 N23	PMUIO2 Domain IO Power
APIO1_VDD	J23	GPIO group 1 Digital Power
APIO1_VDDPST	K23	GPIO group 1Bias
APIO2_VDD	L23 J22	GPIO group 2 Digital Power
APIO2_VDDPST	J24	GPIO group 2 Bias
APIO3_VDD	AB8	GPIO group 3 Digital Power
APIO4_VDD	AC9	GPIO group 4 Digital Power
APIO4_VDDPST	AC8	GPIO group 4Bias
APIO5_VDD	Y8	GPIO group 5 Digital Power
APIO5_VDDPST	AA8	GPIO group 5Bias
SDMMC0_VDD	T23, U26	SDMMC Digital IO Power
PLL_AVDD_0V9	R17	PLL 0.9V Analog Power
PLL_AVDD_1V8	P18	PLL 1.8V Analog Power
PLL_AVSS	P17	PLL Analog Ground
NPU_PLL_AVSS	AG31	NPU PLL Analog Ground
NPU_DDR_AVSS	AN33	NPU DDR Analog Ground
NPU_OSC_VSS	AE32,AA39	NPU OSC Digital Ground

Group	Ball #	Descriptions
ADC_AVDD	AC24	SAR-ADC/TSADC Power
EMMC_VDD_1V8	K24	eMMC digital power
EMMC_COREDLL_0V9	L24	eMMC core digital power
USB20_AVDD_0V9	V24	USB 2.0 Digital Power
USB20_AVDD_1V8	U24	USB 2.0 Analog Power
USB20_AVDD_3V3	Y24	USB 2.0 Analog Power
TYPEC0_AVDD_0V9	Y18,Y19	Type-C Digital Power
TYPEC0_AVDD_1V8	AA18	Type-C Analog Power
TYPEC0_AVDD_3V3	AB18	Type-C Analog Power
USB30_AVDD_0V9	Y21,Y22	Type-C Digital Power
USB30_AVDD_1V8	AA21	Type-C Analog Power
USB30_AVDD_3V3	AA22	Type-C Analog Power
EFUSE	AD23	eFuse IO Digital Power
USIC_AVDD_1V2	AC24	USIC 1.2V Power Supply
USIC_AVDD_0V9	AB24	USIC 0.9V Power Supply
EDP_AVDD_0V9	H20	eDP0.9V Power Supply
EDP_AVDD_1V8	J19,J20	eDP 1.8V Power Supply
EDP_AVSS	C32,H22,C29,C30,H19,J21,C27	eDP analog ground
HDMI_AVDD_0V9	AA16,AA17	HDMI 0.9V Power Supply
HDMI_AVDD_1V8	AD16	HDMI 1.8V Power Supply
MIPI_AVDD_1V8	AB14 AB12 AC10	MIPI 1.8V Power Supply
PCIE_AVDD_0V9	V25	PCIE 0.9V analog power
PCIE_AVDD_1V8	W24	PCIE 1.8V analog power
NPU_PLL_AVDD_1V8	AH31	NPU PLL Analog Power
NPU_PLL_AVDD_0V8	AJ31	NPU PLL Analog Power
NPU_OSC_VDD_1V8	AF32	NPU OSC IO Analog Power
NPU_PMU_VDD_0V8	AF30	NPU PMU Power Domain Power
NPU_PMUIO1_VDD_1V8	AF29	NPU PMUIO1 Power Domain Power
NPU_PMUIO2_VDD	AG29	NPU PMUIO2 Power Domain Power
NPU_PPLL_AVDD_1V8	AF31	NPU PMU PLL Analog Power
NPU_PPLL_AVDD_0V8	AG30	NPU PMU PLL Analog Power
NPU_PCIE/USB3_VDDREF_0V8	AG32	NPU PCIE REF Power
NPU_ADC_AVDD_1V8	AK24	NPU ADC Analog Power
NPU_USB2_AVDD_1V8	AL33	NPU USB2.0 1.8V Analog Power
NPU_USB2_AVDD_3V3	AK33	NPU USB2.0 3.3V Analog Power
NPU_USB2_AVDD_0V8	AJ33	NPU USB2.0 0.8V Analog Power
NPU_CORE_VDD	AH27,AJ27,AK27,AL27,AM27,AJ28,AK28,AL28,AM28	NPU NN Power
NPU_CPU_VDD	AH30,AJ30	NPU CPU Power

Group	Ball #	Descriptions
NPU_LOGIC_VDD	AN31,AL31AK31,AM31	NPU Logic Power
NPU_DDR_VDD	AM35,AN35,AP35,AR34,AR33,AR32,AR30,AP29	NPU DDR PHY Power
NPU_PCIE/USB3_VCCA_1V8	AF33	NPU PCIE Analog Power
NPU_PCIE/USB3_VCCA_0V8	AH33	NPU PCIE Analog Power
NPU_PCIE/USB3_VCCD_0V8	AG33	NPU PCIE Digital Power
NPU_VCCIO5	AP27	VCCIO5 Power Domain Power
NPU_VCCIO6	AJ25	VCCIO6 Power Domain Power

2.7 Power supply for IO

- PMUIO1 IO domain
  - Only support 1.8v mode, with PMUIO1_VDD_1V8(1.8v typical) power supply.
- PMUIO2 IO domain
  - Support 1.8v and 3.0v mode, controlled by PMUGRF_SOC_CON0[9:8], please refer to GRF TRM chapter for detail control information description.
  - With PMUIO2_VDDPST and PMUIO2_VDD two power supply.
    - 1.8v mode: Both PMUIO2_VDDPST and PMUIO2_VDD power supply with 1.8v(typical).
    - 3.0v mode: PMUIO2_VDDPST power supply with 1.5v(typical) and PMUIO2_VDD power supply with 3.0v(typical).
  - PMUIO2_VDDPST and PMUIO2_VDD power up rise time need to >100us and power down fall time also need to >100us.
  - Change from 3.0v mode to 1.8v mode sequence: change external power supply firstly, then wait >1ms, last configure GFR register to change IO working mode.
  - Change from 1.8v mode to 3.0v mode sequence: configure GFR register to change IO working mode firstly, then wait >1ms, last change external power supply.
  - Power up sequence for 3.0v mode: power up PMUIO2_VDDPST firstly, then wait >20us, last power up PMUIO2_VDD.
  - Power down sequence for 3.0v mode: power down PMUIO2_VDD firstly, then wait >20us, last power down PMUIO2_VDDPST.
  - Not support fail-safe condition (PMUIO2 power off, but signal PAD still with high level input drive), otherwise IO reliability will be uncontrollable.
- APIO1 IO domain
  - Only support 3.3v mode, with APIO1_VDDPST(1.8v typical) and APIO1_VDD(3.3v typical) two power supply.
  - APIO1_VDDPST and APIO1_VDD power up rise time need to >100us and power down fall time also need to >100us.
  - Power up sequence: power up APIO1_VDDPST firstly, then wait >20us, last power up APIO1_VDD.
  - Power down sequence: power down APIO1_VDD firstly, then wait >20us, last power down APIO1_VDDPST.
  - Not support fail-safe condition (APIO1 power off, but signal PAD still with high level input drive), otherwise IO reliability will be uncontrollable.
- APIO2/4/5 IO domain
  - Support 1.8v and 3.0v mode, controlled by GRF_IO_VSEL, please refer to GRF TRM chapter for detail control information description.

- With APIO2/4/5_VDDPST and APIO2/4/5_VDD two power supply.
  - 1.8v mode: Both APIO2/4/5_VDDPST and APIO2/4/5_VDD power supply with 1.8v(typical).
  - 3.0v mode: APIO2/4/5_VDDPST power supply with 1.8v(typical) and APIO2/4/5_VDD power supply with 3.0v(typical).
- APIO2/4/5_VDDPST and APIO2/4/5_VDD power up rise time need to >100us and power down fall time also need to >100us.
- Change from 3.0v mode to 1.8v mode sequence: change external power supply firstly, then wait >1ms, last configure GFR register to change IO working mode.
- Change from 1.8v mode to 3.0v mode sequence: configure GFR register to change IO working mode firstly, then wait >1ms, last change external power supply.
- Power up sequence for 3.0v mode: power up APIO2/4/5_VDDPST firstly, then wait >20us, last power up APIO2/4/5_VDD.
- Power down sequence for 3.0v mode: power down APIO2/4/5_VDD firstly, then wait >20us, last power down APIO2/4/5_VDDPST.
- Not support fail-safe condition (APIO2/4/5 power off, but signal PAD still with high level input drive), otherwise IO reliability will be uncontrollable.

- APIO3 IO domain
  - Only support 1.8v mode, with APIO3_VDD_1V8(1.8v typical) power supply.
- SDMMC IO domain
  - Support 1.8v and 3.0v mode, controlled by GRF_IO_VSEL, please refer to GRF TRM chapter for detail control information description.
  - With only SDMMC0_VDD one power supply.
    - 1.8v mode: SDMMC0_VDD power supply with 1.8v(typical).
    - 3.0v mode: SDMMC0_VDD power supply with 3.0v(typical).
  - SDMMC0_VDD power up rise time need to >100us and power down fall time also need to >100us.
  - Change from 3.0v mode to 1.8v mode sequence: change external power supply firstly, then wait >1ms, last configure GRF register to change IO working mode.
  - Change from 1.8v mode to 3.0v mode sequence: configure GFR register to change IO working mode firstly, then wait >1ms, last change external power supply.
  - Not support fail-safe condition (SDMMC power off, but signal PAD still with high level input drive), otherwise IO reliability will be uncontrollable.
- NPU PMUIO1 IO domain
  - Only support 1.8v mode, with NPU_PMUIO1_VDD_1V8(1.8v typical) power supply.
- NPU PMUIO2/VCCIO5/VCCIO6 IO domain
  - Support 1.8v and 3.3v power supply，with NPU_PMUIO2_VDD. 1.8v and 3.3v are detected automatically。
  - Not support fail-safe condition (NPU PMUIO2 power off, but signal PAD still with high level input drive), otherwise IO reliability will be uncontrollable.

2.8 Function IO description

Table 2-3 Function IO description

Pin Name	Func 1	Func 2	Func 3	Func 4	Type	Def	Pull	Drive Strength
GPIO0_A0/TESTCLKOUT0/CLK32K_IN	gpio0_a[0]	testclkout0	clk32k_in		I/O	I	up	5mA
GPIO0_A1/DDRIO_PWROFF/TCPD_CCDB_EN	gpio0_a[1]	ddrio_pwroff	tcpd_ccdb_en		I/O	I	up	5mA
GPIO0_A2	gpio0_a[2]				I/O	I	down	5mA
GPIO0_A3/SDIO0_WRPT	gpio0_a[3]	sdio0_wrpt			I/O	I	down	5mA
GPIO0_A4/SDIO0_INTN	gpio0_a[4]	sdio0_intn			I/O	I	down	5mA
GPIO0_A5/EMMC_PWRON	gpio0_a[5]	emmc_pwren			I/O	I	up	5mA
GPIO0_A6/PWMA3_IR	gpio0_a[6]	pwma3_ir			I/O	I	down	5mA
GPIO0_A7/SDMMC0_DET	gpio0_a[7]	sdmmc0_dectn			I/O	I	up	5mA
GPIO0_B0/SDMMC0_WRPRT/TEST_CLKOUT2	gpio0_b[0]	sdmmc0_wrprt	test_clkout2		I/O	I	up	5mA
GPIO0_B1/PMUIO2_1833_VOLSEL	gpio0_b[1]	pmuio2_1833_volsel			I/O	I	down	5mA
GPIO0_B2	gpio0_b[2]				I/O	I	down	5mA
GPIO0_B3	gpio0_b[3]				I/O	I	down	5mA
GPIO0_B4/TCPD_VBUS_BDIS	gpio0_b[4]	tcpd_vbus_bdis			I/O	I	down	5mA
GPIO0_B5/TCPD_VBUS_FDIS/TCPD_VBUS_SOURCE3	gpio0_b[5]	tcpd_vbus_fdis	tcpd_vbus_source3		I/O	I	down	5mA
GPIO1_A0/ISP_SHUTTER_EN/TCPD_VBUS_SINK_EN	gpio1_a[0]	isp0_shutter_en	isp1_shutter_en	tcpd_vbus_sink_en	I/O	I	down	3mA
GPIO1_A1/ISP_SHUTTER_TRIG/TCPD_CC0_VCONN_EN	gpio1_a[1]	isp0_shutter_trig	isp1_shutter_trig	tcpd_cc0_vconn_en	I/O	I	down	3mA
GPIO1_A2/ISP_FLASHTRIGIN/TCPD_CC1_VCONN_EN	gpio1_a[2]	isp0_flashtrigin	isp1_flashtrigin	tcpd_cc1_vconn_en	I/O	I	down	3mA
GPIO1_A3/ISP_FLASHTRIGOUT	gpio1_a[3]	isp0_flashtrigout	isp1_flashtrigout		I/O	I	down	3mA
GPIO1_A4/ISP_PRELIGHT_TRIG	gpio1_a[4]	isp0_prelight_trig	isp1_prelight_trig		I/O	I	down	3mA
GPIO1_A5/AP_PWROFF	gpio1_a[5]	ap_pwroff			I/O	I	down	3mA
GPIO1_A6/TSADC_INT	gpio1_a[6]	tsadc_int			I/O	I	high-z	3mA
GPIO1_A7/PMCU_UART4DBG_RX/SPI1_RXD	gpio1_a[7]	pmcu_uart4dbg_rx	spi1_rxd		I/O	I	up	6mA

Pin Name	Func 1	Func 2	Func 3	Func 4	Type	Def	Pull	Drive Strength
GPIO1_B0/PMCU_UART4DBG_TX/SPI1_TXD	gpio1_b[0]	pmcu_uart4dbg_tx	spi1_txd		I/O	I	up	6mA
GPIO1_B1/SPI1_CLK/PMCU_JTAG_TCK	gpio1_b[1]	pmcu_jtag_tck	spi1_clk		I/O	I	up	6mA
GPIO1_B2/SPI1_CSN0/PMCU_JTAG_TMS	gpio1_b[2]	pmcu_jtag_tms	spi1_csn0		I/O	I	up	6mA
GPIO1_B3/I2C4_SDA	gpio1_b[3]	i2c4_sda			I/O	I	up	3mA
GPIO1_B4/I2C4_SCL	gpio1_b[4]	i2c4_scl			I/O	I	up	3mA
GPIO1_B5	gpio1_b[5]				I/O	I	down	3mA
GPIO1_B6/PWMB3_IR	gpio1_b[6]	pwmb3_ir			I/O	I	down	3mA
GPIO1_B7/SPI3_RXD/I2C0_SDA	gpio1_b[7]	spi3_rxd	i2c0_sda		I/O	I	up	3mA
GPIO1_C0/SPI3_TXD/I2C0_SCL	gpio1_c[0]	spi3_txd	i2c0_scl		I/O	I	up	3mA
GPIO1_C1/SPI3_CLK	gpio1_c[1]	spi3_clk			I/O	I	down	3mA
GPIO1_C2/SPI3_CSN0	gpio1_c[2]	spi3_csn0			I/O	I	up	3mA
GPIO1_C3/PWM2	gpio1_c[3]	pwm2			I/O	I	down	3mA
GPIO1_C4/I2C8_SDA	gpio1_c[4]	i2c8_sda			I/O	I	up	3mA
GPIO1_C5/I2C8_SCL	gpio1_c[5]	i2c8_scl			I/O	I	up	3mA
GPIO1_C6/DFTJTAG_TDI/TCPD_VBUS_SOURCE0	gpio1_c[6]	dftjtag_tdi	tcpd_vbus_source0		I/O	I	down	6mA
GPIO1_C7/DFTJTAG_TDO/TCPD_VBUS_SOURCE1	gpio1_c[7]	dftjtag_tdo	tcpd_vbus_source1		I/O	I	down	6mA
GPIO1_D0/DFTJTAG_CLK/TCPD_VBUS_SOURCE2	gpio1_d[0]	dftjtag_clk	tcpd_vbus_source2		I/O	I	down	6mA
GPIO2_A0/VOP_D0/CIF_D0/I2C2_SDA	gpio2_a[0]	vop_data[0]	io_cif_data0	i2c2_sda	I/O	I	up	3mA
GPIO2_A1/VOP_D1/CIF_D1/I2C2_SCL	gpio2_a[1]	vop_data[1]	io_cif_data1	i2c2_scl	I/O	I	up	3mA
GPIO2_A2/VOP_D2/CIF_D2	gpio2_a[2]	vop_data[2]	io_cif_data2		I/O	I	down	3mA
GPIO2_A3/VOP_D3/CIF_D3	gpio2_a[3]	vop_data[3]	io_cif_data3		I/O	I	down	3mA
GPIO2_A4/VOP_D4/CIF_D4	gpio2_a[4]	vop_data[4]	io_cif_data4		I/O	I	down	3mA
GPIO2_A5/VOP_D5/CIF_D5	gpio2_a[5]	vop_data[5]	io_cif_data5		I/O	I	down	3mA
GPIO2_A6/VOP_D6/CIF_D6	gpio2_a[6]	vop_data[6]	io_cif_data6		I/O	I	down	3mA
GPIO2_A7/VOP_D7/CIF_D7/I2C7_SDA	gpio2_a[7]	vop_data[7]	io_cif_data7	i2c7_sda	I/O	I	up	3mA
GPIO2_B0/VOP_CLK/CIF_VSYNC/I2C7_SCL	gpio2_b[0]	vop_clk	io_cif_vsync	i2c7_scl	I/O	I	up	3mA

Pin Name	Func 1	Func 2	Func 3	Func 4	Type	Def	Pull	Drive Strength
GPIO2_B1/SPI2_RXD/CIF_HREF/I2C6_SDA	gpio2_b[1]	spi2_rxd	io_cif_href	i2c6_sda	I/O	I	up	3mA
GPIO2_B2/SPI2_TXD/CIF_CLKIN/I2C6_SCL	gpio2_b[2]	spi2_txd	io_cif_clkin	i2c6_scl	I/O	I	up	3mA
GPIO2_B3/SPI2_CLK/VOP_DEN/CIF_CLKOUT	gpio2_b[3]	spi2_clk	io_cif_clkout	vop_den	I/O	I	up	3mA
GPIO2_B4/SPI2_CSN0	gpio2_b[4]	spi2_csn0			I/O	I	up	3mA
GPIO2_C0/UART0_RX	gpio2_c[0]	uart0_rx			I/O	I	up	5mA
GPIO2_C1/UART0_TX	gpio2_c[1]	uart0_tx			I/O	I	up	5mA
GPIO2_C2/UART0_CTSN	gpio2_c[2]	uart0_ctsn			I/O	I	up	5mA
GPIO2_C3/UART0_RTSN	gpio2_c[3]	uart0_rtsn			I/O	I	up	5mA
GPIO2_C4/SDIO0_D0/SPI5_RXD	gpio2_c[4]	sdio0_data0	spi5_rxd		I/O	I	up	5mA
GPIO2_C5/SDIO0_D1/SPI5_TXD	gpio2_c[5]	sdio0_data1	spi5_txd		I/O	I	up	5mA
GPIO2_C6/SDIO0_D2/SPI5_CLK	gpio2_c[6]	sdio0_data2	spi5_clk		I/O	I	up	5mA
GPIO2_C7/SDIO0_D3/SPI5_CSN0	gpio2_c[7]	sdio0_data3	spi5_csn0		I/O	I	up	5mA
GPIO2_D0/SDIO0_CMD	gpio2_d[0]	sdio0_cmd			I/O	I	up	5mA
GPIO2_D1/SDIO0_CLKOUT/TEST_CLKOUT1	gpio2_d[1]	sdio0_clkout	test_clkout1		I/O	I	up	5mA
GPIO2_D2/SDIO0_DETN/PCIE_CLKREQN	gpio2_d[2]	sdio0_detect_n	pcie_clkreqn		I/O	I	up	5mA
GPIO2_D3/SDIO0_PWREN	gpio2_d[3]	sdio0_pwren			I/O	I	down	5mA
GPIO2_D4/SDIO0_BKPWR	gpio2_d[4]	sdio0_bkpwr			I/O	I	down	5mA
GPIO3_A0/MAC_TXD2/SPI4_RXD	gpio3_a[0]	mac_txd2	spi4_rxd	trace_data12	I/O	I	down	4mA
GPIO3_A1/MAC_TXD3/SPI4_TXD	gpio3_a[1]	mac_txd3	spi4_txd	trace_data13	I/O	I	down	4mA
GPIO3_A2/MAC_RXD2/SPI4_CLK	gpio3_a[2]	mac_rxd2	spi4_clk	trace_data14	I/O	I	up	4mA
GPIO3_A3/MAC_RXD3/SPI4_CSN0	gpio3_a[3]	mac_rxd3	spi4_csn0	trace_data15	I/O	I	up	4mA
GPIO3_A4/MAC_TXD0/SPI0_RXD	gpio3_a[4]	mac_txd0	spi0_rxd		I/O	I	down	4mA
GPIO3_A5/MAC_TXD1/SPI0_TXD	gpio3_a[5]	mac_txd1	spi0_txd		I/O	I	down	4mA
GPIO3_A6/MAC_RXD0/SPI0_CLK	gpio3_a[6]	mac_rxd0	spi0_clk		I/O	I	up	4mA
GPIO3_A7/MAC_RXD1/SPI0_CSN0	gpio3_a[7]	mac_rxd1	spi0_csn0		I/O	I	up	4mA
GPIO3_B0/MAC_MDC/SPI0_CSN1	gpio3_b[0]	mac_mdc	spi0_csn1		I/O	I	up	4mA
GPIO3_B1/MAC_RXDV	gpio3_b[1]	mac_rxdv			I/O	I	down	4mA
GPIO3_B2/MAC_RXER/I2C5_SDA	gpio3_b[2]	mac_rxer	i2c5_sda		I/O	I	up	4mA

Pin Name	Func 1	Func 2	Func 3	Func 4	Type	Def	Pull	Drive Strength
GPIO3_B3/MAC_CLK/I2C5_SCL	gpio3_b[3]	mac_clk	i2c5_scl		I/O	I	up	4mA
GPIO3_B4/MAC_TXEN/UART1_RX	gpio3_b[4]	mac_txen	uart1_rx		I/O	I	up	4mA
GPIO3_B5/MAC_MDIO/UART1_TX	gpio3_b[5]	mac_mdio	uart1_tx		I/O	I	up	4mA
GPIO3_B6/MAC_RXCLK/UART3_RX	gpio3_b[6]	mac_rxclk	uart3_rx		I/O	I	up	4mA
GPIO3_B7/MAC_CRS/UART3_TX/CIF_CLKOUTB	gpio3_b[7]	mac_crs	uart3_tx	cif_clkoutb	I/O	I	up	4mA
GPIO3_C0/MAC_COL/UART3_CTSN/SPDIF_TX	gpio3_c[0]	mac_col	uart3_ctsn	spdif_tx	I/O	I	up	4mA
GPIO3_C1/MAC_TXCLK/UART3_RTSN	gpio3_c[1]	mac_txclk	uart3_rtsn		I/O	I	up	4mA
GPIO3_D0/I2S0_SCLK	gpio3_d[0]	i2s0_sclk	trace_data0		I/O	I	down	3mA
GPIO3_D1/I2S0_LRCK_RX	gpio3_d[1]	i2s0_lrck_rx	trace_data1		I/O	I	down	3mA
GPIO3_D2/I2S0_LRCK_TX	gpio3_d[2]	i2s0_lrck_tx	trace_data2		I/O	I	down	3mA
GPIO3_D3/I2S0_SDI0	gpio3_d[3]	i2s0_sdi0	trace_data3		I/O	I	down	3mA
GPIO3_D4/I2S0_SDI1SDO3	gpio3_d[4]	i2s0_sdi1sdo3	trace_data4		I/O	I	down	3mA
GPIO3_D5/I2S0_SDI2SDO2	gpio3_d[5]	i2s0_sdi2sdo2	trace_data5		I/O	I	down	3mA
GPIO3_D6/I2S0_SDI3SDO1	gpio3_d[6]	i2s0_sdi3sdo1	trace_data6		I/O	I	down	3mA
GPIO3_D7/I2S0_SDO0	gpio3_d[7]	i2s0_sdo0	trace_data7		I/O	I	down	3mA
GPIO4_A0/I2S_CLK	gpio4_a[0]	i2s_clk	trace_ctl		I/O	I	down	3mA
GPIO4_A1/I2C1_SDA	gpio4_a[1]	i2c1_sda	trace_clk		I/O	I	up	3mA
GPIO4_A2/I2C1_SCL	gpio4_a[2]	i2c1_scl	trace_data8		I/O	I	up	3mA
GPIO4_A3/I2S1_SCLK	gpio4_a[3]	i2s1_sclk	trace_data9		I/O	I	down	3mA
GPIO4_A4/I2S1_LRCK_RX	gpio4_a[4]	i2s1_lrck_rx	trace_data10		I/O	I	down	3mA
GPIO4_A5/I2S1_LRCK_TX	gpio4_a[5]	i2s1_lrck_tx	trace_data11		I/O	I	down	3mA
GPIO4_A6/I2S1_SDI0	gpio4_a[6]	i2s1_sdi0			I/O	I	down	3mA
GPIO4_A7/I2S1_SDO0	gpio4_a[7]	i2s1_sdo0			I/O	I	down	3mA
GPIO4_B0/SDMMC0_D0/UART2DBG_RX	gpio4_b[0]	sdmmc0_data0	uart2dbg_rx		I/O	I	up	6mA
GPIO4_B1/SDMMC0_D1/UART2DBG_TX	gpio4_b[1]	sdmmc0_data1	uart2dbg_tx	hdcpjtag_trstn	I/O	I	up	6mA
GPIO4_B2/SDMMC0_D2/APJTAG_TCK	gpio4_b[2]	sdmmc0_data2	ap_jtag_tck	hdcpjtag_tdi	I/O	I	up	6mA
GPIO4_B3/SDMMC0_D3/APJTAG_TMS	gpio4_b[3]	sdmmc0_data3	ap_jtag_tms	hdcpjtag_tdo	I/O	I	up	6mA
GPIO4_B4/SDMMC0_CLKOUT/MUCJTAG_TCK	gpio4_b[4]	sdmmc0_clkout	mcujtag_tck	hdcpjtag_tck	I/O	I	down	6mA

Pin Name	Func 1	Func 2	Func 3	Func 4	Type	Def	Pull	Drive Strength
GPIO4_B5/SDMMC0_CMD/MCUJTAG_TMS	gpio4_b[5]	sdmmc0_cmd	mcujtag_tms	hdcpjtag_tms	I/O	I	up	6mA
GPIO4_C0/I2C3_SDA_HDMI/UART2DBG_RX	gpio4_c[0]	i2c3_sda_hdmi	uart2dbg_rx		I/O	I	up	3mA
GPIO4_C1/I2C3_SCL_HDMI/UART2DBG_TX	gpio4_c[1]	i2c3_scl_hdmi	uart2dbg_tx		I/O	I	up	3mA
GPIO4_C2/PWM0/VOP0_PWM/VOP1_PWM	gpio4_c[2]	pwm0	vop0_pwm	vop1_pwm	I/O	I	down	3mA
GPIO4_C3/UART2DBG_RX/UARTHDCP_RX	gpio4_c[3]	uart2dbg_rx	uarthdcp_rx		I/O	I	up	3mA
GPIO4_C4/UART2DBG_TX/UARTHDCP_TX	gpio4_c[4]	uart2dbg_tx	uarthdcp_tx		I/O	I	up	3mA
GPIO4_C5/SPDIF_TX	gpio4_c[5]	spdif_tx			I/O	I	down	3mA
GPIO4_C6/PWM1	gpio4_c[6]	pwm1			I/O	I	down	3mA
GPIO4_C7/HDMI_CECINOUT/EDP_HOTPLUG	gpio4_c[7]	hdmi_cecinout	edp_hotplug		I/O	I	up	3mA
GPIO4_D0/PCIE_CLKREQN	gpio4_d[0]	pcie_clkreqn			I/O	I	up	3mA
GPIO4_D1/DP_HOTPLUG	gpio4_d[1]	dp_hotplug			I/O	I	down	3mA
GPIO4_D2	gpio4_d[2]				I/O	I	down	3mA
GPIO4_D3	gpio4_d[3]				I/O	I	down	3mA
GPIO4_D4	gpio4_d[4]				I/O	I	down	3mA
GPIO4_D5	gpio4_d[5]				I/O	I	down	3mA
GPIO4_D6	gpio4_d[6]				I/O	I	down	3mA
NPU_GPIO1_B4/SPI0_MOSI	GPIO1_B4	SPI0_MOSI			I/O	I	up	4mA
NPU_GPIO1_B5/SPI0_MISO	GPIO1_B5	SPI0_MISO			I/O	I	up	4mA
NPU_GPIO1_B6/SPI0_CSN	GPIO1_B6	SPI0_CSN			I/O	I	up	4mA
NPU_GPIO1_B7/SPI0_CLK	GPIO1_B7	SPI0_CLK			I/O	I	down	4mA
NPU_GPIO4_A2/UART2_TX	GPIO4_A2		UART2_TXM0		I/O	I	up	8mA
NPU_GPIO4_A3/UART2_RX	GPIO4_A3		UART2_RXM0		I/O	I	up	8mA
NPU_GPIO4_A4/JTAG_TCK	GPIO4_A4		JTAG_TCK		I/O	I	up	8mA
NPU_GPIO4_A5/JTAG_TMS	GPIO4_A5		JTAG_TMS		I/O	I	up	8mA
NPU_GPIO0_A2	GPIO0_A2				I/O	I	up	2mA
NPU_GPIO0_A4/SLEEP_STATUS	GPIO0_A4	SLEEP_STATUS			I/O	I	down	2mA
NPU_GPIO0_A6/TSADC_SHUT	GPIO0_A6	TSADC_SHUT			I/O	I	z	2mA
NPU_OSC_BPASS	OSCBYPASS				I	I	up	2mA

Pin Name	Func 1	Func 2	Func 3	Func 4	Type	Def	Pull	Drive Strength
NPU_GPIO0_B0	GPIO0_B0				I/O	I	up	2mA
NPU_GPIO0_C0/I2C1_SCL	GPIO0_C0	I2C1_SCL			I/O	I	down	2mA
NPU_GPIO0_C1/I2C1_SDA	GPIO0_C1	I2C1_SDA			I/O	I	down	2mA
NPU_GPIO0_C2/CLKIO_32K	GPIO0_C2	CLK_INOUT_32K			I/O	I	z	2mA
NPU_GPIO0_C6	GPIO0_C6				I/O	I	down	2mA
NPU_GPIO0_C7	GPIO0_C7				I/O	I	down	2mA

Notes :

①:Type : I = input , O = output , I/O = input/output (bidirectional) ,

AP = Analog Power , AG = Analog Ground
DP = Digital Power , DG = Digital Ground
A = Analog

②: Reset state: I = input without any pull resistor O = output

③: Output Drive strength is configurable, it's the suggested value in this table. Unit is mA , only Digital IO have drive value

④: The pull up/pull down is configurable.

2.9 IO pin name descriptions

This sub-chapter will focus on the detailed function description of every pins based on different interface.

2.9.1 eMMC

Table 2-4 eMMC pin description

Interface	Pin Name	Dir.	Description
eMMC	EMMC_PWREN	I/O	eMMC power control
	EMMC_STRB	I/O	eMMC strobe signal
	EMMC_CLK	O	eMMC clock
	EMMC_CALIO	I/O	CALIO connects to 10k +/- 1% resistor
	EMMC_TP	O	Analog DLL charge pump test point
	EMMC_DATA*i*	I/O	DATA*i* (*i*=0~7), 8bits data lines
	EMMC_CMD	I/O	eMMC CMD line

2.9.2 PCIe

Table 2-5 PCIe pin description

Interface	Pin Name	Dir.	Description
PCIe	PCIE_RCLK_100M_N PCIE_RCLK_100M_P	O	100MHz differential reference clock out for PCIe peripheral
	PCIE_TX*i*_N PCIE_TX*i*_P (i=0~3)	O	PCIe differential data output signals
	PCIE_RX*i*_N PCIE_RX*i*_P (i=0~3)	I	PCIe differential data input signals
	PCIE_CLKREQN	I	PCIe clock request from PCIe peripheral

2.9.3 USB

Table 2-6 USB pin description

Interface	Pin Name	Dir.	Description
USB2.0 HOST (*i*=0,1)	USB20_HOSTi_DN	I/O	USB 2.0 Host data DN
	USB20_HOSTi_DP	I/O	USB 2.0 Host data DP
	USB*i*_RBIAS	I	Connect 133ohm resister to ground

Interface	Pin Name	Dir.	Description
USB 3.0 And Type-C0	TYPEC_DN	I/O	USB 2.0 data DN
	TYPEC_DP	I/O	USB 2.0 data DP
	USB*0*_RBIAS	I	Connect 135ohm resister to ground (Shared with USB 2.0 host0)
	TYPEC_ID	I	USB 2.0 OTG ID detection
	TYPEC_VBUSDET	I	VBUS BUMP into the PHY for VBUS monitor
	TYPEC_CC2	I/O	Configuration Channel2 pin used for connectiondetect interface configuration and VCONN.
	TYPEC_CC1	I/O	Configuration Channel1 pin used for connectiondetect interface configuration and VCONN.

Interface	Pin Name	Dir.	Description
	TYPEC_TX1P TYPEC_TX1M	O	Lane 0 transmitter serial data - USB Tx or DP Tx. TX+/TX1- USB Type-C receptacle pins (A2/A3)
	TYPEC_TX2P TYPEC_TX2M	O	Lane 3 transmitter serial data - USB Tx or DP Tx. TX2+/TX2- USB Type-C receptacle pins (B2/B3)
	TYPEC_RX1P TYPEC_RX1M	I/O	Lane 1 transmitter/receiver serial data - USB Rx or DP Tx. RX1+/RX1- USB Type-C receptacle pins (B11/B10)
	TYPEC_RX2P TYPEC_RX2M	I/O	Lane 2 transmitter/receiver serial data - USB Rx or DP Tx. RX2+/RX2- USB Type-C receptacle pins (A11/A10)
	TYPEC_RCLKM TYPEC_RCLKP	O	External reference clock. Supports nominal frequencies of19.2, 20, 24, 27, 54 and 108 MHz. The following external referenceclock sources are supported: • AC coupled differential low swing clock (HCSL levels) • DC single ended clock on ref_p pin. In this mode ref_mshouldbe tied to ground. This mode is for test purposes only. A reference clock must be provided either on these external pinsor the refclock internal SoC-side pin.
	TYPEC_REXT	I	External calibration resistor
	TYPEC_REXT_CC	I	Bump to conect external precision resistors for internalcalibration circuits.
	TYPEC_AUXM/PU_PD TYPEC_AUXP/PD_PU	I/O	AUX pull-up/pull-down polarity reversal pins. For normal connectororientation, there is a weak pull-down on aux_p wires and aweak pull-up on aux_m wire. These pins are used to reverse thisfor the flipped connector case.
	TYPEC_AUXM TYPEC_AUXP	I/O	AUX differential Tx/Rx serial data

Table 2-7 USB pins for internal link use description

Interface	Pin Name	Dir.	Description
USB 2.0 (INTERNAL USE ONLY)	USB20_OTG1_DN	I/O	USB 2.0 data DN,link with NPU USB2.0
	USB20_OTG1_DP	I/O	USB 2.0 data DP,link with NPU USB2.0
	USB*1*_RBIAS	I	Connect 135ohm resister to ground (Shared with USB 2.0 host1)
	USB20_OTG1_ID	I	USB 2.0 OTG ID detection,let it floating
	USB20_OTG1_VBUS	I	VBUS BUMP into the PHY for VBUS monitor,let it floating
	NPU_USB2_OTG_DM	I/O	NPU USB 2.0 data DM
	NPU_USB2_OTG_DP	I/O	NPU USB 2.0 data DP
	NPU_USB2_OTG_ID	I	NPU USB 2.0 OTG ID detection,let it floating
	NPU_USB2_OTG_VBUS	I	VBUS BUMP into the PHY for VBUS monitor,external pull-up

Interface	Pin Name	Dir.	Description
USB .0 (INTERNAL USE ONLY)	USB30_TX1M USB30_TX1P	O	USB 3.0 transmission signal DP/DM,,link with NPU USB3.0
	USB30_RX1M USB30_RX1P	I/O	USB 3.0 receive signal DP/DM, link with NPU USB3.0
	USB30_REXT	I	External calibration resistor

Interface	Pin Name	Dir.	Description
	NPU_PCIE_TX0N/USB3_SSTXN NPU_PCIE_TX0P/USB3_SSTXP	O	USB 3.0 transmission signal DP/DM,PCIE function reserved
	NPU_PCIE_RX0N/USB3_SSRXN NPU_PCIE_RX0P/USB3_SSRXP	I	USB 3.0 receive signal DP/DM,PCIE function reserved
	NPU_PCIE/USB3_RBIAS	I	2Kohm external resistance bias to ground

2.9.4 eDP

Table 2-8 eDP pin description

Interface	Pin Name	Dir.	Description
eDP	EDP_TX*i*P(*i*=0~3)	O	eDP data lane positive output
	EDP_TX*i*N(*i*=0~3)	O	eDP data lane negative output
	EDP_DC_TP	O	eDP PHY DC test point
	EDP_AUXP	I/O	eDP CH-AUX positive differential output
	EDP_AUXN	I/O	eDP CH-AUX negative differential output
	EDP_REXT	I	Let it floating
	EDP_CLK24M_IN	I	24MHz input reference clock
	EDP_HOTPLUG	I	eDP external hot plug signal

2.9.5 HDMI

Table 2-9 HDMI pin description

Interface	Pin Name	Dir.	Description
HDMI	HDMI_TX*i*N(*i*=0~2)	O	HDMI negative TMDS differential line driver data output
	HDMI_X*i*P(*i*=0~2)	O	HDMI positive TMDS differential line driver data output
	HDMI_TCN	O	HDMI negative TMDS differential line driver clock output
	HDMI_TCP	O	HDMI positive TMDS differential line driver clock output
	HDMI_REXT	I/O	HDMI reference resistor connection
	HDMI_HPD	I/O	HDMI hot plug detect signal
	I2C3_SDA_HDMI	I/O	I2C data line for HDMI
	I2C3_SCL_HDMI	I/O	I2C clock line for HDMI
	HDMI_CECINOUT	I/O	HDMI CEC signal

2.9.6 MIPI

Table 2-10 MIPI pin description

Interface	Pin Name	Dir.	Description
MIPI_DSI	MIPI_TX0_D*i*N(*i*=0~3)	I/O	MIPI DSI negative differential data line transceiver output
	MIPI_TX0_D*i*P(*i*=0~3)	I/O	MIPI DSI positive differential data line transceiver output
	MIPI_TX0_CLKP	I/O	MIPI DSI positive differential clock line transceiver output
	MIPI_TX0_CLKN	I/O	MIPI DSI negative differential clock line transceiver output
	MIPI_TX0_REXT	I/O	MIPI DSI external resistor connection. Recommend to use a 4.02 KΩ E96 resistor.

Interface	Pin Name	Dir.	Description
MIPI_CSI	MIPI_RX0_D*i*N(*i*=0~3)	I/O	MIPI CSI negative differential data line transceiver output
	MIPI_RX0_D*i*P(*i*=0~3)	I/O	MIPI CSI positive differential data line transceiver output
	MIPI_RX0_CLKP	I/O	MIPI CSI positive differential clock line transceiver output
	MIPI_RX0_CLKN	I/O	MIPI CSI negative differential clock line transceiver output

Interface	Pin Name	Dir.	Description
	MIPI_RX0_REXT	I/O	MIPI CSI external resistor connection. Recommend to use a 4.02 KΩ E96 resistor.

Interface	Pin Name	Dir.	Description
MIPI_CSI/DSI	MIPI_TX1/RX1_D*i*N(*i*=0~3)	I/O	MIPI CSI negative differential data line transceiver output
	MIPI_ TX1/RX1_D*i*P(*i*=0~3)	I/O	MIPI CSI positive differential data line transceiver output
	MIPI_ TX1/RX1_CLKP	I/O	MIPI CSI positive differential clock line transceiver output
	MIPI_ TX1/RX1_CLKN	I/O	MIPI CSI negative differential clock line transceiver output
	MIPI_ TX1/RX1_REXT	I/O	MIPI CSI external resistor connection. Recommend to use a 4.02 KΩ E96 resistor.

2.9.7 ISP

Table 2-11 ISP pin description

Interface	Pin Name	Dir.	Description
ISP	ISP_SHUTTER_EN*i*(*i*=0~1)	O	Hold signal for shutter open
	ISP_FLASHTRIGOUT*i*(*i*=0~1)	O	Hold signal for flash light
	ISP_PRELIGHT_TRIG*i*(*i*=0~1)	O	Hold signal for prelight
	ISP_SHUTTER_TRIG*i*(*i*=0~1)	I	External shutter trigger pulse
	ISP_FLASHTRIGIN*i*(*i*=0~1)	I	External flash trigger pulse

2.9.8 EFUSE

Table 2-12 EFUSE pin description

Interface	Pin Name	Dir.	Description
eFuse	EFUSE	N/A	eFuse program and sense power

2.9.9 SAR-ADC

Table 2-13 SAR-ADC pin description

Interface	Pin Name	Dir.	Description
SARADC	ADC_IN*i*(*i*=0~5)	N/A	SAR-ADC input signal for 3 channel

2.9.10 TSADC

Table 2-14 TSADC pin description

Interface	Pin Name	Dir.	Description
TSADC	TSADC_INT	O	TSADC interrupt signal for over temperature

2.9.11 GMAC

Table 2-15 GMAC pin description

Interface	Pin Name	Dir.	Description
GMAC	MAC_CLK	I/O	RMII REC_CLK output or GMAC external clock input
	MAC_TXCLK	O	RGMII TX clock output
	MAC_RXCLK	I	RGMII RX clock input
	MAC_MDC	O	GMAC management interface clock
	MAC_MDIO	I/O	GMAC management interface data
	MAC_TXD*i*(*i*=0~3)	O	GMAC TX data
	MAC_RXD*i*(*i*=0~3)	I	GMAC RX data
	MAC_TXEN	O	GMAC TX data enable
	MAC_RXDV	I	GMAC RX data valid signal

Interface	Pin Name	Dir.	Description
	MAC_RXER	I	GMAC RX error signal
	MAC_COL	I	PHY Collision signal
	MAC_CRS	I	PHY CRS signal

2.9.12 UART

Table 2-16 UART pin description

Interface	Pin Name	Dir.	Description
UART*i* *i*=0,3	UART*i*_RX	I	UARTsearial data input
	UART*i*_TX	O	UARTsearial data output
	UART*i*_CTSN	I	UART clear to send
	UART*i*_RTSN	O	UART request to send

Interface	Pin Name	Dir.	Description
UART*i* *i*=1,2,4	UART*i*_RX	I	UARTsearial data input
	UART*i*_TX	O	UARTsearial data output

Note: UART2 is to be debug port by default.

2.9.13 I2C

Table 2-17 I2C pin description

Interface	Pin Name	Dir.	Description
I2C*i* *i*=0~8	I2C*i*_SDA	I	I2C data line
	I2C*i*_SCL	O	I2C serial clock line

2.9.14 PWM

Table 2-18 PWM pin description

Interface	Pin Name	Dir.	Description
PWM	PWM0	I/O	Pulse Width Modulation output
	PWM1	I/O	Pulse Width Modulation output
	PWM2	I/O	Pulse Width Modulation output
	PWM3_IR	I/O	Pulse Width Modulation output, special design for IR receiver
	VOP0_PWM	I/O	CABC PWM from VOP0
	VOP1_PWM	I/O	CABC PWM from VOP1

2.9.15 CIF

Table 2-19 CIF pin description

Interface	Pin Name	Dir.	Description
Camera Interface	CIF_CLKIN	I	Camera interface input pixel clock
	CIF_CLKOUT	O	Camera interface output work clock
	CIF_CLKOUTB	O	Camera interface output work clock
	CIF_VSYNC	I	Camera interface vertical sync signal
	CIF_HREF	I	Camera interfacehorizontal sync signal
	CIF_D*i*(*i*=0~7)	I	Camera interface input pixel data

2.9.16 SPI

Table 2-20 SPI pin description

Interface	Pin Name	Dir.	Description
SPI0	SPI0_CLK	I/O	SPI serial clock

Interface	Pin Name	Dir.	Description
	SPI0_CSN0	I/O	SPI first chip select signal, low active
	SPI0_CNS1	I/O	SPI second dchip select signal, low active
	SPI0_TXD	O	SPI serial data output
	SPI0_RXD	I	SPI serial data input

Interface	Pin Name	Dir.	Description
SPI*i* *i*=1~5	SPI*i*_CLK	I/O	SPI serial clock
	SPI*i*_CSN0	I/O	SPI firstchip select signal,low active
	SPI*i*_TXD	O	SPI serial data output
	SPI*i*_RXD	I	SPI serial data input

2.9.17 SPDIF

Table 2-21 SPDIF pin description

Interface	Pin Name	Dir.	Description
SPDIF	SPDIF_TX	O	S/PDIF biphase data output

2.9.18 I2S

Table 2-22 I2S pin description

Interface	Pin Name	Dir.	Description
I2S	I2S_CLK	O	I2S/PCM clock source, shared by I2S0 and I2S1

Interface	Pin Name	Dir.	Description
I2S0/PCM0 8 channels	I2S0_SCLK	I/O	I2S/PCM serial clock
	I2S0_LRCK_RX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S0_LRCK_TX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S0_SDI0	I	I2S/PCM serial data input[0]
	I2S0_SDI1SDO3	I	I2S/PCM serial data input[1] or output[3]
	I2S0_SDI2SDO2	I	I2S/PCM serial data input [2] or output [2]
	I2S0_SDI3SDO1	I	I2S/PCM serial data input [3] or output [1]
	I2S0_SDO0	I	I2S/PCM serial data output [0]

Interface	Pin Name	Dir.	Description
I2S1/PCM1 2 channels	I2S1_SCLK	I/O	I2S/PCM serial clock
	I2S1_LRCK_RX	I/O	I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_LRCK_TX	I/O	I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode
	I2S1_SDI0	I	I2S/PCM serial data input 0]
	I2S1_SDO0	I	I2S/PCM serial data output 0]

2.9.19 DDR Controller

Table 2-23 DDRC pin description

Interface	Pin Name	Dir.	Description
DDR*i*] Controller *(i=0,1)*	DDR*i*_ATB*j* (*j*=0,1)	O	Analog test bus signals
	DDR*i*_CLK*j*N DDR*i*_CLK*j*P (*j*=0~1)	O	Differential clock signal to the memory device
	DDR*i*_CKE*j* (*j*=0,1)	O	Active-high clock enable signal to the memory device for two chip select.
	DDR*i*_CSN*j* (*j*=0~3)	O	Active-low chip select signal to the memory device. There are two chip select.
	DDR*i*_RASN	O	Active-low row address strobe to the memory device.
	DDR*i*_CASN	O	Active-low column address strobe to the memory device.
	DDR*i*_WEN	O	Active-low write enable strobe to the memory device.
	DDR*i*_BA[2:0]	O	Bank address signal to the memory device.
	DDR*i*_A[15:0]	O	Address signal to the memory device.
	DDR*i*_DQ[31:0]	I/O	Bidirectional data line to the memory device.
	DDR*i*_DQS*j*N[*j*=0~3]	I/O	Differential data strobes to/from the memories. For writes, the pad drives these signals. For reads, the memory drives these signals.
	DDR*i*_DQS*j*P[*j*=0~3]	I/O	
	DDR*i*_DM[3:0]	O	Active-low data mask signal to the memory device.
	DDR*i*_ODT*j*(*j*=0,1)	O	On-Die Termination output signal for two chip select.
	DDR*i*_RESETN	O	DDR reset signal to the memory device
	DDR0_PLL_TESTOUT_P DDR0_PLL_TESTOUT_N	O	DDR PLL test point
	DDR*i*_PZQ	I/O	ZQ calibration pad which connects 240ohm±1% resistor

2.9.20 SDIO

Table 2-24 SDIO pin description

Interface	Pin Name	Dir.	Description
SDIO Host Controller	SDIO0_CLKOUT	O	SDIO clock.
	SDIO0_CMD	I/O	SDIO command output and reponse input.
	SDIO0_D[0:3]	I/O	SDIO data input and output.
	SDIO0_DETN	I	SDIO detect signal, a 0 represents presence of card.
	SDIO0_WRPT	I	SDIO write protect signal, a 1 represents write is protected.
	SDIO0_PWREN	O	SDIO power-enable control signal
	SDIO0_INTN	O	SDIO interrupt indication
	SDIO0_BKPWR	O	The back-end power supply for embedded device

2.9.21 SDMMC

Table 2-25 SDMMC pin description

Interface	Pin Name	Description
SD/MMC	SDMMC0_CLKOUT	SDMMC card clock

Interface	Pin Name	Description
Host Controller	SDMMC0_CMD	SDMMC card command output and reponse input
	SDMMC0_D[0:3]	SDMMC card data input and output
	SDMMC0_WRPRT	SDMMC card protect
	SDMMC0_DET	SDMMC card detect signal, a 0 represents presence of card
	SDMMC0_VDDPST	Pin out to external capacitor

2.9.22 JTAG

Table 2-26 JTAG pin description

Interface	Pin Name	Dir.	Description
AP JTAG	APJTAG_TCK	I	APJTAG interface clock input/SWD interface clock input
	APJTAG_TMS	I/O	APJTAG interface TMS input/SWD interface data out

Note: AP means CPU core in RK3399Pro including Cortex A72 and Cortex A53.

Interface	Pin Name	Dir.	Description
MCU JTAG	MCUJTAG_TCK	I	MCUJTAG interface clock input/SWD interface clock input
	MCUJTAG_TMS	I/O	MCUJTAG interface TMS input/SWD interface data out

Note: MCU means built-in micro-controller in RK3399Pro core domain.

Interface	Pin Name	Dir.	Description
PMCU JTAG	PMCU_JTAG_TCK	I	PMU MCU JTAG interface clock input/SWD interface clock input
	PMCU_JTAG_TMS	I/O	PMU MCU JTAG interface TMS input/SWD interface data out

Note: PMCU means built-in micro-controller in RK3399Pro PMU domain.

2.9.23 MISC

Table 2-27 MISC pin description

Interface	Pin Name	Dir.	Description
Misc	XIN_OSC	I	Clock input of 24MHz crystal
	XOUT_OSC	O	Clock output of 24MHz crystal
	CLK32K	I	Clock input of 32.768KHz
	NPOR	I	Chip hardware reset
	AP_PWROFF	O	System power off control port (PMIC_SLEEP)

Chapter 3 Electrical Specification

3.1 Absolute Maximum Ratings

Table 3-1 Absolute maximum ratings

Paramerters	Related Power Group	Max	Unit
DC supply voltage for Internal digital logic	BIGCPU_VDD, LITCPU_VDD, LOGIC_VDD, CENTERLOGIC_VDD	1.3	V
DC supply voltage for Internal digital logic	NPU_CPU_VDD NPU_CORE_VDD	1.045	V
DC supply voltage for Internal digital logic	NPU_LOGIC_VDD	0.98	V
DC supply voltage for DDR IO	DDR_VDD	1.65	V
Storage Temperature	Tstg	125	℃
Max Conjunction Temperature	Tj	125	℃
ESD (HBM)		>2000	V

Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.

3.2 Recommended Operating Conditions

The below table describes the recommended operating condition for every clock domain.

Table 3-2 Recommended operating conditions

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage for Cortex A72 CPU	BIGCPU_VDD	0.80	0.90	1.25	V
Supply voltage for Cortex A53 CPU	LITCPU_VDD	0.80	0.90	1.20	V
Supply voltage for NPU NN Power	NPU_CORE_VDD	0.72	0.80	0.88	V
Max frequency of Cortex A72 CPU	Frequency			1.8	GHz
Max frequency of Cortex A53 CPU	Frequency			1.4	GHz
Max frequency of NPU	Frequency			800	MHz
Supply voltage for GPU	GPU_VDD	0.80	0.90	1.20	V
Max frequency of GPU	Frequency			800	MHz
Internal digital logic Power	CENTERLOGIC_VDD LOGIC_VDD	0.80	0.90	1.0	V
NPU CPU Power	NPU_CPU_VDD	0.72	0.80	0.945	V
NPU digital logic power	NPU_LOGIC_VDD	0.72	0.80	0.88	V
NPU PMU Power	NPU_PMU_VDD	0.72	0.80	0.945	V
PMU digital logic power (0.9V)	PMU_VDD_0V9	0.81	0.9	0.99	V
PMU digital logic power (1.8V)	PMU_VDD_1V8	1.62	1.8	1.98	V
EMMC power	EMMC_VDD_1V8	1.62	1.8	1.98	V
Supply voltage for digital GPIO@1.8V mode	PMUIO1_VDD_1V8 PMUIO2_VDDPST PMUIO2_VDD APIO2_VDDPST	1.62 1.71 1.71 1.71	1.8 1.8 1.8 1.8	1.98 1.89 1.89 1.89	V

Parameters	Symbol	Min	Typ	Max	Unit
	APIO2_VDD	1.71	1.8	1.89	
	APIO3_VDD_1V8	1.62	1.8	1.98	
	APIO4_VDDPST	1.71	1.8	1.89	
	APIO4_VDD	1.71	1.8	1.89	
	APIO5_VDDPST	1.71	1.8	1.89	
	APIO5_VDD	1.71	1.8	1.89	
	SDMMC0_VDD	1.71	1.8	1.89	
	NPU_PMUIO1_VDD_1V8	1.62	1.8	1.98	
	NPU_PMUIO2_VDD_1VB	1.62	1.8	1.98	
	NPU_VCCIO5	1.62/2.97	1.8/3.3	1.98/3.63	
	NPU_VCCIO6	1.62/2.97	1.8/3.3	1.98/3.63	
Supply voltage for digital GPIO@3.0V mode	PMUIO2_VDDPST	1.425	1.5	1.575	V
	PMUIO2_VDD	2.85	3.0	3.15	
	APIO2_VDDPST	1.425	1.5	1.575	
	APIO2_VDD	2.85	3.0	3.15	
	APIO4_VDDPST	1.425	1.5	1.575	
	APIO4_VDD	2.85	3.0	3.15	
	APIO5_VDDPST	1.425	1.5	1.575	
	APIO5_VDD	2.85	3.0	3.15	
	SDMMC0_VDD	2.85	3.0	3.15	
Supply voltage for digital GPIO@3.3V mode	APIO1_VDDPST	1.71	1.8	1.89	V
	APIO1_VDD	3.135	3.3	3.465	
Supply voltage for Dual-Channel DDR	DDRPLL_AVDD_0V9	0.81	0.9	0.99	V
	DDR_VDD@DDR3	1.425	1.5	1.575	
	DDR_VDD@DDR3L	1.28	1.35	1.42	
	DDR_VDD@LPDDR3	1.14	1.2	1.3	
	DDR_VDD@LPDDR4	1.06	1.1	1.17	
	DDR_CLK_VDD@DDR3	1.425	1.5	1.575	
	DDR_CLK_VDD@DDR3L	1.28	1.35	1.42	
	DDR_CLK_VDD@LPDDR3	1.14	1.2	1.3	
	DDR_CLK_VDD@LPDDR4	1.06	1.1	1.17	
Supply voltage for NPU Dedicated DDR	NPU_DDR_VDD@LPDDR3	1.14	1.20	1.32	V
	NPU_DDR_VDD@DDR3	1.425	1.5	1.575	
	NPU_DDR_VDD@DDR3L	1.283	1.35	1.418	
	NPU_DDR_VDD@LPDDR2	1.14	1.20	1.26	
Supply voltage for SAR-ADC	ADC_AVDD	1.62	1.8	1.98	V
Supply voltage for EFUSE	EFUSE	1.62	1.8	1.98	V
Supply voltage for PLL	PLL_AVDD_0V9	0.81	0.9	0.99	V
	PLL_AVDD_1V8	1.62	1.8	1.98	
Supply voltage for NPU PLL	NPU_PPLL_AVDD_0V8	0.72	0.8	0.88	V
	NPU_PPLL_AVDD_1V8	1.62	1.8	1.98	
Supply voltage for EDP	EDP_AVDD_0V9	0.81	0.9	0.99	V
	EDP_AVDD_1V8	1.62	1.8	1.98	
Supply voltage for EMMC	EMMC_COREDLL_0V9	0.81	0.9	0.99	V
	EMMC_VDD_1V8	1.62	1.8	1.98	

Parameters	Symbol	Min	Typ	Max	Unit
Supply voltage for HDMI	HDMI_AVDD_0V9 HDMI_AVDD_1V8	0.81 1.62	0.9 1.8	0.99 1.98	V
Supply voltage for MIPI	MIPI_TX0_AVDD_1V8 MIPI_TX1/RX1_AVDD_1V8 MIPI_RX0_AVDD_1V8	1.62	1.8	1.98	V
Supply voltage for PCIE	PCIE_AVDD_0V9 PCIE_AVDD_1V8	0.81 1.62	0.9 1.8	0.99 1.98	V
Supply voltage for NPU PCIE/USB3.0	NPU_PCIE/USB3_VCCA_0V8 NPU_PCIE/USB3_VCCA_1V8 NPU_PCIE/USB3_VCCD_0V8 NPU_PCIE/USB3_VDDREF_0V8	0.72 1.62 0.72 0.72	0.8 1.8 0.8 0.8	0.88 1.98 0.88 0.88	V
Supply voltage for TYPEC	TYPEC0_AVDD_0V9 TYPEC0_AVDD_1V8 TYPEC0_AVDD_3V3	0.81 1.62 2.97	0.9 1.8 3.3	0.99 1.98 3.63	V
Supply voltage for USIC	USIC_AVDD_0V9 USIC_AVDD_1V2	0.81 1.08	0.9 1.2	0.99 1.32	V
Supply voltage for USB	USB20_AVDD_0V9 USB20_AVDD_1V8 USB20_AVDD_3V3	0.81 1.62 2.97	0.9 1.8 3.3	0.99 1.98 3.63	V
Supply voltage for NPU USB	NPU_USB_AVDD_0V8 NPU_USB_AVDD_1V8 NPU_USB_AVDD_3V3	0.72 1.62 2.97	0.8 1.8 3.3	0.88 1.98 3.63	V
Supply voltage for USB3.0	USB30_AVDD_0V9 USB30_AVDD_1V8 USB30_AVDD_3V3	0.81 1.62 2.97	0.9 1.8 3.3	0.99 1.98 3.63	V
PLL input clock frequency		N/A	24	N/A	MHz
Ambient Operating Temperature for RK3399Pro	Ta	0	25	80	℃

Notes:

1) *Symbol name is same as the pin name in the IO descriptions*
2) *with the reference software setup, the reference software will limit the chipset temperature about 85℃*

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input Low Voltage	Vil	-0.3	N/A	1.07	V
	Input High Voltage	Vih	2.0	N/A	3.6	V
	Output Low Voltage	Vol	N/A	N/A	0.66	V
	Output High Voltage	Voh	2.4	N/A	N/A	V
	Threshold Point	Vtr+	1	1.16	1.34	V
		Vtr-	1.02	1.19	1.39	V

Parameters		Symbol	Min	Typ	Max	Unit
	Pull up resistor	RPU	26	60	100	kΩ
	Pull down resistor	RPD	27	68	110	kΩ
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	N/A	0.63	V
	Input High Voltage	Vih	1.17	N/A	2.1	V
	Output Low Voltage	Vol	N/A	N/A	0.45	V
	Output High Voltage	Voh	1.35	N/A	N/A	V
	Threshold Point	Vtr+	0.82	0.9	1.0	V
		Vtr-	0.84	0.91	1.0	V
	Pull up resistor	RPU	33	63	120	kΩ
	Pull down resistor	RPD	34	61	114	kΩ
Digital GPIO @3.0V	Input Low Voltage	Vil	-0.3	N/A	0.71	V
	Input High Voltage	Vih	1.875	N/A	3.15	V
	Output Low Voltage	Vol	N/A	N/A	0.375	V
	Output High Voltage	Voh	2.25	N/A	N/A	V
	Threshold Point	Vtr+	0.8	0.93	1.1	V
		Vtr-	0.82	0.95	1.13	V
	Pullup Resistor	RPU	33	59	89	kΩ
	Pulldown Resistor	RPD	34	61	95	kΩ
DDR IO	I/O supply voltage VIOS	DDR3	1.425	1.5	1.575	V
		DDR3L	1.28	1.35	1.42	V
		LPDDR3	1.14	1.2	1.3	V
		LPDDR4	1.06	1.1	1.17	V
	I/O output voltage VIOT	DDR3	0.49	0.50	0.51	VIOS
		DDR3L	0.49	0.50	0.51	VIOS
		LPDDR3		1		VIOS
		LPDDR4		0		
MIPI_DSI IO	HS TX static Common-mode voltage	VCMTX	150	200	250	mV
	VCMTX mismatch when output is Differential-1 or Differential-0	|ΔVCMTX(1,0)|	N/A	N/A	5	mV
	HS transmit differential voltage	|VOD|	140	200	270	mV
	VOD mismatch when output is Differential-1 or Differential-0	|ΔVOD|	N/A	N/A	14	mV
	HS output high voltage	VOHHS	N/A	N/A	360	mV
	Single ended output impedance	ZOS	40	50	62.5	Ω
	Single ended output impedance mismatch	ΔZOS	N/A	N/A	10	%
HDMI	Single-ended standby voltage	Voff	avddtmds±10			mV
	Single-ended output swing voltage	Vswing	400	N/A	600	mV
		Vswing_data	400	N/A	600	mV

Parameters		Symbol	Min	Typ	Max	Unit
	RT=50Ω	Vswing_clock	200	N/A	600	mV
	Single-ended output high voltage	Vh	avddtmds±10			mV
			avddtmds-200	N/A	avddtmds+10	mV
		Vh_data	avddtmds-400	N/A	avddtmds+10	mV
		Vh_clock	avddtmds-400	N/A	avddtmds+10	mV
	Single-ended output low voltage	Vl	avddtmds-600	N/A	avddtmds-400	mV
			avddtmds-700	N/A	avddtmds-400	mV
		Vl_data	avddtmds-1000	N/A	avddtmds-400	mV
		Vl_clock	avddtmds-1000	N/A	avddtmds-200	mV
	Differential source termination load	Rterm	50	N/A	200	Ω

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	N/A	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	N/A	N/A	10	uA
	High level output current	Oih	25℃	6	N/A	110	mA
	Low level output current	Oil	25℃	4	N/A	110	mA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	N/A	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	N/A	N/A	10	uA
	High level output current	Oih	25℃	3.7	N/A	65	mA
	Low level output current	Oil	25℃	4.8	N/A	65	mA
Digital GPIO @3.0V	Input leakage current	Ii	Vin = 3.0V or 0V	N/A	N/A	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.0V or 0V	N/A	N/A	10	uA
	Pull up resistor	R_{PU}					
	Pull down resistor	R_{PD}					
	High level output current	Oih	25℃	5.0	N/A	27.9	mA
	Low level output current	Oil	25℃	3.1	N/A	20.1	mA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Output frequency range	Fout		1	N/A	3200	MHz
Lock time	Tlt		N/A	250	500	Input clock cycles
Power consumption (normal mode)	N/A	FVCO=1GHz	N/A	3	N/A	mW

Period jitter (random)	N/A	VCO=3200MHz	N/A	NA	0.11	Ps(RMS)
Junction temperature	N/A		N/A	25	125	℃

3.6 Electrical Characteristics for SAR-ADC

Table 3-6 Electrical Characteristics for SAR-ADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
ADC resolution			N/A	10	N/A	bits
Clock frequency	f_{CLK}		N/A	N/A	13	MHz
Clock period	t_{CLK}		75	N/A	N/A	ns
Conversion time	Fs		13	N/A	N/A	t_{CLK}
Differential Non Linearity	DNL		N/A	±1	N/A	LSB
Integral Nn Linearity	INL		N/A	±2	N/A	LSB
Analog Supply Current	I_{AVDD}		N/A	450	N/A	uA
Digital Supply Current	I_{VDD}		N/A	50	N/A	uA
Power Down Current from AVDD			NA	1	NA	uA
Power Down Current from DVDD			N/A	1	N/A	uA
Setup up time	t_s		N/A	0.5	N/A	t_{CLK}

3.7 Electrical Characteristics for TSADC

Table 3-7 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
ADC resolution			N/A	10	N/A	bits
TSADC Accuracy	Fs		N/A	N/A	5	℃
Active power			N/A	0.17	N/A	mW
Clock Frequency	Fclk		N/A	NA	800	KHz
Power Down Current from DVDD			N/A	1	N/A	uA

3.8 Electrical Characteristics for Type-C PHY

Table 3-8 Electrical Characteristics for Type-C PHY

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
High input level	VIH		NA	1.0	NA	V

3.9 Electrical Characteristics for USB2.0 PHY

Table 3-9 Electrical Characteristics for USB2.0 PHY

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
High input level	VIH		NA	1.0	NA	V
Low input level	VIL		NA	0	NA	V
Output resistance	ROUT	Classic mode (Vout	40.5	45	49.5	ohms

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
		= 0 or 3.3V)				
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	0.3	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode		+-250		mV
		HS mode		+-25		mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High output level	VOH		NA	3.3	NA	V
Low output level	VOL		NA	0	NA	V

3.10 Electrical Characteristics for DDR IO

Table 3-10 Electrical Characteristics for Dual-Chanel DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current		@ 1.5V	-2	N/A	2	uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V	-2	N/A	2	uA
DDR IO @LPDDR3 mode	Input leakage current		@ 1.2V	-2	N/A	2	uA

DDR IO @LPDDR4 mode	Input leakage current		@ 1.1V	-2	N/A	2	uA

Table 3-11 Electrical Characteristics for NPU Dedicated DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current, SSTL mode, unterminated		@ 1.5V , 125℃	NA	0	NA	uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	NA	0	NA	nA
DDR IO @LPDDR2/LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	NA	0	0.49	nA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃	-5	0	+5	uA

3.11 Electrical Characteristics for eFuse

Table 3-12 Electrical Characteristics for eFuse

	Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Active mode	VDD current in Read mode	Iread_vdd	nomal read	N/A	9	N/A	mA
	VDD current in PGM mode	Ipgm_vdd	STROBE high	N/A	17	N/A	mA
	VQPS current in PGM mode	Ipgm_vqps	STROBE high	N/A	0.2	N/A	uA
standby mode	VDD current in standby mode	Istandby_vdd	Standby	N/A	10	N/A	uA

3.12 Electrical Characteristics for HDMI

Table 3-13 Electrical Characteristics for HDMI

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Differential output signal rise time	tR	20~80% RL=50Ω	75	N/A	0.4UI	ps
	tR_DATA	20~80% RL=50Ω	42.5	N/A	N/A	ps
	tR_CLOCK	20~80% RL=50Ω	75	N/A	N/A	ps
Differential output signal fall time	tF	20~80% RL=50Ω	75	N/A	N/A	ps
	tF_DATA	20~80% RL=50Ω	42.5	N/A	N/A	ps
	tF_CLOCK	20~80% RL=50Ω	75	N/A	N/A	ps

3.13 Electrical Characteristics for MIPI PHY

Table 3-14 Electrical Characteristics for MIPI PHY

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
HS Transmitter AC specifications (MIPI mode)						
Common-mode variations above 450 MHz	ΔVCMTX(HF)		N/A	N/A	15	mVRMS
Common-mode variations between 50MHz – 450MHz	ΔVCMTX(LF)		N/A	N/A	25	mVPEAK
20%-80% rise time and fall time	TR and TF		100	N/A	N/A	ps
HS Receiver AC specifications (MIPI mode)						
Common-mode interference beyond 450 MHz	ΔVCMRX(HF)		N/A	N/A	200	mV
Common-mode interference	ΔVCMRX(LF)		-50	NA	50	mV
Common-mode termination	CCM		N/A	N/A	60	pF
LP receiver AC specifications(MIPI mode)						
Input pulse rejection	eSPIKE		N/A	N/A	300	V.ps
Minimum pulse width response	TMIN-RX		20	N/A	N/A	ns
Peak interference amplitude	VINT		N/A	N/A	400	mV
Interference frequency	fINT		450	N/A	N/A	MHz
LP Transmitter AC Specifications(MIPI mode)						
15%-85% rise time and fall time	TRLP/TFLP		N/A	N/A	25	ns
30%-85% rise time and fall time	TREOT		N/A	N/A	35	ns
Slew rate	δV/δtSR		N/A	N/A	150	mV/ns
Load capacitance	CLOAD		0	N/A	70	pF

3.14 Electrical Characteristics for eMMC PHY

Table 3-15 Electrical Characteristics for eMMC PHY

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Input leakage current			N/A	12	N/A	pA
Tri-state output leakage current			N/A	10	N/A	pA

3.15 Electrical Characteristics for PCIe PHY

Table 3-16 Electrical Characteristics for PCIe PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter						
Unit Interval	UI	2.5Gbps	399.88	N/A	400.12	ps
Differential p-pTx voltage swing	$V_{TX-DIFF-PP}$	2.5Gbps	0.8	N/A	1.2	V
Low power differential p-p Tx voltage swing	$V_{TX-DIFF-PP-LOW}$	2.5Gbps	0.4	N/A	1.2	V
Tx de-emphasis level ratio	$V_{TX-DE-RATIO-3.5dB}$	2.5Gbps	3.0	N/A	4.0	dB

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter Eye including all jitter sources	T_{TX-EYE}	2.5Gbps	0.75	N/A	N/A	UI
Maximum time between the jitter median and max deviation from the median	$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	2.5Gbps	N/A	N/A	0.125	UI
Transmitter rise and fall time	$T_{TX-RISE-FALL}$	2.5Gbps	0.125	N/A	N/A	UI
Tx package plus Si differential return loss	$RL_{TX-DIFF}$	2.5Gbps	10	N/A	N/A	dB
Tx package plus Si common mode return loss	RL_{TX-CM}	2.5Gbps	6	N/A	N/A	dB
Tx AC common mode voltage	$V_{TX-CM-AC-P}$	2.5Gbps	20	N/A	N/A	mV
Transmitter short-circuit current limit	$I_{TX-SHORT}$	2.5Gbps	N/A	N/A	90	mA
Transmitter DC common-mode voltage	$V_{TX-DC-CM}$	2.5Gbps	0	N/A	3.6	V
Absolute Delta of DC Common Mode Voltage during L0 and Electrical Idle.	$V_{TX-CM-DC-ACTIVEIDLE-DELTA}$	2.5Gbps	0	N/A	100	mV
Electrical Idle Differential Peak Output Voltage	$V_{TX-IDLE-DIFF-AC-p}$	2.5Gbps	0	N/A	20	mV
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$	2.5Gbps	N/A	N/A	600	mV
Minimum time spent in Electrical Idle	$T_{TX-IDLE-MIN}$	2.5Gbps	20	N/A	N/A	ns
Maximum time to transition to a valid Electrical Idle after sending an EIOS	$T_{TX-IDLE-SET-TOIDLE}$	2.5Gbps	N/A	N/A	8	ns
Maximum time to transition to valid diff signaling after leaving Electrical Idle	$T_{TX-IDLE-TO-DIFFDATA}$	2.5Gbps	N/A	N/A	8	ns
Crosslink random timeout	$T_{CROSSLINK}$	2.5Gbps	N/A	N/A	1.0	ms
AC Coupling Capacitor	C_{TX}	2.5Gbps	75	N/A	200	nF
Receiver						
Unit Interval	UI	2.5Gbps	399.88	N/A	400.12	ps
Differential Rx peak-peak voltage for common Refclk Rx architecture	$V_{RX-DIFF-PP-CC}$	2.5Gbps	0.175	N/A	1.2	V
Differential Rx peak-peak voltage for data clocked Rx architecture	$V_{RX-DIFF-PP-DC}$	2.5Gbps	0.175	N/A	1.2	V
Receiver eye time opening	T_{RX-EYE}	2.5Gbps	0.40	N/A	N/A	UI
Max time delta between median and deviation from	$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	2.5Gbps	0.3	N/A	N/A	UI

Parameters	Symbol	Condition	Min	Typ	Max	Unit
median						
Rx AC common mode voltage	$V_{RX-CM-AC-P}$	2.5Gbps	N/A	N/A	150	mVP
Rx package plus Si differential return loss	$RL_{RX-DIFF}$	2.5Gbps	10	N/A	N/A	dB
Common mode Rx return loss	RL_{RX-CM}	2.5Gbps	6	N/A	N/A	dB
DC differential impedance	$Z_{RX-DIFF-DC}$	2.5Gbps	80	N/A	120	Ω
Receiver DC single ended impedance	Z_{RX-DC}	2.5Gbps	40	N/A	60	Ω
Electrical Idle Detect Threshold	$V_{RX-IDLE-DET-DIFF-p-p}$	2.5Gbps	65	N/A	175	mV
Unexpected Electrical Idle Enter Detect Threshold Integration Time	$T_{RX-IDLE-DET-DIFFENTERTIME}$	2.5Gbps	N/A	N/A	10	ms
Lane to Lane skew	$L_{RX-SKEW}$	2.5Gbps	N/A	N/A	20	ns

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Power Dissipation		7	W
Junction-to-ambient thermal resistance	θ_{JA}	10.545	(℃/W)
Junction-to-board thermal resistance	θ_{JB}	3.045	(℃/W)
Junction-to-case thermal resistance	θ_{JC}	0.497	(℃/W)

Note: The testing JEDEC PCB is based on 8layers, 201.8x137.8 mm, 1.6 mm Thickness, ambient temperature is 25℃.