# Rockchip PX30 Datasheet



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# Revision History

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# Table of Content

Table of Content ..... 3
Figure Index ..... 4
Table Index ..... 5
Waranty Disclaimer ..... 6
Chapter 1 Introduction ..... 7
1.1 Overview ..... 7
1.2 Features ..... 7
1.3 Block Diagram ..... 17
Chapter 2 Package Information ..... 19
2.1 Order Information ..... 19
2.2 Top Marking ..... 19
2.3 TFBGA418LDimension ..... 20
2.4 Ball Map ..... 21
2.5 Pin Number Order ..... 26
2.6 Power/Ground IO Description ..... 31
2.7 Function IO Description ..... 33
2.8 IO Pin Name Description ..... 43
Chapter 3 Electrical Specification ..... 49
3.1 Absolute Ratings ..... 49
3.2 Recommended Operating Condition ..... 49
3.3 DC Characteristics ..... 50
3.4 Electrical Characteristics for General IO ..... 51
3.5 Electrical Characteristics for PLL ..... 52
3.6 Electrical Characteristics for USB 2.0 Interface ..... 53
3.7 Electrical Characteristics for DDR IO ..... 53
3.8 Electrical Characteristics for TSADC ..... 54
3.9 Electrical Characteristics for MIPI DSI ..... 54
3.10 Electrical Characteristics for MIPI CSI ..... 55
Chapter 4 Thermal Management ..... 56
4.1 Overview ..... 56
4.2 Package Thermal Characteristics ..... 56

# Figure Index

Fig.1-1 Block Diagram ..... 17
Fig.2-1 Package definition ..... 19
Fig.2-2 Package Top View ..... 20
Fig.2-3 Package bottom view ..... 20
Fig.2-4 Package side view ..... 21
Fig.2-5 Package dimension ..... 21
Fig.2-6 Ball Map-1 ..... 22
Fig.2-7 Ball Map-2 ..... 23
Fig.2-7 Ball Map-3 ..... 24
Fig.2-7 Ball Map-4 ..... 25

# Table Index

Table 2-1 Pin Number Order Information ..... 26
Table 2-2 Power/Ground IO information ..... 31
Table 2-3 Function IO description ..... 33
Table 2-4 IO function description list ..... 43
Table 3-1 Absolute ratings ..... 49
Table 3-2 Recommended operating condition ..... 49
Table 3-3 DC Characteristics ..... 50
Table 3-4 Electrical Characteristics for Digital General IO ..... 51
Table 3-5 Electrical Characteristics for PLL ..... 52
Table 3-6 Electrical Characteristics for USB 2.0 Interface ..... 53
Table 3-7 Electrical Characteristics for DDR IO ..... 53
Table 3-8 Electrical Characteristics for TSADC ..... 54
Table 3-9 Electrical Characteristics for MIPI DSI ..... 54
Table 3-10 Electrical Characteristics for MIPI CSI ..... 55
Table 4-1 Thermal Resistance Characteristics ..... 56



 

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# Chapter 1 Introduction

## 1.1 Overview

PX30 is a high-performance Quad-core application processor designed for personal mobile internet device and other digital multimedia applications.

Many embedded powerful hardware engines are provided to optimize performance for high-end application. PX30 supports almost full-format H.264 decoder by 1080p@60fps, H.265 decoder by 1080p@60fps, also support H.264 encoder by 1080p@30fps, high-quality JPEG encoder/decoder.

Embedded ARM G31-2EE GPU makes PX30 completely compatible with OpenGL ES 1.1/2.0/3.2, DirectX 11 FL9_3, OpenCL 2.0 and Vulkan 1.0 Special 2D hardware engine will maximize display performance and provide very smoothly operation.

PX30 has high-performance external memory interface (DDR3/DDR3L/DDR4/LPDDR2/LPDDR3) capable of sustaining demanding memory bandwidths.

## 1.2 Features

The features listed below which may or may not be present in actual product, may be subject to the third party licensing requirements. Please contact Rockchip for actual product feature configurations and licensing requirements.

### 1.2.1 Microprocessor

- Quad-core ARM Cortex-A35 CPU
- Full implementation of the ARM architecture v8-A instruction set
- ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- ARMv8 Cryptography Extensions
- In-order pipeline with symmetric dual-issue of most instructions
- 256KB unified system L2 cache
- Include VFP v3 hardware to support single and double-precision operations
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A35_0: 1st Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_A35_1: 2nd Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_A35_2: 3rd Cortex-A35 + Neon + FPU + L1 I/D Cache
  - PD_A35_3: 4th Cortex-A35 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain to support DVFS

### 1.2.2 Memory Organization

- Internal on-chip memory
  - BootROM
  - SYSTEM_SRAM in the voltage domain of VD_LOGIC
  - PMU_SRAM in the voltage domain of VD_PMU for low power application

- External off-chip memory①
  - DDR3/DDR3L/DDR4/LPDDR2/LPDDR3
  - SPI Flash
  - eMMC
  - SD_Card

- 8bits Async Nand Flash
- 8bits toggle Nand Flash
- 8bit ONFI Nand Flash

### 1.2.3 Internal Memory

- Internal BootRom
  - Support system boot from the following device:
    - SPI Flash interface
    - eMMC interface
    - SDMMC interface
    - Toggle Nand Flash
    - Async Nand FLash
  - Support system code download by the following interface:
    - USB OTG interface (Device mode)

- SYSTEM_SRAM
  - Size: 16KB

- PMU_SRAM
  - Size: 8KB

### 1.2.4 External Memory or Storage device

- Dynamic Memory Interface (DDR3/DDR3L/DDR4/LPDDR2/LPDDR3)
  - Compatible with JEDEC standards
  - Compatible with DDR3-1600/DDR3L-1600/DDR4-1600/LPDDR2-1066 /LPDDR3-1600
  - Support 32-bit data width, 2 ranks (chip selects), max 4GB addressing space per rank; total addressing space is 4GB(max) also
  - Low power modes, such as power-down and self-refresh for SDRAM
  - Compensation for board delays and variable latencies through programmable pipelines
  - Programmable output and ODT impedance with dynamic PVT compensation

- eMMC Interface
  - Compatible with standard iNAND interface
  - Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1
  - Support three data bus width: 1-bit, 4-bit or 8-bit
  - Support up to HS200; but not support CMD Queue

- SD/MMC Interface
  - Compatible with SD3.0, MMC ver4.51
  - Data bus width is 4bits

- Nand Flash Interface
  - Support async nand flash, each channel 8bits, up to 4 banks
  - Support ONFI Synchronous Flash Interface, each channel 8bits, up to 4 banks
  - Support Toggle Flash Interface, each channel 8bits, up to 4 banks
  - Support LBA nand flash in async or sync mode
  - Up to 70bits/1KB hardware ECC
  - For DDR nand flash, support DLL bypass and 1/4 or 1/8 clock adjust, maximum clock rate is 75MHz
  - For async nand flash, support configurable interface timing , maximum data rate is 8bit/cycle

### 1.2.5 System Component

- CRU (clock & reset unit)

- Support clock gating control for individual components
- One oscillator with 24MHz clock input
- Support global soft-reset control for whole chip, also individual soft-reset for each component

- PMU(power management unit)
  - 3 separate voltage domains(VD_CORE/VD_LOGIC/VD_PMU)
  - 14 separate power domains, which can be power up/down by software based on different application scenes
  - Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control

- Timer
  - Six 64bits timers with interrupt-based operation for non-secure application
  - Two 64bits timers with interrupt-based operation for secure application
  - Support two operation modes: free-running and user-defined count
  - Support timer work state checkable

- PWM
  - Eight on-chip PWMs(PWM0~PWM7) with interrupt-based operation
  - Programmable pre-scaled operation to bus clock and then further scaled
  - Embedded 32-bit timer/counter facility
  - Support capture mode
  - Support continuous mode or one-shot mode
  - Provides reference mode and output various duty-cycle waveform
  - Optimized for IR application for PWM3 and PWM7

- Watchdog
  - 32-bit watchdog counter
  - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
  - WDT can perform two types of operations when timeout occurs:
    - Generate a system reset
    - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
  - Programmable reset pulse length
  - Totally 16 defined-ranges of main timeout period
  - One Watchdog for non-secure application
  - One Watchdog for secure application

- Interrupt Controller
  - Support 3 PPI interrupt source and 128 SPI interrupt sources input from different components
  - Support 16 software-triggered interrupts
  - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A35, both are low-level sensitive
  - Support different interrupt priority for each interrupt source, and they are always software-programmable

- DMAC
  - Micro-code programming based DMA
  - The specific instruction set provides flexibility for programming DMA transfers
  - Linked list DMA function is supported to complete scatter-gather transfer
  - Support internal instruction cache
  - Embedded DMA manager thread
  - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory

- Signals the occurrence of various DMA events using the interrupt output signals
- Mapping relationship between each channel and different interrupt outputs is software-programmable
- One embedded DMA controller for system
- DMAC features:
  - 8 channels totally
  - 23 hardware request from peripherals
  - 2 interrupt output
  - Dual APB slave interface for register configuration, designated as secure and non-secure
  - Support trustzone technology and programmable secure state for each DMA channel

- Secure system
  - TrustZone based Trusted Execution Environment (TEE) for the following components
    - Cortex-A35, support security and non-security mode, switch by software
    - System general DMAC, support some dedicated channels work only in security mode
    - Secure OTP, only can be accessed by Cortex-A35 in secure mode and secure key reader block
    - SYSTEM_SRAM, part of space is addressed only in security mode, detailed size is software-programmable together with TZMA (TrustZone memory adapter)
    - eight secure address space in DDR device, the start address and end address for each address scope is configurable, maximum 4GB secure address are supported
  - Cipher engine
    - Support SHA-1, SHA-256/224, SHA-512/384, MD5 with hardware padding
    - Support HMAC of SHA-1, SHA-256, SHA-512, MD5 with hardware padding
    - Support AES-128, AES-192, AES-256 encrypt & decrypt cipher
    - Support DES & TDES cipher
    - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
    - Support DES/TDES ECB/CBC/OFB/CFB mode
    - Support up to 4096 bits PKA mathematical operations for RSA/ECC
    - Support hardware key loader from secure OTP, which is not accessable by other devices, including Cort4ex-A35
  - Support data scrambling for DDR3/DDR3L/DDR4/LPDDR2/LPDDR3
  - Support up to 256 bits TRNG Output
  - Support secure OTP
  - Support secure boot
  - Support secure debug

### 1.2.6 Video CODEC

- Video Decoder
  - Real-time decoding of MPEG-4, H.264, H.265/HEVC, VP8, VC-1
  - H.264/AVC Base/Main/High@level4.2; up to 1080P@60fps
  - H.265/HEVC Main10 profile@level4.2; up to 1080P@60fps
  - VP8, up to 1080P@60fps
  - MPEG-4, ISO/IEC 14496-2, SP@L0-3, ASP@L0-5, up to 1080P@60fps
  - VC-1, SP@ML, MP@HL, AP@L0-3, up to 1080P@60fps
  - MVC is supported based on H.264 or H.265, up to 1080P@60fps

- Video Encoder
  - Support H.264 video encoder at BP/MP/HP@level4.1
  - Resolution and frame rate are up to 1920x1080@30FPS
  - 1x1080p@30fps or 2x720p@30fps encoding

### 1.2.7 JPEG CODEC

- JPEG decoder
  - Decoder size is from 48x48 to 8176x8176(66.8Mpixels)
  - Support JPEG ROI (region of image) decode

### 1.2.8 Graphics Engine

- 3D Graphics Engine:
  - Support DirectX 11 FL9_3
  - Support OpenGL ES 1.1, 2.0, and 3.2
  - Support Vulkan 1.0
  - Support OpenCL 2.0 Full Profile

- 2D Graphics Engine:
  - Data format
    - Support input of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Support input of YUV422SP10bit/YUV420SP10bit(YUV-8bits out)
    - Support output of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422
    - Pixel Format conversion, BT.601/BT.709
    - Dither operation
    - Max resolution: 8192x8192 source, 4096x4096 destination
  - Scaling
    - Down-scaling: Average filter
    - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
    - Arbitrary non-integer scaling ratio，from 1/8 to 8
  - Rotation
    - 0, 90, 180, 270 degree rotation
    - x-mirror, y-mirror& rotation operation
  - BitBLT
    - Block transfer
    - Color palette/Color fill, support with alpha
    - Transparency mode (color keying/stencil test, specified value/value range)
    - Two source BitBLT:
    - A+B=B only BitBLT, A support rotate&scale when B fixed
    - A+B=C second source (B) has same attribute with (C) plus rotation function
  - Alpha Blending
    - New comprehensive per-pixel alpha(color/alpha channel separately)
    - Fading
    - SRC1(R2Y)&&SRC0(YUV)—alpha->DST(YUV)

### 1.2.9 Video input interface

- Interface and video input processor
  - Support up to 12bit DPI interface (digital parallel input)
  - Support up MIPI CSI RX interface
  - Support VIP block(Video Input Processor)
  - Support ISP block(Image Signal Processor)
  - Support DPI interface to VIP block
  - Support DPI interface to ISP block
  - Support MIPI CSI RX interface to ISP block
  - Support the following two mode simultaneously
    - DPI interface with VIP
    - MIPI CSI RX interface with ISP

- DPI Interface
  - Support 8bit/10bit/12bit input

- Support up to 150MHz input data
- Support 12MHz/24MHz/48MHz/27MHz/37.125MHz/74.25MHz frequency for master clock output

- MIPI CSI RX Interface
  - Compatible with the MIPI Alliance Interface specification v1.0
  - Up to 4 data lane, 1.0Gbps maximum data rate per lane
  - Support MIPI-HS, MIPI-LP mode

- VIP
  - Support YCbCr422 8bit input
  - Support Raw 8bit/10bit/12bit input
  - Support CCIR656(PAL/NTSC) input
  - Support JPEG input
  - Support YCbCr422/420 output
  - Support UYVY/VYUY/YUYV/YVYU configurable
  - Support up to 8192x8192 resolution source
  - Support picture in picture
  - Support arbitrary size window crop

- ISP
  - Generic Sensor Interface with programmable polarity for synchronization signals
  - ITU-R BT 601/656 compliant video interface supporting YCbCr or RGB Bayer data
  - 12 bit camera interface
  - 12 bit resolution per color component internally
  - YCbCr 4:2:2 processing
  - Flash light control
  - Mechanical shutter support
  - Windowing and frame synchronization
  - Frame skip support for video (e.g. MPEG-4) encoding
  - Macro block line, frame end, capture error, data loss interrupts and sync. (h_start, v_start) interrupts
  - Luminance/chrominance and chrominance blue/red swapping for YUV input signals
  - Continuous resize support
  - Semi planar storage format
  - Color processing (contrast, saturation, brightness, hue, offset, range)
  - Power management by software controlled clock disabling of currently not needed sub-modules
  - Four channel Lens shade correction (Vignetting)
  - Auto focus measurement
  - White balancing and black level measurement
  - Auto exposure support by brightness measurement in 5x5 sub windows
  - Defect pixel cluster correction unit (DPCC) supports on the fly and table based pixel correction
  - De-noising pre filter (DPF)
  - Enhanced color interpolation (RGB Bayer demosaicing)
  - Chromatic aberration correction
  - Combined edge sensitive Sharpening / Blurring filter (Noise filter)
  - Color correction matrix (cross talk matrix)
  - Global Tone Mapping with wide dynamic range unit (WDR)
  - Image Stabilization support and Video Stabilization Measurement
  - Flexible Histogram calculation
  - Digital image effects (Emboss, Sketch, Sepia, B/W (Grayscale), Color Selection, Negative image, sharpening)
  - Solarize effect through gamma correction
  - Maximum input resolution of 3264x2448 pixels
  - Main scaler with pixel-accurate up- and down-scaling to any resolution between

3264x2448 and 32x16 pixel in processing mode
- Self scaler with pixel-accurate up- and down-scaling to any resolution between 1920x1080 and 32x16 pixel in processing mode
- Support of semiplanar NV21 color storage format
- Support of image cropping
- Support Y12BIT and UV 8BIT path output after GAMMAOUT module
- Support RGB output after GAMMAOUT module
- Support hurry for latency FIFO
- Support Two-in-one RK-Tone-Mapping with wide dynamic range unit (Block/Global WDR)
- Support Video Stabilization Measurement (VSM) Programming update to 3264x2448

### 1.2.10 Display interface

- Display interface
  - Support RGB Parallel Display interface
  - Support MIPI_DSI interface
  - Support LVDS interface
  - Support Parallel Display interface and MIPI_DSI display simultaneously
  - Support Parallel Display interface and LVDS display simultaneously
  - Support different or identical source for dual display interface

- RGB Parallel Display interface
  - Up to 1080p@60fps display output
  - Up to 24bit output data

- MIPI_DSI interface
  - Compatible with MIPI Alliance Interface specification v1.0
  - Support 4 data lane, 1.0Gbps maximum data rate per lane
  - Up to 1080p@60fps display output
  - Support HS and LP mode

- LVDS interface
  - Compliant with the TIA/EIA-644-A LVDS specification
  - Compliant with LVTTL IO, support direct RGB data output
  - Support RGB888 and RGB666 for LVDS interface
  - Support VESA/JEIDA LVDS data format transfer
  - Up to 1280x800@60fps

### 1.2.11 Big Video Output Processor (VOPB)

- Display interface
  - Parallel RGB LCD Interface: 24-bit(RGB888),18-bit(RGB666), 16-bit(RGB565)
  - Max output resolution
    - Up to 1920x1080 with CABC disable
    - Up to 1280x800 with CABC enable
- Display process
  - Background layer
    - programmable 24-bit color
  - Win0 layer
    - Input format : RGB888, ARGB888, RGB565, YCbCr422, YCbCr420, YCbCr444
    - 1/8 to 8 scaling-down and scaling-up engine
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
    - RGB2YCbCr(BT601/BT709)

  - Win1 layer
    - Input format : RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YCbCr(BT601/BT709)
    - Support frame buffer data decompression
  - HWC layer
    - Support 8BPP only
    - Size : 32x32 or 64x64
    - 256 level alpha blending (pre-multiplied alpha support)
    - RGB2YCbCr(BT601/BT709)
- Others
  - Win0 layer , Win1 layer and Win2 layer overlay exchangeable
  - Support RGB or YUV domain overlay
  - BCSH(Brightness, Contrast, Saturation, Hue adjustment)
  - BCSH:YCbCr2RGB(rec601-mpeg/ rec601-jpeg/rec709)
  - BCSH:RGB2YCbCr(BT601/BT709)
  - Support Gamma adjust
  - Support CABC (Content Adaptive Backlight Control)
  - Support dither down allegro RGB888to666 RGB888to565 & dither down frc (configurable ) RGB888to666
  - Blank and black display
  - Standby mode

### 1.2.12 Little Video Output Processor(VOPL)

- Display interface
  - Parallel RGB LCD Interface: 24-bit(RGB888),18-bit(RGB666), 16-bit(RGB565)
  - Max output resolution
    - Up to 1920x1080
- Display process
  - Background layer
    - programmable 24-bit color
  - Win1 layer
    - Input format : RGB888, ARGB888, RGB565
    - Support virtual display
    - 256 level alpha blending (pre-multiplied alpha support)
    - Transparency color key
    - RGB2YCbCr(BT601/BT709)
- Others
  - Support RGB or YUV domain overlay
  - BCSH(Brightness, Contrast, Saturation, Hue adjustment)
  - BCSH:YCbCr2RGB(rec601-mpeg/rec601-jpeg/rec709)
  - BCSH:RGB2YCbCr(BT601/BT709)
  - Support Gamma adjust
  - Support dither down allegro RGB888to666 RGB888to565 & dither down for (configurable ) RGB888to666
  - Blank and black display
  - Standby mode

### 1.2.13 Audio Interface

- I2S0 with 8 channel
  - Up to 8 channels TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable

- Support 3 I2S formats (normal, left-justified, right-justified)
- Support 4 PCM formats (early, late1, late2, late3)
- I2S and PCM mode cannot be used at the same time

- I2S1/I2S2 with 2 channel
- Up to 2 channels for TX and 2 channels RX path
- Audio resolution from 16bits to 32bits
- Sample rate up to 192KHz
- Provides master and slave work mode, software configurable
- Support 3 I2S formats (normal, left-justified, right-justified)
- Support 4 PCM formats (early, late1, late2, late3)
- I2S and PCM cannot be used at the same time

- PDM
  - Up to 8 channels
  - Audio resolution from 16bits to 24bits
  - Sample rate up to 192KHz
  - Support PDM master receive mode

- TDM
  - supports up to 8 channels for TX and 8 channels RX path
  - Audio resolution from 16bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)

### 1.2.14 Connectivity

- SDIO interface
  - Compatible with SDIO3.0 protocol
  - 4bits data bus widths

- MAC 10/100 Ethernet Controller
  - Supports 10/100-Mbps data transfer rates with the RMII interfaces
  - Supports both full-duplex and half-duplex operation
  - Supports IEEE 802.1Q VLAN tag detection for reception frames
  - Support detection of LAN wake-up frames and AMD Magic Packet frames
  - Handles automatic retransmission of Collision frames for transmission

- USB 2.0 OTG
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode

- USB 2.0 Host
  - Compatible with USB 2.0 specification
  - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
  - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
  - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a

- SPI interface
  - Support two SPI Controller, one support one chip-select output and the other support two chip-select output
  - Support serial-master and serial-slave mode, software-configurable

- I2C interface
  - Support four I2C interface(I2C0/I2C1/I2C2/I2C3)
  - Support 7bits and 10bits address mode

- Software programmable clock frequency
- Data on the I2C-bus can be transferred at rates of up to 100 kbit/s in the Standard-mode, up to 400 kbit/s in the Fast-mode or up to 1 Mbit/s in Fast-mode Plus.

- UART Controller
  - Support six UART interface(UART0/UART1/UART2/UART3/UART4/UART5)
  - Embedded two 64-byte FIFO for TX and RX operation respectively
  - Support 5bit,6bit,7bit,8bit serial data transmit or receive
  - Standard asynchronous communication bits such as start, stop and parity
  - Support different input clock for UART operation to get up to 4Mbps baud rate
  - Support auto flow control mode for UART0/UART1/UART3/UART4/UART5

### 1.2.15 Others

- Multiple group of GPIO
  - All of GPIOs can be used to generate interrupt to CPU
  - Support level trigger and edge trigger interrupt
  - Support configurable polarity of level trigger interrupt
  - Support configurable rising edge, falling edge and both edge trigger interrupt

- Temperature Sensor(TS-ADC)
  - Up to 50KS/s sampling rate
  - Support two temperature sensor
  - -20~120℃ temperature range and 5℃ temperature resolution

- Successive Approximation ADC (SARADC)
  - 10-bit resolution
  - Up to 1MS/s sampling rate
  - 3 single-ended input channels

- OTP
  - Support 4K bit Size, 3.5K bit for secure application
  - Support Program/Read/Idle mode

- Package Type
  - TFBGA418L (body: 14mm x 14mm; ball size: 0.3mm; ball pitch: 0.65mm)

*Notes:*

① *DDR3/DDR3L/LPDDR2/LPDDR3/DDR4 are not used simultaneously*



 

## 1.3 Block Diagram

The following diagram shows the basic block diagram.

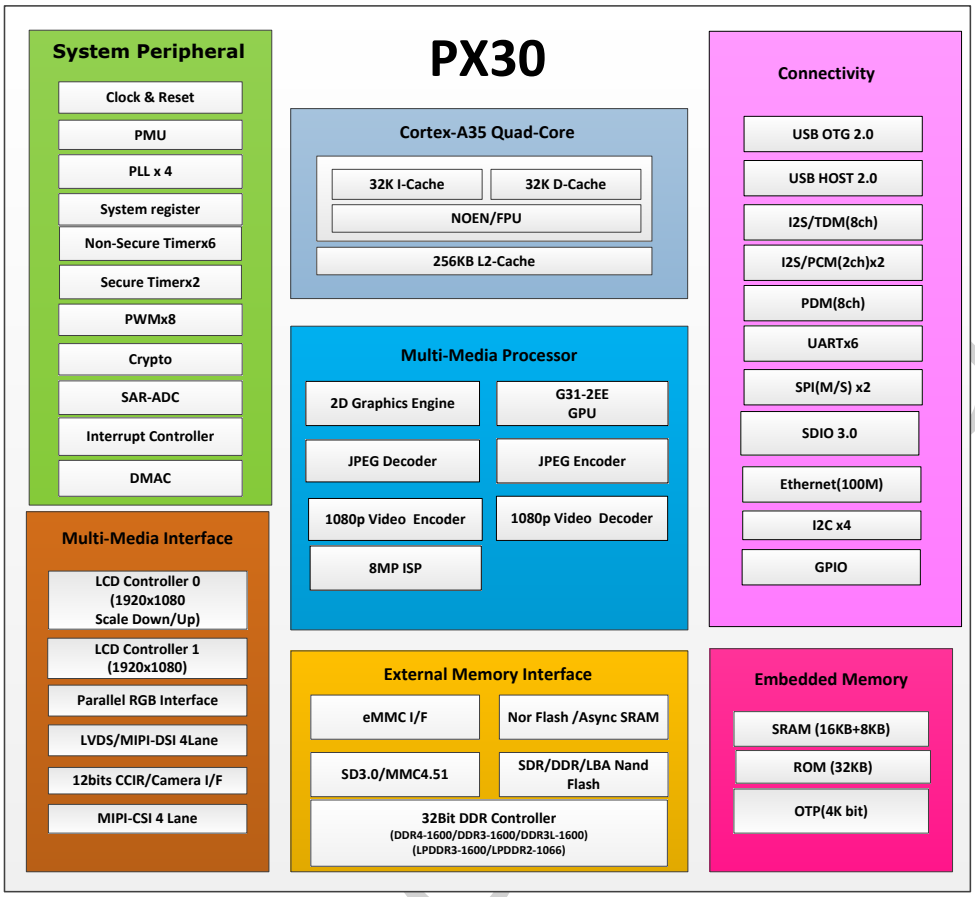


Fig.1-1 Block Diagram

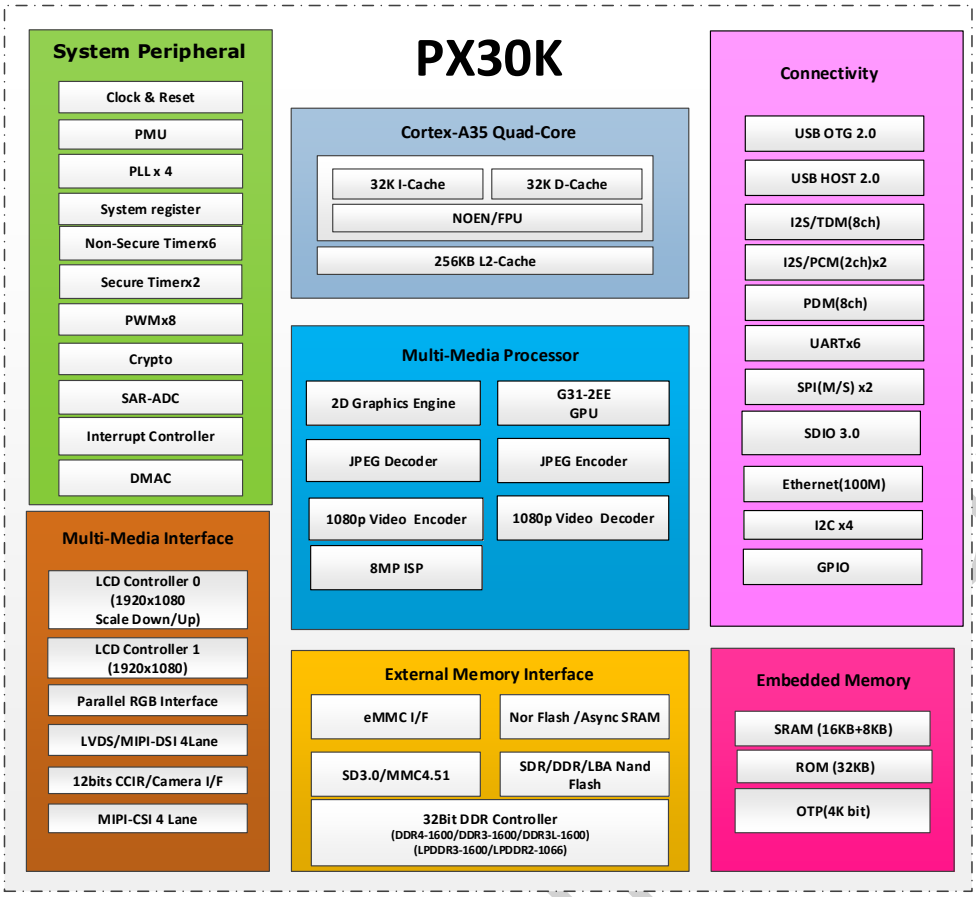


Fig.1-2 Block Diagram

# Chapter 2 Package Information

## 2.1 Order Information

| Orderable Device | RoHS status | Package | Package Qty | Device Feature |
|---|---|---|---|---|
| PX30 | RoHS | TFBGA418L | 1190 by tray | Quad core application processor |
| PX30K | RoHS | TFBGA418L | 1190 by tray | Quad core application processor for commercial application |

## 2.2 Top Marking

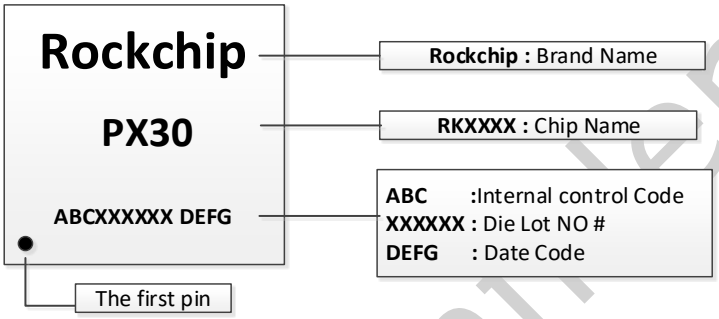


Fig.2-1 Package definition

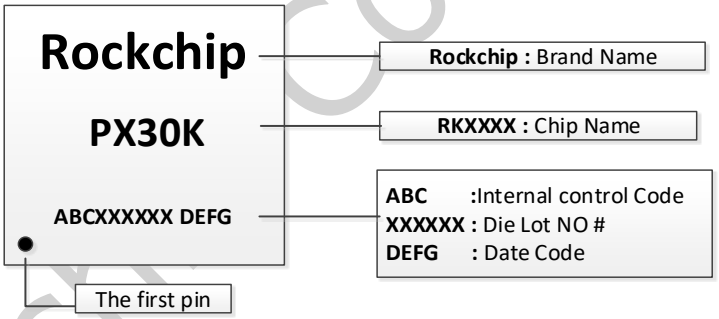


Fig.2-2 Package definition

## 2.3 TFBGA418LDimension

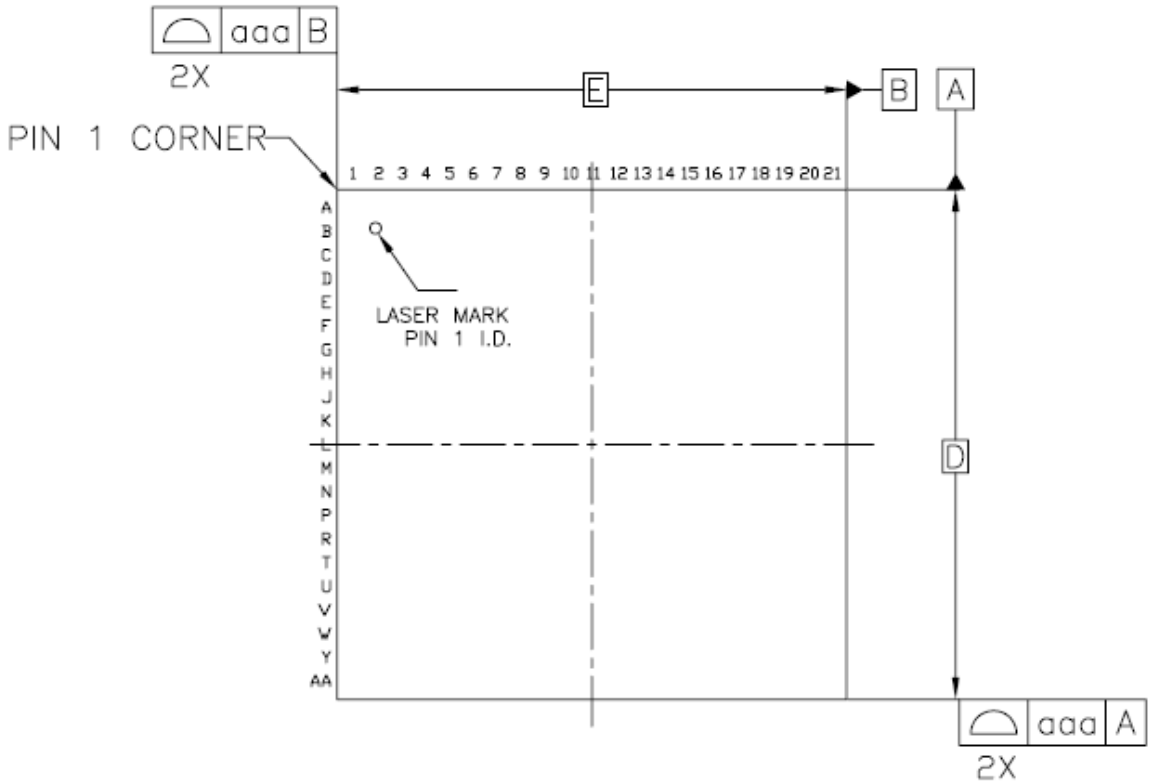


Fig.2-3 Package Top View

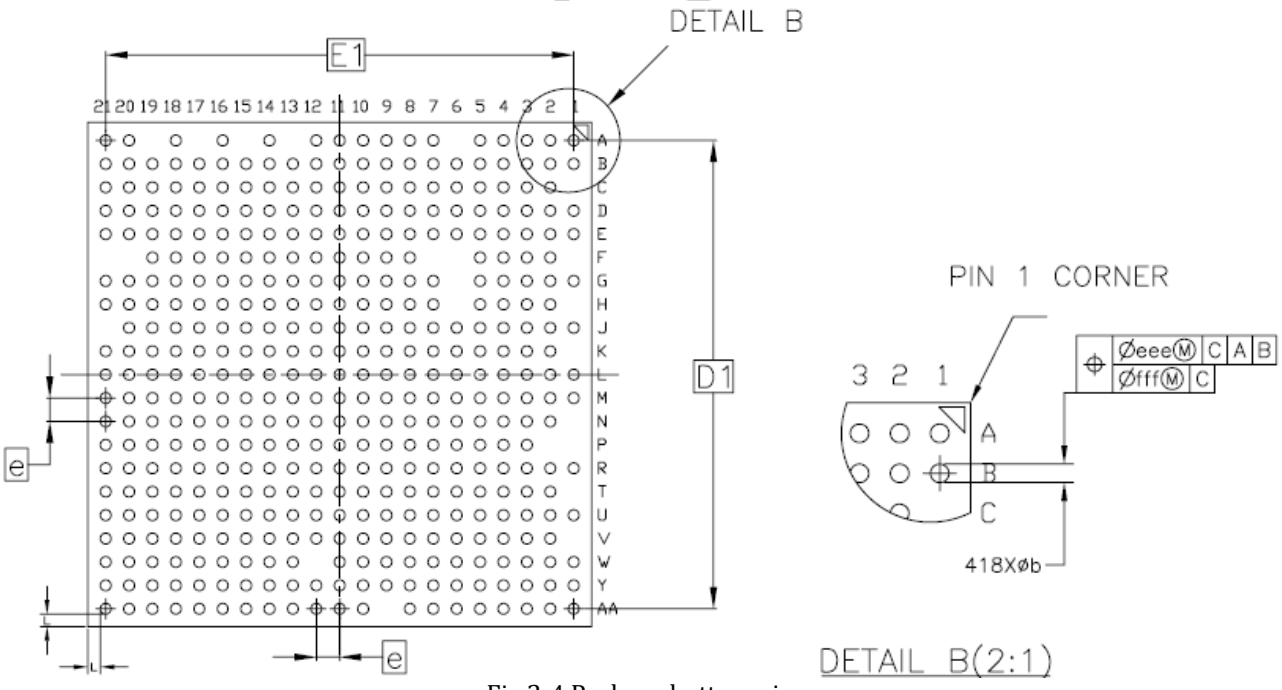


Fig.2-4 Package bottom view

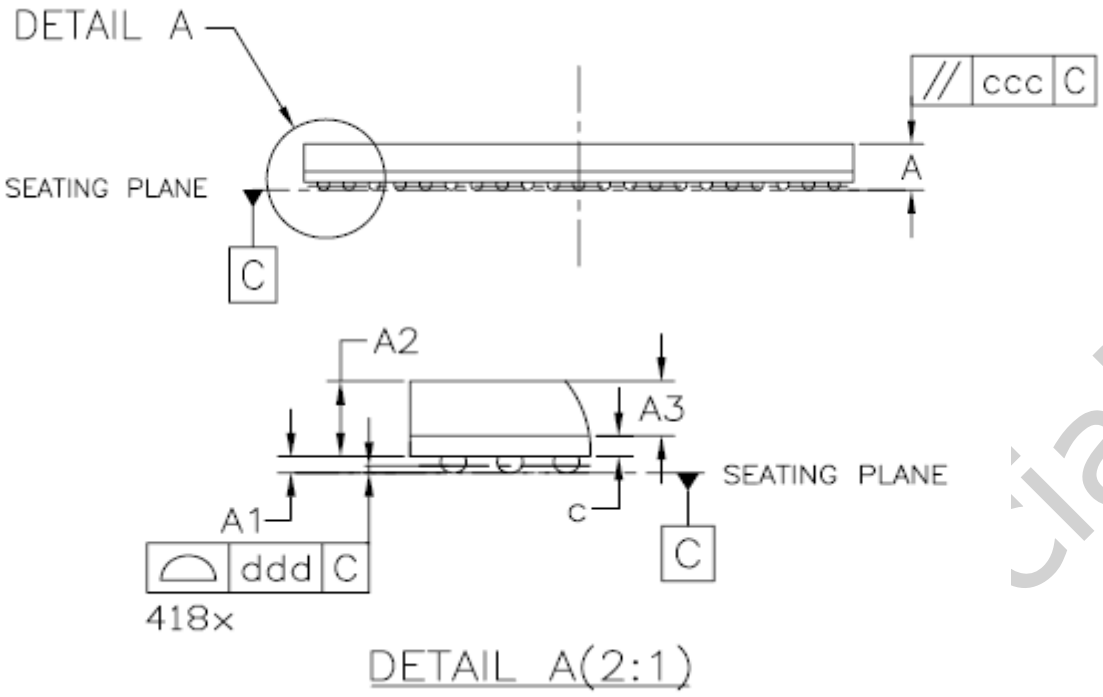


Fig.2-5 Package side view

| SYMBOL | MILLIMETER | | |
|---|---|---|---|
| | MIN | NOM | MAX |
| A | -- | 1.17 | 1.25 |
| A1 | 0.16 | 0.21 | 0.26 |
| A2 | 0.91 | 0.96 | 1.01 |
| A3 | 0.70 BASIC | | |
| c | 0.22 | 0.26 | 0.30 |
| D | 13.90 | 14.00 | 14.10 |
| D1 | 13.00 BASIC | | |
| E | 13.90 | 14.00 | 14.10 |
| E1 | 13.00 BASIC | | |
| e | 0.65 BASIC | | |
| b | 0.25 | 0.30 | 0.35 |
| L | 0.35 REF | | |
| aaa | 0.15 | | |
| ccc | 0.15 | | |
| ddd | 0.10 | | |
| eee | 0.15 | | |
| fff | 0.08 | | |

Fig.2-6 Package dimension

## 2.4 Ball Map

4
1
8

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | VSS_1 | DDR3_RESETN/DDR4_RESETN | DDR3_BA0/DDR4_BG0 | DDR3_A5/DDR4_A8 | DDR3_BA2/DDR4_BA0 | | DDR3_A14/DDR4_A1 | DDR3_A4/DDR4_A5 | DDR3_A12/DDR4_BA1 | DDR3_A10/DDR4_CS0N | VSS_5 | LVDS_TX3P/MIPI_TX_D3P/LCDC_DEN_M1 |
| B | DDR3_CLKN/DDR4_CLKN | DDR3_CLKP/DDR4_CLKP | DDR3_CSN0/DDR4_ACTN | DDR3_A7/DDR4_A11 | DDR3_A3/DDR4_A6 | VSS_6 | DDR3_A11/DDR4_A3 | DDR3_A6/DDR4_A7 | VSS_7 | DDR3_BA1/DDR4_CASN/DDR4_A15 | DDR3_CKE/DDR4_RASN/DDR4_A16 | LVDS_TX3N/MIPI_TX_D3N/LCDC_HSYNC_M1 |
| C | | DDR_DQ26 | VSS_8 | DDR3_RASN/DDR4_CKE | VSS_9 | DDR3_A9/DDR4_A0 | DDR3_A0/DDR4_A10 | DDR3_WEN/DDR4_BG1 | DDR3_A15/DDR4_ODT0 | DDR3_A8/DDR4_A13 | DDR3_ODT1/DDR4_ODT1 | VSS_10 |
| D | DDR_DQ30 | DDR_DQ27 | VSS_11 | VSS_12 | DDR3_ODT0/DDR4_WEN/DDR4_A14 | DDR3_A13/DDR4_A2 | VSS_13 | DDR3_A2/DDR4_A4 | DDR3_CASN/DDR4_A12 | DDR3_A1/DDR4_A9 | DDR3_CSN1/DDR4_CS1N | VCCIO4 |
| E | DDR_DQ31 | DDR_DQ22 | VSS_14 | VSS_15 | VSS_16 | VSS_17 | VSS_18 | VSS_19 | VSS_20 | VSS_21 | VSS_24 | MIPI_DSI_VCCA_3V3 |
| F | | VSS_22 | DDR_DQ18 | DDR_DQ16 | VSS_23 | | | DDRIO_VDD_1 | DDRIO_VDD_2 | DDRIO_VDD_3 | MIPI_DSI_VCCA_1V0 | MIPI_DSI_VCCA_1V8 |
| G | DDR_DQS3_N | DDR_DQS3_P | DDR_DQ17 | DDR_DM2 | VSS_28 | | VSS_29 | VSS_30 | DDRIO_VDD_4 | DDRIO_VDD_5 | VSS_31 | LVDS_RBIAS |
| H | | VSS_37 | VSS_38 | VSS_39 | VSS_40 | | VSS_41 | VSS_42 | VSS_43 | VSS_44 | VSS_45 | VSS_46 |
| J | DDR_DQS2_N | DDR_DQS2_P | DDR_DQ29 | DDR_DQ25 | VSS_49 | DDRIO_VDD_6 | DDRIO_VDD_7 | VSS_50 | VSS_51 | VSS_52 | VSS_53 | VSS_54 |
| K | | DDR_DQ19 | DDR_DQ24 | DDR_DQ28 | VSS_58 | DDRIO_VDD_8 | DDRIO_VDD_9 | VSS_59 | LOGIC_VDD_1 | LOGIC_VDD_3 | VSS_61 | VSS_63 |

Fig.2-7 Ball Map-1

| 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | |
|---|---|---|---|---|---|---|---|---|---|
| | LVDS_CLKP/MIPI_TX_CLKP/LCDC_D3_M1 | | LVDS_TX1P/MIPI_TX_D1P/LCDC_D10_M1 | | GPIO3_C5/LCDC_D17/PWM7/I2S0_8CH_SDI0/TDM_SDI | | GPIO3_C0/LCDC_D12/I2S0_8CH_SDO1 | VSS_2 | A |
| LVDS_TX2P/MIPI_TX_D2P/LCDC_D5_M1 | LVDS_CLKN/MIPI_TX_CLKN/LCDC_D4_M1 | LVDS_TX1N/MIPI_TX_D1N/LCDC_D1_M1 | LVDS_TX0N/MIPI_TX_D0N/LCDC_D11_M1 | LVDS_TX0P/MIPI_TX_D0P/LCDC_D8_M1 | GPIO3_B2/LCDC_D6/SPI1_CSN1 | GPIO3_C3/LCDC_D15/PWM5/I2S0_8CH_SCLKTX/TDM_SCLK | GPIO3_C1/LCDC_D13/I2S0_8CH_MCLK | GPIO1_A7/FLASH_D7/EMMC_D7 | B |
| LVDS_TX2N/MIPI_TX_D2N/LCDC_VSYNC_M1 | GPIO3_A6/LCDC_D2 | GPIO3_A4/LCDC_D0 | GPIO3_B5/LCDC_D9_M0/I2S0_8CH_LRCKRX | GPIO3_B3/LCDC_D7/I2S0_8CH_SDI1 | GPIO3_C4/LCDC_D16/PWM6/I2S0_8CH_SDO0/TDM_SDO | GPIO3_C2/LCDC_D14/PWM4/I2S0_8CH_LRCKTX/TDM_FSYNC | GPIO1_A6/FLASH_D6/EMMC_D6 | GPIO1_A2/FLASH_D2/EMMC_D2/SFC_SIO2 | C |
| GPIO3_C6/LCDC_D18/CIF_D10_M1/PDM_CLK0_M0 | GPIO3_C7/LCDC_D19/CIF_D11_M1/PDM_CLK1 | GPIO3_D0/LCDC_D20/CIF_CLKOUT_M1/PDM_SDI1 | GPIO3_D1/LCDC_D21/CIF_VSYNC_M1/PDM_SDI2/ISP_PRELIGHT_TRIG | GPIO3_D2/LCDC_D22/CIF_HREF_M1/PDM_SDI3/ISP_FLASH_TRIGOUT | GPIO3_D3/LCDC_D23/CIF_CLKIN_M1/PDM_SDI0_M0/ISP_FLASH_TRIGIN | GPIO3_A0/LCDC_CLK | GPIO1_A5/FLASH_D5/EMMC_D5 | GPIO1_A1/FLASH_D1/EMMC_D1/SFC_SIO1 | D |
| GPIO3_A1/LCDC_HSYNC_M0/CIF_D0_M1/I2S2_2CH_MCLK/UART5_RX | GPIO3_A3/LCDC_DEN_M0/CIF_D2_M1/I2S2_2CH_LRCK_TXRX/UART5_CTS | GPIO3_A5/LCDC_D1_M0/CIF_D3_M1/I2S2_2CH_SDI/UART5_RTS | GPIO3_A7/LCDC_D3_M0/CIF_D4_M1/I2S2_2CH_SDO | GPIO3_B0/LCDC_D4_M0/CIF_D5_M1/I2S0_8CH_SDI3 | GPIO1_B3/FLASH_ALE/EMMC_RSTN | GPIO1_A3/FLASH_D3/EMMC_D3/SFC_SIO3 | GPIO1_A0/FLASH_D0/EMMC_D0/SFC_SIO0 | GPIO1_A4/FLASH_D4/EMMC_D4/SFC_CSN0 | E |
| GPIO3_A2/LCDC_VSYNC_M0/CIF_D1_M1/I2S2_2CH_SCLK/UART5_TX | VSS_25 | VSS_26 | VSS_27 | GPIO3_B1/LCDC_D5_M0/CIF_D6_M1/I2S0_8CH_SDI2/SPI1_CSN0 | GPIO3_B4/LCDC_D8_M0/CIF_D7_M1/I2S0_8CH_SCLKRX/SPI1_MOSI | GPIO1_B0/FLASH_CS0 | | | F |
| VSS_33 | VSS_34 | VSS_48 | VSS_47 | GPIO3_B7/LCDC_D11_M0/CIF_D9_M1/I2S0_8CH_SDO2/SPI1_CLK | GPIO3_B6/LCDC_D10_M0/CIF_D8_M1/I2S0_8CH_SDO3/SPI1_MISO | GPIO1_B2/FLASH_DQS/EMMC_CMD | GPIO1_B6/FLASH_CS1/UART3_TX_M1/SPI0_CSN | GPIO1_B4/FLASH_CLE/UART3_CTS_M1/SPI0_MOSI/I2C3_SDA | G |
| VSS_55 | CPU_VDD_1 | CPU_VDD_2 | CPU_VDD_3 | VSS_57 | GPIO1_B1/FLASH_RDY/EMMC_CLKOUT/SFC_CLK | GPIO1_C4/SDMMC1_CMD | GPIO1_B5/FLASH_WRN/UART3_RTS_M1/SPI0_MISO/I2C3_SCL | GPIO1_B7/FLASH_RDN/UART3_RX_M1/SPI0_CLK | H |
| VSS_64 | CPU_VDD_4 | CPU_VDD_5 | CPU_VDD_6 | VSS_56 | VCCIO6 | GPIO1_D1/SDMMC1_D3 | GPIO1_C0/UART1_RX | | J |
| VSS_65 | CPU_VDD_7 | CPU_VDD_8 | CPU_VDD_9 | VSS_67 | VSS_68 | VCCIO1 | GPIO1_C1/UART1_TX | GPIO1_C2/UART1_CTS | K |

Fig.2-8 Ball Map-2

| | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| L | DDR_DQ23 | DDR_DQ20 | VSS_70 | VSS_71 | VSS_72 | DDRIO_VDD_10 | DDRIO_VDD_11 | VSS_73 | LOGIC_VDD_2 | LOGIC_VDD_4 | LOGIC_VDD_9 | VSS_77 |
| M | DDR_DQ21 | DDR_DQ11 | DDR_DQ13 | DDR_DM3 | VSS_80 | DDRIO_VDD_12 | DDRIO_VDD_13 | VSS_81 | VSS_84 | VSS_85 | LOGIC_VDD_8 | VSS_62 |
| N | | DDR_DQ4 | VSS_89 | DDR_DQ15 | VSS_90 | VSS_91 | VSS_92 | VSS_93 | VSS_96 | VSS_97 | LOGIC_VDD_5 | LOGIC_VDD_7 |
| P | | | DDR_DQ9 | VSS_100 | VSS_101 | VSS_102 | VSS_103 | VSS_104 | VSS_105 | VSS_106 | VSS_107 | VSS_108 |
| R | DDR_DQ1 | DDR_DQ6 | DDR_DQ5 | DDR_DQ0 | VSS_113 | VSS_114 | VSS_115 | VSS_116 | VSS_117 | VSS_118 | VSS_119 | VSS_120 |
| T | | DDR_DM0 | VSS_126 | VSS_127 | VSS_128 | VSS_129 | VSS_130 | VSS_131 | VSS_132 | VSS_133 | VSS_134 | VSS_36 |
| U | DDR_DQS1_N | DDR_DQS1_P | DDR_DQ2 | DDR_D_M1 | VSS_141 | VCCIO3 | GPIO2_B7/CIF_D10_M0/I2C2_SCL | MIPI_CSI_VCCA_1V0 | MIPI_CSI_DP2 | MIPI_CSI_CLKN | MIPI_CSI_RBIAS | USB_AVDD_1V0 |
| V | | VSS_147 | DDR_DQ14 | DDR_DQ12 | VSS_148 | GPIO2_C0/CIF_D11_M0/I2C2_SDA | GPIO2_B5/PWM2 | MIPI_CSI_DN2 | MIPI_CSI_DP3 | MIPI_CSI_CLKP | MIPI_CSI_DN0 | GPIO2_B4/CIF_D0_M0/UART2_TX_M1 |
| W | DDR_DQS0_N | DDR_DQS0_P | VSS_32 | VSS_135 | GPIO2_A6/CIF_D8_M0/RMII_RXDV | GPIO2_B6/CIF_D1_M0/UART2_RX_M1 | GPIO2_A7/CIF_D9_M0/RMII_MDIO | MIPI_CSI_DN3 | MIPI_CSI_DN1 | MIPI_CSI_DP0 | VSS_35 | |
| Y | DDR_DQ7 | DDR_DQ3 | DDR_DQ10 | GPIO2_B0/CIF_VSYNC_M0 | GPIO2_B3/CIF_CLKO_M0/CLK_OUT_ETHERNET | GPIO2_A3/CIF_D5_M0/RMII_RXD0 | GPIO2_A5/CIF_D7_M0/RMII_RXER | GPIO2_A4/CIF_D6_M0/RMII_RXD1 | MIPI_CSI_DP1 | USB_OTG_DP | USB_ID | USB_HOST_DM |
| AA | VSS_4 | DDR_DQ8 | VSS_98 | GPIO2_B1/CIF_HREF_M0/RMII_MDC | GPIO2_A0/CIF_D2_M0/RMII_TXEN | GPIO2_B2/CIF_CLKI_M0/RMII_CLK | GPIO2_A2/CIF_D4_M0/RMII_TXD0 | GPIO2_A1/CIF_D3_M0/RMII_TXD1 | | USB_OTG_DM | USB_RBIAS | USB_HOST_DP |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 |

Fig.2-9 Ball Map-3

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| VSS_69 | VSS_66 | VSS_87 | VSS_88 | VSS_78 | VSS_79 | GPIO1_C7/SDMMC1_D1 | GPIO1_C6/SDMMC1_D0 | GPIO1_C3/UART1_RTS | L |
| VSS_60 | VSS_75 | VSS_82 | VSS_83 | VSS_86 | PLL_AVDD_1V8 | GPIO0_B7/PWM0/OTG_DRV | GPIO1_C5/SDMMC1_CLK | GPIO1_D0/SDMMC1_D2 | M |
| LOGIC_VDD_6 | VSS_74 | VSS_94 | VSS_95 | AVSS | PLL_AVDD_1V0 | GPIO0_B5/UART0_RTS/TEST_CLK1 | GPIO0_B2/UART0_TX | GPIO0_C0/UART3_TX_M0/PWM1 | N |
| VSS_109 | VSS_110 | VSS_112 | VSS_111 | PMU_VDD_1V0 | GPIO0_B3/UART0_RX | GPIO0_C1/UART3_RX_M0/PWM3 | GPIO0_C4/CLKIO_32K | GPIO0_B1/I2C0_SDA | P |
| VSS_121 | VSS_122 | VSS_123 | VSS_124 | VSS_125 | GPIO0_B4/UART0_CTS | GPIO0_B6/FLASH_VOLSEL | GPIO0_C3/I2C1_SDA/UART3_RTS_M0 | GPIO0_B0/I2C0_SCL | R |
| OTP_VCC_1V8 | VSS_136 | VSS_137 | VSS_138 | VSS_139 | VSS_140 | PMUIO2 | GPIO0_C2/I2C1_SCL/UART3_CTS_M0 | GPIO0_A5 | T |
| ADC_AVDD_1V8 | VSS_142 | VSS_143 | VSS_144 | VSS_145 | VSS_146 | PMUIO1 | OSC_24M_IN | OSC_24M_OUT | U |
| USB_AVDD_1V8 | ADC_IN0 | ADC_IN2 | VSS_149 | VSS_150 | VSS_151 | VSS_152 | GPIO0_A4/PMIC_SLEEP/TSADC_SHUT_M1 | GPIO0_A2 | V |
| USB_AVDD_3V3 | ADC_IN1 | GPIO2_C6/PDM_CLK0_M1 | VCCIO5 | VSS_99 | VSS_76 | NPOR | TVSS | GPIO0_A6/TSADC_SHUT_M0/TSADC_SHUTORG | W |
| USB_VBUS | GPIO2_C3/I2S1_2CH_MCLK | GPIO2_C4/I2S1_2CH_SDO | GPIO1_D7/SDMMC0_CMD/UART4_RTS | GPIO1_D6/SDMMC0_CLKO/UART4_CTS/TEST_CLKO | VCCIO2 | GPIO0_A7 | GPIO0_A1 | GPIO0_A0/REF_CLKO | Y |
| GPIO2_C5/I2S1_2CH_SDI/PDM_SDI0_M1 | GPIO2_C2/I2S1_2CH__SCLK | GPIO2_C1/I2S1_2CH_LRCK_TXRX | GPIO1_D5/SDMMC0_D3/UART4_TX/JTAG_TMS | GPIO1_D2/SDMMC0_D0/UART2_TX_M0 | GPIO1_D3/SDMMC0_D1/UART2_RX_M0 | GPIO1_D4/SDMMC0_D2/UART4_RX/JTAG_TCK | GPIO0_A3/SDMMC0_DETN | VSS_3 | AA |
| 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | - |

Fig.2-10 Ball Map-4

## 2.5 Pin Number Order

Table 2-1 Pin Number Order Information

| No. | Pin Name | No. | Pin Name |
|---|---|---|---|
| A1 | VSS_1 | K17 | VSS_67 |
| A2 | DDR3_RESETn/DDR4_RESETN | K18 | VSS_68 |
| A3 | DDR3_BA0/DDR4_BG0 | K19 | VCCIO1 |
| A4 | DDR3_A5/DDR4_A8 | K20 | GPIO1_C1/UART1_TX |
| A5 | DDR3_BA2/DDR4_BA0 | K21 | GPIO1_C2/UART1_CTS |
| A7 | DDR3_A14/DDR4_A1 | L1 | DDR_DQ23 |
| A8 | DDR3_A4/DDR4_A5 | L2 | DDR_DQ20 |
| A9 | DDR3_A12/DDR4_BA1 | L3 | VSS_70 |
| A10 | DDR3_A10/DDR4_CS0n | L4 | VSS_71 |
| A11 | VSS_5 | L5 | VSS_72 |
| A12 | LVDS_TX3P/MIPI_TX_D3P/LCDC_DEN_M1 | L6 | DDRIO_VDD_10 |
| A14 | LVDS_CLKP/MIPI_TX_CLKP/LCDC_D3_M1 | L7 | DDRIO_VDD_11 |
| A16 | LVDS_TX1P/MIPI_TX_D1P/LCDC_D10_M1 | L8 | VSS_73 |
| A18 | GPIO3_C5/LCDC_D17/PWM7/I2S0_8CH_SDI0/TDM_SDI | L9 | LOGIC_VDD_2 |
| A20 | GPIO3_C0/LCDC_D12/I2S0_8CH_SDO1 | L10 | LOGIC_VDD_4 |
| A21 | VSS_2 | L11 | LOGIC_VDD_9 |
| AA1 | VSS_4 | L12 | VSS_77 |
| AA2 | DDR_DQ8 | L13 | VSS_69 |
| AA3 | VSS_98 | L14 | VSS_66 |
| AA4 | GPIO2_B1/CIF_HREF_M0/RMII_MDC | L15 | VSS_87 |
| AA5 | GPIO2_A0/CIF_D2_M0/RMII_TXEN | L16 | VSS_88 |
| AA6 | GPIO2_B2/CIF_CLKI_M0/RMII_CLK | L17 | VSS_78 |
| AA7 | GPIO2_A2/CIF_D4_M0/RMII_TXD0 | L18 | VSS_79 |
| AA8 | GPIO2_A1/CIF_D3_M0/RMII_TXD1 | L19 | GPIO1_C7/SDMMC1_D1 |
| AA10 | USB_OTG_DM | L20 | GPIO1_C6/SDMMC1_D0 |
| AA11 | USB_RBIAS | L21 | GPIO1_C3/UART1_RTS |
| AA12 | USB_HOST_DP | M1 | DDR_DQ21 |
| AA13 | GPIO2_C5/I2S1_2CH_SDI/PDM_SDIO_M1 | M2 | DDR_DQ11 |
| AA14 | GPIO2_C2/I2S1_2CH__SCLK | M3 | DDR_DQ13 |
| AA15 | GPIO2_C1/I2S1_2CH_LRCK_TXRX | M4 | DDR_DM3 |
| AA16 | GPIO1_D5/SDMMC0_D3/UART4_TX/JTAG_TMS | M5 | VSS_80 |
| AA17 | GPIO1_D2/SDMMC0_D0/UART2_TX_M0 | M6 | DDRIO_VDD_12 |
| AA18 | GPIO1_D3/SDMMC0_D1/UART2_RX_M0 | M7 | DDRIO_VDD_13 |
| AA19 | GPIO1_D4/SDMMC0_D2/UART4_RX/JTAG_TCK | M8 | VSS_81 |
| AA20 | GPIO0_A3/SDMMC0_DETN | M9 | VSS_84 |
| AA21 | VSS_3 | M10 | VSS_85 |
| B1 | DDR3_CLKN/DDR4_CLKN | M11 | LOGIC_VDD_8 |
| B2 | DDR3_CLKP/DDR4_CLKP | M12 | VSS_62 |
| B3 | DDR3_CSN0/DDR4_ACTn | M13 | VSS_60 |
| B4 | DDR3_A7/DDR4_A11 | M14 | VSS_75 |

| No. | Pin Name | No. | Pin Name |
|---|---|---|---|
| B5 | DDR3_A3/DDR4_A6 | M15 | VSS_82 |
| B6 | VSS_6 | M16 | VSS_83 |
| B7 | DDR3_A11/DDR4_A3 | M17 | VSS_86 |
| B8 | DDR3_A6/DDR4_A7 | M18 | PLL_AVDD_1V8 |
| B9 | VSS_7 | M19 | GPIO0_B7/PWM0/OTG_DRV |
| B10 | DDR3_BA1/DDR4_CASn/DDR4_A15 | M20 | GPIO1_C5/SDMMC1_CLK |
| B11 | DDR3_CKE/DDR4_RASn/DDR4_A16 | M21 | GPIO1_D0/SDMMC1_D2 |
| B12 | LVDS_TX3N/MIPI_TX_D3N/LCDC_HSYNC_M1 | N2 | DDR_DQ4 |
| B13 | LVDS_TX2P/MIPI_TX_D2P/LCDC_D5_M1 | N3 | VSS_89 |
| B14 | LVDS_CLKN/MIPI_TX_CLKN/LCDC_D4_M1 | N4 | DDR_DQ15 |
| B15 | LVDS_TX1N/MIPI_TX_D1N/LCDC_D1_M1 | N5 | VSS_90 |
| B16 | LVDS_TX0N/MIPI_TX_D0N/LCDC_D11_M1 | N6 | VSS_91 |
| B17 | LVDS_TX0P/MIPI_TX_D0P/LCDC_D8_M1 | N7 | VSS_92 |
| B18 | GPIO3_B2/LCDC_D6/SPI1_CSN1 | N8 | VSS_93 |
| B19 | GPIO3_C3/LCDC_D15/PWM5/I2S0_8CH_SCLKTX /TDM_SCLK | N9 | VSS_96 |
| B20 | GPIO3_C1/LCDC_D13/I2S0_8CH_MCLK | N10 | VSS_97 |
| B21 | GPIO1_A7/FLASH_D7/EMMC_D7 | N11 | LOGIC_VDD_5 |
| C2 | DDR_DQ26 | N12 | LOGIC_VDD_7 |
| C3 | VSS_8 | N13 | LOGIC_VDD_6 |
| C4 | DDR3_RASn/DDR4_CKE | N14 | VSS_74 |
| C5 | VSS_9 | N15 | VSS_94 |
| C6 | DDR3_A9/DDR4_A0 | N16 | VSS_95 |
| C7 | DDR3_A0/DDR4_A10 | N17 | AVSS |
| C8 | DDR3_WEn/DDR4_BG1 | N18 | PLL_AVDD_1V0 |
| C9 | DDR3_A15/DDR4_ODT0 | N19 | GPIO0_B5/UART0_RTS/TEST_CLK1 |
| C10 | DDR3_A8/DDR4_A13 | N20 | GPIO0_B2/UART0_TX |
| C11 | DDR3_ODT1/DDR4_ODT1 | N21 | GPIO0_C0/UART3_TX_M0/PWM1 |
| C12 | VSS_10 | P3 | DDR_DQ9 |
| C13 | LVDS_TX2N/MIPI_TX_D2N/LCDC_VSYNC_M1 | P4 | VSS_100 |
| C14 | GPIO3_A6/LCDC_D2 | P5 | VSS_101 |
| C15 | GPIO3_A4/LCDC_D0 | P6 | VSS_102 |
| C16 | GPIO3_B5/LCDC_D9_M0/I2S0_8CH_LRCKRX | P7 | VSS_103 |
| C17 | GPIO3_B3/LCDC_D7/I2S0_8CH_SDI1 | P8 | VSS_104 |
| C18 | GPIO3_C4/LCDC_D16/PWM6/I2S0_8CH_SDO0/T DM_SDO | P9 | VSS_105 |
| C19 | GPIO3_C2/LCDC_D14/PWM4/I2S0_8CH_LRCKTX /TDM_FSYNC | P10 | VSS_106 |
| C20 | GPIO1_A6/FLASH_D6/EMMC_D6 | P11 | VSS_107 |
| C21 | GPIO1_A2/FLASH_D2/EMMC_D2/SFC_SIO2 | P12 | VSS_108 |
| D1 | DDR_DQ30 | P13 | VSS_109 |
| D2 | DDR_DQ27 | P14 | VSS_110 |
| D3 | VSS_11 | P15 | VSS_112 |
| D4 | VSS_12 | P16 | VSS_111 |

| No. | Pin Name | No. | Pin Name |
|---|---|---|---|
| D5 | DDR3_ODT0/DDR4_Wen/DDR4_A14 | P17 | PMU_VDD_1V0 |
| D6 | DDR3_A13/DDR4_A2 | P18 | GPIO0_B3/UART0_RX |
| D7 | VSS_13 | P19 | GPIO0_C1/UART3_RX_M0/PWM3 |
| D8 | DDR3_A2/DDR4_A4 | P20 | GPIO0_C4/CLKIO_32K |
| D9 | DDR3_CASn/DDR4_A12 | P21 | GPIO0_B1/I2C0_SDA |
| D10 | DDR3_A1/DDR4_A9 | R1 | DDR_DQ1 |
| D11 | DDR3_CSN1/DDR4_CS1N | R2 | DDR_DQ6 |
| D12 | VCCIO4 | R3 | DDR_DQ5 |
| D13 | GPIO3_C6/LCDC_D18/CIF_D10_M1/PDM_CLK0_M0 | R4 | DDR_DQ0 |
| D14 | GPIO3_C7/LCDC_D19/CIF_D11_M1/PDM_CLK1 | R5 | VSS_113 |
| D15 | GPIO3_D0/LCDC_D20/CIF_CLKOUT_M1/PDM_SDI1 | R6 | VSS_114 |
| D16 | GPIO3_D1/LCDC_D21/CIF_VSYNC_M1/PDM_SDI2/ISP_PRELIGHT_TRIG | R7 | VSS_115 |
| D17 | GPIO3_D2/LCDC_D22/CIF_HREF_M1/PDM_SDI3/ISP_FLASH_TRIGOUT | R8 | VSS_116 |
| D18 | GPIO3_D3/LCDC_D23/CIF_CLKIN_M1/PDM_SDI0_M0/ISP_FLASH_TRIGIN | R9 | VSS_117 |
| D19 | GPIO3_A0/LCDC_CLK | R10 | VSS_118 |
| D20 | GPIO1_A5/FLASH_D5/EMMC_D5 | R11 | VSS_119 |
| D21 | GPIO1_A1/FLASH_D1/EMMC_D1/SFC_SIO1 | R12 | VSS_120 |
| E1 | DDR_DQ31 | R13 | VSS_121 |
| E2 | DDR_DQ22 | R14 | VSS_122 |
| E3 | VSS_14 | R15 | VSS_123 |
| E4 | VSS_15 | R16 | VSS_124 |
| E5 | VSS_16 | R17 | VSS_125 |
| E6 | VSS_17 | R18 | GPIO0_B4/UART0_CTS |
| E7 | VSS_18 | R19 | GPIO0_B6/FLASH_VOLSEL |
| E8 | VSS_19 | R20 | GPIO0_C3/I2C1_SDA/UART3_RTS_M0 |
| E9 | VSS_20 | R21 | GPIO0_B0/I2C0_SCL |
| E10 | VSS_21 | T2 | DDR_D_m0 |
| E11 | VSS_24 | T3 | VSS_126 |
| E12 | MIPI_DSI_VCCA_3V3 | T4 | VSS_127 |
| E13 | GPIO3_A1/LCDC_HSYNC_M0/CIF_D0_M1/I2S2_2CH_MCLK/UART5_RX | T5 | VSS_128 |
| E14 | GPIO3_A3/LCDC_DEN_M0/CIF_D2_M1/I2S2_2CH_LRCK_TXRX/UART5_CTS | T6 | VSS_129 |
| E15 | GPIO3_A5/LCDC_D1_M0/CIF_D3_M1/I2S2_2CH_SDI/UART5_RTS | T7 | VSS_130 |
| E16 | GPIO3_A7/LCDC_D3_M0/CIF_D4_M1/I2S2_2CH_SDO | T8 | VSS_131 |
| E17 | GPIO3_B0/LCDC_D4_M0/CIF_D5_M1/I2S0_8CH_SDI3 | T9 | VSS_132 |
| E18 | GPIO1_B3/FLASH_ALE/EMMC_RSTN | T10 | VSS_133 |

| No. | Pin Name | No. | Pin Name |
|---|---|---|---|
| E19 | GPIO1_A3/FLASH_D3/EMMC_D3/SFC_SIO3 | T11 | VSS_134 |
| E20 | GPIO1_A0/FLASH_D0/EMMC_D0/SFC_SIO0 | T12 | VSS_36 |
| E21 | GPIO1_A4/FLASH_D4/EMMC_D4/SFC_CSN0 | T13 | OTP_VCC_1V8 |
| F2 | VSS_22 | T14 | VSS_136 |
| F3 | DDR_DQ18 | T15 | VSS_137 |
| F4 | DDR_DQ16 | T16 | VSS_138 |
| F5 | VSS_23 | T17 | VSS_139 |
| F8 | DDRIO_VDD_1 | T18 | VSS_140 |
| F9 | DDRIO_VDD_2 | T19 | PMUIO2 |
| F10 | DDRIO_VDD_3 | T20 | GPIO0_C2/I2C1_SCL/UART3_CTS_M0 |
| F11 | MIPI_DSI_VCCA_1V0 | T21 | GPIO0_A5 |
| F12 | MIPI_DSI_VCCA_1V8 | U1 | DDR_DQS1_N |
| F13 | GPIO3_A2/LCDC_VSYNC_M0/CIF_D1_M1/I2S2_2CH_SCLK/UART5_TX | U2 | DDR_DQS1_P |
| F14 | VSS_25 | U3 | DDR_DQ2 |
| F15 | VSS_26 | U4 | DDR_D_M1 |
| F16 | VSS_27 | U5 | VSS_141 |
| F17 | GPIO3_B1/LCDC_D5_M0/CIF_D6_M1/I2S0_8CH_SDI2/SPI1_CSN0 | U6 | VCCIO3 |
| F18 | GPIO3_B4/LCDC_D8_M0/CIF_D7_M1/I2S0_8CH_SCLKRX/SPI1_MOSI | U7 | GPIO2_B7/CIF_D10_M0/I2C2_SCL |
| F19 | GPIO1_B0/FLASH_CS0 | U8 | MIPI_CSI_VCCA_1V0 |
| G1 | DDR_DQS3_N | U9 | MIPI_CSI_DP2 |
| G2 | DDR_DQS3_P | U10 | MIPI_CSI_CLKN |
| G3 | DDR_DQ17 | U11 | MIPI_CSI_RBIAS |
| G4 | DDR_DM2 | U12 | USB_AVDD_1V0 |
| G5 | VSS_28 | U13 | ADC_AVDD_1V8 |
| G7 | VSS_29 | U14 | VSS_142 |
| G8 | VSS_30 | U15 | VSS_143 |
| G9 | DDRIO_VDD_4 | U16 | VSS_144 |
| G10 | DDRIO_VDD_5 | U17 | VSS_145 |
| G11 | VSS_31 | U18 | VSS_146 |
| G12 | LVDS_RBIAS | U19 | PMUIO1 |
| G13 | VSS_33 | U20 | OSC_24M_IN |
| G14 | VSS_34 | U21 | OSC_24M_OUT |
| G15 | VSS_48 | V2 | VSS_147 |
| G16 | VSS_47 | V3 | DDR_DQ14 |
| G17 | GPIO3_B7/LCDC_D11_M0/CIF_D9_M1/I2S0_8CH_SDO2/SPI1_CLK | V4 | DDR_DQ12 |
| G18 | GPIO3_B6/LCDC_D10_M0/CIF_D8_M1/I2S0_8CH_SDO3/SPI1_MISO | V5 | VSS_148 |
| G19 | GPIO1_B2/FLASH_DQS/EMMC_CMD | V6 | GPIO2_C0/CIF_D11_M0/I2C2_SDA |
| G20 | GPIO1_B6/FLASH_CS1/UART3_TX_M1/SPI0_CSN | V7 | GPIO2_B5/PWM2 |

| No. | Pin Name | No. | Pin Name |
|---|---|---|---|
| G21 | GPIO1_B4/FLASH_CLE/UART3_CTS_M1/SPI0_MOSI/I2C3_SDA | V8 | MIPI_CSI_DN2 |
| H2 | VSS_37 | V9 | MIPI_CSI_DP3 |
| H3 | VSS_38 | V10 | MIPI_CSI_CLKP |
| H4 | VSS_39 | V11 | MIPI_CSI_DN0 |
| H5 | VSS_40 | V12 | GPIO2_B4/CIF_D0_M0/UART2_TX_M1 |
| H7 | VSS_41 | V13 | USB_AVDD_1V8 |
| H8 | VSS_42 | V14 | ADC_IN0 |
| H9 | VSS_43 | V15 | ADC_IN2 |
| H10 | VSS_44 | V16 | VSS_149 |
| H11 | VSS_45 | V17 | VSS_150 |
| H12 | VSS_46 | V18 | VSS_151 |
| H13 | VSS_55 | V19 | VSS_152 |
| H14 | CPU_VDD_1 | V20 | GPIO0_A4/PMIC_SLEEP/TSADC_SHUT_M1 |
| H15 | CPU_VDD_2 | V21 | GPIO0_A2 |
| H16 | CPU_VDD_3 | W1 | DDR_DQS0_N |
| H17 | VSS_57 | W2 | DDR_DQS0_P |
| H18 | GPIO1_B1/FLASH_RDY/EMMC_CLKOUT/SFC_CLK | W3 | VSS_32 |
| H19 | GPIO1_C4/SDMMC1_CMD | W4 | VSS_135 |
| H20 | GPIO1_B5/FLASH_WRN/UART3_RTS_M1/SPI0_MISO/I2C3_SCL | W5 | GPIO2_A6/CIF_D8_M0/RMII_RXDV |
| H21 | GPIO1_B7/FLASH_RDN/UART3_RX_M1/SPI0_CLK | W6 | GPIO2_B6/CIF_D1_M0/UART2_RX_M1 |
| J1 | DDR_DQS2_N | W7 | GPIO2_A7/CIF_D9_M0/RMII_MDIO |
| J2 | DDR_DQS2_P | W8 | MIPI_CSI_DN3 |
| J3 | DDR_DQ29 | W9 | MIPI_CSI_DN1 |
| J4 | DDR_DQ25 | W10 | MIPI_CSI_DP0 |
| J5 | VSS_49 | W11 | VSS_35 |
| J6 | DDRIO_VDD_6 | W13 | USB_AVDD_3V3 |
| J7 | DDRIO_VDD_7 | W14 | ADC_IN1 |
| J8 | VSS_50 | W15 | GPIO2_C6/PDM_CLK0_M1 |
| J9 | VSS_51 | W16 | VCCIO5 |
| J10 | VSS_52 | W17 | VSS_99 |
| J11 | VSS_53 | W18 | VSS_76 |
| J12 | VSS_54 | W19 | NPOR |
| J13 | VSS_64 | W20 | TVSS |
| J14 | CPU_VDD_4 | W21 | GPIO0_A6/TSADC_SHUT_M0/TSADC_SHUTORG |
| J15 | CPU_VDD_5 | Y1 | DDR_DQ7 |
| J16 | CPU_VDD_6 | Y2 | DDR_DQ3 |
| J17 | VSS_56 | Y3 | DDR_DQ10 |
| J18 | VCCIO6 | Y4 | GPIO2_B0/CIF_VSYNC_M0 |
| J19 | GPIO1_D1/SDMMC1_D3 | Y5 | GPIO2_B3/CIF_CLKO_M0/CLK_OUT_ETHERNET |
| J20 | GPIO1_C0/UART1_RX | Y6 | GPIO2_A3/CIF_D5_M0/RMII_RXD0 |

| No. | Pin Name | No. | Pin Name |
|---|---|---|---|
| K2 | DDR_DQ19 | Y7 | GPIO2_A5/CIF_D7_M0/RMII_RXER |
| K3 | DDR_DQ24 | Y8 | GPIO2_A4/CIF_D6_M0/RMII_RXD1 |
| K4 | DDR_DQ28 | Y9 | MIPI_CSI_DP1 |
| K5 | VSS_58 | Y10 | USB_OTG_DP |
| K6 | DDRIO_VDD_8 | Y11 | USB_ID |
| K7 | DDRIO_VDD_9 | Y12 | USB_HOST_DM |
| K8 | VSS_59 | Y13 | USB_VBUS |
| K9 | LOGIC_VDD_1 | Y14 | GPIO2_C3/I2S1_2CH_MCLK |
| K10 | LOGIC_VDD_3 | Y15 | GPIO2_C4/I2S1_2CH_SDO |
| K11 | VSS_61 | Y16 | GPIO1_D7/SDMMC0_CMD/UART4_RTS |
| K12 | VSS_63 | Y17 | GPIO1_D6/SDMMC0_CLKO/UART4_CTS/TEST_CLKO |
| K13 | VSS_65 | Y18 | VCCIO2 |
| K14 | CPU_VDD_7 | Y19 | GPIO0_A7 |
| K15 | CPU_VDD_8 | Y20 | GPIO0_A1 |
| K16 | CPU_VDD_9 | Y21 | GPIO0_A0/REF_CLKO |

## 2.6 Power/Ground IO Description

Table 2-2 Power/Ground IO information

| Group | Ball# | Descriptions |
|---|---|---|
| VSS | A1 A11 A21 AA1 AA21 AA3 B6 B9 C12 C3 C5 D3 D4 D7 E10 E11 E3 E4 E5 E6 E7 E8 E9 F14 F15 F16 F2 F5 G11 G13 G14 G15 G16 G5 G7 G8 H10 H11 H12 H13 H17 H2 H3 H4 H5 H7 H8 H9 J10 J11 J12 J13 J17 J5 J8 J9 K11 K12 K13 K17 K18 K5 K8 L12 L13 L14 L15 L16 L17 L18 L3 L4 L5 L8 M10 M12 M13 M14 M15 M16 M17 M5 M8 M9 N10 N14 N15 N16 N3 N5 N6 N7 N8 N9 P10 P11 P12 P13 P14 P15 P16 P4 P5 P6 P7 P8 P9 R10 R11 R12 R13 R14 R15 R16 R17 R5 R6 R7 R8 R9 T10 T11 T12 T14 T15 T16 T17 T18 T3 T4 T5 T6 T7 T8 T9 U14 U15 U16 U17 U18 U5 V16 V17 V18 V19 V2 V5 W11 W17 W18 W20 W3 W4 | Internal Core Ground,<br>Digital IO Ground, |
| AVSS | N17 | Analog Ground |
| | | |
| CPU_VDD | H14 H15 H16 J14 J15 J16 K14 K15 K16 | ARM Core Power |
| LOGIC_VDD | K9 K10 L9 L10 L11 M11 N11 N12 N13 | GPU, Logic Power |
| PMU_VDD_1V0 | P17 | PMU digital Power |
| | | |
| VCCIO1 | K19 | VCCIO1 Power Domain Power |

| Group | Ball# | Descriptions |
|---|---|---|
| VCCIO2 | Y18 | VCCIO2 Power Domain Power |
| VCCIO3 | U6 | VCCIO3 Power Domain Power |
| VCCIO4 | D12 | VCCIO4 Power Domain Power |
| VCCIO5 | W16 | VCCIO5 Power Domain Power |
| VCCIO6 | J18 | VCCIO6 Power Domain Power |
| PMUIO1 | U19 | PMU VCCIO1 Power Domain Power |
| PMUIO2 | T19 | PMU VCCIO2 Power Domain Power |
| | | |
| DDRIO_VDD | F8 F9 F10 G9 G10 J6 J7 K6 K7 L6 L7 M6 M7 | DDR PHY Power |
| | | |
| PLL_AVDD_1V0 | N18 | PLL Analog Power |
| PLL_AVDD_1V8 | M18 | PLL Analog Power |
| | | |
| USB_AVDD_1V0 | U12 | USB OTG2.0/Host2.0 Digital Power |
| USB_AVDD_1V8 | V13 | USB OTG2.0/Host2.0 Analog Power |
| USB_AVDD_3V3 | W13 | USB OTG2.0/Host2.0 Analog Power |
| | | |
| MIPI_DSI_VCCA_1V0 | F11 | MIPI DSI TX Analog Power |
| MIPI_DSI_VCCA _1V8 | F12 | MIPI DSI TX Analog Power |
| MIPI_DSI_VCCA _3V3 | E12 | MIPI DSI TX Analog Power |
| | | |
| MIPI_CSI_VCCA_1V0 | U8 | MIPI CSI RX Analog Power |
| | | |
| ADC_AVDD_1V8 | U13 | SARADC Analog Power |
| | | |
| OTP_VCC_1V8 | T13 | OTP Analog Power |

## 2.7 Function IO Description

Table 2-3 Function IO description

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| W19 | NPOR | NPOR | | | | | I | I | up | 2 | | |
| Y21 | GPIO0_A0/REF_CLKO | GPIO0_A0 | REF_CLKO | | | | I/O | I | down | 4 | √ | |
| Y20 | GPIO0_A1 | GPIO0_A1 | | | | | I/O | I | down | 2 | √ | |
| V21 | GPIO0_A2 | GPIO0_A2 | | | | | I/O | I | down | 2 | √ | |
| AA20 | GPIO0_A3/SDMMC0_DETN | GPIO0_A3 | SDMMC0_DETN | | | | I/O | I | up | 2 | √ | |
| V20 | GPIO0_A4/PMIC_SLEEP/TSADC_SHUT_M1 | GPIO0_A4 | PMIC_SLEEP | TSADC_SHUT_M1 | | | I/O | I | down | 2 | √ | |
| T21 | GPIO0_A5 | GPIO0_A5 | | | | | I/O | I | up | 2 | √ | |
| W21 | GPIO0_A6/TSADC_SHUT_M0/TSADC_SHUTORG | GPIO0_A6 | TSADC_SHUT_M0 | TSADC_SHUTORG | | | I/O | I | z | 2 | √ | PMUIO1 |
| Y19 | GPIO0_A7 | GPIO0_A7 | | | | | I/O | I | up | 2 | √ | |
| R21 | GPIO0_B0/I2C0_SCL | GPIO0_B0 | I2C0_SCL | | | | I/O | I | up | 2 | √ | |
| P21 | GPIO0_B1/I2C0_SDA | GPIO0_B1 | I2C0_SDA | | | | I/O | I | up | 2 | √ | |
| N20 | GPIO0_B2/UART0_TX | GPIO0_B2 | UART0_TX | | | | I/O | I | down | 2 | √ | |
| P18 | GPIO0_B3/UART0_RX | GPIO0_B3 | UART0_RX | | | | I/O | I | down | 2 | √ | |
| R18 | GPIO0_B4/UART0_CTS | GPIO0_B4 | UART0_CTS | | | | I/O | I | up | 2 | √ | |
| N19 | GPIO0_B5/UART0_RTS/TEST_CLK1 | GPIO0_B5 | UART0_RTS | TEST_CLK1 | | | I/O | I | up | 2 | √ | |
| R19 | GPIO0_B6/FLASH_VOLSEL | GPIO0_B6 | FLASH_VOLSEL | | | | I/O | I | up | 2 | √ | |
| M19 | GPIO0_B7/PWM0/OTG_DRV | GPIO0_B7 | PWM0 | OTG_DRV | | | I/O | I | down | 2 | √ | |
| N21 | GPIO0_C0/UART3_TX_M0/PWM1 | GPIO0_C0 | UART3_TX_M0 | PWM1 | | | I/O | I | down | 2 | √ | |
| P19 | GPIO0_C1/UART3_RX_M0/PWM3 | GPIO0_C1 | UART3_RX_M0 | PWM3 | | | I/O | I | down | 2 | √ | PMUIO2 |
| T20 | GPIO0_C2/I2C1_SCL/UART3_CTS_M0 | GPIO0_C2 | I2C1_SCL | UART3_CTS_M0 | | | I/O | I | down | 2 | √ | |
| R20 | GPIO0_C3/I2C1_SDA/UART3_RTS_M0 | GPIO0_C3 | I2C1_SDA | UART3_RTS_M0 | | | I/O | I | down | 2 | √ | |
| P20 | GPIO0_C4/CLKIO_32K | GPIO0_C4 | CLKIO_32K | | | | I/O | I | z | 2 | √ | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| E20 | GPIO1_A0/FLASH_D0/EMMC_D0/SFC_SIO0 | GPIO1_A0 | FLASH_D0 | EMMC_D0 | SFC_SIO0 | | I/O | I | up | 8 | √ | |
| D21 | GPIO1_A1/FLASH_D1/EMMC_D1/SFC_SIO1 | GPIO1_A1 | FLASH_D1 | EMMC_D1 | SFC_SIO1 | | I/O | I | up | 8 | √ | |
| C21 | GPIO1_A2/FLASH_D2/EMMC_D2/SFC_SIO2 | GPIO1_A2 | FLASH_D2 | EMMC_D2 | SFC_SIO2 | | I/O | I | up | 8 | √ | |
| E19 | GPIO1_A3/FLASH_D3/EMMC_D3/SFC_SIO3 | GPIO1_A3 | FLASH_D3 | EMMC_D3 | SFC_SIO3 | | I/O | I | up | 8 | √ | |
| E21 | GPIO1_A4/FLASH_D4/EMMC_D4/SFC_CSN0 | GPIO1_A4 | FLASH_D4 | EMMC_D4 | SFC_CSN0 | | I/O | I | up | 8 | √ | |
| D20 | GPIO1_A5/FLASH_D5/EMMC_D5 | GPIO1_A5 | FLASH_D5 | EMMC_D5 | | | I/O | I | up | 8 | √ | |
| C20 | GPIO1_A6/FLASH_D6/EMMC_D6 | GPIO1_A6 | FLASH_D6 | EMMC_D6 | | | I/O | I | up | 8 | √ | |
| B21 | GPIO1_A7/FLASH_D7/EMMC_D7 | GPIO1_A7 | FLASH_D7 | EMMC_D7 | | | I/O | I | up | 8 | √ | |
| F19 | GPIO1_B0/FLASH_CS0 | GPIO1_B0 | FLASH_CS0 | | | | I/O | I | up | 8 | √ | |
| H18 | GPIO1_B1/FLASH_RDY/EMMC_CLKOUT/SFC_CLK | GPIO1_B1 | FLASH_RDY | EMMC_CLKOUT | SFC_CLK | | I/O | I | up | 8 | √ | |
| G19 | GPIO1_B2/FLASH_DQS/EMMC_CMD | GPIO1_B2 | FLASH_DQS | EMMC_CMD | | | I/O | I | up | 8 | √ | |
| E18 | GPIO1_B3/FLASH_ALE/EMMC_RSTN | GPIO1_B3 | FLASH_ALE | EMMC_RSTN | | | I/O | I | down | 8 | √ | |
| G21 | GPIO1_B4/FLASH_CLE/UART3_CTS_M1/SPI0_MOSI/I2C3_SDA | GPIO1_B4 | FLASH_CLE | UART3_CTS_M1 | SPI0_MOSI | I2C3_SDA | I/O | I | down | 8 | √ | VCCIO6 |
| H20 | GPIO1_B5/FLASH_WRN/UART3_RTS_M1/SPI0_MISO/I2C3_SCL | GPIO1_B5 | FLASH_WRN | UART3_RTS_M1 | SPI0_MISO | I2C3_SCL | I/O | I | up | 8 | √ | |
| G20 | GPIO1_B6/FLASH_CS1/UART3_TX_M1/SPI0_CSN | GPIO1_B6 | FLASH_CS1 | UART3_TX_M1 | SPI0_CSN | | I/O | I | up | 8 | √ | |
| H21 | GPIO1_B7/FLASH_RDN/UART3_RX_M1/SPI0_CLK | GPIO1_B7 | FLASH_RDN | UART3_RX_M1 | SPI0_CLK | | I/O | I | up | 8 | √ | |
| J20 | GPIO1_C0/UART1_RX | GPIO1_C0 | UART1_RX | | | | I/O | I | up | 4 | √ | |
| K20 | GPIO1_C1/UART1_TX | GPIO1_C1 | UART1_TX | | | | I/O | I | up | 4 | √ | |
| K21 | GPIO1_C2/UART1_CTS | GPIO1_C2 | UART1_CTS | | | | I/O | I | up | 4 | √ | |
| L21 | GPIO1_C3/UART1_RTS | GPIO1_C3 | UART1_RTS | | | | I/O | I | up | 4 | √ | |
| H19 | GPIO1_C4/SDMMC1_CMD | GPIO1_C4 | SDMMC1_CMD | | | | I/O | I | up | 8 | √ | |
| M20 | GPIO1_C5/SDMMC1_CLK | GPIO1_C5 | SDMMC1_CLK | | | | I/O | I | down | 8 | √ | VCCIO1 |
| L20 | GPIO1_C6/SDMMC1_D0 | GPIO1_C6 | SDMMC1_D0 | | | | I/O | I | up | 8 | √ | |
| L19 | GPIO1_C7/SDMMC1_D1 | GPIO1_C7 | SDMMC1_D1 | | | | I/O | I | up | 8 | √ | |
| M21 | GPIO1_D0/SDMMC1_D2 | GPIO1_D0 | SDMMC1_D2 | | | | I/O | I | up | 8 | √ | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| J19 | GPIO1_D1/SDMMC1_D3 | GPIO1_D1 | SDMMC1_D3 | | | | I/O | I | up | 8 | √ | |
| AA17 | GPIO1_D2/SDMMC0_D0/UART2_TX_M0 | GPIO1_D2 | SDMMC0_D0 | UART2_TX_M0 | | | I/O | I | up | 8 | √ | |
| AA18 | GPIO1_D3/SDMMC0_D1/UART2_RX_M0 | GPIO1_D3 | SDMMC0_D1 | UART2_RX_M0 | | | I/O | I | up | 8 | √ | |
| AA19 | GPIO1_D4/SDMMC0_D2/UART4_RX/JTAG_TCK | GPIO1_D4 | SDMMC0_D2 | UART4_RX | JTAG_TCK | | I/O | I | up | 8 | √ | |
| AA16 | GPIO1_D5/SDMMC0_D3/UART4_TX/JTAG_TMS | GPIO1_D5 | SDMMC0_D3 | UART4_TX | JTAG_TMS | | I/O | I | up | 8 | √ | |
| Y17 | GPIO1_D6/SDMMC0_CLKO/UART4_CTS/TEST_CLKO | GPIO1_D6 | SDMMC0_CLKO | UART4_CTS | TEST_CLKO | | I/O | I | down | 8 | √ | |
| Y16 | GPIO1_D7/SDMMC0_CMD/UART4_RTS | GPIO1_D7 | SDMMC0_CMD | UART4_RTS | | | I/O | I | up | 8 | √ | VCCIO2 |
| AA5 | GPIO2_A0/CIF_D2_M0/RMII_TXEN | GPIO2_A0 | CIF_D2_M0 | RMII_TXEN | | | I/O | I | down | 4 | √ | |
| AA8 | GPIO2_A1/CIF_D3_M0/RMII_TXD1 | GPIO2_A1 | CIF_D3_M0 | RMII_TXD1 | | | I/O | I | down | 4 | √ | |
| AA7 | GPIO2_A2/CIF_D4_M0/RMII_TXD0 | GPIO2_A2 | CIF_D4_M0 | RMII_TXD0 | | | I/O | I | down | 4 | √ | |
| Y6 | GPIO2_A3/CIF_D5_M0/RMII_RXD0 | GPIO2_A3 | CIF_D5_M0 | RMII_RXD0 | | | I/O | I | down | 4 | √ | |
| Y8 | GPIO2_A4/CIF_D6_M0/RMII_RXD1 | GPIO2_A4 | CIF_D6_M0 | RMII_RXD1 | | | I/O | I | down | 4 | √ | |
| Y7 | GPIO2_A5/CIF_D7_M0/RMII_RXER | GPIO2_A5 | CIF_D7_M0 | RMII_RXER | | | I/O | I | down | 4 | √ | |
| W5 | GPIO2_A6/CIF_D8_M0/RMII_RXDV | GPIO2_A6 | CIF_D8_M0 | RMII_RXDV | | | I/O | I | down | 4 | √ | |
| W7 | GPIO2_A7/CIF_D9_M0/RMII_MDIO | GPIO2_A7 | CIF_D9_M0 | RMII_MDIO | | | I/O | I | down | 4 | √ | |
| Y4 | GPIO2_B0/CIF_VSYNC_M0 | GPIO2_B0 | CIF_VSYNC_M0 | | | | I/O | I | down | 2 | √ | |
| AA4 | GPIO2_B1/CIF_HREF_M0/RMII_MDC | GPIO2_B1 | CIF_HREF_M0 | RMII_MDC | | | I/O | I | down | 2 | √ | |
| AA6 | GPIO2_B2/CIF_CLKI_M0/RMII_CLK | GPIO2_B2 | CIF_CLKI_M0 | RMII_CLK | | | I/O | I | down | 2 | √ | |
| Y5 | GPIO2_B3/CIF_CLKO_M0/CLK_OUT_ETHERNET | GPIO2_B3 | CIF_CLKO_M0 | CLK_OUT_ETHERNET | | | I/O | I | down | 2 | √ | VCCIO3 |
| V12 | GPIO2_B4/CIF_D0_M0/UART2_TX_M1 | GPIO2_B4 | CIF_D0_M0 | UART2_TX_M1 | | | I/O | I | down | 2 | √ | |
| V7 | GPIO2_B5/PWM2 | GPIO2_B5 | PWM2 | | | | I/O | I | down | 2 | √ | |
| W6 | GPIO2_B6/CIF_D1_M0/UART2_RX_M1 | GPIO2_B6 | CIF_D1_M0 | UART2_RX_M1 | | | I/O | I | down | 2 | √ | |
| U7 | GPIO2_B7/CIF_D10_M0/I2C2_SCL | GPIO2_B7 | CIF_D10_M0 | I2C2_SCL | | | I/O | I | up | 2 | √ | |
| V6 | GPIO2_C0/CIF_D11_M0/I2C2_SDA | GPIO2_C0 | CIF_D11_M0 | I2C2_SDA | | | I/O | I | up | 2 | √ | |
| AA15 | GPIO2_C1/I2S1_2CH_LRCK_TXRX | GPIO2_C1 | I2S1_2CH_LRCK_TXRX | | | | I/O | I | down | 4 | √ | VCCIO5 |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AA14 | GPIO2_C2/I2S1_2CH__SCLK | GPIO2_C2 | I2S1_2CH__SCLK | | | | I/O | I | down | 4 | √ | |
| Y14 | GPIO2_C3/I2S1_2CH_MCLK | GPIO2_C3 | I2S1_2CH_MCLK | | | | I/O | I | down | 4 | √ | |
| Y15 | GPIO2_C4/I2S1_2CH_SDO | GPIO2_C4 | I2S1_2CH_SDO | | | | I/O | I | down | 4 | √ | |
| AA13 | GPIO2_C5/I2S1_2CH_SDI/PDM_SDIO_M1 | GPIO2_C5 | I2S1_2CH_SDI | PDM_SDIO_M1 | | | I/O | I | down | 4 | √ | |
| W15 | GPIO2_C6/PDM_CLK0_M1 | GPIO2_C6 | PDM_CLK0_M1 | | | | I/O | I | down | 4 | √ | |
| D19 | GPIO3_A0/LCDC_CLK | GPIO3_A0 | LCDC_CLK | | | | I/O | I | down | 8 | √ | |
| E13 | GPIO3_A1/LCDC_HSYNC_M0/CIF_D0_M1/I2S2_2CH_MCLK/UART5_RX | GPIO3_A1 | LCDC_HSYNC_M0 | CIF_D0_M1 | I2S2_2CH_MCLK | UART5_RX | I/O | I | down | 8 | √ | |
| F13 | GPIO3_A2/LCDC_VSYNC_M0/CIF_D1_M1/I2S2_2CH_SCLK/UART5_TX | GPIO3_A2 | LCDC_VSYNC_M0 | CIF_D1_M1 | I2S2_2CH_SCLK | UART5_TX | I/O | I | down | 8 | √ | |
| E14 | GPIO3_A3/LCDC_DEN_M0/CIF_D2_M1/I2S2_2CH_LRCK_TXRX/UART5_CTS | GPIO3_A3 | LCDC_DEN_M0 | CIF_D2_M1 | I2S2_2CH_LRCK_TXRX | UART5_CTS | I/O | I | down | 8 | √ | |
| C15 | GPIO3_A4/LCDC_D0 | GPIO3_A4 | LCDC_D0 | | | | I/O | I | down | 8 | √ | |
| E15 | GPIO3_A5/LCDC_D1_M0/CIF_D3_M1/I2S2_2CH_SDI/UART5_RTS | GPIO3_A5 | LCDC_D1_M0 | CIF_D3_M1 | I2S2_2CH_SDI | UART5_RTS | I/O | I | down | 8 | √ | |
| C14 | GPIO3_A6/LCDC_D2 | GPIO3_A6 | LCDC_D2 | | | | I/O | I | down | 8 | √ | |
| E16 | GPIO3_A7/LCDC_D3_M0/CIF_D4_M1/I2S2_2CH_SDO | GPIO3_A7 | LCDC_D3_M0 | CIF_D4_M1 | I2S2_2CH_SDO | | I/O | I | down | 8 | √ | |
| E17 | GPIO3_B0/LCDC_D4_M0/CIF_D5_M1/I2S0_8CH_SDI3 | GPIO3_B0 | LCDC_D4_M0 | CIF_D5_M1 | I2S0_8CH_SDI3 | | I/O | I | down | 8 | √ | |
| F17 | GPIO3_B1/LCDC_D5_M0/CIF_D6_M1/I2S0_8CH_SDI2/SPI1_CSN0 | GPIO3_B1 | LCDC_D5_M0 | CIF_D6_M1 | I2S0_8CH_SDI2 | SPI1_CSN0 | I/O | I | down | 8 | √ | |
| B18 | GPIO3_B2/LCDC_D6/SPI1_CSN1 | GPIO3_B2 | LCDC_D6 | SPI1_CSN1 | | | I/O | I | down | 8 | √ | |
| C17 | GPIO3_B3/LCDC_D7/I2S0_8CH_SDI1 | GPIO3_B3 | LCDC_D7 | I2S0_8CH_SDI1 | | | I/O | I | down | 8 | √ | VCCIO4 |
| F18 | GPIO3_B4/LCDC_D8_M0/CIF_D7_M1/I2S0_8CH_SCLKRX/SPI1_MOSI | GPIO3_B4 | LCDC_D8_M0 | CIF_D7_M1 | I2S0_8CH_SCLKRX | SPI1_MOSI | I/O | I | down | 8 | √ | |
| C16 | GPIO3_B5/LCDC_D9_M0/I2S0_8CH_LRCKRX | GPIO3_B5 | LCDC_D9_M0 | I2S0_8CH_LRCKRX | | | I/O | I | down | 8 | √ | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| G18 | GPIO3_B6/LCDC_D10_M0/CIF_D8_M1/I2S0_8CH_SDO3/SPI1_MISO | GPIO3_B6 | LCDC_D10_M0 | CIF_D8_M1 | I2S0_8CH_SDO3 | SPI1_MISO | I/O | I | down | 8 | √ | |
| G17 | GPIO3_B7/LCDC_D11_M0/CIF_D9_M1/I2S0_8CH_SDO2/SPI1_CLK | GPIO3_B7 | LCDC_D11_M0 | CIF_D9_M1 | I2S0_8CH_SDO2 | SPI1_CLK | I/O | I | down | 8 | √ | |
| A20 | GPIO3_C0/LCDC_D12/I2S0_8CH_SDO1 | GPIO3_C0 | LCDC_D12 | I2S0_8CH_SDO1 | | | I/O | I | down | 8 | √ | |
| B20 | GPIO3_C1/LCDC_D13/I2S0_8CH_MCLK | GPIO3_C1 | LCDC_D13 | I2S0_8CH_MCLK | | | I/O | I | down | 8 | √ | |
| C19 | GPIO3_C2/LCDC_D14/PWM4/I2S0_8CH_LRCKTX/TDM_FSYNC | GPIO3_C2 | LCDC_D14 | PWM4 | I2S0_8CH_LRCKTX | TDM_FSYNC | I/O | I | down | 8 | √ | |
| B19 | GPIO3_C3/LCDC_D15/PWM5/I2S0_8CH_SCLKTX/TDM_SCLK | GPIO3_C3 | LCDC_D15 | PWM5 | I2S0_8CH_SCLKTX | TDM_SCLK | I/O | I | down | 8 | √ | |
| C18 | GPIO3_C4/LCDC_D16/PWM6/I2S0_8CH_SDO0/TDM_SDO | GPIO3_C4 | LCDC_D16 | PWM6 | I2S0_8CH_SDO0 | TDM_SDO | I/O | I | down | 8 | √ | |
| A18 | GPIO3_C5/LCDC_D17/PWM7/I2S0_8CH_SDI0/TDM_SDI | GPIO3_C5 | LCDC_D17 | PWM7 | I2S0_8CH_SDI0 | TDM_SDI | I/O | I | down | 8 | √ | |
| D13 | GPIO3_C6/LCDC_D18/CIF_D10_M1/PDM_CLK0_M0 | GPIO3_C6 | LCDC_D18 | CIF_D10_M1 | PDM_CLK0_M0 | | I/O | I | down | 8 | √ | |
| D14 | GPIO3_C7/LCDC_D19/CIF_D11_M1/PDM_CLK1 | GPIO3_C7 | LCDC_D19 | CIF_D11_M1 | PDM_CLK1 | | I/O | I | down | 8 | √ | |
| D15 | GPIO3_D0/LCDC_D20/CIF_CLKOUT_M1/PDM_SDI1 | GPIO3_D0 | LCDC_D20 | CIF_CLKOUT_M1 | PDM_SDI1 | | I/O | I | down | 8 | √ | |
| D16 | GPIO3_D1/LCDC_D21/CIF_VSYNC_M1/PDM_SDI2/ISP_PRELIGHT_TRIG | GPIO3_D1 | LCDC_D21 | CIF_VSYNC_M1 | PDM_SDI2 | ISP_PRELIGHT_TRIG | I/O | I | down | 8 | √ | |
| D17 | GPIO3_D2/LCDC_D22/CIF_HREF_M1/PDM_SDI3/ISP_FLASH_TRIGOUT | GPIO3_D2 | LCDC_D22 | CIF_HREF_M1 | PDM_SDI3 | ISP_FLASH_TRIGOUT | I/O | I | down | 8 | √ | |
| D18 | GPIO3_D3/LCDC_D23/CIF_CLKIN_M1/PDM_SDI0_M0/ISP_FLASH_TRIGIN | GPIO3_D3 | LCDC_D23 | CIF_CLKIN_M1 | PDM_SDI0_M0 | ISP_FLASH_TRIGIN | I/O | I | down | 8 | √ | |
| V14 | ADC_IN0 | ADC_IN0 | | | | | A | | N/A | | | |
| W14 | ADC_IN1 | ADC_IN1 | | | | | A | | N/A | | | ADC_AVDD |
| V15 | ADC_IN2 | ADC_IN2 | | | | | A | | N/A | | | |
| T2 | DDR_D_m0 | DDR3_D_m0 | DDR4_D_m0 | | | | A | | N/A | | | DDRIO |
| U4 | DDR_D_M1 | DDR3_D_M1 | DDR4_D_M1 | | | | A | | N/A | | | |
| G4 | DDR_DM2 | DDR3_DM2 | DDR4_DM2 | | | | A | | N/A | | | |
| M4 | DDR_DM3 | DDR3_DM3 | DDR4_DM3 | | | | A | | N/A | | | |
| R4 | DDR_DQ0 | DDR3_DQ0 | DDR4_DQ0 | | | | A | | N/A | | | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R1 | DDR_DQ1 | DDR3_DQ1 | DDR4_DQ1 | | | | A | | N/A | | | |
| Y3 | DDR_DQ10 | DDR3_DQ10 | DDR4_DQ10 | | | | A | | N/A | | | |
| M2 | DDR_DQ11 | DDR3_DQ11 | DDR4_DQ11 | | | | A | | N/A | | | |
| V4 | DDR_DQ12 | DDR3_DQ12 | DDR4_DQ12 | | | | A | | N/A | | | |
| M3 | DDR_DQ13 | DDR3_DQ13 | DDR4_DQ13 | | | | A | | N/A | | | |
| V3 | DDR_DQ14 | DDR3_DQ14 | DDR4_DQ14 | | | | A | | N/A | | | |
| N4 | DDR_DQ15 | DDR3_DQ15 | DDR4_DQ15 | | | | A | | N/A | | | |
| F4 | DDR_DQ16 | DDR3_DQ16 | DDR4_DQ16 | | | | A | | N/A | | | |
| G3 | DDR_DQ17 | DDR3_DQ17 | DDR4_DQ17 | | | | A | | N/A | | | |
| F3 | DDR_DQ18 | DDR3_DQ18 | DDR4_DQ18 | | | | A | | N/A | | | |
| K2 | DDR_DQ19 | DDR3_DQ19 | DDR4_DQ19 | | | | A | | N/A | | | |
| U3 | DDR_DQ2 | DDR3_DQ2 | DDR4_DQ2 | | | | A | | N/A | | | |
| L2 | DDR_DQ20 | DDR3_DQ20 | DDR4_DQ20 | | | | A | | N/A | | | |
| M1 | DDR_DQ21 | DDR3_DQ21 | DDR4_DQ21 | | | | A | | N/A | | | |
| E2 | DDR_DQ22 | DDR3_DQ22 | DDR4_DQ22 | | | | A | | N/A | | | |
| L1 | DDR_DQ23 | DDR3_DQ23 | DDR4_DQ23 | | | | A | | N/A | | | |
| K3 | DDR_DQ24 | DDR3_DQ24 | DDR4_DQ24 | | | | A | | N/A | | | |
| J4 | DDR_DQ25 | DDR3_DQ25 | DDR4_DQ25 | | | | A | | N/A | | | |
| C2 | DDR_DQ26 | DDR3_DQ26 | DDR4_DQ26 | | | | A | | N/A | | | |
| D2 | DDR_DQ27 | DDR3_DQ27 | DDR4_DQ27 | | | | A | | N/A | | | |
| K4 | DDR_DQ28 | DDR3_DQ28 | DDR4_DQ28 | | | | A | | N/A | | | |
| J3 | DDR_DQ29 | DDR3_DQ29 | DDR4_DQ29 | | | | A | | N/A | | | |
| Y2 | DDR_DQ3 | DDR3_DQ3 | DDR4_DQ3 | | | | A | | N/A | | | |
| D1 | DDR_DQ30 | DDR3_DQ30 | DDR4_DQ30 | | | | A | | N/A | | | |
| E1 | DDR_DQ31 | DDR3_DQ31 | DDR4_DQ31 | | | | A | | N/A | | | |
| N2 | DDR_DQ4 | DDR3_DQ4 | DDR4_DQ4 | | | | A | | N/A | | | |
| R3 | DDR_DQ5 | DDR3_DQ5 | DDR4_DQ5 | | | | A | | N/A | | | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R2 | DDR_DQ6 | DDR3_DQ6 | DDR4_DQ6 | | | | A | | N/A | | | |
| Y1 | DDR_DQ7 | DDR3_DQ7 | DDR4_DQ7 | | | | A | | N/A | | | |
| AA2 | DDR_DQ8 | DDR3_DQ8 | DDR4_DQ8 | | | | A | | N/A | | | |
| P3 | DDR_DQ9 | DDR3_DQ9 | DDR4_DQ9 | | | | A | | N/A | | | |
| W1 | DDR_DQS0_N | DDR3_DQS0_N | DDR4_DQS0_N | | | | A | | N/A | | | |
| W2 | DDR_DQS0_P | DDR3_DQS0_P | DDR4_DQS0_P | | | | A | | N/A | | | |
| U1 | DDR_DQS1_N | DDR3_DQS1_N | DDR4_DQS1_N | | | | A | | N/A | | | |
| U2 | DDR_DQS1_P | DDR3_DQS1_P | DDR4_DQS1_P | | | | A | | N/A | | | |
| J1 | DDR_DQS2_N | DDR3_DQS2_N | DDR4_DQS2_N | | | | A | | N/A | | | |
| J2 | DDR_DQS2_P | DDR3_DQS2_P | DDR4_DQS2_P | | | | A | | N/A | | | |
| G1 | DDR_DQS3_N | DDR3_DQS3_N | DDR4_DQS3_N | | | | A | | N/A | | | |
| G2 | DDR_DQS3_P | DDR3_DQS3_P | DDR4_DQS3_P | | | | A | | N/A | | | |
| C7 | DDR3_A0/DDR4_A10 | DDR3_A0 | DDR4_A10 | | | | A | | N/A | | | |
| D10 | DDR3_A1/DDR4_A9 | DDR3_A1 | DDR4_A9 | | | | A | | N/A | | | |
| A10 | DDR3_A10/DDR4_CS0n | DDR3_A10 | DDR4_CS0n | | | | A | | N/A | | | |
| B7 | DDR3_A11/DDR4_A3 | DDR3_A11 | DDR4_A3 | | | | A | | N/A | | | |
| A9 | DDR3_A12/DDR4_BA1 | DDR3_A12 | DDR4_BA1 | | | | A | | N/A | | | |
| D6 | DDR3_A13/DDR4_A2 | DDR3_A13 | DDR4_A2 | | | | A | | N/A | | | |
| A7 | DDR3_A14/DDR4_A1 | DDR3_A14 | DDR4_A1 | | | | A | | N/A | | | |
| C9 | DDR3_A15/DDR4_ODT0 | DDR3_A15 | DDR4_ODT0 | | | | A | | N/A | | | |
| D8 | DDR3_A2/DDR4_A4 | DDR3_A2 | DDR4_A4 | | | | A | | N/A | | | |
| B5 | DDR3_A3/DDR4_A6 | DDR3_A3 | DDR4_A6 | | | | A | | N/A | | | |
| A8 | DDR3_A4/DDR4_A5 | DDR3_A4 | DDR4_A5 | | | | A | | N/A | | | |
| A4 | DDR3_A5/DDR4_A8 | DDR3_A5 | DDR4_A8 | | | | A | | N/A | | | |
| B8 | DDR3_A6/DDR4_A7 | DDR3_A6 | DDR4_A7 | | | | A | | N/A | | | |
| B4 | DDR3_A7/DDR4_A11 | DDR3_A7 | DDR4_A11 | | | | A | | N/A | | | |
| C10 | DDR3_A8/DDR4_A13 | DDR3_A8 | DDR4_A13 | | | | A | | N/A | | | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| C6 | DDR3_A9/DDR4_A0 | DDR3_A9 | DDR4_A0 | | | | A | | N/A | | | |
| A3 | DDR3_BA0/DDR4_BG0 | DDR3_BA0 | DDR4_BG0 | | | | A | | N/A | | | |
| B10 | DDR3_BA1/DDR4_CASn/DDR4_A15 | DDR3_BA1 | DDR4_CASn | DDR4_A15 | | | A | | N/A | | | |
| A5 | DDR3_BA2/DDR4_BA0 | DDR3_BA2 | DDR4_BA0 | | | | A | | N/A | | | |
| D9 | DDR3_CASn/DDR4_A12 | DDR3_CASn | DDR4_A12 | | | | A | | N/A | | | |
| B11 | DDR3_CKE/DDR4_RASn/DDR4_A16 | DDR3_CKE | DDR4_RASn | DDR4_A16 | | | A | | N/A | | | |
| B1 | DDR3_CLKN/DDR4_CLKN | DDR3_CLKN | DDR4_CLKN | | | | A | | N/A | | | |
| B2 | DDR3_CLKP/DDR4_CLKP | DDR3_CLKP | DDR4_CLKP | | | | A | | N/A | | | |
| B3 | DDR3_CSN0/DDR4_ACTn | DDR3_CSN0 | DDR4_ACTn | | | | A | | N/A | | | |
| D11 | DDR3_CSN1/DDR4_CS1N | DDR3_CSN1 | DDR4_CS1N | | | | A | | N/A | | | |
| D5 | DDR3_ODT0/DDR4_Wen/DDR4_A14 | DDR3_ODT0 | DDR4_Wen | DDR4_A14 | | | A | | N/A | | | |
| C11 | DDR3_ODT1/DDR4_ODT1 | DDR3_ODT1 | DDR4_ODT1 | | | | A | | N/A | | | |
| C4 | DDR3_RASn/DDR4_CKE | DDR3_RASn | DDR4_CKE | | | | A | | N/A | | | |
| A2 | DDR3_RESETn/DDR4_RESETN | DDR3_RESETn | DDR4_RESETN | | | | A | | N/A | | | |
| C8 | DDR3_WEn/DDR4_BG1 | DDR3_WEn | DDR4_BG1 | | | | A | | N/A | | | |
| B14 | LVDS_CLKN/MIPI_TX_CLKN/LCDC_D4_M1 | LVDS_CLKN | MIPI_TX_CLKN | LCDC_D4_M1 | | | A | | N/A | | | |
| A14 | LVDS_CLKP/MIPI_TX_CLKP/LCDC_D3_M1 | LVDS_CLKP | MIPI_TX_CLKP | LCDC_D3_M1 | | | A | | N/A | | | |
| G12 | LVDS_RBIAS | LVDS_RBIAS | | | | | A | | N/A | | | |
| B16 | LVDS_TX0N/MIPI_TX_D0N/LCDC_D11_M1 | LVDS_TX0N | MIPI_TX_D0N | LCDC_D11_M1 | | | A | | N/A | | | |
| B17 | LVDS_TX0P/MIPI_TX_D0P/LCDC_D8_M1 | LVDS_TX0P | MIPI_TX_D0P | LCDC_D8_M1 | | | A | | N/A | | | |
| B15 | LVDS_TX1N/MIPI_TX_D1N/LCDC_D1_M1 | LVDS_TX1N | MIPI_TX_D1N | LCDC_D1_M1 | | | A | | N/A | | | |
| A16 | LVDS_TX1P/MIPI_TX_D1P/LCDC_D10_M1 | LVDS_TX1P | MIPI_TX_D1P | LCDC_D10_M1 | | | A | | N/A | | | |
| C13 | LVDS_TX2N/MIPI_TX_D2N/LCDC_VSYNC_M1 | LVDS_TX2N | MIPI_TX_D2N | LCDC_VSYNC_M1 | | | A | | N/A | | | MIPI_DSI |
| B13 | LVDS_TX2P/MIPI_TX_D2P/LCDC_D5_M1 | LVDS_TX2P | MIPI_TX_D2P | LCDC_D5_M1 | | | A | | N/A | | | |
| B12 | LVDS_TX3N/MIPI_TX_D3N/LCDC_HSYNC_M1 | LVDS_TX3N | MIPI_TX_D3N | LCDC_HSYNC_M1 | | | A | | N/A | | | |

| Pin | Pin Name | Func1 | Func2 | Func3 | Func4 | Func5 | Pad Type① | Def ③ | Pull | Drive Strength② | INT ④ | DIE Power domain |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A12 | LVDS_TX3P/MIPI_TX_D3P/LCDC_DEN_M1 | LVDS_TX3P | MIPI_TX_D3P | LCDC_DEN_M1 | | | A | | N/A | | | |
| U10 | MIPI_CSI_CLKN | MIPI_CSI_CLKN | | | | | A | | N/A | | | |
| V10 | MIPI_CSI_CLKP | MIPI_CSI_CLKP | | | | | A | | N/A | | | |
| V11 | MIPI_CSI_DN0 | MIPI_CSI_DN0 | | | | | A | | N/A | | | |
| W9 | MIPI_CSI_DN1 | MIPI_CSI_DN1 | | | | | A | | N/A | | | |
| V8 | MIPI_CSI_DN2 | MIPI_CSI_DN2 | | | | | A | | N/A | | | |
| W8 | MIPI_CSI_DN3 | MIPI_CSI_DN3 | | | | | A | | N/A | | | |
| W10 | MIPI_CSI_DP0 | MIPI_CSI_DP0 | | | | | A | | N/A | | | |
| Y9 | MIPI_CSI_DP1 | MIPI_CSI_DP1 | | | | | A | | N/A | | | |
| U9 | MIPI_CSI_DP2 | MIPI_CSI_DP2 | | | | | A | | N/A | | | |
| V9 | MIPI_CSI_DP3 | MIPI_CSI_DP3 | | | | | A | | N/A | | | |
| U11 | MIPI_CSI_RBIAS | MIPI_CSI_RBIAS | | | | | A | | N/A | | | MIPI_CSI |
| U20 | OSC_24M_IN | OSC_24M_IN | | | | | A | | N/A | | | |
| U21 | OSC_24M_OUT | OSC_24M_OUT | | | | | A | | N/A | | | PMU_VDD |
| Y12 | USB_HOST_DM | USB_HOST_DM | | | | | A | | N/A | | | |
| AA12 | USB_HOST_DP | USB_HOST_DP | | | | | A | | N/A | | | |
| Y11 | USB_ID | USB_ID | | | | | A | | N/A | | | |
| AA10 | USB_OTG_DM | USB_OTG_DM | | | | | A | | N/A | | | |
| Y10 | USB_OTG_DP | USB_OTG_DP | | | | | A | | N/A | | | |
| Y13 | USB_VBUS | USB_VBUS | | | | | A | | N/A | | | USB |

*Notes:*

① *Pad types: I = digital-input, O = digital-output, I/O = digital input/output (bidirectional) , A=Analog IO*

② *Def default IO direction for digital IO*

③ *Output Drive Unit is mA, only Digital IO has drive value;*

④ *INT: interrupt support;*

## 2.8 IO Pin Name Description

This sub-chapter will focus on the detailed function description of every pins based on different interface.

Table 2-4 IO function description list

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| Misc | OSC_24M_IN | I | Clock input of 24MHz crystal |
| | OSC_24M_OUT | O | Clock output of 24MHz crystal |
| | NPOR | I | Chip hardware reset |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SWJ-DP | JTAG_TCK | I | JTAG interface clock input/SWD interface clock input |
| | JTAG_TMS | I/O | JTAG interface TMS input/SWD interface data out |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SD/MMC Host Controller | SDMMC0_CLK | O | sdmmc card clock |
| | SDMMC0_CMD | I/O | sdmmc card command output and response input |
| | SDMMC0_D[*i*] (*i*=0~3) | I/O | sdmmc card data input and output |
| | SDMMC0_DETN | I | sdmmc card detect signal, 0 represents presence of card |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SDIO Host Controller | SDMMC1_CLK | O | sdio card clock |
| | SDMMC1_CMD | I/O | sdio card command output and response input |
| | SDMMC1_D[*i*] (*i*=0~3) | I/O | sdio card data input and output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| eMMC Interface | EMMC_CLKOUT | O | emmc card clock |
| | EMMC_CMD | I/O | emmc card command output and response input |
| | EMMC_D[*i*] (*i*=0~7) | I/O | emmc card data input and output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| Nand Flash Interface | FLASH_ALE | O | Flash address latch enable signal |
| | FLASH_CLE | O | Flash command latch enable signal |
| | FLASH_WRN | O | Flash write enable and clock signal |
| | FLASH_RDN | O | Flash read enable and write/read signal |
| | FLASH_D*i*(*i*=0~7) | I/O | Flash data inputs/outputs signal |
| | FLASH*x*_DQS | I/O | Flash data strobe signal |
| | FLASH*x*_RDY | I | Flash ready/busy signal |

| | | | |
|---|---|---|---|
| | FLASH*x*_CSN*i*=0~1) | O | Flash chip enable signal for chip i, i=0~7 |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SFC Controller | SFC_CLK | I/O | sfc serial clock |
| | SFC_CSNx*(x=0)* | I/O | sfc chip select signal,low active |
| | SFC_SIOx*(x=0,3)* | O | sfc serial data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| LCDC | LCDC_DCLK | O | LCDC RGB interface display clock out, MCU i80 interface RS signal |
| | LCDC_VSYNC | O | LCDC RGB interface vertical sync pulse, MCU i80 interface CSN signal |
| | LDCD_HSYNC | O | LCDC RGB interface horizontal sync pulse, MCU i80 interface WEN signal |
| | LCDC_DEN | O | LCDC RGB interface data enable, MCU i80 interface REN signal |
| | LCDC_D*i*(*i*=0~23) | O | LCDC data output/input |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| DDR Interface | CLKP | O | Active-high clock signal to the memory device. |
| | CLKN | O | Active-low clock signal to the memory device. |
| | CKE | O | Active-high clock enable signal to the memory device |
| | CSNi (i=0,1) | O | Active-low chip select signal to the memory device. AThere are two chip select. |
| | RASn | O | Active-low row address strobe to the memory device. |
| | CASn | O | Active-low column address strobe to the memory device. |
| | WEn | O | Active-low write enable strobe to the memory device. |
| | BAi(i=0,1,2) | O | Bank address signal to the memory device. |
| | Ai(i=0~15) | O | Address signal to the memory device. |
| | DQi(i=0~31) | I/O | Bidirectional data line to the memory device. |
| | DQS[*i*]_P (i=0~3) | I/O | Active-high bidirectional data strobes to the memory device. |
| | DQS[*i*]_N (i=0~3) | I/O | Active-low bidirectional data strobes to the memory device. |
| | DMi(i=0~3) | O | Active-low data mask signal to the memory device. |
| | ODTi(i=0,1) | O | On-Die Termination output signal for two chip select. |
| | RESETn | O | DDR3/DDR4 reset signal to the memory device |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| I2S0/PCM Controller | I2S0_8CH_MCLK | O | I2S/PCM clock source |
| | I2S0_8CH_SCLK | I/O | I2S/PCM serial clock |
| | I2S0_8CH_LRCKRX | I/O | I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S0_8CH_LRCKTX | I/O | I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S0_8CH_SDI*i* (*i*=1~3) | I | I2S/PCM serial data input |
| | I2S0_8CH_SDO*i* (*i*=1~3) | O | I2S/PCM serial data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| I2S1/PCM Controller | I2S1_2CH_MCLK | O | I2S/PCM clock source |
| | I2S1_2CH_SCLK | I/O | I2S/PCM serial clock |
| | I2S1_2CH_LRCKRX | I/O | I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S1_2CH_LRCKTX | I/O | I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S1_2CH_SDI | I | I2S/PCM serial data input |
| | I2S1_2CH_SDO | O | I2S/PCM serial data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| I2S2/PCM Controller | I2S2_2CH_MCLK | O | I2S/PCM clock source |
| | I2S2_2CH_SCLK | I/O | I2S/PCM serial clock |
| | I2S2_2CH_LRCKRX | I/O | I2S/PCM left & right channel signal for receiving serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S2_2CH_LRCKTX | I/O | I2S/PCM left & right channel signal for transmitting serial data, synchronous left & right channel in I2S mode and the beginning of a group of left & right channels in PCM mode |
| | I2S2_2CH_SDI | I | I2S/PCM serial data input |
| | I2S2_2CH_SDO | O | I2S/PCM serial data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| PDM | PDM_CLK | O | PDM sampling clock |
| | PDM_SDI[*i*] (*i*=0~3) | I | PDM data |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| TDM | TDM_SCLK | I/O | TDM serial clock |
| | TDM_FSYNC | I/O | TDM frame synchronization pulse |
| | TDM_SDI | I | TDM serial data input |
| | TDM_SDO | O | TDM data output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SPI0 | SPI0_CLK | I/O | SPI serial clock |
| | SPI0_CSN[*i*](*i*=0) | I/O | SPI chip select signal, low active |
| | SPI0_TXD | O | SPI serial data output |
| | SPI0_RXD | I | SPI serial data input |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| SPI1 | SPI1_CLK | I/O | SPI serial clock |
| | SPI1_CSN[*i*](*i*=0,1) | I/O | SPI chip select signal, low active |
| | SPI1_TXD | O | SPI serial data output |
| | SPI_RXD | I | SPI serial data input |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| PWM | PWM0 | I/O | Pulse Width Modulation input and output |
| | PWM1 | I/O | Pulse Width Modulation input and output, used for VOPB CABAC PWM control |
| | PWM2 | I/O | Pulse Width Modulation input and output |
| | PWM3 | I/O | Pulse Width Modulation input and output, used for IR application recommended |
| | PWM4 | I/O | Pulse Width Modulation input and output |
| | PWM5 | I/O | Pulse Width Modulation input and output |
| | PWM6 | I/O | Pulse Width Modulation input and output |
| | PWM7 | I/O | Pulse Width Modulation input and output, used for IR application recommended |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| I2C | I2C[*i*]_SDA (*i*=0,1,2,3) | I/O | I2C data |
| | I2C[*i*]_SCL (*i*=0,1,2,3) | I/O | I2C clock |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| UART | UART[*i*]_RX (*i*=0,1,2,3,4,5) | I | UART serial data input |
| | UART[*i*]_TX (*i*=0,1,2,3,4,5) | O | UART serial data output |
| | UART[*i*]_CTS (*i*=0,1,3,4,5) | I | UART clear to send modem tatus input |
| | UART[*i*]_RTS (*i*=0,1,3,4,5) | O | UART modem control request to send output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| MAC | RMII_CLK | I/O | MAC REC_CLK output or external clock input |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| | RMII_MDC | O | MAC management interface clock |
| | RMII_MDIO | I/O | MAC management interface data |
| | RMII_TXD[*i*](*i*=0~1) | O | MAC TX data |
| | RMII_RXD[*i*](*i*=0~1) | I | MAC RX data |
| | RMII_TXEN | O | MAC TX data enable |
| | RMII_RXER | I | MAC RX error signal |
| | RMII_RXDV | O | MAC RX enable |
| | RMII_CRS | I | PHY CRS signal |
| | RMII_MDIO | I/O | PHY MDC data line |
| | RMII_MDC | O | PHY MDC control |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| USB 2.0 | USB_HOST_DP | I/O | USB 2.0 Data signal DP |
| | USB_HOST_DM | I/O | USB 2.0 Data signal DM |
| | USB_OTG_DP | I/O | USB 2.0 Data signal DP |
| | USB_OTG_DM | I/O | USB 2.0 Data signal DM |
| | USB_RBIAS | O | Connect 133 ohm resistor to ground to generate reference current |
| | USB_VBUS | I | Insert detect when act as USB device |
| | USB_ID | I | USB Mini-Receptacle Identifier |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| MIPI_DSI | MIPI_TX_D*i*N(*i*=0~3) | O | MIPI DSI negative differential data line transceiver output |
| | MIPI_TX_D*i*P(*i*=0~3) | O | MIPI DSI positive differential data line transceiver output |
| | MIPI_TX_CLKP | O | MIPI DSI positive differential clock line transceiver output |
| | MIPI_TX_CLKN | O | MIPI DSI negative differential clock line transceiver output |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| LVDS | LVDS_TX*i*N(*i*=0~3) | O | LVDS negative differential data line transceiver output |
| | LVDS_TX*i*P(*i*=0~3) | O | LVDS positive differential data line transceiver output |
| | LVDS_CLKP | O | LVDS positive differential clock line transceiver output |
| | LVDS_CLKN | O | LVDS negative differential clock line transceiver output |
| | LVDS_RBIAS | O | LVDS external resistor connection, connect 2K ohm resistor to ground |

| Interface | Pin Name | Direction | Description |
|---|---|---|---|
| MIPI_CSI | MIPI_CSI_DN*i*(*i*=0~3) | I | MIPI CSI negative differential data line transceiver output |
| | MIPI_CSI_DP*i*(*i*=0~3) | I | MIPI CSI positive differential data line transceiver output |
| | MIPI_CSI_CLKP | I | MIPI CSI positive differential clock line transceiver output |
| | MIPI_CSI_CLKN | I | MIPI CSI negative differential clock line transceiver output |
| | MIPI_CSI_RBIAS | I | MIPI CSI external resistor connection, connect 2K ohm resistor to ground |

# Chapter 3 Electrical Specification

## 3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.
Absolute minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute minimum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

| Parameters | Related Power Group | Min | Max | Unit |
|---|---|---|---|---|
| Supply voltage for CPU | VDD_CORE | -0.3 | 1.40 | V |
| Supply voltage for GPU and core logic | VDD_LOGIC | -0.3 | 1.15 | V |
| 1.0V supply voltage | | -0.3 | 1.15 | V |
| 1.8V supply voltage | | -0.3 | 1.98 | V |
| 3.3V supply voltage | | -0.3 | 3.63 | V |
| Supply voltage for DDR IO | | -0.3 | 1.65 | V |
| Storage Temperature | Tstg | -40 | 125 | ℃ |
| Max Conjunction Temperature | Tj | N/A | 125 | ℃ |

## 3.2 Recommended Operating Condition

Following table describes the recommended operating condition.

Table 3-2 Recommended operating condition

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Voltage for CPU | CPU_VDD | 0.95 | 1.00 | 1.35 | V |
| Voltage for GPU and core logic | LOGIC_VDD | 0.90 | 1.00 | 1.10 | V |
| Voltage for PMU | PMU_VDD_1V0 | 0.90 | 1.00 | 1.10 | V |
| Digital GPIO Power (3.3V/1.8V) | VCCIO1,VCCIO2, VCCIO3, VCCIO4VCCIO5, VCCIO6, PMUIO1, PMUIO2 | 2.97<br>1.62 | 3.30<br>1.8 | 3.63<br>1.98 | V |
| DDR3 IO power | DDR_VDD | 1.425 | 1.5 | 1.575 | V |
| DDR3L IO Power | DDR_VDD | 1.283 | 1.35 | 1.417 | V |
| LPDDR3 IO Power | DDR_VDD | 1.14 | 1.2 | 1.3 | V |
| DDR4 IO Power | DDR_VDD | 1.14 | 1.2 | 1.3 | V |
| OTP Analog Power | OTP_VCC_1V8 | 1.62 | 1.8 | 1.98 | V |
| PLL Analog Power(1.0V) | PLL_DVDD_1V0 | 0.9 | 1.0 | 1.1 | V |
| PLL Analog Power(1.8V) | PLL_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| SARADC Analog Power | ADC_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| USB 2.0 OTG/Host Analog Power (1.0V) | USB20_DVDD_1V0 | 0.90 | 1.00 | 1.10 | V |
| USB 2.0 OTG/Host Analog Power (1.8V) | USB20_AVDD_1V8 | 1.62 | 1.8 | 1.98 | V |
| USB 2.0 OTG/Host Analog Power (3.3V) | USB20_AVDD_3V3 | 2.97 | 3.3 | 3.63 | V |
| MIPI DSI Analog Power(1.0V) | MIPI_DSI_VCCA_1V0 | 0.90 | 1.00 | 1.10 | V |
| MIPI DSI Analog Power (1.8V) | MIPI_DSI_VCCA_1V8 | 1.62 | 1.8 | 1.98 | V |
| MIPI DSI Analog Power (3.3V) | MIPI_DSI_VCCA_3V3 | 2.97 | 3.3 | 3.63 | V |

| Parameters | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| MIPI CSI Analog Power(1.0V) | MIPI_CSI_VCCA_1V0 | 0.9 | 1.0 | 1.1 | V |
| OSC input clock frequency | | N/A | 24 | N/A | MHz |
| Max CPU frequency of A35 | | N/A | N/A | TBD | GHz |
| Max GPU frequency | | N/A | N/A | TBD | MHz |
| Ambient Operating Temperature for PX30 | $T_A$ | 0 | 25 | 80 | ℃ |
| Ambient Operating Temperature for PX30K | Ta | -20 | 25 | 85 | ℃ |

*Notes:*

① *Symbol name is same as the pin name in the io descriptions*

② *with the reference software setup, the reference software will limit the chipset temperature about 85℃*

## 3.3 DC Characteristics

Table 3-3 DC Characteristics

| Parameters | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Digital GPIO @3.3V | Input Low Voltage | Vil | -0.3 | 0 | 3.3x0.3 | V |
| | Input High Voltage | Vih | 3.3x0.7 | 3.3 | 3.3+0.3 | V |
| | Output Low Voltage | Vol | NA | NA | 0.4 | V |
| | Output High Voltage | Voh | 3.3-0.4 | NA | NA | V |
| | Threshold Point | Vtr+ | 1.53 | 1.46 | 1.43 | V |
| | | Vtr- | 1.19 | 1.12 | 1.05 | V |
| | Pullup Resistor | Rpu | 33.7 | 58 | 101.5 | Kohm |
| | Pulldown Resistor | Rpd | 34.2 | 60.1 | 109.3 | Kohm |
| Digital GPIO @1.8V | Input Low Voltage | Vil | -0.3 | 0 | 1.8x0.3 | V |
| | Input High Voltage | Vih | 1.8x0.7 | 1.8 | 1.8 + 0.3 | V |
| | Output Low Voltage | Vol | NA | NA | 0.4 | V |
| | Output High Voltage | Voh | 1.8-0.4 | NA | NA | V |
| | Threshold Point | Vtr+ | 1.23 | 1.12 | 1.03 | V |
| | | Vtr- | 0.91 | 0.82 | 0.73 | V |
| | Pullup Resistor | Rpu | 35 | 62.9 | 120 | Kohm |
| | Pulldown Resistor | Rpd | 35.1 | 61 | 113.9 | Kohm |

| Parameters | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| DDR IO @ LPDDR2 mode | Input High Voltage | Vih_ddr | VREF + 0.13 | NA | DDR_VDD | V |
| | Input Low Voltage | Vil_ddr | VSS | NA | VREF - 0.13 | V |
| | Output High Voltage | Voh_ddr | VREF + 0.13 | NA | DDR_VDD | V |
| | Output Low Voltage | Vol_ddr | VSS | NA | Vref-0.13 | V |
| DDR IO @ LPDDR3 mode | Input High Voltage | Vih_ddr | VREF + 0.1 | NA | DDR_VDD | V |
| | Input Low Voltage | Vil_ddr | VSS | NA | VREF - 0.1 | V |
| | Output High Voltage | Voh_ddr | VREF + 0.1 | NA | DDR_VDD | V |
| | Output Low Voltage | Vol_ddr | VSS | NA | VREF - 0.1 | V |
| DDR IO @DDR3 mode | Input High Voltage | Vih_ddr | VREF + 0.10 | NA | DDR_VDD | V |
| | Input Low Voltage | Vil_ddr | VSS | NA | VREF - 0.10 | V |

| Parameters | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| | Output High Voltage | Voh_ddr | VREF + 0.10 | NA | DDR_VDD | V |
| | Output Low Voltage | Vol_ddr | VSS | NA | VREF - 0.10 | V |
| | On die termination (ODT) resistance | Rtt | 10 | 75 | 220 | Ohm |
| DDR IO @DDR4 mode | Input High Voltage | Vih_ddr | VREF +0.075 | NA | DDR_VDD | V |
| | Input Low Voltage | Vil_ddr | VSS | NA | VREF -0.075 | V |
| | Output High Voltage | Voh_ddr | VREF +0.075 | NA | DDR_VDD | V |
| | Output Low Voltage | Vol_ddr | VSS | NA | Vref-0.075 | V |

| Parameters | | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| MIPI_DSI IO @LVDS mode | Output High Voltage | Voh | 1050 | NA | NA | mV |
| | Output Low Voltage | Vol | NA | NA | 750 | mV |
| | Output differential voltage | \|VOD\| | 250 | NA | 400 | mV |
| | Output offset voltage | Vos | 825 | NA | 975 | mV |
| | Output impedance, single ended | Ro | 40 | NA | 140 | Ω |
| | Ro mismatch between A & B | ΔRo | NA | NA | 10 | % |
| | Change in \|Vod\| between 0 and 1 | \|ΔVod\| | NA | NA | 25 | mV |
| | Change in Vod between 0 and 1 | ΔVos | NA | NA | 25 | mV |
| MIPI_DSI IO @TTL mode | Output High Voltage | Voh | 1.8 | NA | NA | V |
| | Output Low Voltage | Vol | NA | NA | 0 | V |
| | Short-Circuit Output Current | Ios | NA | 35 | 60 | mA |
| | Output impedance | Zolp | 40 | NA | 460 | Ω |
| MIPI_DSI IO @MIPI mode | Output High Voltage | Voh | 300 | NA | NA | mV |
| | Output Low Voltage | Vol | NA | NA | 100 | mV |
| | HS TX static Common-mode voltage | VCMTX | 150 | 200 | 250 | mV |
| | VCMTX mismatch when output is Differential-1 or Differential-0 | \|ΔVCMTX(1,0)\| | NA | NA | 5 | mV |
| | HS transmit differential voltage | \|VOD\| | 140 | 200 | 270 | mV |
| | VOD mismatch when output is Differential-1 or Differential-0 | \|ΔVOD\| | NA | NA | 10 | mV |
| | HS output high voltage | VOHHS | NA | NA | 360 | mV |
| | Single ended output impedance | ZOS | 40 | 50 | 62.5 | Ω |
| | Single ended output impedance mismatch | ΔZOS | NA | NA | 10 | % |

## 3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Digital GPIO @3.3V | Input leakage current | Ii | Vin = 3.3V or 0V | NA | NA | 10 | uA |
| | Tri-state output leakage current | Ioz | Vout = 3.3V or 0V | NA | NA | 10 | uA |
| | High level input current | Iih | Vin = 3.3V, pulldown disabled | NA | NA | 10 | uA |

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | | Vin = 3.3V, pulldown enabled | NA | NA | 110 | uA |
| | Low level input current | Iil | Vin = 0V, pullup disabled | NA | NA | 10 | uA |
| | | | Vin = 0V, pullup enabled | NA | NA | 110 | uA |
| Digital GPIO @1.8V | Input leakage current | Ii | Vin = 1.8V or 0V | NA | NA | 10 | uA |
| | Tri-state output leakage current | Ioz | Vout = 1.8V or 0V | NA | NA | 10 | uA |
| | High level input current | Iih | Vin = 1.8V, pulldown disabled | NA | NA | 10 | uA |
| | | | Vin = 1.8V, pulldown enabled | NA | NA | 60 | uA |
| | Low level input current | Iil | Vin = 0V, pullup disabled | NA | NA | 10 | uA |
| | | | Vin = 0V, pullup enabled | NA | NA | 60 | uA |

## 3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for PLL

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| PLL | Input clock frequency(Int) | $F_{in}$ | Fin = FREF @3.3V/1.1V | 1 | | 800 | MHz |
| | Input clock frequency(Frac) | $F_{in}$ | Fin = FREF @3.3V/1.1V | 10 | | 800 | MHz |
| | VCO operating range | $F_{vco}$ | Fvco = Fref * FBDIV @3.3V/1.1V | 800 | | 3200 | MHz |
| | Output clock frequency | $F_{out}$ | Fout = Fvco/POSTDIV @3.3V/1.1V | 16 | | 3200 | MHz |
| | Lock time | $T_{lt}$ | @ 3.3V/1.1V, FREF=24M,REFDIV=1 | | 250 | 500 | Input clock cycles |
| | VDDHV current consumption | | Fvco = 1000MHz, @3.3V Current scale as $(Fvco/1GHz)^{1.5}$ | | 1.0 | 1.2 | mA |
| | VDD Current consumption | | VDD =1.1V | | 1.3 | 1.56 | uA/MHz |
| | Power consumption (power-down mode) | | PD=HIGH, @27 ℃ | | 13 | | uA |

*Notes:*

① *REFDIV is the input divider value;*

② *FBDIV is the feedback divider value;*

③ *POSTDIV is the output divider value*

## 3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-6 Electrical Characteristics for USB 2.0 Interface

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Transmitter | | | | | | |
| High output level | VOH | | 2.8 | NA | NA | V |
| Low output level | VOL | | NA | NA | 0.3 | V |
| Output resistance | ROUT | Classic mode (Vout = 0 or 3.3V) | 40.5 | 45 | 49.5 | ohms |
| | | HS mode (Vout = 0 to 800mV) | 40.5 | 45 | 49.5 | ohms |
| Output Capacitance | COUT | seen from D+ or D- | | | 3 | pF |
| Output Common Mode Voltage | VM | Classic (LS/FS) mode | 1.45 | 1.65 | 1.85 | V |
| | | HS mode | 0.175 | 0.2 | 0.225 | V |
| Differential output signal high | VOH | Classic (LS/FS); Io=0mA | 2.97 | 3.3 | 3.63 | V |
| | | Classic (LS/FS); Io=6mA | 2.2 | NA | NA | V |
| | | HS mode; Io=0mA | 360 | 400 | 440 | mV |
| Differential output signal low | VOL | Classic (LS/FS); Io=0mA | -0.33 | 0 | 0.33 | V |
| | | Classic (LS/FS); Io=6mA | NA | 0.3 | 0.8 | V |
| | | HS mode; Io=0mA | -40 | 0 | 40 | mV |
| Receiver | | | | | | |
| Receiver sensitivity | RSENS | Classic mode | | +-250 | | mV |
| | | HS mode | | +-25 | | mV |
| Receiver common mode | RCM | Classic mode | 0.8 | 1.65 | 2.5 | V |
| | | HS mode (differential and squelch comparator) | 0.1 | 0.2 | 0.3 | V |
| | | HS mode (disconnect comparator) | 0.5 | 0.6 | 0.7 | V |
| Input capacitance (seen at D+ or D-) | | | NA | NA | 3 | pF |
| Squelch threshold | | | 100 | 112 | 150 | mV |
| Disconnect threshold | | | 570 | 590 | 625 | mV |
| High input level | VIH | | NA | 1.0 | NA | V |
| Low input level | VIL | | NA | 0 | NA | V |

## 3.7 Electrical Characteristics for DDR IO

Table 3-7 Electrical Characteristics for DDR IO

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| DDR IO @DDR3 mode | Input leakage current, SSTL mode, unterminated | | @ 1.5V , 125℃ | NA | 0 | | uA |
| DDR IO @DDR3L mode | Input leakage current | | @ 1.35V , 125℃ | NA | 0 | NA | nA |

| Parameters | | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| DDR IO @LPDDR2/LPDDR3 mode | Input leakage current | | @ 1.2V , 125℃ | NA | 0 | 0.49 | nA |
| DDR IO @DDR4 mode | Input leakage current | | @ 1.2V , 125℃ | -5 | 0 | +5 | uA |

## 3.8 Electrical Characteristics for TSADC

Table 3-8 Electrical Characteristics for TSADC

| Parameters | Symbol | Test condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Temperature Resolution | | | | 5 | | ℃ |
| Temperature Range | | | -20 | | 120 | ℃ |
| Analog power | IAVDD | Fs= 50KS/s | | 190 | | uA |
| Digital power | IVDD | Fs= 50KS/s | | 10 | | uA |
| Clock Frequency | Fclk | Fclk | | | 50 | KHz |
| Power Down Current from Analog | IAVDD | Power down | | 1 | | uA |
| Power Down Current from Digital | IVDD | Power down | | 1 | | uA |

## 3.9 Electrical Characteristics for MIPI DSI

Table 3-9 Electrical Characteristics for MIPI DSI

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| HS TX static common-mode | Vcmtx | | 150 | 200 | 250 | mV |
| Vcmtx mismatch when output is Differential-1 or Differential-0 | ΔVcmtx(1,0) | | | | 5 | mV |
| HS Transmit differential voltage | Vod | | 140 | 200 | 270 | mV |
| Vod mismatch when output is Differential-1 or Differential-0 | ΔVod | | | | 10 | mV |
| HS output high voltage | Vohhs | | | | 360 | mV |
| Single ended output impedance | Zos | | 40 | 50 | 62.5 | Ohm |
| Single ended output impedance mismacth | ΔZos | | | | 10 | % |
| The venin output high level | Voh | | 0.9 | 1 | 1.1 | V |
| The venin output low level | Vol | | -50 | | 50 | mV |
| Output impedance of LP | Zolp | | 110 | | | Ω |
| High-level output voltage | Voh | | 3 | 3.3 | | V |
| Low-level output voltage | Vol | | | 0 | 0.2 | V |
| Output impedance | Zolp | | 40 | | 460 | Ω |
| Common-mode variations above 450 MHz | ΔVcmtx(HF) | | | | 15 | mVrms |

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Common-mode variations between 50MHz – 450MHz | ΔVcmtx(LF) | | | | | mVpeak |
| 20%-80% rise time and fall time | Tr and Tf | | | | 0.3 | UI |
| | | | 150 | | | ps |
| Maximum data rate | Dmax | | | 200 | | Mbit/s |
| 15%-85% rise time and fall time | Trlp/Tflp | | 1 | 1.5 | 2 | ns |
| Slew rate, transition region | SR | | 20 | 27 | 30 | V/ns |

# 3.10 Electrical Characteristics for MIPI CSI

Table 3-10 Electrical Characteristics for MIPI CSI

| Parameters | Symbol | Test condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| Common-mode voltage HS receive mode | Vcmrx(dc) | | 70 | | 300 | mV |
| Differential input high threshold | Vidth | | | | 70 | mV |
| Differential input low threshold | Vidtl | | -70 | | | mV |
| Single-ended input high voltage | Vihhs | | | | 460 | mV |
| Single-ended input low voltage | Vilhs | | -40 | | | mV |
| Single-ended threshold for HS termination enable | Vterm-en | | | | 450 | mV |
| Differential input impedance | Zid | | 80 | 100 | 125 | Ω |
| Logic 1 input voltage | Vih | | 880 | | | mV |
| Logic 0 input voltage, not in ULP state | Vil | | | | 550 | mV |
| Logic 0 input voltage, ULP state | Vil-ulps | | | | 300 | mV |
| Input hysteresis | Vhyst | | 25 | | | mV |
| Common-mode interference beyond 450 MHz | ΔVcmrx(HF) | | | | 100 | mV |
| Common-mode interference 50MHz-450MHz | ΔVcmrx(LF) | | -50 | | 50 | mV |
| Common-mode termination | Ccm | | | | 60 | pF |
| Input pulse rejection | Espike | | | | 300 | V.ps |
| Minimum pulse width response | Tmin-rx | | 20 | | | ns |
| Peak interference amplitude | Vint | | | | 200 | mV |
| Interference frequency | Fint | | 450 | | | MHz |

# Chapter 4 Thermal Management

## 4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

## 4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

| Parameter | Symbol | Typical | Unit |
|---|---|---|---|
| Junction-to-ambient thermal resistance | $\boldsymbol{\theta_{JA}}$ | 26.9 | (℃/$\boldsymbol{W}$) |
| Junction-to-board thermal resistance | $\boldsymbol{\theta_{JB}}$ | N/A | (℃/$\boldsymbol{W}$) |
| Junction-to-case thermal resistance | $\boldsymbol{\theta_{JC}}$ | 8.2 | (℃/$\boldsymbol{W}$) |

*Note: The testing PCB is 4 layers,* 114.3*mmx* 101.5*mm, 1.6mm thickness, Ambient temperature is 25℃.*