Key Features

Processors

- Quad-core Arm® Cortex®-A7
  - L1 32 KB I/D-cache per core + L2 512 KB
- Single-core RISC-V E907
  - 16 KB I-cache+16 KB D-cache

Memory & Storage

- 16-bit DDR3/DDR3L/DDR4
- 160 KB SRAM
- SD 2.0/3.0, eMMC 5.0/5.1, SPI Flash

ISP

- Up to 2 sensor inputs
- Time Division Multiplexing (TDM) mode
- Maximum frame rate: 1M@30fps online, 2M@30fps offline

Video Input

- Parallel CSI Interface
  - 8/10/12/16-bit width
  - BT.656, BT.601, BT.1120, and Digital Camera (DC) protocol
  - BT.656 up to 2*720P@30fps and BT.1120 up to 2*1080P@30fps
- MIPI CSI Interface
  - 4-/2+2/1+1+1-lane MIPI CSI, up to 1.0 Gbit/s per lane

Video output

- 1x RGB, up to 1920x1080@60fps
- 1x dual-link LVDS, up to 1920x1080@60fps
- 1x 4-lane MIPI DSI output, up to 1920x1080@60fps and 1.0 Gbit/s per lane

Audio

- 1x DAC
- 1 x audio output: LINEOUTP/N
- 3x I2S
- 1x 8-channel DMIC, up to 8 KHz-48 KHz sampling rate
- 1x OWA input and 1x OWA output

Automation Connectivity

- 3x RMII/RGMII
- 2x CAN-FD
- 1x 8-/16-/32-bit Local Bus

General Connectivity

- 1x USB2.0 DRD, 1x USB2.0 Host
- 2x SDIO 3.0
- 4x SPI
- 10x UART
- 6x TWI
- 30-channel PWM (multiplex with 16-channel PWMCS OUT&16-channel PWMCS IN)
- 24-channel GPADC
- 4-channel TPADC
- 1x LEDC
- 4x IR_RX, 1x IR_TX

Security Subsystem

- AES/DES/3DES/SM4 symmetrical algorithm
- MD5/SHA/HMAC/SM3 hash algorithm
- RSA/ECC/SM2 public key algorithm
- PRNG/TRNG random bit generate algorithm
- Supports secure boot
- Supports secure memory isolation

Device summary

Orderable Device(s)	Package
T153MX-BCX	WBBGA 327 balls, 13 mm x 13 mm size
T153M4-QCX T153M3-QCX T153L3-QXX	eQFP 128 pins, 14 mm x 14 mm size

See Table 2-1 Ordering Information

Revision History

Revision	Date	Author	Description
0.90	November 13, 2025	KPA0570	Initial Version Release
0.91	December 18, 2025	KPA0570	**Chapter 4 Pin Description** Update the PIN No. 11, 12, 127, 128 functions as GND-CPU，VDD-CPU1, VDD-CPU2, VDD-CPU3 for the chip model T153Mx-QCX **Chapter 7 Pin Assignment** 1. Update the PIN No. 11, 12, 127, 128 functions as GND-CPU，VDD-CPU1, VDD-CPU2, VDD-CPU3 in section 7.1.1.2 T153Mx-QCX Pin Map 2. Update the T153Mx-QCX package dimension in section 7.1.2.2
0.92	February 6, 2026	KPA0570	1. In the T153Mx-QCX packages, the Power Pin VCC-PA-PD is changed to VCC-PD, and the power pin VCC-PK is changed to VCC-PA-PK. 2. Add “VCC-PA must power on after VCC18-ADC." to the description of the power-up sequence in section 5.11.1.1 WBBGA Power-Up Sequence. 3. Update WBBGA Power-Up/Down Sequence in section 5.11.1.1 and 5.11.2.1. 4. Update eQFP Power-Up/Down Sequence in section 5.11.1.2 and 5.11.2.2. 5. Add Figure 9 3 Measuring the QFP Reflow Soldering Process in section 9 Reflow Profile.

Content

Figures

Tables

About This Document

Purpose and Scope

The documentation describes features of each module, pin/signal characteristics, current consumption, interface timing, thermal and package of the T153 family. For details about register descriptions of each module, see the *T153_User_Manual*.

Intended Audience

The document is intended for:

- Hardware designers and maintenance personnel for electronics
- Sales personnel for electronic parts and components

Related Documentation

For a complete listing of related documentation and development-support tools for the device, contact the Allwinner FAE or access the Allwinner Customer Service Platform by visiting https://open.allwinnertech.com/.

Revision Number Definition

Revision 0.90-0.9x

This document is released based on the design completion products yet to be mass-produced. Therefore, the information in this document may be modified by reason of mass-produced verification.

All statements, information and recommendations in this document do not constitute any express or implied representation or warranty (including, but not limited to, the warranties of fitness for a particular purpose, merchantability, non-infringement, and accuracy and completeness of the document). Allwinner shall not be liable for any person's use of such information or/and this document.

If you have any questions about the document, please contact us to confirm and obtain the latest version.

Conventions

Symbol Conventions

The symbols that may be found in this document are defined as follows.

Symbol	Description
 CAUTION	A caution means that damage to equipment is possible.
 NOTE	Provides additional information to emphasize or supplement important points of the main text.

Table Content Conventions

The table content conventions that may be found in this document are defined as follows.

Symbol	Description
-	The cell is blank.

Numerical System

The expressions of the data capacity, the frequency, and the data rate are described as follows.

Type	Symbol	Value
Data capacity	K	1024
	M	1,048,576
	G	1,073,741,824
Frequency, data rate	k	1000
	M	1,000,000
	G	1,000,000,000

FT/QA/QC Test

All Allwinner chips provided for clients have passed the following tests.

Test Item	Description
FT Test	FT test is the finished product testing after the chip is packaged, and it is a functional test of all modules for each produced chip.
QA Test	QA test is a system-level sampling test for good-quality chips. According to the application level of the chip, a certain percentage of good-quality chips are selected for system-level testing to make the chip work in a typical application scenario, and judge whether the chip works normally in this scenario.

Test Item	Description
QC Test	QC test is a module-level sampling test for good-quality chips. According to the chip application level, a certain percentage of good-quality chips are selected for module-level functional testing to monitor whether the chip production process is normal.

1 Overview

T153 is a quad-core architecture solution targeted for automation applications, such as programmable logic controllers (PLCs), human-machine interface (HMI), etc.

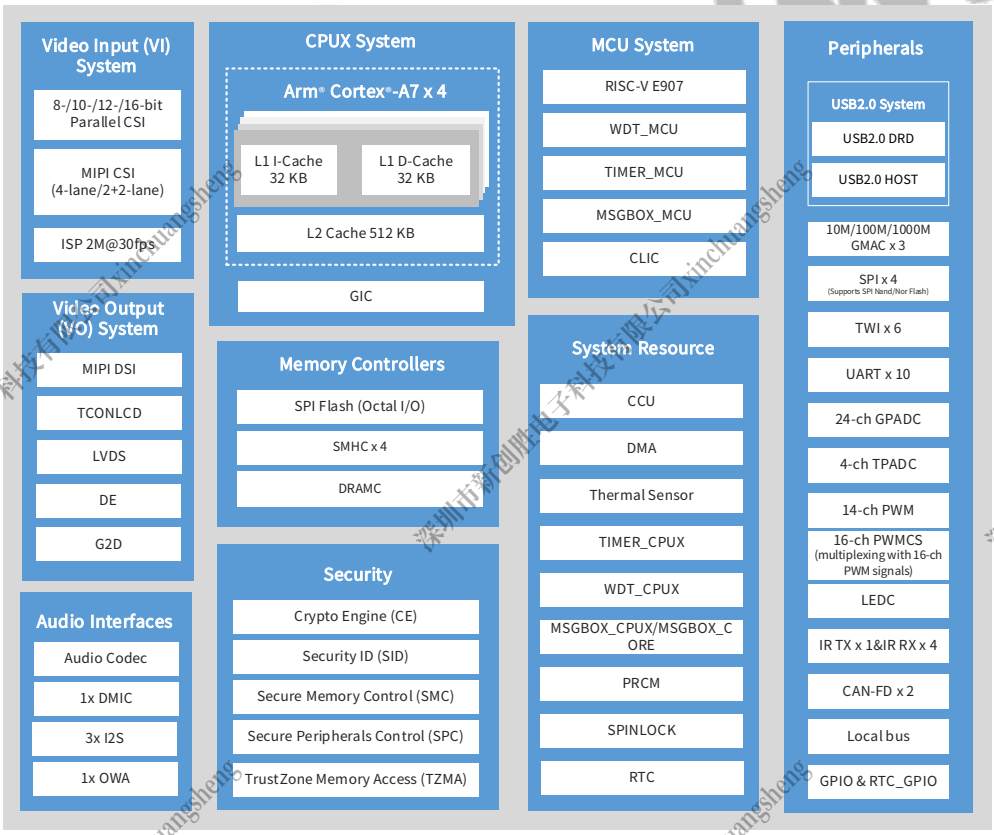
Equipped with a quad-core Arm® Cortex®-A7, a single-core RISC-V E907, and support for DDR3/DDR3L/DDR4 memory, the T153 delivers powerful compute performance and fast response, making it ideal for demanding automation tasks.

The processor features three Gigabit Ethernet interfaces, two CAN_FD interfaces, and 16-/32-bit local bus, supporting high-throughput networking for complex data-driven use cases. Its integrated image signal processor and display engine enable clear, real-time visual feedback for managing intricate manufacturing processes.

With extensive peripheral support, the T153 offers 24-channel GPADC, 6 TWIs, 30-channel PWM. These interfaces provide flexibility for diverse applications, enabling easy integration and scalability in automation systems.

The following figure shows the system block diagram for the device.

Figure 1-1 System Block Diagram



NOTE

Some modules shown in this block diagram are not offered on all devices, please refer to Table 2-1 Ordering Information for details.

2 Ordering Information

The following table provides the differences of orderable device(s) covered by this document.

Table 2-1 Ordering Information

Features	T153MX-BCX	T153M4-QCX	T153M3-QCX	T153L3-QXX
CPU	4xA7, 1xE907	4xA7, 1xE907	4xA7, 1xE907	4xA7
DDR	External DDR3/DDR3L/DDR4	SIP 256MB DDR3	SIP 128MB DDR3	SIP 128MB DDR3
CAN-FD	2 x CAN-FD	2 x CAN-FD	2 x CAN-FD	Not Support
Local Bus	1 x 32-bit local bus	1 x 32-bit local bus	1 x 32-bit local bus	Not Support
GMAC	RMII/RGMII 0/1/2	RMII/RGMII 0/1/2	RMII/RGMII 0/1/2	RMII/RGMII 0/1
SDIO2.0/3.0	2 (SDC1/3)	1 (SDC1)	1 (SDC1)	1 (SDC1)
MIPI CSI	4-lane/2+2/1+1+1-lane	4-lane	4-lane	4-lane
Parallel CSI	8/10/12/16-bit width	8-bit width	8-bit width	8-bit width
Line out	Differential (LINEOUTP/N)	Single-end (LINEOUTP)	Single-end (LINEOUTP)	Single-end (LINEOUTP)
OWA	IN/OUT	OUT	OUT	OUT
I2S	3 (I2S0/1/2)	2 (I2S1/2)	2 (I2S1/2)	2 (I2S1/2)
SPI	4 (SPI0/1/2/3)	3 (SPI0/1/3)	3 (SPI0/1/3)	3 (SPI0/1/3)
TWI	6 (TWI0/1/2/3/4/5)	5 (TWI0/1/2/4/5)	5 (TWI0/1/2/4/5)	5 (TWI0/1/2/4/5)
GPADC	24 channels	16 channels	16 channels	16 channels
PWM&PWMCS	30 channels (multiplexing with 16-ch PWMCS IN, 16-ch PWMCS OUT)	22 channels (multiplexing with 14-ch PWMCS IN, 16-ch PWMCS OUT)	22 channels (multiplexing with 14-ch PWMCS IN, 16-ch PWMCS OUT)	22 channels (multiplexing with 14-ch PWMCS IN, 16-ch PWMCS OUT)
GPIO	140 I/Os	90 I/Os	90 I/Os	90 I/Os
Package	WBBGA 327 balls, 13 mm x 13 mm	eQFP 128 pins, 14 mm x 14 mm	eQFP 128 pins, 14 mm x 14 mm	eQFP 128 pins, 14 mm x 14 mm

3 Features

3.1 Processors

- Armv7 Architecture quad-core Arm® Cortex®-A7
  - 32 KB L1 I -cache + 32 KB L1 D-cache per core
  - 512 KB L2 cache
- RISC-V E907

3.2 Memory

3.2.1 Boot ROM (BROM)

- Supports CPU0 Boot Process
- Supports system boot from the following devices:
  - SD Card
  - eMMC
  - SPI NOR Flash (Quad Mode and Single Mode)
  - SPI NAND Flash
- Supports GPIO to select the kind of boot media to boot
- Supports eFuse to select the kind of boot media to boot
- Supports Normal Boot and Secure Boot
- Supports loading only certified firmware in Secure Boot
- Ensures that the Secure Boot is a trusted environment

3.2.2 SRAM

- 160 KB SRAMC, mainly used for boot0, hibernation, and wakeup
- 16 KB DE_SHARE_SRAM can be shared with system during boot process.

3.2.3 SDRAM

- 16-bit DDR3/DDR3L/DDR4
- Clock frequency up to 933 MHz for DDR3 and DDR3L
- Clock frequency up to 1066 MHz for DDR4

3.2.4 SD/MMC Host Controller (SMHC)

- Four SD/MMC Host Controller (SMHC) interfaces
  - SMHC0, compliant with the protocol Secure Digital Memory (up to SD3.0)

- SMHC1/3, compliant with the protocol Secure Digital I/O (up to SDIO3.0)
- SMHC2, compliant with the protocol Multimedia Card (up to eMMC5.1)

- The SMHC0 and the SMHC1/3 support the following:
  - 1-bit or 4-bit data width
  - Maximum performance:
    - SDR mode 200 MHz@1.8 V IO pad
    - DDR mode 50 MHz@1.8 V IO pad
    - SDR mode 50 MHz@3.3 V IO pad
- The SMHC2 supports the following:
  - 1-bit, 4-bit, or 8-bit data width
  - Supports HS400 mode and HS200 mode
  - Maximum performance:
    - SDR mode 200 MHz@1.8V IO pad
    - DDR mode 150 MHz@1.8V IO pad
    - SDR mode 50 MHz@3.3V IO pad
    - DDR mode 50 MHz@3.3V IO pad
- Supports block size of 1 to 65535 bytes
- Supports hardware CRC generation and error detection

3.2.5 SPI Flash Controller (SPIF)

- Supports multiple SPI modes
  - Standard SPI
  - Dual-Input/Dual-Output SPI, and Dual-I/O SPI
  - Quad-Input/Quad-Output SPI, Quad-I/O SPI, and QPI
  - Octal-Input/Octal-Output SPI, Octal-I/O SPI, and OPI
  - 3-wire SPI with programmable serial data frame length of 1 bit to 32 bits
- Supports XIP mode of operation for executing code from FLASH memory
- Supports STR mode and DTR mode, and DTR mode supports DQS signal
- High Speed Clock Frequency
  - 150MHz for STR Mode
  - 100MHz for DTR Mode
- Software Write Protection
  - Write protect all/portion of memory via software
  - Top/Bottom Block protection
- Programmable delays between transactions
- Supports data sample mode0, mode1, mode2 and mode3
- Supports Control signal configuration
  - One chip selection
  - Polarity and phase of the Chip Select (SPIF_CS) and SPI Clock (SPIF_CLK) are configurable

- Supports data scramble/descramble
- Supports private DMA
  - Supports chain transmission
  - Supports descriptor in 8-word length
- Supports byte transfer

3.3 Image Processing

3.3.1 Image Signal Processor (ISP)

- Support multiple sensors (up to 2) input
- Support raw8/10/12
- Maximum resolution:
  - online: 1280x4224
  - offline: 1920x4224
- Performance of one sensor:
  - online: 1M@30fps (linear)
  - offline: 2M@30fps (linear)
- Support multiple data streams (up to 4) output
  - Support YUV422/YUV420/RGB888/RGB565 output
  - Support graphics mirror and flip
  - Support 1/64~1x scale down
- Support ISP adjustment tool on the PC
- Support Algorithm Features:
  - Crop
  - Dynamic Range Compression (DRC)
  - Black Level Correction
  - Digital Gain
  - White Balance
  - Len Shading Correction (LSC)
  - Gamma Correction
  - Defect Pixel Correction (DPC)
  - Cross Talk Correction (CTC)
  - Noise Reduction (2D)
  - Bayer Interpolation
  - Sharpness
  - Color Enhancement (3D-LUT)
  - Adjustable 2A functions: Automatic White Balance (AWB), Automatic Exposure (AE)
  - Supports Anti-flick Detection Statistics
  - Histogram Statistics

3.4 Graphics Processing

3.4.1 Display Engine (DE)

- One display output, up to 1080P
- Two alpha blending channels optional
- Four overlay layers in UI channel, one overlay layers in video channel.
- Video channel and UI channel share one scaler function.
- Supports potter-duff compatible blending operation
- Supports dither output to TCON
- Supports 3DFIFO for Dual Link LVDs to display
- Input format
  - Semi-planar of YUV422/YUV420/YUV411
  - Planar of YUV422/YUV420/ YUV411
  - ARGB8888/XRGB8888/RGB888/ARGB4444/ARGB1555/RGB565
- Support Frame Packing/Top-and-Bottom/Side-by-Side Full/Side-by-Side Half 3D format data.
- SmartColor2.0 for excellent display experience
  - Flesh tone protection
  - Hue gain, saturation gain, and value gain controller
  - Fully programmable color matrix
  - Dynamic gamma
  - 17x17x17 programmable 3D LUT
- Supports write back for verification
- Supports RGB444/RGB565/RGB666 with dither function

3.4.2 Graphic 2D (G2D)

- Supports mixer layer size up to 2048x2048 pixels, rotate size up to 4096x4096 pixels
- Supports gradient color fill
- Supports pre-multiply alpha image data
- Supports color key
- Supports two pipes Porter-Duff alpha blending
- Supports multiple video formats 4:2:0, 4:2:2, 4:1:1 and multiple pixel formats (8/16/24/32 bits graphics layer)
- Supports memory scan order option
- Supports any format convert function above
- Supports 1/16x to 32x resize ratio
- Supports 32-phase 8-tap horizontal anti-alias filter, 32-phase 4-tap vertical anti-alias filter.
- Supports window clip
- Supports FillRectangle, FillGradient, BitBlt, StretchBlt and MaskBlt
- Supports horizontal and vertical flip, clockwise 0/90/180/270 degree rotate

- Supports 4 Thread RCQ function for mixer and rotate
- Supports dither

3.5 Video Input Interfaces

3.5.1 MIPI CSI

- Complaint with MIPI CSI-2 specification v1.1 and MIPI D-PHY specification v1.0
- 1.0 Gbit/s per lane
- Configurable number of data lanes and sequence of data lanes for MIPI interface:
  - 4-lane
  - 2+2-lane
  - 1+1+1-lane
- Pixel formats
  - RAW 8/10/12/14/16 bit
  - YUV422 8 bit
  - YUV420 8 bit
  - RGB888 and RGB565

3.5.2 Parallel CSI

- Supports 8/10/12/16-bit width
- Supports BT.656 2-channel time-multiplexed format
- Supports Digital Camera (DC), BT.656, BT.601, and, BT.1120 protocol
- Dual Data Rate (DDR) sample mode with maximum pixel clock of 148.5MHz
- Supports BT656 2CH 720P@30fps
- Supports BT1120 2CH 1080P@30fps

3.6 Video Output Interfaces

3.6.1 LCD

- One panel interface
  - RGB interface with DE/SYNC RGB mode, up to 1920x1080@60fps
  - Serial RGB interface, up to 800 x 480@60fps
  - i8080 interface, up to 800x480@60fps
  - RGB888, RGB666 and RGB565 pixel formats
  - Supports BT.656 interface

3.6.2 LVDS

- Two LVDS interfaces

- Up to 1920x1080@60fps for dual-link
- Up to 1366x768@60fps for single-link

3.6.3 MIPI DSI

- Compliant with MIPI DSI specification v1.02 and MIPI D-PHY specification v1.0
- Up to 1.0 Gbit/s per lane
- Supports one 4-lane MIPI DSI display, up to 1920x1080@60fps

3.7 System Peripherals

3.7.1 Clock Controller Unit (CCU)

- Three clock sources: an on-chip 16 MHz RC oscillator, an external 24 MHz HOSC, and an external 32.768 kHz LOSC
- Supports clock configuration, clock generation, gating, and reset for modules
- Phase-Locked Loop (PLL) management (5 PLLs: PLL_PERI0, PLL_PERI1, PLL_VIDEO0, PLL_AUDIO0, PLL_CPU)

3.7.2 Power Reset Clock Management (PRCM)

- Bus gating, bus reset, and clock configuration

3.7.3 Message Box (MSGBOX)

- Two sets of system general-purpose MSGBOXs for communication between CPUX subsystem and MCU subsystem.
  - MSGBOX_CPUX: MCU write, CPUX read
  - MSGBOX_MCU: CPUX write, MCU read
- Four sets of separate MSGBOXs for priority adjustment among four A7 cores
  - MSGBOX_CORE0: CORE1/2/3 write, CORE0 read
  - MSGBOX_CORE1: CORE0/2/3 write, CORE1 read
  - MSGBOX_CORE2: CORE0/1/3 write, CORE2 read
  - MSGBOX_CORE3: CORE0/1/2 write, CORE3 read
- Supports interrupts

3.7.4 Spinlock

- Supports 32 lock units
- Two lock status: locked and unlocked
- Lock time of the processor is predictable, which is less than 200 cycles

3.7.5 RTC

- Provides a 16-bit counter for counting day, 5-bit counter for counting hour, 6-bit counter for counting minute, 6-bit counter for counting second
- Uses a 32.867 kHz low-frequency oscillator as the count clock
- 1 kHz counting frequency
- Configurable initial value by software anytime
- Supports alarm function that can generate interrupts and wake up peripheral devices
- Supports fanout function of internal 32.768 kHz clock
- 8 general purpose registers for storing power-off information in RTC domain
- Supports recording reboot events

3.7.6 Thermal Sensor Controller (THS)

- Two thermal sensors, distributed in CPU and DDR.
- Averaging filter for thermal sensor reading
- Supports over-temperature protection interrupt and over-temperature alarm interrupt
- Supports ±3°C error limit from 60°C to 125°C, and ±5°C from -40°C to 60°C

3.7.7 Timer

- Twelve programmable 56-bit down timers
- Configurable counting clock: 32KHz, 24MHz, 16MHz, or 200MHz
- Two working modes: periodic mode and single count mode
- Generates an interrupt after counting ends

3.7.8 Watchdog Timer (WDT)

- Two watchdog timers
- Supports over 1-minute timeout
- Supports the generation of timeout interrupts
- Supports the generation of timeout reset signals
- Supports restarting timing by watchdog
- Supports the generation of reset signals through software configuration

3.8 Audio

3.8.1 Audio Codec

- One audio differential lineout output: LINEOUTP/N
- One audio digital-to-analog converter (DAC) channel
  - 16-bit and 20-bit sample resolution

- 8 kHz to 192 kHz DAC sample rate
- 99 ± 3 dB SNR@A-weight, -83 ± 3 dB THD+N

- Analog audio outputs: one differential lineout output, it can be configured as a single-ended output
- Supports Dynamic Range Controller adjusting the DAC playback
- TX_FIFO with 128 depths for DAC data transmit
- Programmable FIFO thresholds
- Supports interrupts and DMA

3.8.2 I2S/PCM

- Three I2S/PCM interfaces (I2S0, I2S1, and I2S2)
  - I2S0/2 support 4-lane application
  - I2S1 supports 2-lane application
- Compliant with standard Philips Inter-IC sound (I2S) bus specification
  - Left-justified, Right-justified, PCM mode, and TDM format
  - Programmable PCM frame width: 1 BCLK width (short frame) and 2 BCLKs width (long frame)
- Transmit and receive data FIFOs
  - Programmable FIFO thresholds
  - TXFIFO with 128 depths, RXFIFO with 64 depths
- Supports multiple function clocks
  - Clock up to 24.576 MHz Data Output of I2S/PCM in Master mode
  - Clock up to 12.288 MHz Data Input of I2S/PCM in Master mode
- Supports TX/RX DMA slave interface
- Supports multiple application scenarios
  - Up to 16 channels (fs = 48 kHz) which has adjustable width from 8 bits to 32 bits
  - Sample rate from 8 kHz to 384 kHz (sample rate * channel * slot width ⩽ 24.576 MHz)
  - 8-bit u-law and 8-bit A-law companded sample
- Supports master/slave mode

3.8.3 DMIC

- One DMIC interface
- Supports PDM master receiver mode
- Receives Data FIFO:
  - RX_FIFO with 128 depths for audio data receiving
  - Programmable FIFO thresholds
- Supports RX DMA slave interface
- Supports interrupts
- Supports multiple application scenarios:

- Up to 8 channels
- Each channel can enable and disable individually
- Sample rate: 8KHz~48KHz
- Oversample rate: 64*fs/128*fs
- Sample resolution: 16bits/24bits

- Programmable channels exchange and mapping
- Supports High Pass Filter and Digital Volume Controller

3.8.4 One Wire Audio (OWA)

- One OWA TX and One OWA RX, compliant with S/PDIF interface
- Compatible with IEC-60958 and IEC-61937
  - IEC-60958 supports data formats: 16 bits, 20 bits, and 24 bits
- Transmit and Receive data FIFOs
  - TXFIFO with 128 depths, RXFIFO with 64 depths
  - Programmable FIFO thresholds
- Supports TX/RX DMA Slave interface
- Supports Multiple function clock
  - Separate OWA TX and RX clock
  - OWA TX function clock includes a series of 24.576 MHz/49.152 MHz and 22.579 MHz frequency (TX function clock 49.152 MHz support ample rate 384 KHz)
  - OWA RX function clock includes a series of 400 MHz frequency（RX function clock 40 0MHz support CDR of sample rate from 8 KHz to 384 KHz）
- Supports Hardware Parity On TX/RX
  - Hardware Parity generation on the transmitter
  - Hardware Parity checking on the receiver
- Supports channel status capture on the receiver
- Supports channel sample rate capture on the receiver
- Supports insertion detection for the receiver
- Supports channel status insertion for the transmitter

3.9 Peripheral Interfaces

3.9.1 GMAC

- Three 10/100/1000 Mbit/s Ethernet port with RGMII and RMII PHY interface
- Compliant with IEEE 802.3-2015 standard
- Supports both full-duplex and half-duplex operation
- Full-duplex flow control

- IEEE 1588-2008 for precision networked clock synchronization, supports Ethernet packet timestamping as described in IEEE 1588-2002 and IEEE 1588-2008
- Programmable frame length to support Standard or Jumbo Ethernet frames with sizes up to 16 KB
- Source Address field and VLAN insertion or replacement, Double VLAN
- Transmits TCP/IP Checksum Offload
- Supports a variety of flexible address filtering modes (include Hash filter function)
- Optimization for packet-oriented DMA transfers with frame delimiters
  - Supports linked-list descriptor list structure
  - Descriptor architecture, allowing large blocks of data transfer with minimum CPU intervention: each descriptor can transfer up to 32 KB of data
  - Comprehensive status reporting for normal operation and transfers with errors
- Supports 4KB TXFIFO for transmission packets and 8KB RXFIFO for reception packets
- Supports 16 Descriptors Descriptor Pre-fetch cache for TXDMA and RX DMA
- Programmable interrupt options for different operational conditions
- Supports MDIO (Clause22 and Clause45) Interface for PHY device configuration and management
- Configurable big-endian and little-endian mode for Transmit and Receive paths
- Supports statistics on the received and transmitted packets
- Split Header Support
- Supports Energy Efficient Ethernet (EEE)

3.9.2 CAN-FD

- Two CAN-FD ports (up to 64 data bytes)
- Conforms with ISO 11898-1:2015
- Supports CAN 2.0A and 2.0B protocol specification
- Supports AUTomotive Open System ARchitecture (AUTOSAR)
- Supports SAE J1939 standards
- CAN error logging
- Improved acceptance filtering
- Two configurable receive FIFOs
- Separate signaling on reception of high priority messages
- Up to 64 dedicated receive buffers
- Up to 32 dedicated transmit buffers
- Configurable transmit FIFO
- Configurable transmit queue
- Configurable transmit event FIFO
- Direct message RAM access for host CPU
- Supports DMA Master

3.9.3 Local Bus Controller (LBC)

- One local bus controller with privatized synchronous transport protocol
  - Maximum interface speed: 150 MHz@16bits, 100MHz@32bits
  - Address bus and data bus time-multiplexed
  - 8/16/32-bit data width
  - Supports big endian and little endian
  - Parity check
  - FIX/INCR type address transmission with configurable burst length (maximum 128 beats in one transmission)
- Up to 4 chip selects
  - Independent timing parameter configuration for each chip select signal
  - Configurable polarity
- Multiple accessing methods
  - Direct access/indirect access/private DMA access
  - Indirect access supports data transfer through system DMA

3.9.4 USB2.0 DRD

- One USB2.0 DRD interface
- Supports USB Host Function
  - Compatible with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0
  - Compatible with Open Host Controller Interface (OHCI) Specification, Version 1.0a
  - Supports High-Speed (HS, 480 Mbps)
  - Supports Full-Speed (FS, 12 Mbps)
  - Supports Low-Speed (LS, 1.5 Mbps)
  - Supports only 1 USB Root Port shared between EHCI and OHCI
- Supports USB Device Function
  - Supports High-Speed (HS, 480 Mbps)
  - Supports Full-Speed (FS, 12 Mbps)
  - Supports bi-directional Endpoint0 for Control transfer
  - Supports up to 16 User-Configurable Endpoints for Bulk, Isochronous and Interrupt bi-directional transfers (Endpoint1-8)
  - Supports up to (8KB+64Bytes) FIFO for EPs (Including EP0)
  - Supports interface to an external Normal DMA controller for every EPs (Endpoint1-8)
- Supports an internal DMA Controller for data transfer with memory
- Supports High-Bandwidth Isochronous & Interrupt transfers
- Supports Automated splitting/combining of packets for Bulk transfers
- Supports point-to-point and point-to-multipoint transfer in both Host and Peripheral mode
- Supports Automatic ping capabilities
- Supports Soft connect/disconnect function

- Supports all transaction scheduling in hardware
- Power Optimization and Power Management capabilities
- Device and Host controller share an 8K SRAM and a physical PHY

3.9.5 USB2.0 Host

- One USB 2.0 Host interface
- Supports industry-standard AMBA High-Performance Bus (AHB) and it is fully compliant with the AMBA Specification, Revision 2.0. Supports bus.
- Includes an internal DMA Controller for data transfer with memory.
- Complies with Enhanced Host Controller Interface (EHCI) Specification, Version 1.0, and the Open Host Controller Interface (OHCI) Specification, Version 1.0a.
- Supports High-Speed (HS, 480-Mbps), Full-Speed (FS, 12-Mbps), and Low-Speed (LS, 1.5-Mbps) Device.
- Supports only 1 USB Root Port shared between EHCI and OHCI.

3.9.6 PWM

- One PWM controller has 14-channel PWM Input/Output
- 14 separate channel waveform output
  - Supports PWM periodic mode output
  - Supports PWM pulse mode output, and the pulse number is configurable
  - Output frequency range:
    - 0 to 24 MHz (when the clock source is DCXO)
    - 0 to 100 MHz (when the clock source is APB0 clock)
  - Various duty-cycle: 0% -100%
  - Minimum resolution: 1/65536
- 7 complementary pairs waveform output
  - Supports dead-zone generator, and the dead-zone time is configurable
- Up to 4 groups of waveform output for controlling stepping motors
  - Supports any plural channels to form a group, and output the same duty-cycle pulse
  - In group mode, the relative phase of the output waveform for each channel is configurable
- 14-channel input waveform capture
  - Supports rising/falling edge detection and falling edge detection
  - Supports pulse-width measurement
- 14-channel input waveform periodic count

3.9.7 PWMCS

PWMCS is compatible with the original PWM functionality and expands it with new features. There are two PWMCS controllers in this device, containing total 16 PWM channels which are multiplexed

with 16-channel PWMCS output and 16-channel PWMCS input. The following takes one PWMCS controller as an example to describe PWMCS features, and the two PWMCS controller are consistent.

- Supports waveform output
  - Up to 8-channel independent output
  - Up to 4-channel group mode output
  - Up to 4-channel complementary pairs mode output
  - Up to 4-channel IO pairs mode output
  - Supports cycle output (not support in group mode and IO pair mode) and pulse output
  - Supports outputting high/low level and high resistance
  - Configurable initial phase and polarity
  - Configurable pulse output suspension state
  - Supports pulse output delay
  - Configurable output waveform duty cycle (0-100%)
  - 0~4 MHz output frequency. Supports maximum and minimum frequency limit
- Supports input waveform capture
  - Up to 8-channel independent capture
  - Up to 4-channel IO pairs mode capture
  - Supports INDEX, STROB, software initiation and capture position counter
  - Supports input level detection
  - Supports input filter

3.9.8 SPI

- Four SPI controllers: SPI0, SPI2, and SPI3 support SPI mode; SPI1 supports SPI mode and DBI mode.

SPI mode

- Multiple SPI modes:
  - Master mode and slave mode for standard SPI
  - Master mode for Dual-Output/Dual-Input SPI and Dual I/O SPI
  - Master mode for Quad-Output/Quad-Input SPI
  - Master mode for 3-wire SPI, with programmable serial data frame length of 1 bit to 32 bits
  - Camera mode Dual-Input SPI
  - Camera mode Quad-Input SPI
- Master mode support the Maximum clock frequency: 100MHz
- Camera mode support the Maximum clock frequency: 50MHz
- Supports TX/RX DMA Slave interface
- Master mode and Slave mode supports Data Sample Mode
  - Mode0, Mode1, Mode2 and Mode3
- Master mode and Slave mode support Control signal configuration

- Multiple chip selects
  - SPI0 supports two chip select
  - SPI1/2/3 support three chip select
- Polarity and phase of the Chip Select (SPI_CS) and SPI Clock (SPI_CLK) are configurable

DBI Mode

- Supports DBI Type C 3 Line, 4 Line Interface Mode and 2 Data Lane Interface Mode
- Supports data source from CPU or DMA
- Supports RGB111/444/565/666/888 video format
- Supports Maximum resolution RGB666 240*320 @30HZ with Single Data Lane
- Supports Maximum resolution RGB888, 320*480 @30HZ or 240*320 @60HZ with Dual Data Lane
- Supports Tearing Effect
- Supports software flexible control video frame rate

3.9.9 UART

- Ten UART controllers (UART 0-9)
- Compatible with industry-standard 16450/16550 UARTs
- Transmit and Receive data FIFOs
  - UART0, UART6-9: RX-64 Layer, TX-64 Layer
  - UART1-5: RX-128 Layer, TX-128 Layer
- Supports baud rate generator from APB bus clock
  - Speed up to 1.5 Mbps with 24MHz APB clock
  - Speed up to 3.75 Mbps with 60MHz APB clock
  - Speed up to 5 Mbps with 80MHz APB clock
  - Speed up to 10 Mbps with 160MHz APB clock
- Supports 5-8 data bits and 1/1.5/2 stop bits
- Supports Even, Odd or No Parity
- Supports TX/RX DMA Slave interface
- Supports Software/ Hardware Flow Control
- Supports IrDA 1.0 SIR
- Supports RS-485/9-bit mode
- Supports RS-485 full duplex mode
- Supports Auto-Flow by using CTS & RTS (exclude UART0)

3.9.10 Two Wire Interface (TWI)

- Six TWI controllers: TWI0/1/2/3/4/5
- Supports master mode or slave mode
- Supports 7-bit standard address and 10-bit extended address.

- Supports standard mode (100 kbit/s), fast-mode (400 kbit/s)
- Supports general call and start byte.
- Clock Stretch up to 15 ms
- Master mode features:
  - Supports the bus arbitration in the case of multiple master devices.
  - Supports clock synchronization and bit and byte waiting.
  - Supports packet transmission and DMA
- Salve mode features:
  - Interrupt on address detection

3.9.11 General Purpose ADC (GPADC)

- 12-bit Resolution SAR type A/D converter
- Include 3 GPADCs:
  - GPADC0 has 10 channels
  - GPADC1 has 10 channels
  - GPADC2 has 4 channels, which is multiplexed with TPADC and can be enabled by PWM
- 64 FIFO depths of data register
- Analog Input Range: 0 to 1.8 V
- Maximum Sampling frequency: 2 MHz
- Supports data compare and interrupt
- Supports three operation modes
  - Single conversion mode
  - Continuous conversion mode
  - Burst conversion mode
- Supports calibration averaging filter

3.9.12 Touch Panel ADC (TPADC)

- A 12-bit SAR A/D converter provided
- A/D Conversion with Configurable sample frequency up to 750 KHz
- A/D can buffer up to 32 sample results
- Supports DMA Slave interface
- Supports Aux ADC with up to 4 channels
- Supports 4-Wire Resistive Touch Panel Input Detection
  - Supports Pen Down Detection with programmable sensitivity
  - Supports Single Touch Coordinate Measurement
  - Supports Dual Touch Detection
  - Supports Touch Pressure Measurement with programmable threshold
  - Supports Median and averaging filter for noise reduction
  - Supports X,Y Coordinate exchange function

- TPADC has 4 pads, multiplexing with GPADC2

3.9.13 LED Controller (LEDC)

- LEDC is used to control the external intelligent control LED lamp
- Configurable LED output high/low level width and reset time
- LEDC data supports DMA configuration mode and CPU configuration mode
- Maximum 1024 LEDs serial connect
- Configurable interval time between data packets and frame data
- Configurable RGB display mode

3.9.14 Consumer Infrared Transmitter (IR_TX)

- One IR_TX interface
- Full physical layer implementation
- 128 bytes FIFO for data buffer
- Configurable carrier frequency
- Configurable carrier duty cycle
- Supports Interrupt and DMA
- Supports DMA shake and wait mode
- Supports arbitrary wave generator
- Supports data transfer in RLC encoding format
- Compatible NEC format
- Supports single/cyclic sending mode

3.9.15 Consumer Infrared Receiver (IR_RX)

- Four IR_RX interfaces
- Supports CIR remote control receiver
- Supports Interrupts
- Sample clock up to 1MHz
- Supports 64-byte RX FIFO
- Programmable FIFO thresholds
- Supports data reception in RLC encoding format
- Compatible with NEC format
- Supports noise filtering function

3.10 Security

3.10.1 Crypto Engine (CE)

- Symmetrical Algorithm

- Supports AES Symmetrical Algorithm
  - Supports key size: 128/192/256 bits
  - Supports CFB mode, include CFB1/CFB8/CFB64/CFB128
  - Supports CTR mode, include CTR16/CTR32/CTR64/CTR128
  - Supports ECB, CBC, CTS, OFB, CBC-MAC, GCM, XTS modes
- Support XTS-AES symmetrical algorithm: key size: 256/512 bits
- Supports DES Symmetrical Algorithm
  - Supports CTR mode, include CTR16/CTR32/CTR64
  - Supports ECB, CBC, CBC-MAC mode
- Supports 3DES, SM4 Symmetrical Algorithm

- Hash Algorithms
  - Supports MD5, SHA1, SHA224, SHA256, SHA384, SHA512, SM3
  - Supports HMAC-SHA1, HMAC-SHA256
  - Supports multi-package mode for these ones
  - Supports hardware padding
- Radom bit generate Algorithms
  - Supports PRNG, 175 bits seed width, and output with multiple of 5 words
  - Supports TRNG, post-process by hardware with SHA256, output with multiple of 8 words
  - Supports TRNG single/double entropy source mode
  - Supports TRNG healthy test
  - Supports Instantiate/Reseed/Generate/Uninstantiate 4 process
  - Supports prediction resistance requests
  - Supports 8 separate suits of Internal State
  - Maximum 2^32 BYTE length of Entropy input、Nonce、Personalization、Additional input, and length is multiple of word
- Public Key Algorithms
  - Supports RSA Public Key Algorithms, include 512/1024/2048/3072/4096-bit width
  - Supports ECC Public Key Algorithms, include 160/224/256/384/521-bit width
  - Supports SM2 Algorithms
- Security Strategy and System Feature
  - Symmetric, asymmetric, HASH/RBG ctrl logics are separate, can handle task simultaneously. Symmetric logic can select instantiate 2 suits at implementation time.
  - Supports task chain mode for each request. Task or task chain are executed at request order.
  - 8 scatter group(sg) are supported for both input and output data
  - Supports secure and non-secure interfaces respectively. Each world issues task request through its own interface, and doesn’t know each other’s existence.

- Each world has 4 channels for software request, each channel has an interrupt control and status bit, and channels are independent with each other.
- All configurations can support byte align address.

3.10.2 Security ID (SID)

- Supports secure and non-secure world in eFuse
- Supports one-time programming the eFuse on the chip
- Supports data scrambling
- Supports reading and writing protection
- Supports eFuse power switch
- Supports the password function through secure debug

3.10.3 Secure Memory Control (SMC)

- The SMC is always secure and can only be accessed by secure CPU
- Sets the secure area of DRAM
- Supports DDR data scrambling and descrambling
- Supports setting the secure property that the Master accesses to DRAM
- Supports address isolation based on Master

3.10.4 Secure Peripherals Control (SPC)

- The SPC is always secure and can only be accessed by secure CPU
- Sets the secure area of peripherals

3.10.5 TrustZone Memory Access (TZMA)

- The TZMA is always secure and can only be accessed by secure CPU
- Sets the secure area of SRAMC

3.11 Package

- WBBGA 327 balls, 13 mm x 13 mm body size, 1.241 mm height (maximum), 0.65&0.6 mm ball pitch, 0.31 mm ball size.
- eQFP 128 pins, 14 mm x 14 mm, 1.600 mm height (maximum)

4 Pin Description

4.1 Pin Characteristics

4.1.1 T153MX-BCX Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Ball#**: Package ball numbers associated with each signal.

[2] **Ball Name**: The name of the package ball.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] **I/O Power Supply**: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

4.1.1.1 SDRAM

Table 4-1 SDRAM Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1P3	SDQ0	I/O	N/A	N/A	N/A	VCC-DRAM
1N4	SDQ1	I/O	N/A	N/A	N/A	VCC-DRAM
W9	SDQ2	I/O	N/A	N/A	N/A	VCC-DRAM
1M4	SDQ3	I/O	N/A	N/A	N/A	VCC-DRAM
W10	SDQ4	I/O	N/A	N/A	N/A	VCC-DRAM
1N3	SDQ5	I/O	N/A	N/A	N/A	VCC-DRAM
AA11	SDQ6	I/O	N/A	N/A	N/A	VCC-DRAM
Y9	SDQ7	I/O	N/A	N/A	N/A	VCC-DRAM
AA3	SDQ8	I/O	N/A	N/A	N/A	VCC-DRAM
AA2	SDQ9	I/O	N/A	N/A	N/A	VCC-DRAM
Y7	SDQ10	I/O	N/A	N/A	N/A	VCC-DRAM
Y3	SDQ11	I/O	N/A	N/A	N/A	VCC-DRAM
Y4	SDQ12	I/O	N/A	N/A	N/A	VCC-DRAM
1M1	SDQ13	I/O	N/A	N/A	N/A	VCC-DRAM
1N1	SDQ14	I/O	N/A	N/A	N/A	VCC-DRAM
W4	SDQ15	I/O	N/A	N/A	N/A	VCC-DRAM
Y8	SDQS0P	I/O	N/A	N/A	N/A	VCC-DRAM
W5	SDQS1P	I/O	N/A	N/A	N/A	VCC-DRAM
W8	SDQS0N	I/O	N/A	N/A	N/A	VCC-DRAM
Y5	SDQS1N	I/O	N/A	N/A	N/A	VCC-DRAM
W6	SDQM0	I/O	N/A	N/A	N/A	VCC-DRAM
1L3	SDQM1	I/O	N/A	N/A	N/A	VCC-DRAM
AA13	SCKP	O	N/A	N/A	N/A	VCC-DRAM
Y13	SCKN	O	N/A	N/A	N/A	VCC-DRAM

Ball#[2]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
Y15	SCKE0	O	N/A	N/A	N/A	VCC-DRAM
W17	SA0	O	N/A	N/A	N/A	VCC-DRAM
W16	SA1	O	N/A	N/A	N/A	VCC-DRAM
AA19	SA2	O	N/A	N/A	N/A	VCC-DRAM
1L12	SA3	O	N/A	N/A	N/A	VCC-DRAM
W14	SA4	O	N/A	N/A	N/A	VCC-DRAM
Y17	SA5	O	N/A	N/A	N/A	VCC-DRAM
1L9	SA6	O	N/A	N/A	N/A	VCC-DRAM
Y19	SA7	O	N/A	N/A	N/A	VCC-DRAM
W18	SA8	O	N/A	N/A	N/A	VCC-DRAM
1M12	SA9	O	N/A	N/A	N/A	VCC-DRAM
1N7	SA10	O	N/A	N/A	N/A	VCC-DRAM
1N13	SA11	O	N/A	N/A	N/A	VCC-DRAM
Y14	SA12	O	N/A	N/A	N/A	VCC-DRAM
1P13	SA13	O	N/A	N/A	N/A	VCC-DRAM
1M10	SA14	O	N/A	N/A	N/A	VCC-DRAM
1L10	SA15	O	N/A	N/A	N/A	VCC-DRAM
W11	SWE	O	N/A	N/A	N/A	VCC-DRAM
1L6	SRAS	O	N/A	N/A	N/A	VCC-DRAM
Y12	SBA0	O	N/A	N/A	N/A	VCC-DRAM
Y16	SBA1	O	N/A	N/A	N/A	VCC-DRAM
AA20	SBA2	O	N/A	N/A	N/A	VCC-DRAM
1N6	SCAS	O	N/A	N/A	N/A	VCC-DRAM
1P6	SCS0	O	N/A	N/A	N/A	VCC-DRAM
1L7	SCS1	O	N/A	N/A	N/A	VCC-DRAM
1P7	SODT0	O	N/A	N/A	N/A	VCC-DRAM
1M9	SODT1	O	N/A	N/A	N/A	VCC-DRAM
1P10	SRST	O	N/A	N/A	N/A	VCC-DRAM
1K7	SZQ	AI	N/A	N/A	N/A	VCC-DRAM

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1M13	SVREF	O	N/A	N/A	N/A	VCC-DRAM
1J7, 1G8, 1H8, 1J8	VCC-DRAM	P	N/A	N/A	N/A	N/A
1K10	VDD18-DRAM	P	N/A	N/A	N/A	N/A

4.1.1.2 GPIO Groups

Port A

Table 4-2 Port A Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1C13	PA0	I/O	Z	PU/PD	4 mA	VCC18-ADC
1C14	PA1	I/O	Z	PU/PD	4 mA	VCC18-ADC
1C12	PA2	I/O	Z	PU/PD	4 mA	VCC18-ADC
E20	PA3	I/O	Z	PU/PD	4 mA	VCC18-ADC
J21	PA4	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
J20	PA5	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
K19	PA6	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1D14	PA7	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
G19	PA8	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
G21	PA9	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
H19	PA10	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
G20	PA11	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1F13	PA12	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1D13	PA13	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1D12	PA14	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
H20	PA15	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
J19	PA16	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA

Ball#[2]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
K20	PA17	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
F19	PA18	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
F20	PA19	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1G14	PA20	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1F14	PA21	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1G13	PA22	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1F12	PA23	I/O	Z	PU/PD	4 mA	VCC18-ADC/VCC-PA
1E10	VCC-PA	P	N/A	N/A	N/A	N/A
1A12	VCC18-ADC	P	N/A	N/A	N/A	N/A
1A11	AGND-ADC	G	Z	PU/PD	4 mA	N/A

Port B

Table 4-3 Port B Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
H2	PB0	I/O	Z	PU/PD	4 mA	VCC-IO
G3	PB1	I/O	Z	PU/PD	4 mA	VCC-IO
G2	PB2	I/O	Z	PU/PD	4 mA	VCC-IO
G1	PB3	I/O	Z	PU/PD	4 mA	VCC-IO
J2	PB4	I/O	Z	PU/PD	4 mA	VCC-IO
J1	PB5	I/O	Z	PU/PD	4 mA	VCC-IO
H3	PB6	I/O	Z	PU/PD	4 mA	VCC-IO
J3	PB7	I/O	Z	PU/PD	4 mA	VCC-IO
K2	PB8	I/O	Z	PU/PD	4 mA	VCC-IO
K3	PB9	I/O	Z	PU/PD	4 mA	VCC-IO
L1	PB10	I/O	Z	PU/PD	4 mA	VCC-IO
F3	PB11	I/O	Z	PU/PD	4 mA	VCC-IO
F2	PB12	I/O	Z	PU/PD	4 mA	VCC-IO
1B1	PB13	I/O	Z	PU/PD	4 mA	VCC-IO

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1B2	PB14	I/O	Z	PU/PD	4 mA	VCC-IO

Port C

Table 4-4 Port C Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
T2	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
R3	PC1	I/O	PU	PU/PD	4 mA	VCC-PC
Y1	PC2	I/O	PU	PU/PD	4 mA	VCC-PC
W1	PC3	I/O	PU	PU/PD	4 mA	VCC-PC
V2	PC4	I/O	Z	PU/PD	4 mA	VCC-PC
U2	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
U3	PC6	I/O	Z	PU/PD	4 mA	VCC-PC
V3	PC7	I/O	Z	PU/PD	4 mA	VCC-PC
W2	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
Y2	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
U1	PC10	I/O	Z	PU/PD	4 mA	VCC-PC
T3	PC11	I/O	Z	PU/PD	4 mA	VCC-PC
1J1	VCC-PC	P	N/A	N/A	N/A	N/A

Port D

Table 4-5 Port D Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
R20	PD0	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
R19	PD1	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
P19	PD2	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
R21	PD3	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
N19	PD4	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
P20	PD5	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
N21	PD6	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
N20	PD7	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
M20	PD8	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
M19	PD9	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
Y21	PD10	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
Y20	PD11	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
W21	PD12	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
W20	PD13	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
V20	PD14	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
V19	PD15	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
U20	PD16	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
U19	PD17	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
T19	PD18	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
U21	PD19	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
L21	PD20	I/O	Z	PU/PD	4 mA	VCC-PD
L20	PD21	I/O	Z	PU/PD	4 mA	VCC-PD
1J14	PD22	I/O	Z	PU/PD	4 mA	VCC-PD
1J13	PD23	I/O	Z	PU/PD	4 mA	VCC-PD
1F10	VCC-PD	P	N/A	N/A	N/A	N/A
1G11	VCC18-LVDS	P	N/A	N/A	N/A	N/A

Port E

Table 4-6 Port E Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
C20	PE0	I/O	Z	PU/PD	4 mA	VCC-PE
D19	PE1	I/O	Z	PU/PD	4 mA	VCC-PE
E21	PE2	I/O	Z	PU/PD	4 mA	VCC-PE
E19	PE3	I/O	Z	PU/PD	4 mA	VCC-PE

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1A13	PE4	I/O	Z	PU/PD	4 mA	VCC-PE
C21	PE5	I/O	Z	PU/PD	4 mA	VCC-PE
1A14	PE6	I/O	Z	PU/PD	4 mA	VCC-PE
D20	PE7	I/O	Z	PU/PD	4 mA	VCC-PE
B21	PE8	I/O	Z	PU/PD	4 mA	VCC-PE
C19	PE9	I/O	Z	PU/PD	4 mA	VCC-PE
1C9	VCC-PE	P	N/A	N/A	N/A	N/A

Port F

Table 4-7 Port F Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B7	PF0	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
C7	PF1	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
B6	PF2	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
C6	PF3	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
A5	PF4	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
B5	PF5	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
A7	PF6	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-PF
1A6	VCC18-PF	P	N/A	N/A	N/A	N/A

Port G

Table 4-8 Port G Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
N3	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
P2	PG1	I/O	Z	PU/PD	4 mA	VCC-PG
N2	PG2	I/O	Z	PU/PD	4 mA	VCC-PG
N1	PG3	I/O	Z	PU/PD	4 mA	VCC-PG
R1	PG4	I/O	Z	PU/PD	4 mA	VCC-PG

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
P3	PG5	I/O	Z	PU/PD	4 mA	VCC-PG
M3	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
M2	PG7	I/O	Z	PU/PD	4 mA	VCC-PG
L3	PG8	I/O	Z	PU/PD	4 mA	VCC-PG
1J2	PG9	I/O	Z	PU/PD	4 mA	VCC-PG
1H2	PG10	I/O	Z	PU/PD	4 mA	VCC-PG
1J3	PG11	I/O	Z	PU/PD	4 mA	VCC-PG
1G3	PG12	I/O	Z	PU/PD	4 mA	VCC-PG
1H3	PG13	I/O	Z	PU/PD	4 mA	VCC-PG
1G2	PG14	I/O	Z	PU/PD	4 mA	VCC-PG
1G1	PG15	I/O	Z	PU/PD	4 mA	VCC-PG
1H1	VCC-PG	P	N/A	N/A	N/A	N/A

Port J

Table 4-9 Port J Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
C2	PJ0	I/O	Z	PU/PD	4 mA	VCC-PJ
C1	PJ1	I/O	Z	PU/PD	4 mA	VCC-PJ
C3	PJ2	I/O	Z	PU/PD	4 mA	VCC-PJ
B1	PJ3	I/O	Z	PU/PD	4 mA	VCC-PJ
A3	PJ4	I/O	Z	PU/PD	4 mA	VCC-PJ
B3	PJ5	I/O	Z	PU/PD	4 mA	VCC-PJ
A2	PJ6	I/O	Z	PU/PD	4 mA	VCC-PJ
B2	PJ7	I/O	Z	PU/PD	4 mA	VCC-PJ
B4	PJ8	I/O	Z	PU/PD	4 mA	VCC-PJ
C4	PJ9	I/O	Z	PU/PD	4 mA	VCC-PJ
E1	PJ10	I/O	Z	PU/PD	4 mA	VCC-PJ
E3	PJ11	I/O	Z	PU/PD	4 mA	VCC-PJ
D2	PJ12	I/O	Z	PU/PD	4 mA	VCC-PJ

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
D3	PJ13	I/O	Z	PU/PD	4 mA	VCC-PJ
1A2	PJ14	I/O	Z	PU/PD	4 mA	VCC-PJ
1A1	PJ15	I/O	Z	PU/PD	4 mA	VCC-PJ
1A3	VCC-PJ	P	N/A	N/A	N/A	N/A

Port K

Table 4-10 Port K Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B19	PK0	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
A19	PK1	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
C18	PK2	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
B18	PK3	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
B20	PK4	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
A20	PK5	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
B17	PK6	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
A17	PK7	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
B15	PK8	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
A15	PK9	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
C16	PK10	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI
B16	PK11	I/O	Z	PU/PD	4 mA	VCC-PK/VCC18-LDOA-MCSI

Ball#[2]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1B9	VCC-PK	P	N/A	N/A	N/A	N/A
1D11	VCC18-LDOA-MCSI	P	N/A	N/A	N/A	N/A

RTC_GPIO

Table 4-11 RTC_GPIO Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
C8	GPIO0	I/O, OD	Z	N/A	N/A	VCC-RTC
1A4	GPIO1	I/O, OD	Z	N/A	N/A	VCC-RTC
1B5	GPIO2	I/O, OD	Z	N/A	N/A	VCC-RTC
C9	GPIO4	I/O, OD	Z	N/A	N/A	VCC-RTC
1C4	NMI	I/O, OD	N/A	N/A	N/A	VCC-RTC

4.1.1.3 USB

Table 4-12 USB Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
B13	USB0-DM	I/O	N/A	N/A	N/A	VCC33-USB0-USB1
C13	USB0-DP	I/O	N/A	N/A	N/A	VCC33-USB0-USB1
B14	USB1-DM	I/O	N/A	N/A	N/A	VCC33-USB0-USB1
C14	USB1-DP	I/O	N/A	N/A	N/A	VCC33-USB0-USB1
1B8	VCC33-USB0-USB1	P	N/A	N/A	N/A	N/A

4.1.1.4 Audio Codec

Table 4-13 Audio Codec Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1B7	VRA1	A I/O	N/A	N/A	N/A	AVCC
1A7	AVCC	P	N/A	N/A	N/A	N/A
C12	LINEOUTP	AO	N/A	N/A	N/A	AVCC
B12	LINEOUTN	AO	N/A	N/A	N/A	AVCC
1C7	AGND	G	N/A	N/A	N/A	N/A

4.1.1.5 Boot

Table 4-14 System Control Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
E2	FEL	I	PU	PU/PD	N/A	VCC-IO

4.1.1.6 RTC

Table 4-15 RTC Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
C10	X32KIN	AI	N/A	N/A	N/A	VCC-RTC
B10	X32KOUT	AO	N/A	N/A	N/A	VCC-RTC
A11	X32KFOUT	AO, OD	N/A	N/A	N/A	VCC-RTC
1A8	TEST	I	PD	PU/PD	N/A	VCC-RTC
C11	RESET	I/O, OD	N/A	N/A	N/A	VCC-RTC
1A9	VCC-RTC	P	N/A	N/A	N/A	N/A

4.1.1.7 Power

Table 4-16 Power Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1C10	VCC18-EFUSE	P	N/A	N/A	N/A	N/A
1D1, 1E1, 1E2, 1E3, 1E4	VDD-CPU	P	N/A	N/A	N/A	N/A
1E8, 1F8, 1E9	VDD-SYS	P	N/A	N/A	N/A	N/A
1D2	VDD-CPUFB	P	N/A	N/A	N/A	N/A
1B4	VCC-IO	P	N/A	N/A	N/A	N/A
1D10	LDOA-IN	P	N/A	N/A	N/A	N/A

4.1.1.8 PLL

Table 4-17 PLL Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
1B6	PLLTEST	AO, OD	N/A	N/A	N/A	AVCC

4.1.1.9 DCXO

Table 4-18 DCXO Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
A9	DXIN	AI	N/A	N/A	N/A	VCC-RTC
B9	DXOUT	AO	N/A	N/A	N/A	VCC-RTC
B8	REFCLK-OUT	AO	N/A	N/A	N/A	VCC-RTC

4.1.1.10 Ground

Table 4-19 Ground Pin Characteristics

Ball#[1]	Ball Name[2]	Type[3]
A1, AA1, L2, R2, W3, C5, B11, A13, C15, C17, A21, L19, W19, T20, AA21, AA5, Y6, W7, AA7, AA9, Y10, Y11, W12, W13, W15, AA15, AA17, Y18, 1L1, 1P1, 1B3, 1D3, 1K3, 1M3, 1D4, 1F4, 1G4, 1J4, 1K4, 1L4, 1P4, 1C5, 1D5, 1E5, 1F5, 1G5, 1H5, 1J5, 1C6, 1D6, 1E6, 1F6, 1G6, 1H6, 1J6, 1M6, 1D7, 1E7, 1G7, 1M7, 1C8, 1D8, 1D9, 1F9, 1G9, 1H9, 1J9, 1K9, 1P9, 1G10, 1H10, 1J10, 1N10, 1G12, 1J12, 1K12, 1N12, 1P12, 1K13, 1L13, 1K14, 1L14	GND	G

4.1.2 T153Mx-QCX Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Pin#**: Package pin numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] **I/O Power Supply**: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

4.1.2.1 SDRAM

Table 4-20 SDRAM Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
44	VCC-DRAM0	P	N/A	N/A	N/A	N/A
47	VCC-DRAM1	P	N/A	N/A	N/A	N/A
46	VDD18-DRAM	P	N/A	N/A	N/A	N/A

4.1.2.2 GPIO Groups

Port A

Table 4-21 Port A Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
87	PA0	I/O	Z	PU/PD	4 mA	AVCC
86	PA1	I/O	Z	PU/PD	4 mA	AVCC
88	PA2	I/O	Z	PU/PD	4 mA	AVCC
89	PA3	I/O	Z	PU/PD	4 mA	AVCC
79	PA4	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
78	PA5	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
77	PA6	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
76	PA7	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
83	PA8	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
82	PA9	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
80	PA10	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
81	PA11	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
85	PA12	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
84	PA13	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK
75	PA14	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
74	PA15	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PK

Port B

Table 4-22 Port B Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
9	PB8	I/O	Z	PU/PD	4 mA	VCC-IO
8	PB9	I/O	Z	PU/PD	4 mA	VCC-IO
7	PB10	I/O	Z	PU/PD	4 mA	VCC-IO
6	PB11	I/O	Z	PU/PD	4 mA	VCC-IO
5	PB12	I/O	Z	PU/PD	4 mA	VCC-IO
4	PB13	I/O	Z	PU/PD	4 mA	VCC-IO
3	PB14	I/O	Z	PU/PD	4 mA	VCC-IO

Port C

Table 4-23 Port C Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
31	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
30	PC1	I/O	PU	PU/PD	4 mA	VCC-PC
41	PC2	I/O	PU	PU/PD	4 mA	VCC-PC
39	PC3	I/O	PU	PU/PD	4 mA	VCC-PC
37	PC4	I/O	Z	PU/PD	4 mA	VCC-PC
35	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
36	PC6	I/O	Z	PU/PD	4 mA	VCC-PC
38	PC7	I/O	Z	PU/PD	4 mA	VCC-PC
40	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
42	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
34	PC10	I/O	Z	PU/PD	4 mA	VCC-PC
33	PC11	I/O	Z	PU/PD	4 mA	VCC-PC

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
32	VCC-PC	P	N/A	N/A	N/A	N/A

Port D

Table 4-24 Port D Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
61	PD0	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
60	PD1	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
63	PD2	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
62	PD3	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
65	PD4	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
64	PD5	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
68	PD6	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
67	PD7	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
70	PD8	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
69	PD9	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
50	PD10	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
49	PD11	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
52	PD12	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
51	PD13	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
55	PD14	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
54	PD15	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
57	PD16	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
56	PD17	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
59	PD18	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
58	PD19	I/O	Z	PU/PD	4 mA	VCC-PD/VCC18-LVDS
72	PD20	I/O	Z	PU/PD	4 mA	VCC-PD
71	PD21	I/O	Z	PU/PD	4 mA	VCC-PD
66	VCC-PD	P	N/A	N/A	N/A	N/A

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
53	VCC18-LVDS	P	N/A	N/A	N/A	N/A

Port F

Table 4-25 Port F Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
121	PF0	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
122	PF1	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
123	PF2	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
124	PF3	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
125	PF4	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
126	PF5	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS

Port G

Table 4-26 Port G Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
21	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
20	PG1	I/O	Z	PU/PD	4 mA	VCC-PG
15	PG2	I/O	Z	PU/PD	4 mA	VCC-PG
27	PG3	I/O	Z	PU/PD	4 mA	VCC-PG
26	PG4	I/O	Z	PU/PD	4 mA	VCC-PG
13	PG5	I/O	Z	PU/PD	4 mA	VCC-PG
18	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
17	PG7	I/O	Z	PU/PD	4 mA	VCC-PG
16	PG8	I/O	Z	PU/PD	4 mA	VCC-PG
14	PG9	I/O	Z	PU/PD	4 mA	VCC-PG
25	PG10	I/O	Z	PU/PD	4 mA	VCC-PG
24	PG11	I/O	Z	PU/PD	4 mA	VCC-PG
22	PG12	I/O	Z	PU/PD	4 mA	VCC-PG

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
23	PG13	I/O	Z	PU/PD	4 mA	VCC-PG
29	PG14	I/O	Z	PU/PD	4 mA	VCC-PG
28	PG15	I/O	Z	PU/PD	4 mA	VCC-PG
19	VCC-PG	P	N/A	N/A	N/A	N/A

Port K

Table 4-27 Port K Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
92	PK0	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
93	PK1	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
95	PK2	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
94	PK3	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
97	PK4	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
96	PK5	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
98	PK6	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
99	PK7	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
100	PK8	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
101	PK9	I/O	Z	PU/PD	4 mA	VCC-PA-PK/ VCC18-LDOA-MCSI
102	PK10	I/O	Z	PU/PD	4 mA	VCC-PA-PK
91	VCC-PA-PK	P	N/A	N/A	N/A	N/A

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
103	VCC18-LDOA-MCSI	P	N/A	N/A	N/A	N/A

RTC_GPIO

Table 4-28 RTC_GPIO Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
115	NMI	I/O, OD	N/A	N/A	N/A	VCC-RTC

4.1.2.3 USB

Table 4-29 USB Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
107	USB0-DM	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
108	USB0-DP	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
105	USB1-DM	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
106	USB1-DP	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
104	VCC33-USB-LDOAIN	P	N/A	N/A	N/A	N/A

4.1.2.4 Audio Codec

Table 4-30 Audio Codec Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
111	VRA1	A I/O	N/A	N/A	N/A	AVCC
112	AVCC	P	N/A	N/A	N/A	N/A
109	LINEOUTP	AO	N/A	N/A	N/A	AVCC
110	AGND	G	N/A	N/A	N/A	N/A

4.1.2.5 RTC

Table 4-31 RTC Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
117	X32KIN	AI	N/A	N/A	N/A	VCC-RTC
118	X32KOUT	AO	N/A	N/A	N/A	VCC-RTC
114	RESET	I/O, OD	N/A	N/A	N/A	VCC-RTC
116	VCC-RTC	P	N/A	N/A	N/A	N/A

4.1.2.6 Power

Table 4-32 Power Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
10	VDD-CPU0	P	N/A	N/A	N/A	N/A
12	VDD-CPU1	P	N/A	N/A	N/A	N/A
127	VDD-CPU2	P	N/A	N/A	N/A	N/A
128	VDD-CPU3	P	N/A	N/A	N/A	N/A
1	VDD-SYS0	P	N/A	N/A	N/A	N/A
43	VDD-SYS1	P	N/A	N/A	N/A	N/A
48	VDD-SYS2	P	N/A	N/A	N/A	N/A
73	VDD-SYS3	P	N/A	N/A	N/A	N/A
90	VDD-SYS4	P	N/A	N/A	N/A	N/A
113	VDD-SYS5	P	N/A	N/A	N/A	N/A
2	VCC-IO	P	N/A	N/A	N/A	N/A

4.1.2.7 DCXO

Table 4-33 DCXO Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
119	DXIN	AI	N/A	N/A	N/A	VCC-RTC
120	DXOUT	AO	N/A	N/A	N/A	VCC-RTC

4.1.2.8 Ground

Table 4-34 Ground Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]
11	GND-CPU	G
45	VSS	G
E-Pad	GND	G

4.1.3 T153L3-QXX Pin Characteristics

This section lists the characteristics of the device pins from the following seven aspects.

[1] **Pin#**: Package pin numbers associated with each signal.

[2] **Pin Name**: The name of the package pin.

NC means these pins are not connected.

[3] **Type**: Denotes the signal direction

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

P (Power),

G (Ground)

N/A (Not Applicable)

[4] **Ball Reset State**: The state of the terminal at reset.

PU: Pull Up

PD: Pull Down

Z: High Impedance

N/A: Not Applicable

[5] **Pull Up/Down**: Denotes the presence of an internal pull-up or pull-down resistor. Pull-up and pull-down resistors can be enabled or disabled via software.

PU: Internal pullup

PD: Internal pulldown

PU/PD: Internal pullup and pulldown

N/A: Not Applicable

[6] **Default Buffer Strength**: Defines the default drive strength of the associated output buffer. The maximum drive strength of each GPIO is 6 mA.

N/A means Not Applicable.

[7] **I/O Power Supply**: The voltage supplies for the IO buffers of the terminal.

N/A means Not Applicable.

4.1.3.1 SDRAM

Table 4-35 SDRAM Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
44	VCC-DRAM0	P	N/A	N/A	N/A	N/A
47	VCC-DRAM1	P	N/A	N/A	N/A	N/A
46	VDD18-DRAM	P	N/A	N/A	N/A	N/A

4.1.3.2 GPIO Groups

Port A

Table 4-36 Port A Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
87	PA0	I/O	Z	PU/PD	4 mA	AVCC
86	PA1	I/O	Z	PU/PD	4 mA	AVCC
88	PA2	I/O	Z	PU/PD	4 mA	AVCC
89	PA3	I/O	Z	PU/PD	4 mA	AVCC
79	PA4	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
78	PA5	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
77	PA6	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
76	PA7	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
83	PA8	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
82	PA9	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
80	PA10	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
81	PA11	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
85	PA12	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
84	PA13	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD
75	PA14	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
74	PA15	I/O	Z	PU/PD	4 mA	AVCC/VCC-PA-PD

Port B

Table 4-37 Port B Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
9	PB8	I/O	Z	PU/PD	4 mA	VCC-IO
8	PB9	I/O	Z	PU/PD	4 mA	VCC-IO
7	PB10	I/O	Z	PU/PD	4 mA	VCC-IO
6	PB11	I/O	Z	PU/PD	4 mA	VCC-IO
5	PB12	I/O	Z	PU/PD	4 mA	VCC-IO
4	PB13	I/O	Z	PU/PD	4 mA	VCC-IO
3	PB14	I/O	Z	PU/PD	4 mA	VCC-IO

Port C

Table 4-38 Port C Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
31	PC0	I/O	Z	PU/PD	4 mA	VCC-PC
30	PC1	I/O	PU	PU/PD	4 mA	VCC-PC
41	PC2	I/O	PU	PU/PD	4 mA	VCC-PC
39	PC3	I/O	PU	PU/PD	4 mA	VCC-PC
37	PC4	I/O	Z	PU/PD	4 mA	VCC-PC
35	PC5	I/O	Z	PU/PD	4 mA	VCC-PC
36	PC6	I/O	Z	PU/PD	4 mA	VCC-PC
38	PC7	I/O	Z	PU/PD	4 mA	VCC-PC
40	PC8	I/O	Z	PU/PD	4 mA	VCC-PC
42	PC9	I/O	Z	PU/PD	4 mA	VCC-PC
34	PC10	I/O	Z	PU/PD	4 mA	VCC-PC
33	PC11	I/O	Z	PU/PD	4 mA	VCC-PC

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
32	VCC-PC	P	N/A	N/A	N/A	N/A

Port D

Table 4-39 Port D Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
61	PD0	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
60	PD1	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
63	PD2	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
62	PD3	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
65	PD4	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
64	PD5	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
68	PD6	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
67	PD7	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
70	PD8	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
69	PD9	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
50	PD10	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
49	PD11	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
52	PD12	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
51	PD13	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
55	PD14	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
54	PD15	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
57	PD16	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
56	PD17	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
59	PD18	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
58	PD19	I/O	Z	PU/PD	4 mA	VCC-PA-PD/VCC18-LVDS
72	PD20	I/O	Z	PU/PD	4 mA	VCC-PA-PD
71	PD21	I/O	Z	PU/PD	4 mA	VCC-PA-PD
66	VCC-PA-PD	P	N/A	N/A	N/A	N/A
53	VCC18-LVDS	P	N/A	N/A	N/A	N/A

Port F

Table 4-40 Port F Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
121	PF0	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
122	PF1	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
123	PF2	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
124	PF3	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
125	PF4	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS
126	PF5	I/O	Z	PU/PD	4 mA	VCC-IO/VCC18-LVDS

Port G

Table 4-41 Port G Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
21	PG0	I/O	Z	PU/PD	4 mA	VCC-PG
20	PG1	I/O	Z	PU/PD	4 mA	VCC-PG
15	PG2	I/O	Z	PU/PD	4 mA	VCC-PG
27	PG3	I/O	Z	PU/PD	4 mA	VCC-PG
26	PG4	I/O	Z	PU/PD	4 mA	VCC-PG
13	PG5	I/O	Z	PU/PD	4 mA	VCC-PG
18	PG6	I/O	Z	PU/PD	4 mA	VCC-PG
17	PG7	I/O	Z	PU/PD	4 mA	VCC-PG
16	PG8	I/O	Z	PU/PD	4 mA	VCC-PG
14	PG9	I/O	Z	PU/PD	4 mA	VCC-PG
25	PG10	I/O	Z	PU/PD	4 mA	VCC-PG
24	PG11	I/O	Z	PU/PD	4 mA	VCC-PG
22	PG12	I/O	Z	PU/PD	4 mA	VCC-PG
23	PG13	I/O	Z	PU/PD	4 mA	VCC-PG
29	PG14	I/O	Z	PU/PD	4 mA	VCC-PG
28	PG15	I/O	Z	PU/PD	4 mA	VCC-PG
19	VCC-PG	P	N/A	N/A	N/A	N/A

Port K

Table 4-42 Port K Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
92	PK0	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
93	PK1	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
95	PK2	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
94	PK3	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
97	PK4	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
96	PK5	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
98	PK6	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
99	PK7	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
100	PK8	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
101	PK9	I/O	Z	PU/PD	4 mA	VCC-PK/ VCC18-LDOA-MCSI
102	PK10	I/O	Z	PU/PD	4 mA	VCC-PK
91	VCC-PK	P	N/A	N/A	N/A	N/A
103	VCC18-LDOA-MCSI	P	N/A	N/A	N/A	N/A

RTC_GPIO

Table 4-43 RTC_GPIO Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
115	NMI	I/O, OD	N/A	N/A	N/A	VCC-RTC

4.1.3.3 USB

Table 4-44 USB Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
107	USB0-DM	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
108	USB0-DP	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
105	USB1-DM	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
106	USB1-DP	A I/O	N/A	N/A	N/A	VCC33-USB-LDOAIN
104	VCC33-USB-LDOAIN	P	N/A	N/A	N/A	N/A

4.1.3.4 Audio Codec

Table 4-45 Audio Codec Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
111	VRA1	A I/O	N/A	N/A	N/A	AVCC
112	AVCC	P	N/A	N/A	N/A	N/A
109	LINEOUTP	AO	N/A	N/A	N/A	AVCC
110	AGND	G	N/A	N/A	N/A	N/A

4.1.3.5 RTC

Table 4-46 RTC Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
117	X32KIN	AI	N/A	N/A	N/A	VCC-RTC
118	X32KOUT	AO	N/A	N/A	N/A	VCC-RTC
114	RESET	I/O, OD	N/A	N/A	N/A	VCC-RTC
116	VCC-RTC	P	N/A	N/A	N/A	N/A

4.1.3.6 Power

Table 4-47 Power Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
10	VDD-CPU0	P	N/A	N/A	N/A	N/A
11	VDD-CPU1	P	N/A	N/A	N/A	N/A
12	VDD-CPU2	P	N/A	N/A	N/A	N/A

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
127	VDD-CPU3	P	N/A	N/A	N/A	N/A
128	VDD-CPU4	P	N/A	N/A	N/A	N/A
1	VDD-SYS0	P	N/A	N/A	N/A	N/A
43	VDD-SYS1	P	N/A	N/A	N/A	N/A
48	VDD-SYS2	P	N/A	N/A	N/A	N/A
73	VDD-SYS3	P	N/A	N/A	N/A	N/A
90	VDD-SYS4	P	N/A	N/A	N/A	N/A
113	VDD-SYS5	P	N/A	N/A	N/A	N/A
2	VCC-IO	P	N/A	N/A	N/A	N/A

4.1.3.7 DCXO

Table 4-48 DCXO Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]	Ball Reset State[4]	Pull Up/Down[5]	Default Buffer Strength[6]	I/O Power Supply[7]
119	DXIN	AI	N/A	N/A	N/A	VCC-RTC
120	DXOUT	AO	N/A	N/A	N/A	VCC-RTC

4.1.3.8 Ground

Table 4-49 Ground Pin Characteristics

Pin#[1]	Pin Name[2]	Type[3]
45	VSS	G
E-Pad	GND	G

4.2 GPIO Multiplexing

The following tables provide a description of the GPIO multiplex function.

NOTE

(1) For Port A/B/C/D/E/F/G/J/K, Function0 is input function; Function1 is output function; Function12 to Function13 are reserved.

(2) For RTC_GPIO, Function0 is input function; Function1 is output function; Function 3 to Function13 are IO disabled.

4.2.1 T153MX-BCX GPIO Multiplexing

4.2.1.1 Port A

Table 4-50 Port A Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PA0	I/O	GPADC2-0	TP-X1			LBUS-READY3	LBUS-LBE2					PA-EINT0
PA1	I/O	GPADC2-1	TP-X2			LBUS-READY2	LBUS-DP1					PA-EINT1
PA2	I/O	GPADC2-2	TP-Y1			LBUS-DP2						PA-EINT2
PA3	I/O	GPADC2-3	TP-Y2			LBUS-DP3						PA-EINT3
PA4	I/O	GPADC0-0		RGMII0-RXD1/RMII0-RXD1	NCSI-HSYNC	LBUS-CLK						PA-EINT4
PA5	I/O	GPADC0-1		RGMII0-RXD0/RMII0-RXD0	NCSI-VSYNC	LBUS-ALE						PA-EINT5
PA6	I/O	GPADC0-2		RGMII0-RXCTL/RMII0-CRS-DV	NCSI-MCLK	LBUS-CS1	PWMCS-I8		LCD-D0			PA-EINT6
PA7	I/O	GPADC0-3		RGMII0-CLKIN/RMII0-RXER	NCSI-PCLK	LBUS-CS0	PWMCS-I9		LCD-D1			PA-EINT7
PA8	I/O	GPADC0-4		RGMII0-TXD1/RMII0-TXD1	NCSI-D0	LBUS-DP0	PWMCS-IA		LCD-D8			PA-EINT8
PA9	I/O	GPADC0-5		RGMII0-TXD0/RMII0-TXD0	NCSI-D1	LBUS-DP1	PWMCS-IB	LBUS-LBE3	LCD-D9			PA-EINT9
PA10	I/O	GPADC0-6		RGMII0-TXCK/RMII0-TXCK	NCSI-D2	LBUS-LBE0	PWMCS-IC		LCD-D16			PA-EINT10
PA11	I/O	GPADC0-7		RGMII0-TXCTL/RMII0-TXEN	NCSI-D3	LBUS-LBE1	PWMCS-ID		LCD-D17			PA-EINT11
PA12	I/O	GPADC0-8		RGMII0-MDC	NCSI-D4	LBUS-LD8	PWMCS-IE					PA-EINT12
PA13	I/O	GPADC0-9		RGMII0-MDIO	NCSI-D5	LBUS-LD9	PWMCS-IF					PA-EINT13
PA14	I/O	GPADC1-0		RGMII0-EPHY-25/50M	NCSI-D6	LBUS-LD10	UART6-TX					PA-EINT14

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PA15	I/O	GPADC1-1		RGMII0-RXD3/RMII0-NULL	NCSI-D7	LBUS-LD11	UART6-RX					PA-EINT15
PA16	I/O	GPADC1-2		RGMII0-RXD2/RMII0-NULL	NCSI-D8	LBUS-LD12	TWI3-SCK					PA-EINT16
PA17	I/O	GPADC1-3		RGMII0-RXCK/RMII0-NULL	NCSI-D9	LBUS-LD13	TWI3-SDA					PA-EINT17
PA18	I/O	GPADC1-4		RGMII0-TXD3/RMII0-NULL	NCSI-D10	LBUS-LD14						PA-EINT18
PA19	I/O	GPADC1-5		RGMII0-TXD2/RMII0-NULL	NCSI-D11	LBUS-LD15						PA-EINT19
PA20	I/O	GPADC1-6			NCSI-D12	LBUS-WAIT						PA-EINT20
PA21	I/O	GPADC1-7			NCSI-D13	LBUS-CS3	SPI2-CS1					PA-EINT21
PA22	I/O	GPADC1-8			NCSI-D14	LBUS-CS2						PA-EINT22
PA23	I/O	GPADC1-9			NCSI-D15	LBUS-DE						PA-EINT23

4.2.1.2 Port B

Table 4-51 Port B Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PB0	I/O	UART2-TX	SPI3-CS0	JTAG-MS	PWM0-6		RJTAG-MS		RGMII2-RXD1/RMII2-RXD1			PB-EINT0
PB1	I/O	UART2-RX	SPI3-CLK	JTAG-CK	PWM0-7		RJTAG-CK		RGMII2-RXD0/RMII2-RXD0			PB-EINT1
PB2	I/O	UART2-RTS	SPI3-MOSI	JTAG-DO	TWI2-SCK		RJTAG-DO		RGMII2-RXCTL/RMII2-CRS-DV			PB-EINT2
PB3	I/O	UART2-CTS	SPI3-MISO	JTAG-DI	TWI2-SDA		RJTAG-DI		RGMII2-CLKIN/RMII2-RXER			PB-EINT3
PB4	I/O	TWI1-SCK	I2S0-MCLK	SPI3-CS1	PWM1-0	IR0-RX	UART8-TX		RGMII2-TXD1/RMII2-TXD1			PB-EINT4
PB5	I/O	TWI1-SDA	I2S0-BCLK	SPI3-CS2	PWM1-1	IR1-RX	UART8-RX		RGMII2-TXD0/RMII2-TXD0			PB-EINT5
PB6	I/O		I2S0-LRCK		PWM1-2	IR-TX	UART8-RTS	TWI0-SCK	RGMII2-TXCK/RMII2-TXCK			PB-EINT6
PB7	I/O	OWA-IN	I2S0-DOUT0	I2S0-DIN1	PWM1-3	CAN1-TX0	UART8-CTS	TWI0-SDA	RGMII2-TXCTL/RMII2-TXEN			PB-EINT7

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PB8	I/O	OWA-OUT	I2S0-DIN0	I2S0-DOUT1	PWM0-0	CAN1-RX0	UART8-DCD					PB-EINT8
PB9	I/O	UART0-TX	I2S0-DIN2	I2S0-DOUT2		TWI0-SCK	UART8-DSR					PB-EINT9
PB10	I/O	UART0-RX	I2S0-DIN3	I2S0-DOUT3	PWM0-1	TWI0-SDA	UART8-DTR					PB-EINT10
PB11	I/O	TWI5-SCK	UART7-RTS	SPI3-CS0	PWM0-2		UART8-RI		RGMII2-MDC			PB-EINT11
PB12	I/O	TWI5-SDA	UART7-CTS	SPI3-CLK	PWM0-3				RGMII2-MDIO			PB-EINT12
PB13	I/O	TWI4-SCK	UART7-TX	SPI3-MOSI	PWM0-4	IR2-RX	CLK-FANOUT0		RGMII2-EPHY-25/50M			PB-EINT13
PB14	I/O	TWI4-SDA	UART7-RX	SPI3-MISO	PWM0-5	IR3-RX	CLK-FANOUT1					PB-EINT14

4.2.1.3 Port C

Table 4-52 Port C Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PC0	I/O	SDC2-CLK	SPI0-CLK	SPIF0-CLK								PC-EINT0
PC1	I/O	SDC2-CMD	SPI0-CS0	SPIF0-CS0								PC-EINT1
PC2	I/O	SDC2-D2	SPI0-MOSI	SPIF0-MOSI	BOOT-SEL0							PC-EINT2
PC3	I/O	SDC2-D1	SPI0-MISO	SPIF0-MISO	BOOT-SEL1							PC-EINT3
PC4	I/O	SDC2-D0	SPI0-WP	SPIF0-WP	CAN1-TX0							PC-EINT4
PC5	I/O	SDC2-D3	SPI0-HOLD	SPIF0-HOLD	CAN1-RX0							PC-EINT5
PC6	I/O	SDC2-D4	SPI0-CS1	SPIF0-D4	CAN0-TX0	UART6-TX						PC-EINT6
PC7	I/O	SDC2-D5		SPIF0-D5	CAN0-RX0	UART6-RX						PC-EINT7
PC8	I/O	SDC2-D6		SPIF0-D6	UART5-CTS							PC-EINT8
PC9	I/O	SDC2-D7		SPIF0-D7	UART5-TX							PC-EINT9
PC10	I/O	SDC2-DS		SPIF0-DQS	UART5-RX							PC-EINT10
PC11	I/O	SDC2-RST			UART5-RTS							PC-EINT11

4.2.1.4 Port D

Table 4-53 Port D Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PD0	I/O	LCD-D2	LVDS0-D0P	DSI-D0P	PWM0-0	UART2-CTS	UART9-TX	LBUS-LD20	PWMCS-O0		RGMII2-RXD1/RMII2-RXD1	PD-EINT0
PD1	I/O	LCD-D3	LVDS0-D0N	DSI-D0N	PWM0-1	UART2-RTS	UART9-RX	LBUS-LD21	PWMCS-O1		RGMII2-RXD0/RMII2-RXD0	PD-EINT1

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PD2	I/O	LCD-D4	LVDS0-D1P	DSI-D1P	PWM0-2	UART2-TX	UART9-RTS	LBUS-LD22	PWMCS-O2		RGMII2-RXCTL/RMII2-CRS-DV	PD-EINT2
PD3	I/O	LCD-D5	LVDS0-D1N	DSI-D1N	PWM0-3	UART2-RX	UART9-CTS	LBUS-LD23	PWMCS-O3		RGMII2-CLKIN/RMII2-RXER	PD-EINT3
PD4	I/O	LCD-D6	LVDS0-D2P	DSI-CKP	PWM0-4	UART4-CTS	UART6-TX	LBUS-LD24	PWMCS-O4		RGMII2-TXD1/RMII2-TXD1	PD-EINT4
PD5	I/O	LCD-D7	LVDS0-D2N	DSI-CKN	PWM0-5	UART4-RTS	UART6-RX	LBUS-LD25	PWMCS-O5	LBUS-CS3	RGMII2-TXD0/RMII2-TXD0	PD-EINT5
PD6	I/O	LCD-D10	LVDS0-CKP	DSI-D2P	PWM0-6	UART4-TX	UART6-RTS	LBUS-LD26	PWMCS-O6	LBUS-CS2	RGMII2-TXCK/RMII2-TXCK	PD-EINT6
PD7	I/O	LCD-D11	LVDS0-CKN	DSI-D2N	PWM0-7	UART4-RX	UART6-CTS	LBUS-LD27	PWMCS-O7	LBUS-READY3	RGMII2-TXCTL/RMII2-TXEN	PD-EINT7
PD8	I/O	LCD-D12	LVDS0-D3P	DSI-D3P	PWM1-0		CAN1-TX0	LBUS-LD28	PWMCS-O8	LBUS-DE	RGMII2-MDC	PD-EINT8
PD9	I/O	LCD-D13	LVDS0-D3N	DSI-D3N	PWM1-1	DMIC-CLK	CAN1-RX0	LBUS-LD29	PWMCS-O9	LBUS-READY2	RGMII2-MDIO	PD-EINT9
PD10	I/O	LCD-D14	LVDS1-D0P	SPI1-CS0/DBI-CSX	PWM1-2	DMIC-DATA0	UART8-TX	LBUS-LD30	PWMCS-OA	LBUS-READY1		PD-EINT10
PD11	I/O	LCD-D15	LVDS1-D0N	SPI1-CLK/DBI-SCLK	PWM1-3	DMIC-DATA1	UART8-RX	LBUS-LD31	PWMCS-OB	LBUS-READY0		PD-EINT11
PD12	I/O	LCD-D18	LVDS1-D1P	SPI1-MOSI/DBI-SDO	PWM1-4	DMIC-DATA2	UART8-RTS	LBUS-LD0	PWMCS-OC			PD-EINT12
PD13	I/O	LCD-D19	LVDS1-D1N	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PWM1-5	DMIC-DATA3	UART8-CTS	LBUS-LD1	PWMCS-OD			PD-EINT13
PD14	I/O	LCD-D20	LVDS1-D2P	SPI1-HOLD/DBI-DCX/DBI-WRX	PWM1-6	UART3-TX	UART8-DCD	LBUS-LD2	PWMCS-OE			PD-EINT14
PD15	I/O	LCD-D21	LVDS1-D2N	SPI1-WP/DBI-TE	PWM1-7	UART3-RX	UART8-DSR	LBUS-LD3	PWMCS-OF			PD-EINT15
PD16	I/O	LCD-D22	LVDS1-CKP		PWM2-0	UART3-RTS	UART8-DTR	LBUS-LD4	PWMCS-I0		RGMII2-EPHY-25/50M	PD-EINT16
PD17	I/O	LCD-D23	LVDS1-CKN		PWM2-1	UART3-CTS	UART8-RI	LBUS-LD5	PWMCS-I1		RGMII2-RXD3/RMII2-NULL	PD-EINT17
PD18	I/O	LCD-CLK	LVDS1-D3P	TWI5-SCK	PWM2-2		CAN0-TX0	LBUS-LD6	PWMCS-I2		RGMII2-RXD2/RMII2-NULL	PD-EINT18
PD19	I/O	LCD-DE	LVDS1-D3N	TWI5-SDA	PWM2-3		CAN0-RX0	LBUS-LD7	PWMCS-I3		RGMII2-RXCK/RMII2-NULL	PD-EINT19

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PD20	I/O	LCD-HSYNC	PWM2-4	UART3-TX	TWI5-SCK			LBUS-WR	PWMCS-I4		RGMII2-TXD3/RMII2-NULL	PD-EINT20
PD21	I/O	LCD-VSYNC	PWM2-5	UART3-RX	TWI5-SDA			LBUS-OE	PWMCS-I5		RGMII2-TXD2/RMII2-NULL	PD-EINT21
PD22	I/O		PWM2-6	UART3-RTS	TWI4-SCK	TWI0-SCK	CSI0-XHS	LBUS-DRQ0	PWMCS-I6			PD-EINT22
PD23	I/O		PWM2-7	UART3-CTS	TWI4-SDA	TWI0-SDA	CSI1-XHS	LBUS-DRQ1	PWMCS-I7			PD-EINT23

4.2.1.5 Port E

Table 4-54 Port E Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PE0	I/O	MCSI0-MCLK		NCSI-D8	CLK-FANOUT1		DMIC-CLK		SDC3-CLK			PE-EINT0
PE1	I/O	TWI1-SCK		NCSI-D9		SPI2-CS0	DMIC-DATA0					PE-EINT1
PE2	I/O	TWI1-SDA	PWM0-3	NCSI-D10		SPI2-CLK	DMIC-DATA1					PE-EINT2
PE3	I/O	TWI2-SCK	UART5-RTS	NCSI-D11	UART6-TX	SPI2-MOSI	DMIC-DATA2					PE-EINT3
PE4	I/O	TWI2-SDA	UART5-CTS	NCSI-D12	UART6-RX	SPI2-MISO	DMIC-DATA3					PE-EINT4
PE5	I/O	MCSI1-MCLK	UART5-TX	NCSI-D13	UART6-RTS	SPI2-WP			SDC3-CMD			PE-EINT5
PE6	I/O	TWI3-SCK	UART5-RX	NCSI-D14	UART6-CTS	SPI2-HOLD			SDC3-D0			PE-EINT6
PE7	I/O	TWI3-SDA	PWM0-2	NCSI-D15		SPI2-CS1			SDC3-D1			PE-EINT7
PE8	I/O	MCSI2-MCLK	PWM0-4	CSI0-XVS-FSYNC	CLK-FANOUT0	SPI2-CS2			SDC3-D2			PE-EINT8
PE9	I/O	TCON-FSYNC0	PWM0-5	CSI1-XVS-FSYNC					SDC3-D3			PE-EINT9

4.2.1.6 Port F

Table 4-55 Port F Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PF0	I/O	SDC0-D1	JTAG-MS	UART1-TX			RJTAG-MS	IR0-RX	LBUS-DRQ0			PF-EINT0
PF1	I/O	SDC0-D0	JTAG-DI	UART1-RX			RJTAG-DI	IR1-RX	LBUS-DRQ1			PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX	DMIC-CLK		SPI3-CLK		IR2-RX				PF-EINT2
PF3	I/O	SDC0-CMD	JTAG-DO	DMIC-DATA0		SPI3-CS0	RJTAG-DO	IR3-RX				PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX	DMIC-DATA1		SPI3-MOSI		IR-TX				PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK	DMIC-DATA2		SPI3-MISO	RJTAG-CK					PF-EINT5

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PF6	I/O			DMIC-DATA3								PF-EINT6

4.2.1.7 Port G

Table 4-56 Port G Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PG0	I/O	SDC1-CLK		UART8-TX	RGMII1-RXD3/RMII1-NULL							PG-EINT0
PG1	I/O	SDC1-CMD		UART8-RX	RGMII1-RXD2/RMII1-NULL							PG-EINT1
PG2	I/O	SDC1-D0		UART8-RTS	RGMII1-RXCK/RMII1-NULL							PG-EINT2
PG3	I/O	SDC1-D1		UART8-CTS	RGMII1-TXD3/RMII1-NULL							PG-EINT3
PG4	I/O	SDC1-D2		CAN0-TX0	RGMII1-TXD2/RMII1-NULL							PG-EINT4
PG5	I/O	SDC1-D3		CAN0-RX0	RGMII1-EPHY-25/50M							PG-EINT5
PG6	I/O	UART1-TX	TWI4-SCK	UART9-CTS	RGMII1-RXD1/RMII1-RXD1	I2S2-MCLK						PG-EINT6
PG7	I/O	UART1-RX	TWI4-SDA	UART9-RTS	RGMII1-RXD0/RMII1-RXD0	I2S2-BCLK						PG-EINT7
PG8	I/O	UART1-RTS	TWI5-SCK	UART9-TX	RGMII1-RXCTL/RMII1-CRS-DV	I2S2-LRCK						PG-EINT8
PG9	I/O	UART1-CTS	TWI5-SDA	UART9-RX	RGMII1-CLKIN/RMII1-RXER	I2S2-DOUT0	I2S2-DIN1					PG-EINT9
PG10	I/O	UART4-TX	I2S1-MCLK	TWI2-SCK	RGMII1-TXD1/RMII1-TXD1	I2S2-DIN0	I2S2-DOUT1					PG-EINT10
PG11	I/O	UART4-RX	I2S1-BCLK	TWI2-SDA	RGMII1-TXD0/RMII1-TXD0	DMIC-CLK						PG-EINT11
PG12	I/O	UART4-RTS	I2S1-LRCK		RGMII1-TXCK/RMII1-TXCK	DMIC-DATA0						PG-EINT12
PG13	I/O	UART4-CTS	I2S1-DOUT0	I2S1-DIN1	RGMII1-TXCTL/RMII1-TXEN	DMIC-DATA1						PG-EINT13
PG14	I/O	CAN1-TX0	I2S1-DIN0	I2S1-DOUT1	RGMII1-MDC	DMIC-DATA2		LBUS-DRQ0				PG-EINT14
PG15	I/O	CAN1-RX0			RGMII1-MDIO	DMIC-DATA3		LBUS-DRQ1				PG-EINT15

4.2.1.8 Port J

Table 4-57 Port J Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PJ0	I/O	PWM2-0	I2S2-MCLK	TWI4-SCK	RGMII0-RXD1/RMII0-RXD1	DMIC-CLK	UART5-TX					PJ-EINT0
PJ1	I/O	PWM2-1	I2S2-BCLK	TWI4-SDA	RGMII0-RXD0/RMII0-RXD0	DMIC-DATA0	UART5-RX					PJ-EINT1
PJ2	I/O	PWM2-2	I2S2-LRCK		RGMII0-RXCTL/RMII0-CRS-DV	DMIC-DATA1	UART5-RTS					PJ-EINT2
PJ3	I/O	PWM2-3	I2S2-DOUT0	I2S2-DIN1	RGMII0-CLKIN/RMII0-RXER	DMIC-DATA2	UART5-CTS					PJ-EINT3
PJ4	I/O	PWM2-4	I2S2-DIN0	I2S2-DOUT1	RGMII0-TXD1/RMII0-TXD1	DMIC-DATA3	UART7-TX					PJ-EINT4
PJ5	I/O	PWM2-5	I2S2-DIN2	I2S2-DOUT2	RGMII0-TXD0/RMII0-TXD0		UART7-RX					PJ-EINT5
PJ6	I/O	PWM2-6	I2S2-DIN3	I2S2-DOUT3	RGMII0-TXCK/RMII0-TXCK		UART7-RTS					PJ-EINT6
PJ7	I/O	PWM2-7	I2S1-MCLK		RGMII0-TXCTL/RMII0-TXEN		UART7-CTS					PJ-EINT7
PJ8	I/O	PWM2-8	I2S1-BCLK	LEDC	RGMII0-MDC		UART2-TX					PJ-EINT8
PJ9	I/O	PWM2-9	I2S1-LRCK	IR-TX	RGMII0-MDIO		UART2-RX					PJ-EINT9
PJ10	I/O	PWM2-10	I2S1-DOUT0	I2S1-DIN1	RGMII0-EPHY-25/50M		UART2-RTS					PJ-EINT10
PJ11	I/O	PWM2-11	I2S1-DIN0	I2S1-DOUT1	RGMII0-RXD3/RMII0-NULL		UART2-CTS					PJ-EINT11
PJ12	I/O	PWM2-12	CAN0-TX0	IR0-RX	RGMII0-RXD2/RMII0-NULL	TWI0-SCK	UART9-TX					PJ-EINT12
PJ13	I/O	PWM2-13	CAN0-RX0	IR1-RX	RGMII0-RXCK/RMII0-NULL	TWI0-SDA	UART9-RX					PJ-EINT13
PJ14	I/O		CAN1-TX0	IR2-RX	RGMII0-TXD3/RMII0-NULL	TWI5-SCK	UART9-RTS					PJ-EINT14
PJ15	I/O		CAN1-RX0	IR3-RX	RGMII0-TXD2/RMII0-NULL	TWI5-SDA	UART9-CTS					PJ-EINT15

4.2.1.9 Port K

Table 4-58 Port K Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
PK0	I/O		MCSIA-CKP		UART7-TX	TWI1-SCK	NCSI-D0	LBUS-READY1	I2S1-MCLK	LBUS-DRQ0	LCD-D0	PK-EINT0
PK1	I/O		MCSIA-CKN		UART7-RX	TWI1-SDA	NCSI-D1	LBUS-READY0	I2S1-BCLK	LBUS-DRQ1	LCD-D1	PK-EINT1
PK2	I/O		MCSIA-D0P		UART7-RTS	SPI1-CS0	NCSI-D2	LBUS-LD19	I2S1-LRCK	LBUS-LBE3	LCD-D8	PK-EINT2
PK3	I/O		MCSIA-D0N		UART7-CTS	SPI1-CLK	NCSI-D3	LBUS-LD18	I2S1-DOUT0	LBUS-DE	LCD-D9	PK-EINT3
PK4	I/O		MCSIA-D1P/MCSIC-D0P		TWI1-SCK	SPI1-MOSI	NCSI-D4	LBUS-LD17	I2S1-DIN0	LBUS-CS3	LCD-D16	PK-EINT4
PK5	I/O		MCSIA-D1N/MCSIC-D0N		TWI1-SDA	SPI1-MISO	NCSI-D5	LBUS-LD16		LBUS-CS2	LCD-D17	PK-EINT5
PK6	I/O		MCSIB-D1P/MCSIC-CKP/MCSIA-D2P		MCSI0-MCLK	SPI1-WP	NCSI-D6	LBUS-LD15	UART3-RTS		RGMII0-RXD3/RMII0-NULL	PK-EINT6
PK7	I/O		MCSIB-D1N/MCSIC-CKN/MCSIA-D2N		TWI2-SCK	SPI1-HOLD	NCSI-D7	LBUS-LD14			RGMII0-RXD2/RMII0-NULL	PK-EINT7
PK8	I/O		MCSIB-D0P/MCSIA-D3P		TWI2-SDA	SPI1-CS1	NCSI-PCLK	LBUS-LD13		CLK-FANOUT0	RGMII0-RXCK/RMII0-NULL	PK-EINT8
PK9	I/O		MCSIB-D0N/MCSIA-D3N		MCSI1-MCLK	SPI1-CS2	NCSI-MCLK	LBUS-LD12	UART3-TX	CLK-FANOUT1	RGMII0-TXD3/RMII0-NULL	PK-EINT9
PK10	I/O		MCSIB-CKP		TWI3-SCK	PWM0-6	NCSI-HSYNC	LBUS-WAIT	UART3-RX	LBUS-LBE2	RGMII0-TXD2/RMII0-NULL	PK-EINT10
PK11	I/O		MCSIB-CKN		TWI3-SDA	PWM0-7	NCSI-VSYNC	LBUS-CS2	UART3-CTS			PK-EINT11

4.2.1.10 RTC_GPIO

Table 4-59 RTC_GPIO Multiplex Function

Pin Name	IO Type	Function										
		2	3	4	5	6	7	8	9	10	11	14
GPIO0	I/O, OD											IRQ-EINT0
GPIO1	I/O, OD											IRQ-EINT1
GPIO2	I/O, OD											IRQ-EINT2
GPIO4	I/O, OD											IRQ-EINT4
NMI	I/O, OD	NMI										NMI-EINT0

4.2.2 T153Mx-QCX GPIO Multiplexing

The following tables provide a description of the GPIO multiplex function.

NOTE

a. For Port A/B/C/D/F/G/K, Function0 is input function; Function1 is output function;
b. For RTC_GPIO, Function0 is input function; Function1 is output function; Function 3 to Function13 are IO disabled.
c. T153Mx-QCX series include T153M3-QCX and T153M4-QCX.

4.2.2.1 Port A

Table 4-60 Port A Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PA0	I/O	GPADC2-0	TP-X1			LBUS-READY3	LBUS-LBE2							PA-EINT0
PA1	I/O	GPADC2-1	TP-X2			LBUS-READY2	LBUS-DP1							PA-EINT1
PA2	I/O	GPADC2-2	TP-Y1			LBUS-DP2								PA-EINT2
PA3	I/O	GPADC2-3	TP-Y2			LBUS-DP3								PA-EINT3
PA4	I/O	GPADC0-0		RGMII0-RXD1/RMII0-RXD1	NCSI-HSYNC	LBUS-CLK								PA-EINT4
PA5	I/O	GPADC0-1		RGMII0-RXD0/RMII0-RXD0	NCSI-VSYNC	LBUS-ALE								PA-EINT5
PA6	I/O	GPADC0-2		RGMII0-RXCTL/RMII0-CRS-DV	NCSI-MCLK	LBUS-CS1	PWMCS-I8		LCD-D0					PA-EINT6
PA7	I/O	GPADC0-3		RGMII0-CLKIN/RMII0-RXER	NCSI-PCLK	LBUS-CS0	PWMCS-I9		LCD-D1					PA-EINT7
PA8	I/O	GPADC0-4		RGMII0-TXD1/RMII0-TXD1	NCSI-D0	LBUS-DP0	PWMCS-IA		LCD-D8					PA-EINT8
PA9	I/O	GPADC0-5		RGMII0-TXD0/RMII0-TXD0	NCSI-D1	LBUS-DP1	PWMCS-IB	LBUS-LBE3	LCD-D9					PA-EINT9
PA10	I/O	GPADC0-6		RGMII0-TXCK/RMII0-TXCK	NCSI-D2	LBUS-LBE0	PWMCS-IC		LCD-D16					PA-EINT10
PA11	I/O	GPADC0-7		RGMII0-TXCTL/RMII0-TXEN	NCSI-D3	LBUS-LBE1	PWMCS-ID		LCD-D17					PA-EINT11
PA12	I/O	GPADC0-8		RGMII0-MDC	NCSI-D4	LBUS-LD8	PWMCS-IE							PA-EINT12
PA13	I/O	GPADC0-9		RGMII0-MDIO	NCSI-D5	LBUS-LD9	PWMCS-IF							PA-EINT13
PA14	I/O	GPADC1-0		RGMII0-EPHY-25/50M	NCSI-D6	LBUS-LD10	UART6-TX							PA-EINT14
PA15	I/O	GPADC1-1		RGMII0-RXD3/RMII0-NULL	NCSI-D7	LBUS-LD11	UART6-RX							PA-EINT15

4.2.2.2 Port B

Table 4-61 Port B Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PB8	I/O	OWA-OUT			PWM0-0		UART8-DCD							PB-EINT8
PB9	I/O	UART0-TX				TWI0-SCK	UART8-DSR							PB-EINT9
PB10	I/O	UART0-RX			PWM0-1	TWI0-SDA	UART8-DTR							PB-EINT10
PB11	I/O	TWI5-SCK	UART7-RTS	SPI3-CS0	PWM0-2		UART8-RI		RGMII2-MDC					PB-EINT11
PB12	I/O	TWI5-SDA	UART7-CTS	SPI3-CLK	PWM0-3				RGMII2-MDIO					PB-EINT12
PB13	I/O	TWI4-SCK	UART7-TX	SPI3-MOSI	PWM0-4	IR2-RX	CLK-FANOUT0		RGMII2-EPHY-25/50M					PB-EINT13
PB14	I/O	TWI4-SDA	UART7-RX	SPI3-MISO	PWM0-5	IR3-RX	CLK-FANOUT1							PB-EINT14

4.2.2.3 Port C

Table 4-62 Port C Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PC0	I/O	SDC2-CLK	SPI0-CLK	SPIF0-CLK										PC-EINT0
PC1	I/O	SDC2-CMD	SPI0-CS0	SPIF0-CS0										PC-EINT1
PC2	I/O	SDC2-D2	SPI0-MOSI	SPIF0-MOSI	BOOT-SEL0									PC-EINT2
PC3	I/O	SDC2-D1	SPI0-MISO	SPIF0-MISO	BOOT-SEL1									PC-EINT3
PC4	I/O	SDC2-D0	SPI0-WP	SPIF0-WP	CAN1-TX0									PC-EINT4
PC5	I/O	SDC2-D3	SPI0-HOLD	SPIF0-HOLD	CAN1-RX0									PC-EINT5
PC6	I/O	SDC2-D4	SPI0-CS1	SPIF0-D4	CAN0-TX0	UART6-TX								PC-EINT6
PC7	I/O	SDC2-D5		SPIF0-D5	CAN0-RX0	UART6-RX								PC-EINT7
PC8	I/O	SDC2-D6		SPIF0-D6	UART5-CTS									PC-EINT8
PC9	I/O	SDC2-D7		SPIF0-D7	UART5-TX									PC-EINT9
PC10	I/O	SDC2-DS		SPIF0-DQS	UART5-RX									PC-EINT10
PC11	I/O	SDC2-RST			UART5-RTS									PC-EINT11

4.2.2.4 Port D

Table 4-63 Port D Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PD0	I/O	LCD-D2	LVDS0-D0P	DSI-D0P	PWM0-0	UART2-CTS	UART9-TX	LBUS-LD20	PWMCS-O0		RGMII2-RXD1/RMII2-RXD1			PD-EINT0
PD1	I/O	LCD-D3	LVDS0-D0N	DSI-D0N	PWM0-1	UART2-RTS	UART9-RX	LBUS-LD21	PWMCS-O1		RGMII2-RXD0/RMII2-RXD0			PD-EINT1
PD2	I/O	LCD-D4	LVDS0-D1P	DSI-D1P	PWM0-2	UART2-TX	UART9-RTS	LBUS-LD22	PWMCS-O2		RGMII2-RXCTL/RMII2-CRS-DV			PD-EINT2
PD3	I/O	LCD-D5	LVDS0-D1N	DSI-D1N	PWM0-3	UART2-RX	UART9-CTS	LBUS-LD23	PWMCS-O3		RGMII2-CLKIN/RMII2-RXER			PD-EINT3
PD4	I/O	LCD-D6	LVDS0-D2P	DSI-CKP	PWM0-4	UART4-CTS	UART6-TX	LBUS-LD24	PWMCS-O4		RGMII2-TXD1/RMII2-TXD1			PD-EINT4
PD5	I/O	LCD-D7	LVDS0-D2N	DSI-CKN	PWM0-5	UART4-RTS	UART6-RX	LBUS-LD25	PWMCS-O5	LBUS-CS3	RGMII2-TXD0/RMII2-TXD0			PD-EINT5
PD6	I/O	LCD-D10	LVDS0-CKP	DSI-D2P	PWM0-6	UART4-TX	UART6-RTS	LBUS-LD26	PWMCS-O6	LBUS-CS2	RGMII2-TXCK/RMII2-TXCK			PD-EINT6
PD7	I/O	LCD-D11	LVDS0-CKN	DSI-D2N	PWM0-7	UART4-RX	UART6-CTS	LBUS-LD27	PWMCS-O7	LBUS-READY3	RGMII2-TXCTL/RMII2-TXEN			PD-EINT7
PD8	I/O	LCD-D12	LVDS0-D3P	DSI-D3P	PWM1-0		CAN1-TX0	LBUS-LD28	PWMCS-O8	LBUS-DE	RGMII2-MDC			PD-EINT8
PD9	I/O	LCD-D13	LVDS0-D3N	DSI-D3N	PWM1-1	DMIC-CLK	CAN1-RX0	LBUS-LD29	PWMCS-O9	LBUS-READY2	RGMII2-MDIO			PD-EINT9
PD10	I/O	LCD-D14	LVDS1-D0P	SPI1-CS0/DBI-CSX	PWM1-2	DMIC-DATA0	UART8-TX	LBUS-LD30	PWMCS-OA	LBUS-READY1				PD-EINT10
PD11	I/O	LCD-D15	LVDS1-D0N	SPI1-CLK/DBI-SCLK	PWM1-3	DMIC-DATA1	UART8-RX	LBUS-LD31	PWMCS-OB	LBUS-READY0				PD-EINT11
PD12	I/O	LCD-D18	LVDS1-D1P	SPI1-MOSI/DBI-SDO	PWM1-4	DMIC-DATA2	UART8-RTS	LBUS-LD0	PWMCS-OC					PD-EINT12
PD13	I/O	LCD-D19	LVDS1-D1N	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PWM1-5	DMIC-DATA3	UART8-CTS	LBUS-LD1	PWMCS-OD					PD-EINT13
PD14	I/O	LCD-D20	LVDS1-D2P	SPI1-HOLD/DBI-DCX/DBI-WRX	PWM1-6	UART3-TX	UART8-DCD	LBUS-LD2	PWMCS-OE					PD-EINT14
PD15	I/O	LCD-D21	LVDS1-D2N	SPI1-WP/DBI-TE	PWM1-7	UART3-RX	UART8-DSR	LBUS-LD3	PWMCS-OF					PD-EINT15
PD16	I/O	LCD-D22	LVDS1-CKP		PWM2-0	UART3-RTS	UART8-DTR	LBUS-LD4	PWMCS-I0		RGMII2-EPHY-25/50M			PD-EINT16

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PD17	I/O	LCD-D23	LVDS1-CKN		PWM2-1	UART3-CTS	UART8-RI	LBUS-LD5	PWMCS-I1		RGMII2-RXD3/RMII2-NULL			PD-EINT17
PD18	I/O	LCD-CLK	LVDS1-D3P	TWI5-SCK	PWM2-2		CAN0-TX0	LBUS-LD6	PWMCS-I2		RGMII2-RXD2/RMII2-NULL			PD-EINT18
PD19	I/O	LCD-DE	LVDS1-D3N	TWI5-SDA	PWM2-3		CAN0-RX0	LBUS-LD7	PWMCS-I3		RGMII2-RXCK/RMII2-NULL			PD-EINT19
PD20	I/O	LCD-HSYNC	PWM2-4	UART3-TX	TWI5-SCK			LBUS-WR	PWMCS-I4		RGMII2-TXD3/RMII2-NULL			PD-EINT20
PD21	I/O	LCD-VSYNC	PWM2-5	UART3-RX	TWI5-SDA			LBUS-OE	PWMCS-I5		RGMII2-TXD2/RMII2-NULL			PD-EINT21

4.2.2.5 Port F

Table 4-64 Port F Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PF0	I/O	SDC0-D1	JTAG-MS	UART1-TX			RJTAG-MS	IR0-RX	LBUS-DRQ0					PF-EINT0
PF1	I/O	SDC0-D0	JTAG-DI	UART1-RX			RJTAG-DI	IR1-RX	LBUS-DRQ1					PF-EINT1
PF2	I/O	SDC0-CLK	UART0-TX	DMIC-CLK		SPI3-CLK		IR2-RX						PF-EINT2
PF3	I/O	SDC0-CMD	JTAG-DO	DMIC-DATA0		SPI3-CS0	RJTAG-DO	IR3-RX						PF-EINT3
PF4	I/O	SDC0-D3	UART0-RX	DMIC-DATA1		SPI3-MOSI		IR-TX						PF-EINT4
PF5	I/O	SDC0-D2	JTAG-CK	DMIC-DATA2		SPI3-MISO	RJTAG-CK							PF-EINT5

4.2.2.6 Port G

Table 4-65 Port G Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PG0	I/O	SDC1-CLK		UART8-TX	RGMII1-RXD3/RMII1-NULL									PG-EINT0
PG1	I/O	SDC1-CMD		UART8-RX	RGMII1-RXD2/RMII1-NULL									PG-EINT1
PG2	I/O	SDC1-D0		UART8-RTS	RGMII1-RXCK/RMII1-NULL									PG-EINT2
PG3	I/O	SDC1-D1		UART8-CTS	RGMII1-TXD3/RMII1-NULL									PG-EINT3

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PG4	I/O	SDC1-D2		CAN0-TX0	RGMII1-TXD2/RMII1-NULL									PG-EINT4
PG5	I/O	SDC1-D3		CAN0-RX0	RGMII1-EPHY-25/50M									PG-EINT5
PG6	I/O	UART1-TX	TWI4-SCK	UART9-CTS	RGMII1-RXD1/RMII1-RXD1	I2S2-MCLK								PG-EINT6
PG7	I/O	UART1-RX	TWI4-SDA	UART9-RTS	RGMII1-RXD0/RMII1-RXD0	I2S2-BCLK								PG-EINT7
PG8	I/O	UART1-RTS	TWI5-SCK	UART9-TX	RGMII1-RXCTL/RMII1-CRS-DV	I2S2-LRCK								PG-EINT8
PG9	I/O	UART1-CTS	TWI5-SDA	UART9-RX	RGMII1-CLKIN/RMII1-RXER	I2S2-DOUT0	I2S2-DIN1							PG-EINT9
PG10	I/O	UART4-TX	I2S1-MCLK	TWI2-SCK	RGMII1-TXD1/RMII1-TXD1	I2S2-DIN0	I2S2-DOUT1							PG-EINT10
PG11	I/O	UART4-RX	I2S1-BCLK	TWI2-SDA	RGMII1-TXD0/RMII1-TXD0	DMIC-CLK								PG-EINT11
PG12	I/O	UART4-RTS	I2S1-LRCK		RGMII1-TXCK/RMII1-TXCK	DMIC-DATA0								PG-EINT12
PG13	I/O	UART4-CTS	I2S1-DOUT0	I2S1-DIN1	RGMII1-TXCTL/RMII1-TXEN	DMIC-DATA1								PG-EINT13
PG14	I/O	CAN1-TX0	I2S1-DIN0	I2S1-DOUT1	RGMII1-MDC	DMIC-DATA2		LBUS-DRQ0						PG-EINT14
PG15	I/O	CAN1-RX0			RGMII1-MDIO	DMIC-DATA3		LBUS-DRQ1						PG-EINT15

4.2.2.7 Port K

Table 4-66 Port K Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PK0	I/O		MCSIA-CKP		UART7-TX	TWI1-SCK	NCSI-D0	LBUS-READY1	I2S1-MCLK	LBUS-DRQ0	LCD-D0			PK-EINT0
PK1	I/O		MCSIA-CKN		UART7-RX	TWI1-SDA	NCSI-D1	LBUS-READY0	I2S1-BCLK	LBUS-DRQ1	LCD-D1			PK-EINT1
PK2	I/O		MCSIA-D0P		UART7-RTS	SPI1-CS0	NCSI-D2	LBUS-LD19	I2S1-LRCK	LBUS-LBE3	LCD-D8			PK-EINT2
PK3	I/O		MCSIA-D0N		UART7-CTS	SPI1-CLK	NCSI-D3	LBUS-LD18	I2S1-DOUT0	LBUS-DE	LCD-D9			PK-EINT3
PK4	I/O		MCSIA-D1P		TWI1-SCK	SPI1-MOSI	NCSI-D4	LBUS-LD17	I2S1-DIN0	LBUS-CS3	LCD-D16			PK-EINT4
PK5	I/O		MCSIA-D1N		TWI1-SDA	SPI1-MISO	NCSI-D5	LBUS-LD16		LBUS-CS2	LCD-D17			PK-EINT5
PK6	I/O		MCSIA-D2P		MCSI0-MCLK	SPI1-WP	NCSI-D6	LBUS-LD15	UART3-RTS		RGMII0-RXD3/RMII0-NULL			PK-EINT6

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PK7	I/O		MCSIA-D2N		TWI2-SCK	SPI1-HOLD	NCSI-D7	LBUS-LD14			RGMII0-RXD2/RMII0-NULL			PK-EINT7
PK8	I/O		MCSIA-D3P		TWI2-SDA	SPI1-CS1	NCSI-PCLK	LBUS-LD13		CLK-FANOUT0	RGMII0-RXCK/RMII0-NULL			PK-EINT8
PK9	I/O		MCSIA-D3N			SPI1-CS2	NCSI-MCLK	LBUS-LD12	UART3-TX	CLK-FANOUT1	RGMII0-TXD3/RMII0-NULL			PK-EINT9
PK10	I/O					PWM0-6	NCSI-HSYNC	LBUS-WAIT	UART3-RX	LBUS-LBE2	RGMII0-TXD2/RMII0-NULL			PK-EINT10

4.2.2.8 RTC_GPIO

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
NMI	I/O, OD	NMI												NMI-EINTT0

4.2.3 T153L3-QXX GPIO Multiplexing

The following tables provide a description of the GPIO multiplex function.

NOTE

(1) For Port A/B/C/D/F/G/K, Function0 is input function; Function1 is output function;

(2) For RTC_GPIO, Function0 is input function; Function1 is output function; Function 3 to Function13 are IO disabled.

4.2.3.1 Port A

Table 4-67 Port A Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PA0	I/O	GPADC2-0	TP-X1									PA-EINT0	PA0	I/O
PA1	I/O	GPADC2-1	TP-X2									PA-EINT1	PA1	I/O
PA2	I/O	GPADC2-2	TP-Y1									PA-EINT2	PA2	I/O
PA3	I/O	GPADC2-3	TP-Y2									PA-EINT3	PA3	I/O
PA4	I/O	GPADC0-0		RGMII0-RXD1/RMII0-RXD1	NCSI-HSYNC							PA-EINT4	PA4	I/O
PA5	I/O	GPADC0-1		RGMII0-RXD0/RMII0-RXD0	NCSI-VSYNC							PA-EINT5	PA5	I/O
PA6	I/O	GPADC0-2		RGMII0-RXCTL/RMII0-CRS-DV	NCSI-MCLK		PWMCS-I8		LCD-D0			PA-EINT6	PA6	I/O
PA7	I/O	GPADC0-3		RGMII0-CLKIN/RMII0-RXER	NCSI-PCLK		PWMCS-I9		LCD-D1			PA-EINT7	PA7	I/O

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PA8	I/O	GPADC0-4		RGMII0-TXD1/RMII0-TXD1	NCSI-D0		PWMCS-IA		LCD-D8			PA-EINT8	PA8	I/O
PA9	I/O	GPADC0-5		RGMII0-TXD0/RMII0-TXD0	NCSI-D1		PWMCS-IB		LCD-D9			PA-EINT9	PA9	I/O
PA10	I/O	GPADC0-6		RGMII0-TXCK/RMII0-TXCK	NCSI-D2		PWMCS-IC		LCD-D16			PA-EINT10	PA10	I/O
PA11	I/O	GPADC0-7		RGMII0-TXCTL/RMII0-TXEN	NCSI-D3		PWMCS-ID		LCD-D17			PA-EINT11	PA11	I/O
PA12	I/O	GPADC0-8		RGMII0-MDC	NCSI-D4		PWMCS-IE					PA-EINT12	PA12	I/O
PA13	I/O	GPADC0-9		RGMII0-MDIO	NCSI-D5		PWMCS-IF					PA-EINT13	PA13	I/O
PA14	I/O	GPADC1-0		RGMII0-EPHY-25/50M	NCSI-D6		UART6-TX					PA-EINT14	PA14	I/O
PA15	I/O	GPADC1-1		RGMII0-RXD3/RMII0-NULL	NCSI-D7		UART6-RX					PA-EINT15	PA15	I/O

4.2.3.2 Port B

Table 4-68 Port B Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PB8	I/O	OWA-OUT			PWM0-0		UART8-DCD					PB-EINT8	PB8	I/O
PB9	I/O	UART0-TX				TWI0-SCK	UART8-DSR					PB-EINT9	PB9	I/O
PB10	I/O	UART0-RX			PWM0-1	TWI0-SDA	UART8-DTR					PB-EINT10	PB10	I/O
PB11	I/O	TWI5-SCK	UART7-RTS	SPI3-CS0	PWM0-2		UART8-RI					PB-EINT11	PB11	I/O
PB12	I/O	TWI5-SDA	UART7-CTS	SPI3-CLK	PWM0-3							PB-EINT12	PB12	I/O
PB13	I/O	TWI4-SCK	UART7-TX	SPI3-MOSI	PWM0-4	IR2-RX	CLK-FANOUT0					PB-EINT13	PB13	I/O
PB14	I/O	TWI4-SDA	UART7-RX	SPI3-MISO	PWM0-5	IR3-RX	CLK-FANOUT1					PB-EINT14	PB14	I/O

4.2.3.3 Port C

Table 4-69 Port C Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PC0	I/O	SDC2-CLK	SPI0-CLK	SPIF0-CLK								PC-EINT0	PC0	I/O
PC1	I/O	SDC2-CMD	SPI0-CS0	SPIF0-CS0								PC-EINT1	PC1	I/O
PC2	I/O	SDC2-D2	SPI0-MOSI	SPIF0-MOSI	BOOT-SEL0							PC-EINT2	PC2	I/O

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PC3	I/O	SDC2-D1	SPI0-MISO	SPIF0-MISO	BOOT-SEL1							PC-EINT3	PC3	I/O
PC4	I/O	SDC2-D0	SPI0-WP	SPIF0-WP								PC-EINT4	PC4	I/O
PC5	I/O	SDC2-D3	SPI0-HOLD	SPIF0-HOLD								PC-EINT5	PC5	I/O
PC6	I/O	SDC2-D4	SPI0-CS1	SPIF0-D4		UART6-TX						PC-EINT6	PC6	I/O
PC7	I/O	SDC2-D5		SPIF0-D5		UART6-RX						PC-EINT7	PC7	I/O
PC8	I/O	SDC2-D6		SPIF0-D6	UART5-CTS							PC-EINT8	PC8	I/O
PC9	I/O	SDC2-D7		SPIF0-D7	UART5-TX							PC-EINT9	PC9	I/O
PC10	I/O	SDC2-DS		SPIF0-DQS	UART5-RX							PC-EINT10	PC10	I/O
PC11	I/O	SDC2-RST			UART5-RTS							PC-EINT11	PC11	I/O

4.2.3.4 Port D

Table 4-70 Port D Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PD0	I/O	LCD-D2	LVDS0-D0P	DSI-D0P	PWM0-0	UART2-CTS	UART9-TX		PWMCS-O0			PD-EINT0	PD0	I/O
PD1	I/O	LCD-D3	LVDS0-D0N	DSI-D0N	PWM0-1	UART2-RTS	UART9-RX		PWMCS-O1			PD-EINT1	PD1	I/O
PD2	I/O	LCD-D4	LVDS0-D1P	DSI-D1P	PWM0-2	UART2-TX	UART9-RTS		PWMCS-O2			PD-EINT2	PD2	I/O
PD3	I/O	LCD-D5	LVDS0-D1N	DSI-D1N	PWM0-3	UART2-RX	UART9-CTS		PWMCS-O3			PD-EINT3	PD3	I/O
PD4	I/O	LCD-D6	LVDS0-D2P	DSI-CKP	PWM0-4	UART4-CTS	UART6-TX		PWMCS-O4			PD-EINT4	PD4	I/O
PD5	I/O	LCD-D7	LVDS0-D2N	DSI-CKN	PWM0-5	UART4-RTS	UART6-RX		PWMCS-O5			PD-EINT5	PD5	I/O
PD6	I/O	LCD-D10	LVDS0-CKP	DSI-D2P	PWM0-6	UART4-TX	UART6-RTS		PWMCS-O6			PD-EINT6	PD6	I/O
PD7	I/O	LCD-D11	LVDS0-CKN	DSI-D2N	PWM0-7	UART4-RX	UART6-CTS		PWMCS-O7			PD-EINT7	PD7	I/O
PD8	I/O	LCD-D12	LVDS0-D3P	DSI-D3P	PWM1-0				PWMCS-O8			PD-EINT8	PD8	I/O
PD9	I/O	LCD-D13	LVDS0-D3N	DSI-D3N	PWM1-1	DMIC-CLK			PWMCS-O9			PD-EINT9	PD9	I/O
PD10	I/O	LCD-D14	LVDS1-D0P	SPI1-CS0/DBI-CSX	PWM1-2	DMIC-DATA0	UART8-TX		PWMCS-OA			PD-EINT10	PD10	I/O
PD11	I/O	LCD-D15	LVDS1-D0N	SPI1-CLK/DBI-SCLK	PWM1-3	DMIC-DATA1	UART8-RX		PWMCS-OB			PD-EINT11	PD11	I/O

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PD12	I/O	LCD-D18	LVDS1-D1P	SPI1-MOSI/DBI-SDO	PWM1-4	DMIC-DATA2	UART8-RTS		PWMCS-OC			PD-EINT12	PD12	I/O
PD13	I/O	LCD-D19	LVDS1-D1N	SPI1-MISO/DBI-SDI/DBI-TE/DBI-DCX	PWM1-5	DMIC-DATA3	UART8-CTS		PWMCS-OD			PD-EINT13	PD13	I/O
PD14	I/O	LCD-D20	LVDS1-D2P	SPI1-HOLD/DBI-DCX/DBI-WRX	PWM1-6	UART3-TX	UART8-DCD		PWMCS-OE			PD-EINT14	PD14	I/O
PD15	I/O	LCD-D21	LVDS1-D2N	SPI1-WP/DBI-TE	PWM1-7	UART3-RX	UART8-DSR		PWMCS-OF			PD-EINT15	PD15	I/O
PD16	I/O	LCD-D22	LVDS1-CKP		PWM2-0	UART3-RTS	UART8-DTR		PWMCS-I0			PD-EINT16	PD16	I/O
PD17	I/O	LCD-D23	LVDS1-CKN		PWM2-1	UART3-CTS	UART8-RI		PWMCS-I1			PD-EINT17	PD17	I/O
PD18	I/O	LCD-CLK	LVDS1-D3P	TWI5-SCK	PWM2-2				PWMCS-I2			PD-EINT18	PD18	I/O
PD19	I/O	LCD-DE	LVDS1-D3N	TWI5-SDA	PWM2-3				PWMCS-I3			PD-EINT19	PD19	I/O
PD20	I/O	LCD-HSYNC	PWM2-4	UART3-TX	TWI5-SCK				PWMCS-I4			PD-EINT20	PD20	I/O
PD21	I/O	LCD-VSYNC	PWM2-5	UART3-RX	TWI5-SDA				PWMCS-I5			PD-EINT21	PD21	I/O

4.2.3.5 Port F

Table 4-71 Port F Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PF0	I/O	SDC0-D1	JTAG-MS	UART1-TX			RJTAG-MS	IR0-RX				PF-EINT0	PF0	I/O
PF1	I/O	SDC0-D0	JTAG-DI	UART1-RX			RJTAG-DI	IR1-RX				PF-EINT1	PF1	I/O
PF2	I/O	SDC0-CLK	UART0-TX	DMIC-CLK		SPI3-CLK		IR2-RX				PF-EINT2	PF2	I/O
PF3	I/O	SDC0-CMD	JTAG-DO	DMIC-DATA0		SPI3-CS0	RJTAG-DO	IR3-RX				PF-EINT3	PF3	I/O
PF4	I/O	SDC0-D3	UART0-RX	DMIC-DATA1		SPI3-MOSI		IR-TX				PF-EINT4	PF4	I/O
PF5	I/O	SDC0-D2	JTAG-CK	DMIC-DATA2		SPI3-MISO	RJTAG-CK					PF-EINT5	PF5	I/O

4.2.3.6 Port G

Table 4-72 Port G Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PG0	I/O	SDC1-CLK		UART8-TX	RGMII1-RXD3/RMII1-NULL							PG-EINT0	PG0	I/O

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PG1	I/O	SDC1-CMD		UART8-RX	RGMII1-RXD2/RMII1-NULL							PG-EINT1	PG1	I/O
PG2	I/O	SDC1-D0		UART8-RTS	RGMII1-RXCK/RMII1-NULL							PG-EINT2	PG2	I/O
PG3	I/O	SDC1-D1		UART8-CTS	RGMII1-TXD3/RMII1-NULL							PG-EINT3	PG3	I/O
PG4	I/O	SDC1-D2			RGMII1-TXD2/RMII1-NULL							PG-EINT4	PG4	I/O
PG5	I/O	SDC1-D3			RGMII1-EPHY-25/50M							PG-EINT5	PG5	I/O
PG6	I/O	UART1-TX	TWI4-SCK	UART9-CTS	RGMII1-RXD1/RMII1-RXD1	I2S2-MCLK						PG-EINT6	PG6	I/O
PG7	I/O	UART1-RX	TWI4-SDA	UART9-RTS	RGMII1-RXD0/RMII1-RXD0	I2S2-BCLK						PG-EINT7	PG7	I/O
PG8	I/O	UART1-RTS	TWI5-SCK	UART9-TX	RGMII1-RXCTL/RMII1-CRS-DV	I2S2-LRCK						PG-EINT8	PG8	I/O
PG9	I/O	UART1-CTS	TWI5-SDA	UART9-RX	RGMII1-CLKIN/RMII1-RXER	I2S2-DOUT0	I2S2-DIN1					PG-EINT9	PG9	I/O
PG10	I/O	UART4-TX	I2S1-MCLK	TWI2-SCK	RGMII1-TXD1/RMII1-TXD1	I2S2-DIN0	I2S2-DOUT1					PG-EINT10	PG10	I/O
PG11	I/O	UART4-RX	I2S1-BCLK	TWI2-SDA	RGMII1-TXD0/RMII1-TXD0	DMIC-CLK						PG-EINT11	PG11	I/O
PG12	I/O	UART4-RTS	I2S1-LRCK		RGMII1-TXCK/RMII1-TXCK	DMIC-DATA0						PG-EINT12	PG12	I/O
PG13	I/O	UART4-CTS	I2S1-DOUT0	I2S1-DIN1	RGMII1-TXCTL/RMII1-TXEN	DMIC-DATA1						PG-EINT13	PG13	I/O
PG14	I/O		I2S1-DIN0	I2S1-DOUT1	RGMII1-MDC	DMIC-DATA2						PG-EINT14	PG14	I/O
PG15	I/O				RGMII1-MDIO	DMIC-DATA3						PG-EINT15	PG15	I/O

4.2.3.7 Port K

Table 4-73 Port K Multiplex Function

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PK0	I/O		MCSIA-CKP		UART7-TX	TWI1-SCK	NCSI-D0		I2S1-MCLK		LCD-D0	PK-EINT0	PK0	I/O
PK1	I/O		MCSIA-CKN		UART7-RX	TWI1-SDA	NCSI-D1		I2S1-BCLK		LCD-D1	PK-EINT1	PK1	I/O
PK2	I/O		MCSIA-D0P		UART7-RTS	SPI1-CS0	NCSI-D2		I2S1-LRCK		LCD-D8	PK-EINT2	PK2	I/O

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
PK3	I/O		MCSIA-D0N		UART7-CTS	SPI1-CLK	NCSI-D3		I2S1-DOUT0		LCD-D9	PK-EINT3	PK3	I/O
PK4	I/O		MCSIA-D1P		TWI1-SCK	SPI1-MOSI	NCSI-D4		I2S1-DIN0		LCD-D16	PK-EINT4	PK4	I/O
PK5	I/O		MCSIA-D1N		TWI1-SDA	SPI1-MISO	NCSI-D5				LCD-D17	PK-EINT5	PK5	I/O
PK6	I/O		MCSIA-D2P		MCSI0-MCLK	SPI1-WP	NCSI-D6		UART3-RTS		RGMII0-RXD3/RMII0-NULL	PK-EINT6	PK6	I/O
PK7	I/O		MCSIA-D2N		TWI2-SCK	SPI1-HOLD	NCSI-D7				RGMII0-RXD2/RMII0-NULL	PK-EINT7	PK7	I/O
PK8	I/O		MCSIA-D3P		TWI2-SDA	SPI1-CS1	NCSI-PCLK			CLK-FANOUT0	RGMII0-RXCK/RMII0-NULL	PK-EINT8	PK8	I/O
PK9	I/O		MCSIA-D3N			SPI1-CS2	NCSI-MCLK		UART3-TX	CLK-FANOUT1	RGMII0-TXD3/RMII0-NULL	PK-EINT9	PK9	I/O
PK10	I/O					PWM0-6	NCSI-HSYNC		UART3-RX		RGMII0-TXD2/RMII0-NULL	PK-EINT10	PK10	I/O

4.2.3.8 RTC_GPIO

Pin Name	IO Type	Function												
		2	3	4	5	6	7	8	9	10	11	12	13	14
NMI	I/O, OD	NMI										NMI-EINT0	NMI	I/O, OD

4.3 Detailed Signal Description

The following tables show the detailed function description of every signal based on the different interfaces.

[1] **Signal Name**: The name of every signal.

[2] **Description**: The detailed function description of every signal.

[3] **Type**: Denotes the signal direction:

I (Input),

O (Output),

I/O (Input/Output),

OD (Open-Drain),

A (Analog),

AI (Analog Input),

AO (Analog Output),

A I/O (Analog Input/Output),

P (Power),

G (Ground)

4.3.1 SDRAM

Table 4-74 SDRAM Signal Description

Signal Name[1]	Description[2]	Type[3]
SZQ	DRAM ZQ Calibration(the signal connects to an external reference resistor which is used to calibrate DRAM input/output buffer)	AI
SRST	DRAM Reset Signal	O
SWE	DRAM Write Enable	O
SA0	DRAM Address Signal 0	O
SA1	DRAM Address Signal 1	O
SA2	DRAM Address Signal 2	O
SA3	DRAM Address Signal 3	O
SA4	DRAM Address Signal 4	O
SA5	DRAM Address Signal 5	O
SA6	DRAM Address Signal 6	O

Signal Name[1]	Description[2]	Type[3]
SA7	DRAM Address Signal 7	O
SA8	DRAM Address Signal 8	O
SA9	DRAM Address Signal 9	O
SA10	DRAM Address Signal 10	O
SA11	DRAM Address Signal 11	O
SA12	DRAM Address Signal 12	O
SA13	DRAM Address Signal 13	O
SA14	DRAM Address Signal 14	O
SA15	DRAM Address Signal 15	O
SBA0	DRAM Bank Address Signal 0	O
SBA1	DRAM Bank Address Signal 1	O
SBA2	DRAM Bank Address Signal 2	O
SRAS	DRAM Row Address Strobe	O
SCAS	DRAM Column Address Strobe	O
SCKE0	DRAM Clock Enable Signal to the Memory Device 0	O
SCKN	DRAM Differential Clock (Negative)	O
SCKP	DRAM Differential Clock (Positive)	O
SCS0	DRAM Chip Select Signal to the Memory Device for RANK 0	O
SCS1	DRAM Chip Select Signal to the Memory Device for RANK 1	O
SDQ0	DRAM Bidirectional Data Line 0	I/O
SDQ1	DRAM Bidirectional Data Line 1	I/O
SDQ2	DRAM Bidirectional Data Line 2	I/O
SDQ3	DRAM Bidirectional Data Line 3	I/O
SDQ4	DRAM Bidirectional Data Line 4	I/O
SDQ5	DRAM Bidirectional Data Line 5	I/O
SDQ6	DRAM Bidirectional Data Line 6	I/O
SDQ7	DRAM Bidirectional Data Line 7	I/O
SDQ8	DRAM Bidirectional Data Line 8	I/O
SDQ9	DRAM Bidirectional Data Line 9	I/O
SDQ10	DRAM Bidirectional Data Line 10	I/O

Signal Name[1]	Description[2]	Type[3]
SDQ11	DRAM Bidirectional Data Line 11	I/O
SDQ12	DRAM Bidirectional Data Line 12	I/O
SDQ13	DRAM Bidirectional Data Line 13	I/O
SDQ14	DRAM Bidirectional Data Line 14	I/O
SDQ15	DRAM Bidirectional Data Line 15	I/O
SDQM0	DRAM Data Mask Signal 0	I/O
SDQM1	DRAM Data Mask Signal 1	I/O
SDQS0N	DRAM Bidirectional Data Strobe 0 (Active Low)	I/O
SDQS0P	DRAM Bidirectional Data Strobe 0 (Active High)	I/O
SDQS1N	DRAM Bidirectional Data Strobe 1 (Active Low)	I/O
SDQS1P	DRAM Bidirectional Data Strobe 1 (Active High)	I/O
SODT0	DRAM On-Die Termination Output Signal 0	O
SODT1	DRAM On-Die Termination Output Signal 1	O
SVREF	DRAM Reference Voltage Out	O
VCC-DRAM	DRAM IO Power Supply	P
VDD18-DRAM	SDRAM Controller Power Supply	P

4.3.2 Boot

Table 4-75 Boot Signal Description

Signal Name[1]	Description[2]	Type[3]
FEL	Boot Select Jump to the Try Media Boot process when FEL is high level, or else enter into the mandatory upgrade process.	I
BOOT-SEL0	Boot Media Select 0	I
BOOT-SEL1	Boot Media Select 1	I

4.3.3 RTC_GPIO

Table 4-76 RTC_GPIO Signal Description

Signal Name[1]	Description[2]	Type[3]
GPIO0/1/2/4	General-purpose I/O in RTC power domain	I/O, OD
NMI	Non-Maskable Interrupt	I/O, OD

Signal Name[1]	Description[2]	Type[3]
	NMI pin can act as GPIO by configuring RTC_GPIO_CFG in section GPIO in user manual.	

4.3.4 RTC

Table 4-77 RTC Signal Description

Signal Name[1]	Description[2]	Type[3]
X32KIN	Clock Input of 32.768 kHz Crystal	AI
X32KOUT	Clock Output of 32.768 kHz Crystal	AO
X32KFOUT	32.768 kHz clock Fanout	AO, OD
NMI	Non-Maskable Interrupt NMI pin can act as GPIO by configuring RTC_GPIO_CFG in section GPIO in user manual.	I/O, OD
VCC-RTC	RTC Power Supply	P
TEST	Test Signal	I
RESET	SoC Reset Signal (Active Low)	I/O, OD

4.3.5 PLL

Table 4-78 PLL Signal Description

Signal Name[1]	Description[2]	Type[3]
PLLTEST	PLL Test Signal	AO, OD

4.3.6 DCXO

Table 4-79 DCXO Signal Description

Signal Name[1]	Description[2]	Type[3]
DXIN	Digital Compensated Crystal Oscillator Input	AI
DXOUT	Digital Compensated Crystal Oscillator Output	AO
REFCLK-OUT	Digital Compensated Crystal Oscillator Clock Fanout	AO

4.3.7 Clock Fanout

Table 4-80 Clock Fanout Signal Description

Signal Name[1]	Description[2]	Type[3]
CLK-FANOUT0	Internal Clock Fanout 0	O

Signal Name[1]	Description[2]	Type[3]
	Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, 50 MHz, and so on.	
CLK-FANOUT1	Internal Clock Fanout 1 Optional Frequency: 32 kHz, 12 MHz, 16 MHz, 24 MHz, 25 MHz, 27 MHz, 50 MHz, and so on.	O

4.3.8 SD Card/SDIO/eMMC

Table 4-81 SD Card/SDIO/eMMC Signal Description

Signal Name[1]	Description[2]	Type[3]
SDC0-CMD	SD Card Command Output/Response Input	I/O, OD
SDC0-CLK	SD Card Clock Output	O
SDC0-D0	SD Card Data Input/ Output 0	I/O
SDC0-D1	SD Card Data Input/ Output 1	I/O
SDC0-D2	SD Card Data Input/ Output 2	I/O
SDC0-D3	SD Card Data Input/ Output 3	I/O
SDC1-CMD	SDIO WIFI Command Output/Response Input	I/O, OD
SDC1-CLK	SDIO WIFI Clock Output	O
SDC1-D0	SDIO WIFI Data Input/ Output 0	I/O
SDC1-D1	SDIO WIFI Data Input/ Output 1	I/O
SDC1-D2	SDIO WIFI Data Input/ Output 2	I/O
SDC1-D3	SDIO WIFI Data Input/ Output 3	I/O
SDC2-CMD	eMMC Command Output/Response Input	I/O, OD
SDC2-CLK	eMMC Clock Output	O
SDC2-D0	eMMC Data Input/ Output 0	I/O
SDC2-D1	eMMC Data Input/ Output 1	I/O
SDC2-D2	eMMC Data Input/ Output 2	I/O
SDC2-D3	eMMC Data Input/ Output 3	I/O
SDC2-D4	eMMC Data Input/ Output 4	I/O
SDC2-D5	eMMC Data Input/ Output 5	I/O
SDC2-D6	eMMC Data Input/ Output 6	I/O
SDC2-D7	eMMC Data Input/ Output 7	I/O

Signal Name[1]	Description[2]	Type[3]
SDC2-RST	eMMC Reset	O
SDC2-DS	eMMC Data Strobe	I
SDC3-CMD	SDIO WIFI Command Output/Response Input	I/O, OD
SDC3-CLK	SDIO WIFI Clock Output	O
SDC3-D0	SDIO WIFI Data Input/ Output 0	I/O
SDC3-D1	SDIO WIFI Data Input/ Output 1	I/O
SDC3-D2	SDIO WIFI Data Input/ Output 2	I/O
SDC3-D3	SDIO WIFI Data Input/ Output 3	I/O

4.3.9 Audio Codec

Table 4-82 Audio Codec Signal Description

Signal Name[1]	Description[2]	Type[3]
LINEOUTN	Lineout Negative Differential Output	AO
LINEOUTP	Lineout Positive Differential Output	AO
VRA1	Internal Reference Voltage	A I/O
AVCC	Power Supply for Analog Part	P
AGND	Analog Ground	G

4.3.10 I2S/PCM

Table 4-83 I2S/PCM Signal Description

Signal Name[1]	Description[2]	Type[3]
I2S0-MCLK	I2S0 Master Clock	O
I2S0-LRCK	I2S0/PCM0 Sample Rate Clock/Sync	I/O
I2S0-BCLK	I2S0/PCM0 Bit Rate Clock	I/O
I2S0-DIN0	I2S0/PCM0 Serial Data Input 0	I
I2S0-DIN1	I2S0/PCM0 Serial Data Input 1	I
I2S0-DIN2	I2S0/PCM0 Serial Data Input 2	I
I2S0-DIN3	I2S0/PCM0 Serial Data Input 3	I
I2S0-DOUT0	I2S0/PCM0 Serial Data Output 0	O
I2S0-DOUT1	I2S0/PCM0 Serial Data Output 1	O
I2S0-DOUT2	I2S0/PCM0 Serial Data Output 2	O

Signal Name[1]	Description[2]	Type[3]
I2S0-DOUT3	I2S0/PCM0 Serial Data Output 3	O
I2S1-MCLK	I2S1 Master Clock	O
I2S1-LRCK	I2S1/PCM1 Sample Rate Clock/Sync	I/O
I2S1-BCLK	I2S1/PCM1 Bit Rate Clock	I/O
I2S1-DIN0	I2S1/PCM1 Serial Data Input 0	I
I2S1-DIN1	I2S1/PCM1 Serial Data Input 1	I
I2S1-DOUT0	I2S1/PCM1 Serial Data Output 0	O
I2S1-DOUT1	I2S1/PCM1 Serial Data Output 1	O
I2S2-MCLK	I2S2 Master Clock	O
I2S2-LRCK	I2S2/PCM2 Sample Rate Clock/Sync	I/O
I2S2-BCLK	I2S2/PCM2 Bit Rate Clock	I/O
I2S2-DIN0	I2S2/PCM2 Serial Data Input 0	I
I2S2-DIN1	I2S2/PCM2 Serial Data Input 1	I
I2S2-DIN2	I2S2/PCM2 Serial Data Input 2	I
I2S2-DIN3	I2S2/PCM2 Serial Data Input 3	I
I2S2-DOUT0	I2S2/PCM2 Serial Data Output 0	O
I2S2-DOUT1	I2S2/PCM2 Serial Data Output 1	O
I2S2-DOUT2	I2S2/PCM2 Serial Data Output 2	O
I2S2-DOUT3	I2S2/PCM2 Serial Data Output 3	O

4.3.11 DMIC

Table 4-84 DMIC Signal Description

Signal Name[1]	Description[2]	Type[3]
DMIC-CLK	Digital Microphone Clock Output	O
DMIC-DATA0	Digital Microphone Data Input 0	I
DMIC-DATA1	Digital Microphone Data Input 1	I
DMIC-DATA2	Digital Microphone Data Input 2	I
DMIC-DATA3	Digital Microphone Data Input 3	I

4.3.12 OWA

Table 4-85 OWA Signal Description

Signal Name[1]	Description[2]	Type[3]
OWA-IN	One Wire Audio Input	I
OWA-OUT	One Wire Audio Output	O

4.3.13 SPI_Flash

Table 4-86 SPI_Flash Signal Description

Signal Name[1]	Description[2]	Type[3]
SPIF0-CS0	SPIF0 Peripheral Chip Select Signal 0, Low Active	O
SPIF0-D4	SPIF0 Master Mode Data 4 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF0-D5	SPIF0 Master Mode Data 5 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF0-D6	SPIF0 Master Mode Data 6 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF0-D7	SPIF0 Master Mode Data 7 in Octal Mode In single/dual/quad mode, this port should stay low.	I/O
SPIF0-CLK	SPIF0 Master Mode Clock Output	O
SPIF0-MOSI	SPIF0 Master Data Out, Slave Data In	I/O
SPIF0-MISO	SPIF0Master Data In, Slave Data Out	I/O
SPIF0-DQS	SPIF0 Data Strobe Signal	I
SPIF0-WP	SPIF0 Write Protection (Active Low)	I/O
SPIF0-HOLD	SPIF0Hold Signal	I/O

4.3.14 MIPI CSI

Table 4-87 MIPI CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
MCSI0-MCLK	MIPI CSI A Master Clock	O
MCSIA-CKN	MIPI CSI A Differential Receive Clock Signal (Negative)	AI
MCSIA-CKP	MIPI CSI A Differential Receive Clock Signal (Positive)	AI
MCSIA-D0N	MIPI CSI A Data Line 0 Input (Negative)	AI

Signal Name[1]	Description[2]	Type[3]
MCSIA-D0P	MIPI CSI A Data Line 0 Input (Positive)	AI
MCSIA-D1N/MCSIC-D0N	MIPI CSI A Data Line 1 Input (Negative) / MIPI CSI C Data Line 0 Input (Negative)	AI
MCSIA-D1P/MCSIC-D0P	MIPI CSI A Data Line 1 Input (Positive) / MIPI CSI C Data Line 0 Input (Positive)	AI
MCSI1-MCLK	MIPI CSI B Master Clock	O
MCSIB-CKN	MIPI CSI B Differential Receive Clock Signal (Negative)	AI
MCSIB-CKP	MIPI CSI B Differential Receive Clock Signal (Positive)	AI
MCSIB-D0N/MCSIA-D3N	MIPI CSI B Data Line 0 Input (Negative)/MIPI CSI A Data Line 3 Input (Negative)	AI
MCSIB-D0P/MCSIA-D3P	MIPI CSI B Data Line 0 Input (Positive)/MIPI CSI A Data Line 3 Input (Positive)	AI
MCSIB-D1N/MCSIC-CKN/MCSIA-D2N	MIPI CSI B Data Line 1 Input (Negative)/MIPI CSI C Differential Receive Clock Signal (Negative)/MIPI CSI A Data Line 2 Input (Negative)	AI
MCSIB-D1P/MCSIC-CKP/MCSIA-D2P	MIPI CSI B Data Line 1 Input (Positive)/MIPI CSI C Differential Receive Clock Signal (Positive)/MIPI CSI A Data Line 2 Input (Positive)	AI
MCSI2-MCLK	MIPI CSI C Master Clock	O
CSI0-XHS	CSI Horizontal SYNC 0	O
CSI1-XHS	CSI Horizontal SYNC 1	O
CSI0-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC 0	I/O
CSI1-XVS-FSYNC	CSI Vertical SYNC/Frame SYNC 1	I/O

4.3.15 Parallel CSI

Table 4-88 Parallel CSI Signal Description

Signal Name[1]	Description[2]	Type[3]
NCSI-PCLK	Parallel CSI Pixel Clock Input	I
NCSI-MCLK	Parallel CSI Master Clock Output	O
NCSI-HSYNC	Parallel CSI Horizontal Synchronous Input	I
NCSI-VSYNC	Parallel CSI Vertical Synchronous Input	I
NCSI-D0	Parallel CSI Pixel Data 0	I
NCSI-D1	Parallel CSI Pixel Data 1	I

Signal Name[1]	Description[2]	Type[3]
NCSI-D2	Parallel CSI Pixel Data 2	I
NCSI-D3	Parallel CSI Pixel Data 3	I
NCSI-D4	Parallel CSI Pixel Data 4	I
NCSI-D5	Parallel CSI Pixel Data 5	I
NCSI-D6	Parallel CSI Pixel Data 6	I
NCSI-D7	Parallel CSI Pixel Data 7	I
NCSI-D8	Parallel CSI Pixel Data 8	I
NCSI-D9	Parallel CSI Pixel Data 9	I
NCSI-D10	Parallel CSI Pixel Data 10	I
NCSI-D11	Parallel CSI Pixel Data 11	I
NCSI-D12	Parallel CSI Pixel Data 12	I
NCSI-D13	Parallel CSI Pixel Data 13	I
NCSI-D14	Parallel CSI Pixel Data 14	I
NCSI-D15	Parallel CSI Pixel Data 15	I

4.3.16 LCD

Table 4-89 LCD Signal Description

Signal Name[1]	Description[2]	Type[3]
LCD-CLK	LCD Clock	O
LCD-VSYNC	LCD Vertical Synchronization	O
LCD-HSYNC	LCD Horizontal Synchronization	O
LCD-DE	LCD Data Enable	O
TCON-FSYNC0	Frame Synchronization Signal for TCON and Sensor	O
LCD-D0	LCD Data Input/Output 0	I/O
LCD-D1	LCD Data Input/Output 1	I/O
LCD-D2	LCD Data Input/Output 2	I/O
LCD-D3	LCD Data Input/Output 3	I/O
LCD-D4	LCD Data Input/Output 4	I/O
LCD-D5	LCD Data Input/Output 5	I/O
LCD-D6	LCD Data Input/Output 6	I/O

Signal Name[1]	Description[2]	Type[3]
LCD-D7	LCD Data Input/Output 7	I/O
LCD-D8	LCD Data Input/Output 8	I/O
LCD-D9	LCD Data Input/Output 9	I/O
LCD-D10	LCD Data Input/Output 10	I/O
LCD-D11	LCD Data Input/Output 11	I/O
LCD-D12	LCD Data Input/Output 12	I/O
LCD-D13	LCD Data Input/Output 13	I/O
LCD-D14	LCD Data Input/Output 14	I/O
LCD-D15	LCD Data Input/Output 15	I/O
LCD-D16	LCD Data Input/Output 16	I/O
LCD-D17	LCD Data Input/Output 17	I/O
LCD-D18	LCD Data Input/Output 18	I/O
LCD-D19	LCD Data Input/Output 19	I/O
LCD-D20	LCD Data Input/Output 20	I/O
LCD-D21	LCD Data Input/Output 21	I/O
LCD-D22	LCD Data Input/Output 22	I/O
LCD-D23	LCD Data Input/Output 23	I/O

4.3.17 LVDS

Table 4-90 LVDS Signal Description

Signal Name[1]	Description[2]	Type[3]
LVDS0-CKP	LVDS0 Differential Clock (Positive)	AO
LVDS0-CKN	LVDS0 Differential Clock (Negative)	AO
LVDS0-D0P	LVDS0 Differential Data 0 (Positive)	AO
LVDS0-D0N	LVDS0 Differential Data 0 (Negative)	AO
LVDS0-D1P	LVDS0 Differential Data 1 (Positive)	AO
LVDS0-D1N	LVDS0 Differential Data 1 (Negative)	AO
LVDS0-D2P	LVDS0 Differential Data 2 (Positive)	AO
LVDS0-D2N	LVDS0 Differential Data 2 (Negative)	AO
LVDS0-D3P	LVDS0 Differential Data 3 (Positive)	AO

Signal Name[1]	Description[2]	Type[3]
LVDS0-D3N	LVDS0 Differential Data 3 (Negative)	AO
LVDS1-CKP	LVDS1 Differential Clock (Positive)	AO
LVDS1-CKN	LVDS1 Differential Clock (Negative)	AO
LVDS1-D0P	LVDS1 Differential Data 0 (Positive)	AO
LVDS1-D0N	LVDS1 Differential Data 0 (Negative)	AO
LVDS1-D1P	LVDS1 Differential Data 1 (Positive)	AO
LVDS1-D1N	LVDS1 Differential Data 1 (Negative)	AO
LVDS1-D2P	LVDS1 Differential Data 2 (Positive)	AO
LVDS1-D2N	LVDS1 Differential Data 2 (Negative)	AO
LVDS1-D3P	LVDS1 Differential Data 3 (Positive)	AO
LVDS1-D3N	LVDS1 Differential Data 3 (Negative)	AO
VCC18-LVDS	LVDS 1.8V Power Supply	P

4.3.18 MIPI DSI

Table 4-91 MIPI DSI Signal Description

Signal Name[1]	Description[2]	Type[3]
DSI-CKP	DSI Differential Clock (Positive)	AO
DSI-CKN	DSI Differential Clock (Negative)	AO
DSI-D0P	DSI Differential Data Line 0 (Positive)	A I/O
DSI-D0N	DSI Differential Data Line 0 (Negative)	A I/O
DSI-D1P	DSI Differential Data Line 1 (Positive)	AO
DSI-D1N	DSI Differential Data Line 1 (Negative)	AO
DSI-D2P	DSI Differential Data Line 2 (Positive)	AO
DSI-D2N	DSI Differential Data Line 2 (Negative)	AO
DSI-D3P	DSI Differential Data Line 3 (Positive)	AO
DSI-D3N	DSI Differential Data Line 3 (Negative)	AO

4.3.19 CAN-FD

Table 4-92 CAN-FD Signal Description

Signal Name[1]	Description[2]	Type[3]
CAN0-RX0	CAN0 Receive Data 0	I

Signal Name[1]	Description[2]	Type[3]
CAN0-TX0	CAN0 Transmit Data 0	O
CAN1-RX0	CAN1 Receive Data 0	I
CAN1-TX0	CAN1 Transmit Data 0	O

4.3.20 Local Bus Controller

Table 4-93 Local Bus Controller Signal Description

Signal Name[1]	Description[2]	Type[3]
LBUS-CLK	LBC Clock Output	O
LBUS-CS0	LBC Chip Select Signal 0	O
LBUS-CS1	LBC Chip Select Signal 1	O
LBUS-CS2	LBC Chip Select Signal 2	O
LBUS-CS3	LBC Chip Select Signal 3	O
LBUS-DP0	LBC Data Parity Signal 0	I/O
LBUS-DP1	LBC Data Parity Signal 1	I/O
LBUS-DP2	LBC Data Parity Signal 2	I/O
LBUS-DP3	LBC Data Parity Signal 3	I/O
LBUS-WR	LBC Write Ready	O
LBUS-OE	LBC Output Enable	O
LBUS-DE	LBC Data Enable	O
LBUS-WAIT	LBC Wait	O
LBUS-READY0	LBC Input Ready 0	I
LBUS-READY1	LBC Input Ready 1	I
LBUS-READY2	LBC Input Ready 2	I
LBUS-READY3	LBC Input Ready 3	I
LBUS-ALE	LBC Address Lock Enable	O
LBUS-DRQ0	LBC Asynchronous Data Request 0	I
LBUS-DRQ1	LBC Asynchronous Data Request 1	I
LBUS-LBE0	LBC Byte Enable 0	O
LBUS-LBE1	LBC Byte Enable 1	O
LBUS-LBE2	LBC Byte Enable 2	O

Signal Name[1]	Description[2]	Type[3]
LBUS-LBE3	LBC Byte Enable 3	O
LBUS-LD0	LBC Data 0	I/O
LBUS-LD1	LBC Data 1	I/O
LBUS-LD2	LBC Data 2	I/O
LBUS-LD3	LBC Data 3	I/O
LBUS-LD4	LBC Data 4	I/O
LBUS-LD5	LBC Data 5	I/O
LBUS-LD6	LBC Data 6	I/O
LBUS-LD7	LBC Data 7	I/O
LBUS-LD8	LBC Data 8	I/O
LBUS-LD9	LBC Data 9	I/O
LBUS-LD10	LBC Data 10	I/O
LBUS-LD11	LBC Data 11	I/O
LBUS-LD12	LBC Data 12	I/O
LBUS-LD13	LBC Data 13	I/O
LBUS-LD14	LBC Data 14	I/O
LBUS-LD15	LBC Data 15	I/O
LBUS-LD16	LBC Data 16	I/O
LBUS-LD17	LBC Data 17	I/O
LBUS-LD18	LBC Data 18	I/O
LBUS-LD19	LBC Data 19	I/O
LBUS-LD20	LBC Data 20	I/O
LBUS-LD21	LBC Data 21	I/O
LBUS-LD22	LBC Data 22	I/O
LBUS-LD23	LBC Data 23	I/O
LBUS-LD24	LBC Data 24	I/O
LBUS-LD25	LBC Data 25	I/O
LBUS-LD26	LBC Data 26	I/O
LBUS-LD27	LBC Data 27	I/O
LBUS-LD28	LBC Data 28	I/O

Signal Name[1]	Description[2]	Type[3]
LBUS-LD29	LBC Data 29	I/O
LBUS-LD30	LBC Data 30	I/O
LBUS-LD31	LBC Data 31	I/O

4.3.21 GMAC

Table 4-94 GMAC Signal Description

Signal Name[1]	Description[2]	Type[3]
RGMII0-RXD0/RMII0-RXD0	RGMII0/RMII0 Receive Data 0	I
RGMII0-RXD1/RMII0-RXD1	RGMII0/RMII0 Receive Data 1	I
RGMII0-RXD2/RMII0-NULL	RGMII0 Receive Data 2	I
RGMII0-RXD3/RMII0-NULL	RGMII0 Receive Data 3	I
RGMII0-TXD0/RMII0-TXD0	RGMII0/RMII0 Transmit Data 0	O
RGMII0-TXD1/RMII0-TXD1	RGMII0/RMII0 Transmit Data 1	O
RGMII0-TXD2/RMII0-NULL	RGMII0 Transmit Data 2	O
RGMII0-TXD3/RMII0-NULL	RGMII0 Transmit Data 3	O
RGMII0-RXCTL/RMII0-CRS-DV	RGMII0 Receive Control/RMII0 Carrier Sense Receive Data Valid	I
RGMII0-RXCK/RMII0-NULL	RGMII0 Receive Clock	I
RGMII0-TXCK/RMII0-TXCK	RGMII0/RMII0 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input.	I/O
RGMII0-CLKIN/RMII0-RXER	RGMII0 Transmit Clock from External/RMII0 Receive Error	I
RGMII0-TXCTL/RMII0-TXEN	RGMII0 Transmit Control/RMII0 Transmit Enable	O
RGMII0-MDC	RGMII0 Management Data Clock	O
RGMII0-MDIO	RGMII0 Management Data Input/ Output	I/O
RGMII0-EPHY-25/50M	GMAC PHY 25 MHz or 50 MHz Clock Output	O
RGMII1-RXD0/RMII1-RXD0	RGMII1/RMII1 Receive Data 0	I
RGMII1-RXD1/RMII1-RXD1	RGMII1/RMII1 Receive Data 1	I
RGMII1-RXD2/RMII1-NULL	RGMII1 Receive Data 2	I
RGMII1-RXD3/RMII1-NULL	RGMII1 Receive Data 3	I

Signal Name[1]	Description[2]	Type[3]
RGMII1-TXD0/RMII1-TXD0	RGMII1/RMII1 Transmit Data 0	O
RGMII1-TXD1/RMII1-TXD1	RGMII1/RMII1 Transmit Data 1	O
RGMII1-TXD2/RMII1-NULL	RGMII1 Transmit Data 2	O
RGMII1-TXD3/RMII1-NULL	RGMII1 Transmit Data 3	O
RGMII1-RXCK/RMII1-NULL	RGMII1 Receive Clock	I
RGMII1-TXCK/RMII1-TXCK	RGMII1/RMII1 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input.	I/O
RGMII1-CLKIN/RMII1-RXER	RGMII1 Transmit Clock from External/RMII1 Receive Error	I
RGMII1-RXCTL/RMII1-CRS-DV	RGMII1 Receive Control/RMII1 Carrier Sense Receive Data Valid	I
RGMII1-TXCTL/RMII1-TXEN	RGMII1 Transmit Control/RMII1 Transmit Enable	O
RGMII1-MDC	RGMII1 Management Data Clock	O
RGMII1-MDIO	RGMII1 Management Data Input/ Output	I/O
RGMII1-EPHY-25/50M	GMAC PHY 25 MHz or 50 MHz Clock Output	O
RGMII2-RXD0/RMII2-RXD0	RGMII2/RMII2 Receive Data 0	I
RGMII2-RXD1/RMII2-RXD1	RGMII2/RMII2 Receive Data 1	I
RGMII2-RXD2/RMII2-NULL	RGMII2 Receive Data 2	I
RGMII2-RXD3/RMII2-NULL	RGMII2 Receive Data 3	I
RGMII2-TXD0/RMII2-TXD0	RGMII2/RMII2 Transmit Data 0	O
RGMII2-TXD1/RMII2-TXD1	RGMII2/RMII2 Transmit Data 1	O
RGMII2-TXD2/RMII2-NULL	RGMII2 Transmit Data 2	O
RGMII2-TXD3/RMII2-NULL	RGMII2 Transmit Data 3	O
RGMII2-RXCK/RMII2-NULL	RGMII2 Receive Clock	I
RGMII2-TXCK/RMII2-TXCK	RGMII2/RMII2 Transmit Clock For RGMII, IO type is output; For RMII, IO type is input.	I/O
RGMII2-CLKIN/RMII2-RXER	RGMII2 Transmit Clock from External/RMII2 Receive Error	I
RGMII2-RXCTL/RMII2-CRS-DV	RGMII2 Receive Control/RMII2 Carrier Sense Receive Data Valid	I

Signal Name[1]	Description[2]	Type[3]
RGMII2-TXCTL/RMII2-TXEN	RGMII2 Transmit Control/RMII2 Transmit Enable	O
RGMII2-MDC	RGMII2 Management Data Clock	O
RGMII2-MDIO	RGMII2 Management Data Input/ Output	I/O
RGMII2-EPHY-25/50M	GMAC PHY 25 MHz or 50 MHz Clock Output	O

4.3.22 USB2.0 DRD & USB2.0 Host

Table 4-95 USB2.0 DRD & USB2.0 Host Signal Description

Signal Name[1]	Description[2]	Type[3]
USB0-DM	USB2.0 DRD Data Signal DM	AI/O
USB0-DP	USB2.0 DRD Data Signal DP	AI/O
USB1-DM	USB2.0 Host Data Signal DM	AI/O
USB1-DP	USB2.0 Host Data Signal DP	AI/O
VCC33-USB0-USB1	USB2.0 DRD and USB 2.0 Host 3.3V Power Supply	P
VCC33-USB-LDOAIN	USB2.0 DRD and USB 2.0 Host /LDOA Input Power Supply	P

4.3.23 PWM

Table 4-96 PWM Signal Description

Signal Name[1]	Description[2]	Type[3]
PWM2-0	PWM2 Waveform Output /Capture Waveform Input 0	I/O
PWM2-1	PWM2 Waveform Output /Capture Waveform Input 1	I/O
PWM2-2	PWM2 Waveform Output /Capture Waveform Input 2	I/O
PWM2-3	PWM2 Waveform Output /Capture Waveform Input 3	I/O
PWM2-4	PWM2 Waveform Output /Capture Waveform Input 4	I/O
PWM2-5	PWM2 Waveform Output /Capture Waveform Input 5	I/O
PWM2-6	PWM2 Waveform Output /Capture Waveform Input 6	I/O
PWM2-7	PWM2 Waveform Output /Capture Waveform Input 7	I/O
PWM2-8	PWM2 Waveform Output /Capture Waveform Input 8	I/O
PWM2-9	PWM2 Waveform Output /Capture Waveform Input 9	I/O
PWM2-10	PWM2 Waveform Output /Capture Waveform Input 10	I/O
PWM2-11	PWM2 Waveform Output /Capture Waveform Input 11	I/O
PWM2-12	PWM2 Waveform Output /Capture Waveform Input 12	I/O

Signal Name[1]	Description[2]	Type[3]
PWM2-13	PWM2 Waveform Output /Capture Waveform Input 13	I/O

4.3.24 PWMCS

Table 4-97 PWMCS Signal Description

Signal Name[1]	Description[2]	Type[3]
PWMCS-O0	PWMCS Waveform Output 0	O
PWMCS-O1	PWMCS Waveform Output 1	O
PWMCS-O2	PWMCS Waveform Output 2	O
PWMCS-O3	PWMCS Waveform Output 3	O
PWMCS-O4	PWMCS Waveform Output 4	O
PWMCS-O5	PWMCS Waveform Output 5	O
PWMCS-O6	PWMCS Waveform Output 6	O
PWMCS-O7	PWMCS Waveform Output 7	O
PWMCS-O8	PWMCS Waveform Output 8	O
PWMCS-O9	PWMCS Waveform Output 9	O
PWMCS-OA	PWMCS Waveform Output 10	O
PWMCS-OB	PWMCS Waveform Output 11	O
PWMCS-OC	PWMCS Waveform Output 12	O
PWMCS-OD	PWMCS Waveform Output 13	O
PWMCS-OE	PWMCS Waveform Output 14	O
PWMCS-OF	PWMCS Waveform Output 15	O
PWMCS-I0	PWMCS Capture Waveform Input 0	I
PWMCS-I1	PWMCS Capture Waveform Input 1	I
PWMCS-I2	PWMCS Capture Waveform Input 2	I
PWMCS-I3	PWMCS Capture Waveform Input 3	I
PWMCS-I4	PWMCS Capture Waveform Input 4	I
PWMCS-I5	PWMCS Capture Waveform Input 5	I
PWMCS-I6	PWMCS Capture Waveform Input 6	I
PWMCS-I7	PWMCS Capture Waveform Input 7	I
PWMCS-I8	PWMCS Capture Waveform Input 8	I

Signal Name[1]	Description[2]	Type[3]
PWMCS-I9	PWMCS Capture Waveform Input 9	I
PWMCS-IA	PWMCS Capture Waveform Input 10	I
PWMCS-IB	PWMCS Capture Waveform Input 11	I
PWMCS-IC	PWMCS Capture Waveform Input 12	I
PWMCS-ID	PWMCS Capture Waveform Input 13	I
PWMCS-IE	PWMCS Capture Waveform Input 14	I
PWMCS-IF	PWMCS Capture Waveform Input 15	I
PWM0-0	PWM0 Waveform Output /Capture Waveform Input 0	I/O
PWM0-1	PWM0 Waveform Output /Capture Waveform Input 1	I/O
PWM0-2	PWM0 Waveform Output /Capture Waveform Input 2	I/O
PWM0-3	PWM0 Waveform Output /Capture Waveform Input 3	I/O
PWM0-4	PWM0 Waveform Output /Capture Waveform Input 4	I/O
PWM0-5	PWM0 Waveform Output /Capture Waveform Input 5	I/O
PWM0-6	PWM0 Waveform Output /Capture Waveform Input 6	I/O
PWM0-7	PWM0 Waveform Output /Capture Waveform Input 7	I/O
PWM1-0	PWM1 Waveform Output /Capture Waveform Input 0	I/O
PWM1-1	PWM1 Waveform Output /Capture Waveform Input 1	I/O
PWM1-2	PWM1 Waveform Output /Capture Waveform Input 2	I/O
PWM1-3	PWM1 Waveform Output /Capture Waveform Input 3	I/O
PWM1-4	PWM1 Waveform Output /Capture Waveform Input 4	I/O
PWM1-5	PWM1 Waveform Output /Capture Waveform Input 5	I/O
PWM1-6	PWM1 Waveform Output /Capture Waveform Input 6	I/O
PWM1-7	PWM1 Waveform Output /Capture Waveform Input 7	I/O

4.3.25 SPI&SPI_DBI

Table 4-98 SPI&SPI_DBI Signal Description

Signal Name[1]	Description[2]	Type[3]
SPI0-CS0	SPI0 Chip Select 0 (Active Low)	I/O
SPI0-CS1	SPI0 Chip Select 1 (Active Low)	I/O
SPI0-CLK	SPI0 Clock	I/O

Signal Name[1]	Description[2]	Type[3]
SPI0-MOSI	SPI0 Master Data Out, Slave Data In	I/O
SPI0-MISO	SPI0 Master Data In, Slave Data Out	I/O
SPI0-WP	SPI0 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI0-HOLD	SPI0 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-CS0	SPI1 Chip Select 0 (Active Low)	I/O
SPI1-CS1	SPI1 Chip Select 1 (Active Low)	I/O
SPI1-CS2	SPI1 Chip Select 2 (Active Low)	I/O
SPI1-CLK	SPI1 Clock	I/O
SPI1-MOSI	SPI1 Master Data Out, Slave Data In	I/O
SPI1-MISO	SPI1 Master Data In, Slave Data Out	I/O
SPI1-WP	SPI1 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI1-HOLD	SPI1 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI2-CS0	SPI2 Chip Select 0 (Active Low)	I/O
SPI2-CS1	SPI2 Chip Select 1 (Active Low)	I/O
SPI2-CS2	SPI2 Chip Select 2 (Active Low)	I/O
SPI2-CLK	SPI2 Clock	I/O
SPI2-MOSI	SPI2 Master Data Out, Slave Data In	I/O
SPI2-MISO	SPI2 Master Data In, Slave Data Out	I/O
SPI2-WP	SPI2 Write Protection (Active Low)/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI2-HOLD	SPI2 Hold Signal/ Serial Data Input and Output for Quad Input or Quad Output	I/O
SPI3-CS0	SPI3 Chip Select 0 (Active Low)	I/O
SPI3-CS1	SPI3 Chip Select 1 (Active Low)	I/O
SPI3-CS2	SPI3 Chip Select 2 (Active Low)	I/O
SPI3-CLK	SPI3 Clock	I/O
SPI3-MOSI	SPI3 Master Data Out, Slave Data In	I/O
SPI3-MISO	SPI3 Master Data In, Slave Data Out	I/O

Signal Name[1]	Description[2]	Type[3]
DBI-CSX	Chip Select Signal (Active Low)	I/O
DBI-SCLK	Serial Clock Signal	I/O
DBI-SDO	Data Output Signal	I/O
DBI-SDI	Data Input Signal The data is sampled on the rising edge and the falling edge.	I/O
DBI-TE	Tearing Effect Input It is used to capture the external TE signal edge. The rising and falling edge is configurable.	I/O
DBI-DCX	DCX pin is the select output signal of data and command. DCX = 0: register command; DCX = 1: data or parameter.	I/O
DBI-WRX	When DBI operates in dual data lane format, the RGB666 format 2 can use WRX to transfer data	I/O

4.3.26 UART

Table 4-99 UART Signal Description

Signal Name[1]	Description[2]	Type[3]
UART0-RX	UART0 Data Receiver	I
UART0-TX	UART0 Data Transmitter	O
UART1-RX	UART1 Data Receiver	I
UART1-TX	UART1 Data Transmitter	O
UART1-CTS	UART1 Clear to Send	I
UART1-RTS	UART1 Request to Send	O
UART2-RX	UART2 Data Receiver	I
UART2-TX	UART2 Data Transmitter	O
UART2-CTS	UART2 Clear to Send	I
UART2-RTS	UART2 Request to Send	O
UART3-RX	UART3 Data Receiver	I
UART3-TX	UART3 Data Transmitter	O
UART3-CTS	UART3 Clear to Send	I
UART3-RTS	UART3 Request to Send	O
UART4-RX	UART4 Data Receiver	I

Signal Name[1]	Description[2]	Type[3]
UART4-TX	UART4 Data Transmitter	O
UART4-CTS	UART4 Clear to Send	I
UART4-RTS	UART4 Request to Send	O
UART5-RX	UART5 Data Receiver	I
UART5-TX	UART5 Data Transmitter	O
UART5-CTS	UART5 Clear to Send	I
UART5-RTS	UART5 Request to Send	O
UART6-RX	UART6 Data Receiver	I
UART6-TX	UART6 Data Transmitter	O
UART6-CTS	UART6 Clear to Send	I
UART6-RTS	UART6 Request to Send	O
UART7-RX	UART7 Data Receiver	I
UART7-TX	UART7 Data Transmitter	O
UART7-CTS	UART7 Clear to Send	I
UART7-RTS	UART7 Request to Send	O
UART8-RX	UART8 Data Receiver	I
UART8-TX	UART8 Data Transmitter	O
UART8-CTS	UART8 Clear to Send	I
UART8-RTS	UART8 Request to Send	O
UART8-DCD	UART8 Data Carrier Detect	I
UART8-DSR	UART8 Data Set Ready	I
UART8-DTR	UART8 Data Terminal Ready	O
UART8-RI	UART8 Ring Information	I
UART9-RX	UART9 Data Receiver	I
UART9-TX	UART9 Data Transmitter	O
UART9-CTS	UART9 Clear to Send	I
UART9-RTS	UART9 Request to Send	O

4.3.27 TWI

Table 4-100 TWI Signal Description

Signal Name[1]	Description[2]	Type[3]
TWI0-SCK	TWI0 Serial Clock Signal	I/O
TWI0-SDA	TWI0 Serial Data Signal	I/O
TWI1-SCK	TWI1 Serial Clock Signal	I/O
TWI1-SDA	TWI1 Serial Data Signal	I/O
TWI2-SCK	TWI2 Serial Clock Signal	I/O
TWI2-SDA	TWI2 Serial Data Signal	I/O
TWI3-SCK	TWI3 Serial Clock Signal	I/O
TWI3-SDA	TWI3 Serial Data Signal	I/O
TWI4-SCK	TWI4 Serial Clock Signal	I/O
TWI4-SDA	TWI4 Serial Data Signal	I/O
TWI5-SCK	TWI5 Serial Clock Signal	I/O
TWI5-SDA	TWI5 Serial Data Signal	I/O

4.3.28 GPADC

Table 4-101 GPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
GPADC0-0	General Purpose ADC 0 Input Channel 0	AI
GPADC0-1	General Purpose ADC 0 Input Channel 1	AI
GPADC0-2	General Purpose ADC 0 Input Channel 2	AI
GPADC0-3	General Purpose ADC 0 Input Channel 3	AI
GPADC0-4	General Purpose ADC 0 Input Channel 4	AI
GPADC0-5	General Purpose ADC 0 Input Channel 5	AI
GPADC0-6	General Purpose ADC 0 Input Channel 6	AI
GPADC0-7	General Purpose ADC 0 Input Channel 7	AI
GPADC0-8	General Purpose ADC 0 Input Channel 8	AI
GPADC0-9	General Purpose ADC 0 Input Channel 9	AI
GPADC1-0	General Purpose ADC 1 Input Channel 0	AI
GPADC1-1	General Purpose ADC 1 Input Channel 1	AI

Signal Name[1]	Description[2]	Type[3]
GPADC1-2	General Purpose ADC 1 Input Channel 2	AI
GPADC1-3	General Purpose ADC 1 Input Channel 3	AI
GPADC1-4	General Purpose ADC 1 Input Channel 4	AI
GPADC1-5	General Purpose ADC 1 Input Channel 5	AI
GPADC1-6	General Purpose ADC 1 Input Channel 6	AI
GPADC1-7	General Purpose ADC 1 Input Channel 7	AI
GPADC1-8	General Purpose ADC 1 Input Channel 8	AI
GPADC1-9	General Purpose ADC 1 Input Channel 9	AI
GPADC2-0	General Purpose ADC 2 Input Channel 0	AI
GPADC2-1	General Purpose ADC 2 Input Channel 1	AI
GPADC2-2	General Purpose ADC 2 Input Channel 2	AI
GPADC2-3	General Purpose ADC 2 Input Channel 3	AI
AGND-ADC	Analog Ground	G

4.3.29 TPADC

Table 4-102 TPADC Signal Description

Signal Name[1]	Description[2]	Type[3]
TP-X1	Touch Panel X1 Input	AI
TP-X2	Touch Panel X2 Input	AI
TP-Y1	Touch Panel Y1 Input	AI
TP-Y2	Touch Panel Y2 Input	AI

4.3.30 LEDC

Table 4-103 LEDC Signal Description

Signal Name[1]	Description[2]	Type[3]
LEDC	Intelligent Control LED Signal Output	O

4.3.31 IR_TX

Table 4-104 IR_TX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR-TX	Consumer Infrared Transmitter	O

4.3.32 IR_RX

Table 4-105 IR_RX Signal Description

Signal Name[1]	Description[2]	Type[3]
IR0-RX	Consumer Infrared Receiver	I
IR1-RX	Consumer Infrared Receiver	I
IR2-RX	Consumer Infrared Receiver	I
IR3-RX	Consumer Infrared Receiver	I

4.3.33 JTAG

Table 4-106 JTAG Signal Description

Signal Name[1]	Description[2]	Type[3]
JTAG-MS	Arm® CPU JTAG Mode Selection	I
JTAG-CK	Arm® CPU JTAG Clock Signal	I
JTAG-DI	Arm® CPU JTAG Data Input	I
JTAG-DO	Arm® CPU JTAG Data Output	O
RJTAG-MS	RISC-V JTAG Mode Selection	I
RJTAG-CK	RISC-VJTAG Clock Signal	I
RJTAG-DI	RISC-V JTAG Data Input	I
RJTAG-DO	RISC-V JTAG Data Output	O

4.3.34 Interrupt

Table 4-107 Interrupt Signal Description

Signal Name[1]	Description[2]	Type[3]
PA-EINT [23:0]	Port A Interrupt	I
PB-EINT [14:0]	Port B Interrupt	I
PC-EINT [11:0]	Port C Interrupt	I
PD-EINT [23:0]	Port D Interrupt	I
PE-EINT [9:0]	Port E Interrupt	I
PF-EINT [6:0]	Port F Interrupt	I
PG-EINT [15:0]	Port G Interrupt	I
PJ-EINT [15:0]	Port J Interrupt	I

Signal Name[1]	Description[2]	Type[3]
PK-EINT [11:0]	Port K Interrupt	I
IRQ-EINT[4,2:0]	GPIO0-2,GPIO4 Interrupt	I

4.3.35 Power

Table 4-108 Power Signal Description

Signal Name[1]	Description[2]	Type[3]
VDD-CPU	Arm® Cortex®-A7 Power Supply	P
VDD-CPUFB	Arm® Cortex®-A7 Power Supply Feedback	P
VDD-SYS	System Power Supply	P
VCC-PA	Digital Port A Power Supply	P
VCC-PC	Digital Port C Power Supply	P
VCC-PD	Digital Port D Power Supply (for other devices)	P
VCC-PA-PD	Digital Port A&D Power Supply (only for T153L3-QXX)	P
VCC-PE	Digital Port E Power Supply	P
VCC18-PF	Digital Port F 1.8V Power Supply	P
VCC-PG	Digital Port G Power Supply	P
VCC-PJ	Digital Port J Power Supply	P
VCC-PK	Digital Port K Power Supply (for other devices)	P
VCC-PA-PK	Digital Port A&K Power Supply (only for T153Mx-QCX)	P
VCC-IO	GPIO/FEL Power Supply	P
VCC18-ADC	GPADC and TPADC Power Supply	P
VCC18-EFUSE	eFuse Power Supply	P
VCC18-LDOA-MCSI	LDOA Output & MIPI CSI Power Supply	P
LDOA-IN	Internal LDOA Input Voltage	P

5 Electrical characteristics

5.1 Parameter Conditions

5.1.1 Minimum and Maximum Values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage, and frequencies by tests in production on 100% of the devices with ambient temperature at Ta = 25 °C and Ta = Ta max.

Data based on characterization results, design simulation, and/or technology characteristics are indicated in the table footnotes and are not tested in production.

5.1.2 Typical Values

Unless otherwise specified, the typical data are based on Ta = 25 °C. They are given only as design guidelines.

5.1.3 Temperature Definitions

- Ambient Temperature— the temperature of the surrounding environment.
- Junction Temperature— the hottest temperature of the silicon chip inside the package.
- Absolute Maximum Junction Temperature— the temperature beyond which damage occurs to the device. The device may not function or meet expected performance at this temperature.
- Recommended Operating Temperature— the junction temperature at which the device operates continuously at the designated performance over the designed lifetime. The reliability of the device may be degraded if the device operates above this temperature. Some devices will not function electrically above this temperature.

5.2 Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which damage to the device may occur. The following table specifies the absolute maximum ratings.

CAUTION

Stresses beyond those listed under Table 5-1 may affect reliability or cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under section 5.3 Recommended Operating Conditions is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

Table 5-1 Absolute Maximum Ratings

Supply Name	Description	Min(1)	Max(1)	Unit
VDD-CPU	Arm® Cortex®-A7 Power Supply	-0.3	1.2	V
VDD-SYS	System Power Supply	-0.3	1.05	V
AVCC	Power Supply for Analog Part	-0.3	2.16	V
VCC-RTC	RTC Power Supply	-0.3	2.16	V
VCC-DRAM	DRAM IO Power Supply	-0.3	VDDQ+0.3	V
VDD18-DRAM	SDRAM Controller Power Supply	-0.3	2.16	V
VCC18-LDOA-MCSI	LDOA Output & MIPI CSI Power Supply	-0.3	2.16	V
VCC18-LVDS	LVDS Power Supply	-0.3	2.16	V
VCC-IO	GPIO/FEL Power Supply	-0.3	3.96	V
VCC-PC	Digital Port C Power Supply	-0.3	3.96	V
VCC-PG	Digital Port G Power Supply	-0.3	3.96	V
V_{ESD}(2)	Human Body Model (HBM)(3)	±2000		V
	Charged Device Model (CDM)(4)	±250		V
$I_{Latch-up}$	Latch-up I-test performance current-pulse injection on each IO pin(5)	PASS		
	Latch-up over-voltage performance voltage injection on each IO pin(6)	PASS		
T153MX-BCX only				
VCC18-ADC	GPADC and TPADC Power Supply	-0.3	2.16	V
VCC18-EFUSE	eFuse Power Supply	-0.3	2.16	V
VCC-PA	Digital Port A Power Supply	-0.3	3.96	V
VCC-PD	Digital Port D Power Supply	-0.3	3.96	V
VCC-PE	Digital Port E Power Supply	-0.3	3.96	V
VCC-PJ	Digital Port J Power Supply	-0.3	3.96	V
VCC-PK	Digital Port K Power Supply	-0.3	3.96	V
VCC18-PF	Digital Port F 1.8V Power Supply	-0.3	2.16	V
VCC33-USB0-USB1	USB2.0 DRD and USB 2.0 Host 3.3V Power Supply	-0.3	3.63	V

Supply Name	Description	Min(1)	Max(1)	Unit
LDOA-IN	Internal LDOA Input Voltage	-0.3	3.63	V
T153Mx-QCX only				
VCC33-USB-LDOAIN	USB2.0 DRD and USB 2.0 Host /LDOA Input Power Supply	-0.3	3.63	V
VCC-PA-PK	Digital Port A&K Power Supply	-0.3	3.96	V
VCC-PD	Digital Port D Power Supply	-0.3	3.96	V
T153L3-QCX only				
VCC33-USB-LDOAIN	USB2.0 DRD and USB 2.0 Host /LDOA Input Power Supply	-0.3	3.63	V
VCC-PA-PD	Digital Port A&D Power Supply	-0.3	3.96	V
VCC-PK	Digital Port K Power Supply	-0.3	3.96	V

(1) The min/max voltages of power rails are guaranteed by design, not tested in production.

(2) Electrostatic discharge (ESD) to measure device sensitivity/immunity to damage caused by electrostatic discharges into the devices.

(3) Level listed above is the passing level per ESDA/JEDEC JS-001-2023.

(4) Level listed above is the passing level per ESDA/JEDEC JS-002-2022.

(5) Based on JESD78F, each device is tested with IO pin injection of ±200 mA at room temperature.

(6) Based on JESD78F, each device is tested with a stress voltage of 1.5 x Vddmax at room temperature.

5.3 Recommended Operating Conditions

The following table describes operating conditions of the device.

NOTE

Logic functions and parameter values are not assured out of the range specified in the recommended operating conditions.

Table 5-2 Recommended Operating Conditions

Supply Name	Description	Min	Typ	Max	Unit
VDD-CPU	Arm® Cortex®-A7 Power Supply	0.9	-	1.15	V
VDD-SYS	System Power Supply	0.9	-	1.00	V

Supply Name	Description	Min	Typ	Max	Unit
AVCC	Power Supply for Analog Part	1.782	1.8	1.818	V
VCC-RTC	RTC Power Supply	1.62	1.8	1.98	V
VCC-DRAM	DDR3 Power Supply	1.425	1.5	1.575	V
	DDR3L Power Supply	1.283	1.35	1.417	V
	DDR4 Power Supply	1.14	1.2	1.26	V
VDD18-DRAM	SDRAM Controller Power Supply	1.71	1.8	1.89	V
VCC18-LDOA-MCSI	LDOA Output & MIPI CSI Power Supply	1.71	1.8	1.89	V
VCC18-LVDS	LVDS Power Supply	1.71	1.8	1.89	V
VCC-IO	GPIO/FEL Power Supply	2.97	3.3	3.63	V
VCC-PC	Digital Port C Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PG	Digital Port G Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
T153MX-BCX only					
VCC18-ADC	GPADC and TPADC Power Supply	1.782	1.8	1.818	V
VCC18-EFUSE	eFuse Power Supply	1.71	1.8	1.98	V
VCC-PA	Digital Port A Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PD	Digital Port D Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PE	Digital Port E Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PJ	Digital Port J Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PK	Digital Port K Power	1.62	1.8	1.98	V

Supply Name	Description	Min	Typ	Max	Unit
	1.8 V Voltage 3.3 V Voltage	2.97	3.3	3.63	
VCC18-PF	Digital Port F Power Supply 1.8 V Voltage	1.62	1.8	1.98	V
VCC33-USB0-USB1	USB2.0 DRD and USB 2.0 Host 3.3V Power Supply	2.97	3.3	3.63	V
LDOA-IN	Internal LDOA Input Voltage	2.97	3.3	3.63	V
T153Mx-QCX only					
VCC33-USB-LDOAIN	USB2.0 DRD and USB 2.0 Host /LDOA Input Power Supply	2.97	3.3	3.63	V
VCC-PA-PK	Digital Port A&K Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PD	Digital Port D Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
T153L3-QCX only					
VCC33-USB-LDOAIN	USB2.0 DRD and USB 2.0 Host /LDOA Input Power Supply	2.97	3.3	3.63	V
VCC-PA-PD	Digital Port A&D Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V
VCC-PK	Digital Port K Power 1.8 V Voltage 3.3 V Voltage	1.62 2.97	1.8 3.3	1.98 3.63	V

5.4 GPIO DC Electrical Characteristics

Table 5-3 summarizes the GPIO DC electrical characteristics of the device.

Table 5-3 GPIO DC Electrical Characteristics(1)

(VCC: VCC-PA/VCC-IO/VCC-PC/VCC-PD/VCC-PE/VCC18-PF/VCC-PG/VCC-PJ/VCC-PK/VCC-PA-PK/VCC-PA-PD)

Symbol	Parameter		Min	Typ	Max	Unit
V_{IH}	High-level Input Voltage		0.7 * VCC	-	1.1 * VCC	V
V_{IL}	Low-level Input Voltage		-0.3	-	0.3 * VCC	V
R_{PU}(2)	Output Pull-up Resistance	PC1, PC2, PC3, PC4, PC5, PC6, PC7, PC8, PC9, PC10, PC11, PF3, PF6	9	15	21	kΩ
		PG1, PG2, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
R_{PD}(2)	Output Pull-down Resistance	PC1, PC2, PC3, PC4, PC5, PC6, PC7, PC8, PC9, PC10, PC11, PF3, PF6	9	15	21	kΩ
		PG1, PG2, PG3, PG4, PG5	19.8	33	46.2	kΩ
		Other GPIOs	60	100	140	kΩ
I_{IH}	High-level Input Current		-	-	10	uA
I_{IL}	Low-level Input Current		-	-	10	uA
V_{OH}	High-level Output Voltage		VCC – 0.3	-	VCC	V
V_{OL}	Low-level Output Voltage		0	-	0.2	V
I_{OZ}	Tri-State Output Leakage Current		-10	-	10	uA
VT+	Schmitt Trigger Low to High Threshold Point	GPIO@3.3V	1.6	2	2.4	V
		GPIO@1.8V	0.88	1.1	1.32	V
VT-		GPIO@3.3V	0.96	1.2	1.44	V

Symbol	Parameter		Min	Typ	Max	Unit
	Schmitt Trigger High to Low Threshold Point	GPIO@1.8V	0.6	0.75	0.9	V
C_{IN}	Input Capacitance		-	-	5	pF
C_{OUT}	Output Capacitance		-	-	5	pF

(1) Guaranteed by design.

(2) Not applicable to GPIO0-2 and GPIO4.

5.5 SMHC Electrical Characteristics

The SMHC electrical parameters are related to different supply voltage.

Figure 5-1 SMHC Voltage Waveform

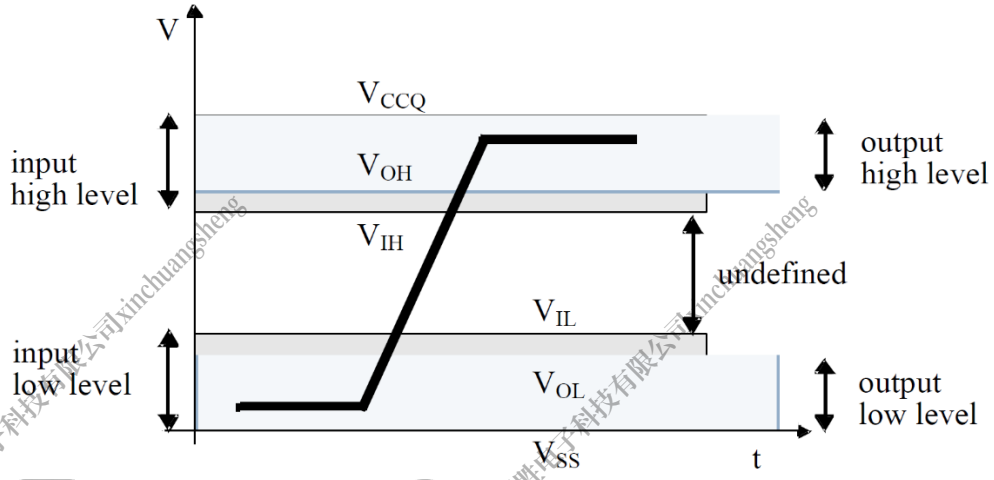


Table 5-4 shows 3.3 V SMHC electrical parameters.

Table 5-4 3.3 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	2.7		3.6	V
V_{OH}	Output high-level voltage	0.75 * V_{CCQ}	-	-	V
V_{OL}	Output low-level voltage	-	-	0.125 * V_{CCQ}	V
V_{IH}	Input high-level voltage	0.625 * V_{CCQ}	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.25 * V_{CCQ}	V

Table 5-5 shows 1.8 V SMHC electrical parameters.

Table 5-5 1.8 V SMHC Electrical Parameters

Symbol	Parameter	Min	Typ	Max	Unit
VDD	Power voltage	2.7	-	3.6	V
V_{CCQ}	I/O voltage	1.7		1.95	V
V_{OH}	Output high-level voltage	V_{CCQ} – 0.45	-	-	V
V_{OL}	Output low-level voltage	-	-	0.45	V
V_{IH}	Input high-level voltage	0.65 * V_{CCQ} (1)	-	V_{CCQ} + 0.3	V
V_{IL}	Input low-level voltage	V_{SS} – 0.3	-	0.35 * V_{CCQ} (2)	V
(1).0.7 * V_{CCQ} for MMC4.3 or lower. (2).0.3 * V_{CCQ} for MMC4.3 or lower.					

5.6 GPADC Electrical Characteristics

Table 5-6 lists the GPADC electrical characteristics.

Table 5-6 GPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	VCC18-ADC	V
Sampling Rate	-	-	2	MHz

5.7 TPADC Electrical Characteristics

Table 5-7 lists the TPADC electrical characteristics.

Table 5-7 TPADC Electrical Characteristics

Parameter	Min	Typ	Max	Unit
ADC Resolution	-	12	-	bits
Full-scale Input Range	0	-	VCC18-ADC	V
Sampling Rate	-	-	750	kHz

5.8 Audio Codec Electrical Characteristics

Test Conditions

VDD-SYS = 0.9 V, AVCC = 1.8 V, Ta = 25 °C, 1 kHz sinusoid signal, DAC fs = 48 kHz.

Table 5-8 Audio Codec Typical Performance Parameters

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
DAC Path	DAC to LINEOUTLP/N (R=100K)					
	Full-scale	0 dBFS 1 kHz	-	1.075	-	Vrms
	SNR (A-weighted)	0data	-	99	-	dB
	THD+N	0 dBFS 1 kHz	-	-83	-	dB

5.9 External Clock Source Electrical Characteristics

5.9.1 High-speed Crystal/Ceramic Resonator Characteristics

The high-speed external clock can be supplied with a 24 MHz crystal resonator (oscillation mode). The 24 MHz crystal resonator provides 24 MHz reference clock which is connected to the DXIN and DXOUT terminals.

Table 5-9 High-speed 24 MHz Crystal Requirements

Symbol	Parameter	Min	Typ	Max	Unit
f_{X24M_IN}	Crystal parallel resonance frequency	-	24	-	MHz
	Crystal frequency stability and tolerance at 25 °C (1)	-50	-	+50	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	6.5	-	pF

1. The 50 ppm frequency stability and tolerance can meet the requirement of the device. We recommend selecting 20 ppm crystal devices. If the REFCLK-OUT (24 MHz fanout) is used for Wi-Fi chip, the crystal uses the recommended specification or the specified model for Wi-Fi chip.
2. The 6.5 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

Table 5-10 Crystal Circuit Parameters

Symbol	Parameter
C_1	C_1 capacitance
C_2	C_2 capacitance
C_L	Equivalent load capacitance, specified by the crystal manufacturer
C_0	Crystal shunt capacitance, specified by the crystal manufacturer

Symbol	Parameter
C_{shunt}	Total shunt capacitance

Frequency stability mainly requires that the total load capacitance (C_L) be constant. The crystal manufacturer typically specifies a total load capacitance which is the series combination of C_1, C_2, and C_{shunt}.

The total load capacitance is $C_L = [(C_1 * C_2)/ (C_1 + C_2)] + C_{shunt}$.

- C_1 and C_2 represent the total capacitance of the respective PCB trace, load capacitor, and other components (excluding the crystal) connected to each crystal terminal. C_1 and C_2 are usually the same size.
- C_{shunt} is the crystal shunt capacitance (C_0) plus any mutual capacitance ($C_{pkg} + C_{PCB}$) seen across the DXIN and DXOUT signals.

In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins in order to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

5.9.2 Low-speed Crystal/Ceramic Resonator Characteristics

This device contains an RC oscillation circuit that generates a 32.768 kHz clock, meanwhile, the DCXO module can calibrate the RC oscillation circuit regularly. If the product does not have a high requirement for the accuracy of the system clock, the external 32.768 kHz crystal circuit can be omitted and the internal RC oscillation circuit can be adopted, meanwhile, the relevant clock configuration needs to be turned on by the software.

This device also can connect to a 32.768 kHz crystal resonator (oscillation mode). The 32.768 kHz crystal resonator provides 32.768 kHz reference clock which is connected to the X32KIN and X32KOUT terminals. In the application, the crystal resonator and the load capacitors must be placed close to the oscillator pins to minimize output distortion and the startup stabilization time. Refer to the crystal resonator manufacturer for more details on the resonator characteristics.

Table 5-11 Low-speed 32.768 kHz Crystal Circuit Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{X32K_IN}	Crystal parallel resonance frequency	-	32.768	-	kHz
	Crystal frequency stability and tolerance at 25 °C (1)	-	-	-	ppm
	Oscillation mode	Fundamental			-
C_0	Shunt capacitance (2)	-	1.35	-	pF

(1) This device has no requirement for the frequency stability and tolerance of 32.768 kHz crystal. If the actual product has requirement for the accuracy of timing function, the 20 ppm stability and tolerance is recommended.

(2) The 1.35 pF is only a simulation value. The crystal shunt capacitance (C_0) is given by the crystal manufacturer.

5.10 Interface Timing Characteristics

5.10.1 SMHC Interface Timing

5.10.1.1 HS-SDR Mode

NOTE

IO voltage is 1.8V or 3.3V.

Figure 5-2 SMHC HS-SDR Mode Output Timing Diagram

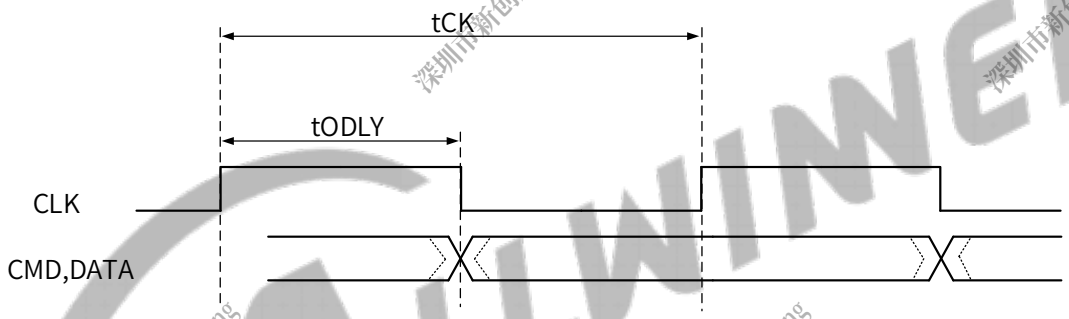


Table 5-12 SMHC HS-SDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					
CMD, Data output delay time	tODLY	-	0.25	0.5	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-3 SMHC HS-SDR Mode Input Timing Diagram

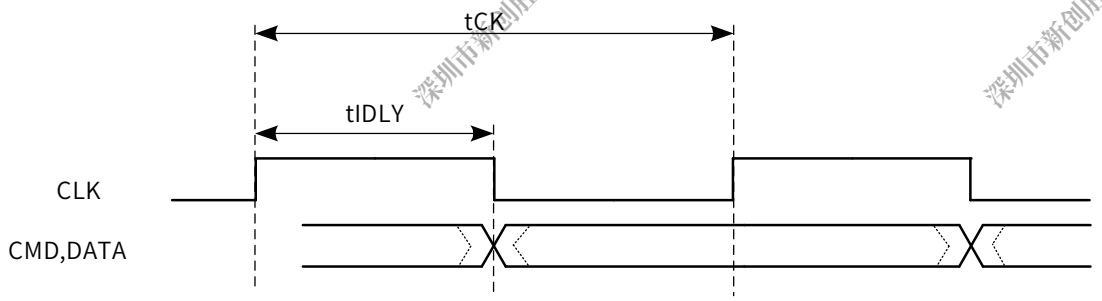


Table 5-13 SMHC HS-SDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in SDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY	-	-	20	ns
The driver strength level of GPIO is 2 for test.					

5.10.1.2 HS-DDR Mode

Figure 5-4 SMHC HS-DDR Mode Output Timing Diagram

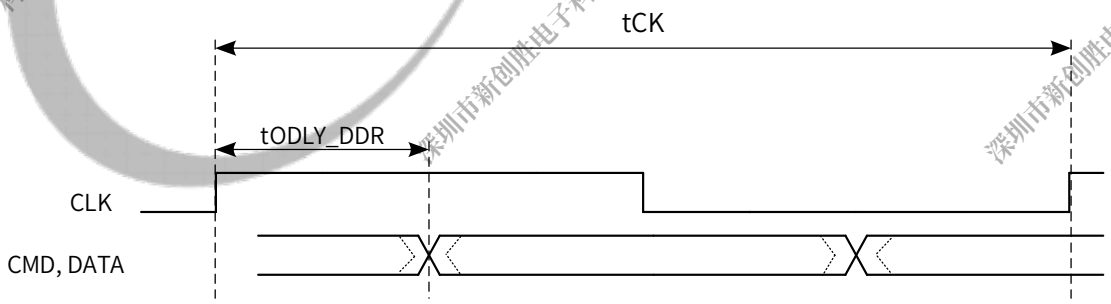


Table 5-14 SMHC HS-DDR Mode Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Output CMD, DATA(referenced to CLK)					

Parameter	Symbol	Min	Typ	Max	Unit
CMD, Data output delay time in DDR mode	tODLY-DDR	-	0.25	0.25	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=20 ns at 50 MHz. (2) The driver strength level of GPIO is 2 for test.					

Figure 5-5 SMHC HS-DDR Mode Input Timing Diagram

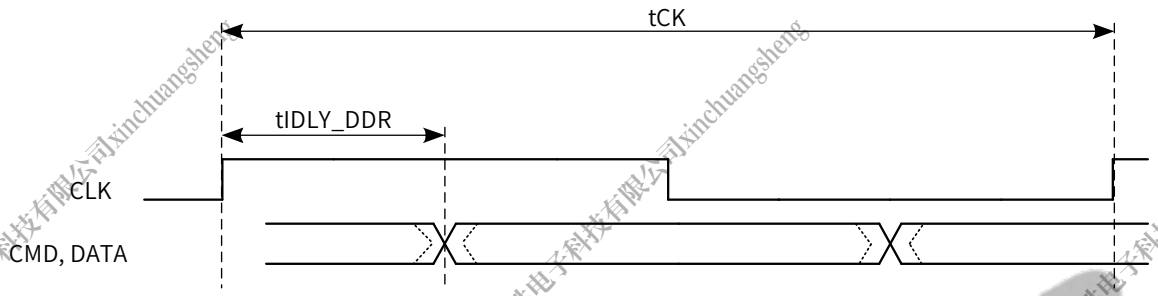


Table 5-15 SMHC HS-DDR Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	0	50	50	MHz
Duty Cycle	DC	45	50	55	%
Input CMD, DATA(referenced to CLK 50MHz)					
Data input delay in DDR mode. It includes the PCB delay time of Clock, the PCB delay time of Data and the data output delay of Device	tIDLY-DDR	-	-	8.3	ns
The driver strength level of GPIO is 2 for test.					

5.10.1.3 HS200/SDR104 Mode

Figure 5-6 SMHC HS200/SDR104 Mode Host Output Timing and Device Input Timing Diagram

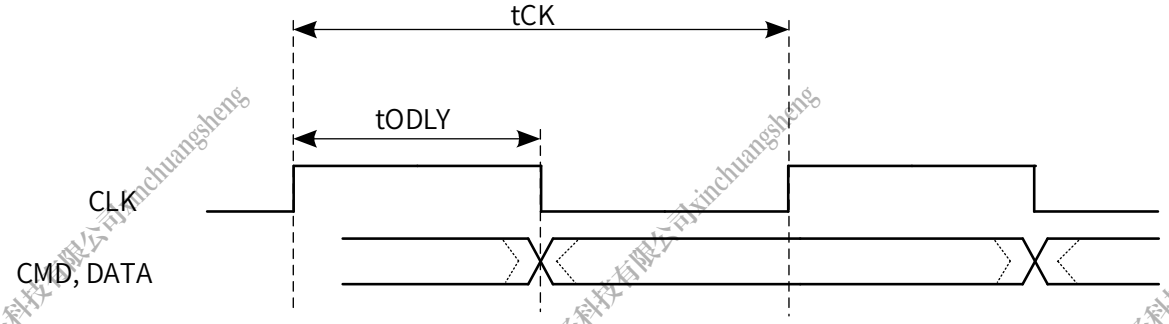


Table 5-16 SMHC HS200/SDR104 Mode Host Output Timing and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CLK					
Clock frequency	tCK	-	-	200	MHz
Duty Cycle	DC	45	50	55	%
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI
Host Output CMD, DATA (referenced to CLK)					
Host CMD, Data output delay time	tODLY	-	0.25	0.5	UI
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.					

Figure 5-7 SMHC HS200/SDR104 Mode Host Input Timing and Device Output Timing Diagram

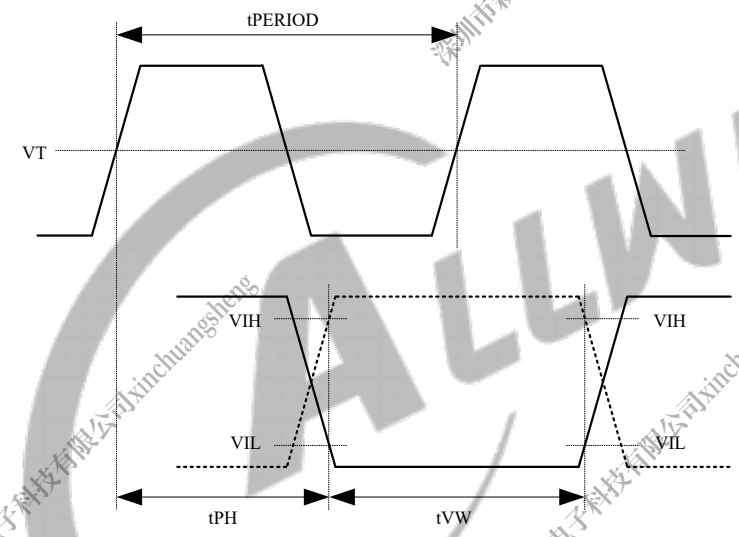


Table 5-17 SMHC HS200/SDR104 Mode Host Input Timing and Device Output Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock Period	tPERIOD	5	-	-	ns	Max: 200 MHz
Duty Cycle	DC	45	50	55	%	
Rise time, fall time	tTLH, tTHL	-	-	0.2	UI	
Host Input CMD, DATA (referenced to CLK)						
Device Output delay	tPH	0	-	2	UI	

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Device Output delay variation due to temperature change after tuning	dPH	-350(3)	-	1550(4)	ps	
Device CMD, Data valid window	tVW	0.575	-	-	UI	

(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz.

(2) The driver strength level of GPIO is 3 for test.

(3) Temperature variation: -20 °C.

(4) Temperature variation: 90 °C.

5.10.1.4 HS400 Mode

The CMD output timing for HS400 mode is the same as CMD output timing for HS200 mode.

Figure 5-8 SMHC HS400 Mode Host Output Timing and Device Input Timing Diagram

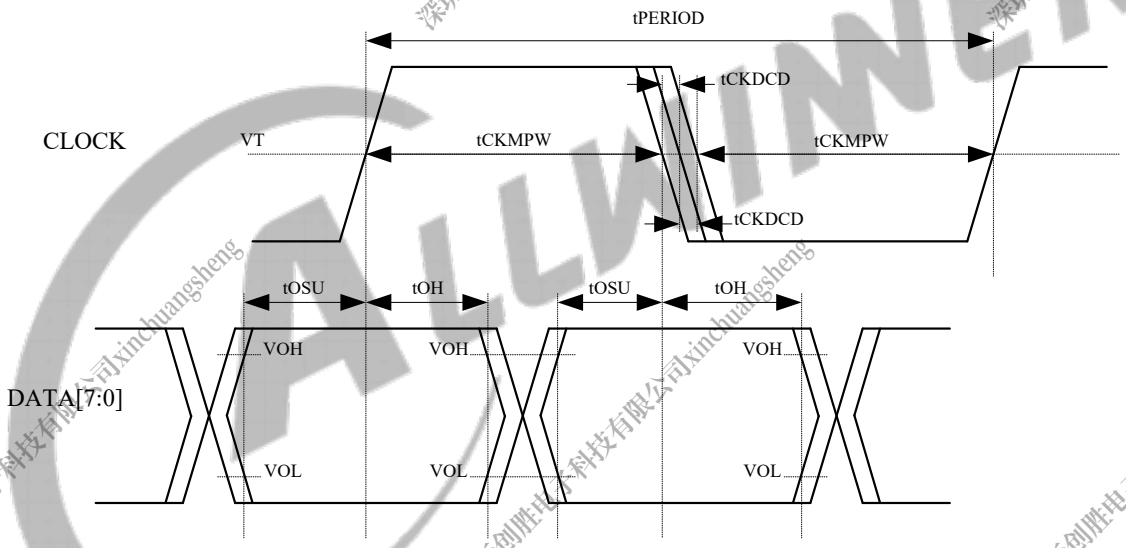


Table 5-18 SMHC HS400 Mode Host Output Timing and Device Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
CLK						
Clock period	tPERIOD	6.67	-	-	ns	Max: 150 MHz
Clock slew rate	SR	1.125	-	-	V/ns	
Clock duty cycle distortion	tCKDCD	0	-	0.5	ns	
Clock minimum pulse width	tCKMPW	2.2	-	-	ns	
Output DATA (referenced to CLK)						

Parameter	Symbol	Min	Typ	Max	Unit	Remark
Data output setup time	tOSU	0.4	-	-	ns	
Data output hold time	tOH	0.4	-	-	ns	
Data output slew rate	SR	0.9	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

Figure 5-9 SMHC HS400 Mode Host Input Timing and Device Output Timing Diagram

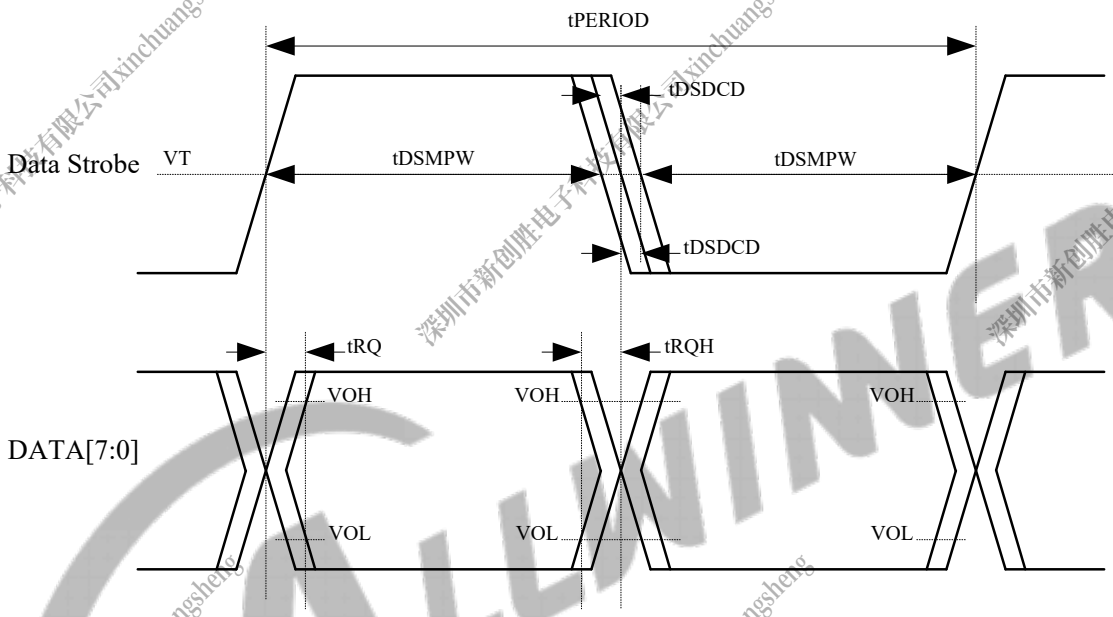


Table 5-19 SMHC HS400 Mode Input Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit	Remark
DS (Data Strobe)						
DS period	tPERIOD	6.67	-	-	ns	Max: 150MHz
DS slew rate	SR	1.125	-	-	V/ns	
DS duty cycle distortion	tDSDCD	0.0	-	0.4	ns	
DS minimum pulse width	tDSMPW	2.0	-	-	ns	
Input DATA (referenced to DS)						
Data input skew	tRQ	-	-	0.4	ns	
Data input hold skew	tRQH	-	-	0.4	ns	
Data input slew rate	SR	0.85	-	-	V/ns	
(1) The Unit Interval (UI) is 1-bit nominal time. For example, UI=10 ns at 100 MHz. (2) The driver strength level of GPIO is 3 for test.						

5.10.2 LCD Interface Timing

Figure 5-10 HV_IF Vertical Timing

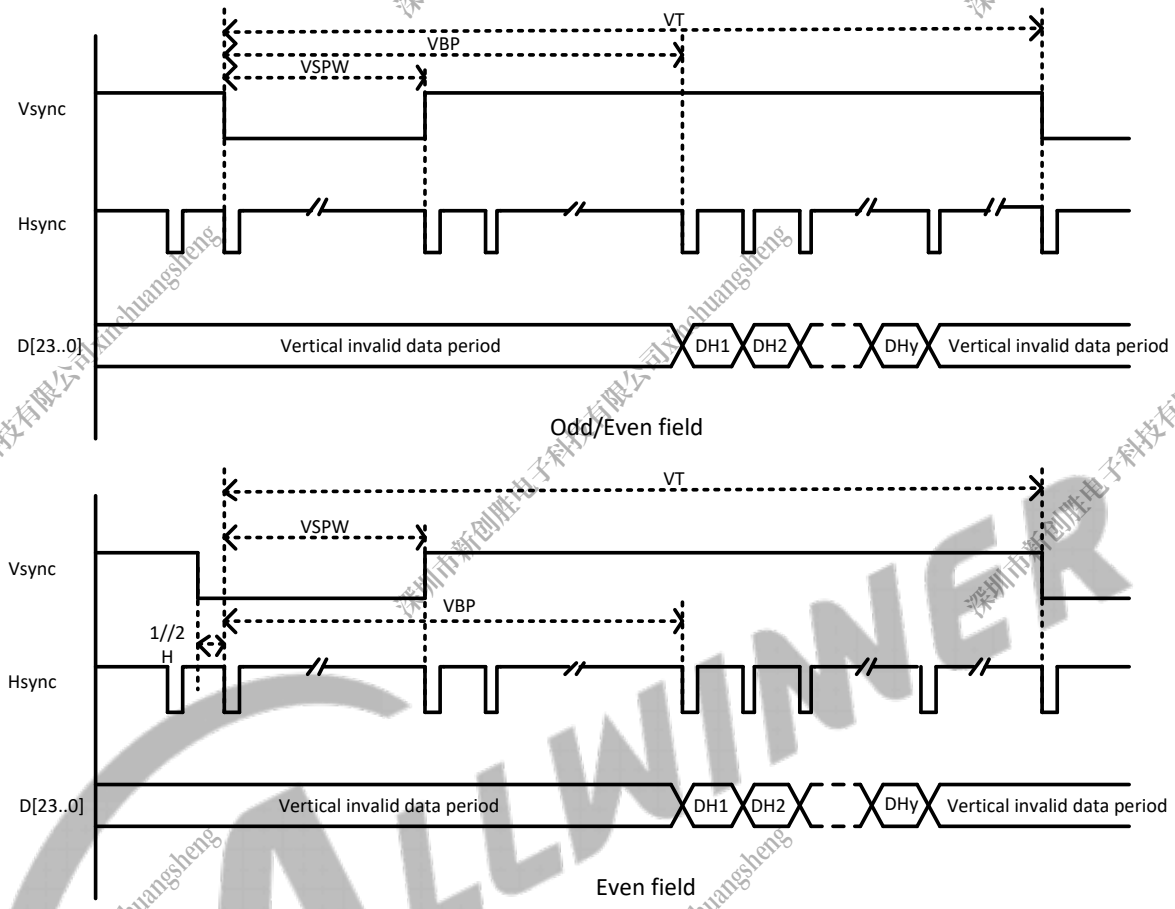
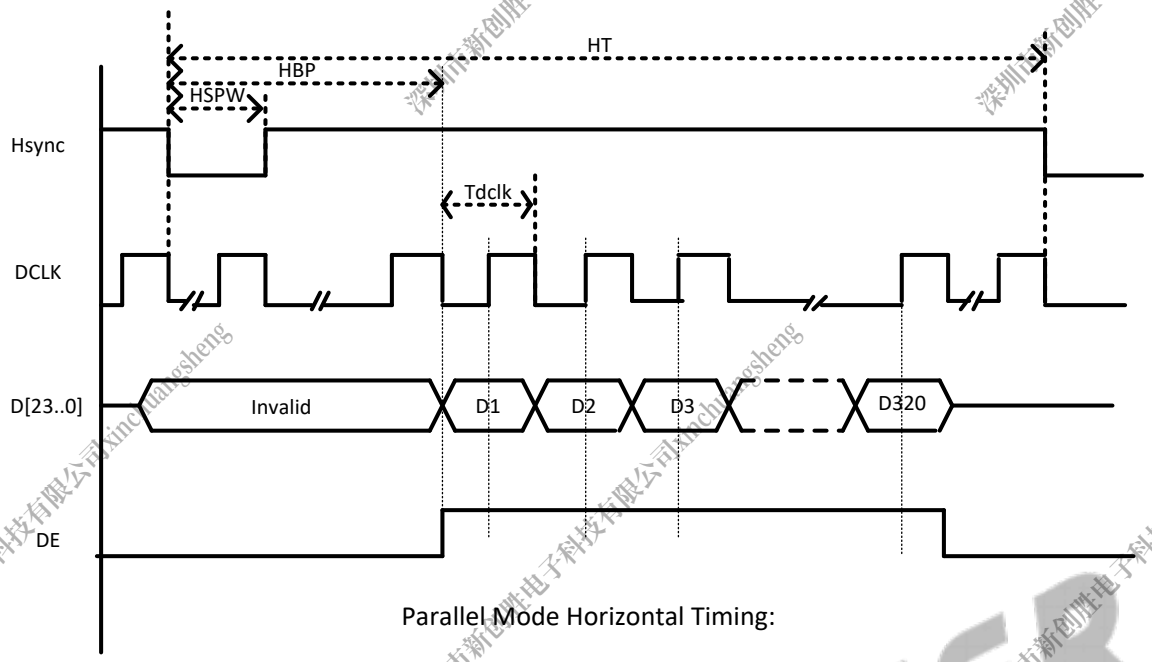
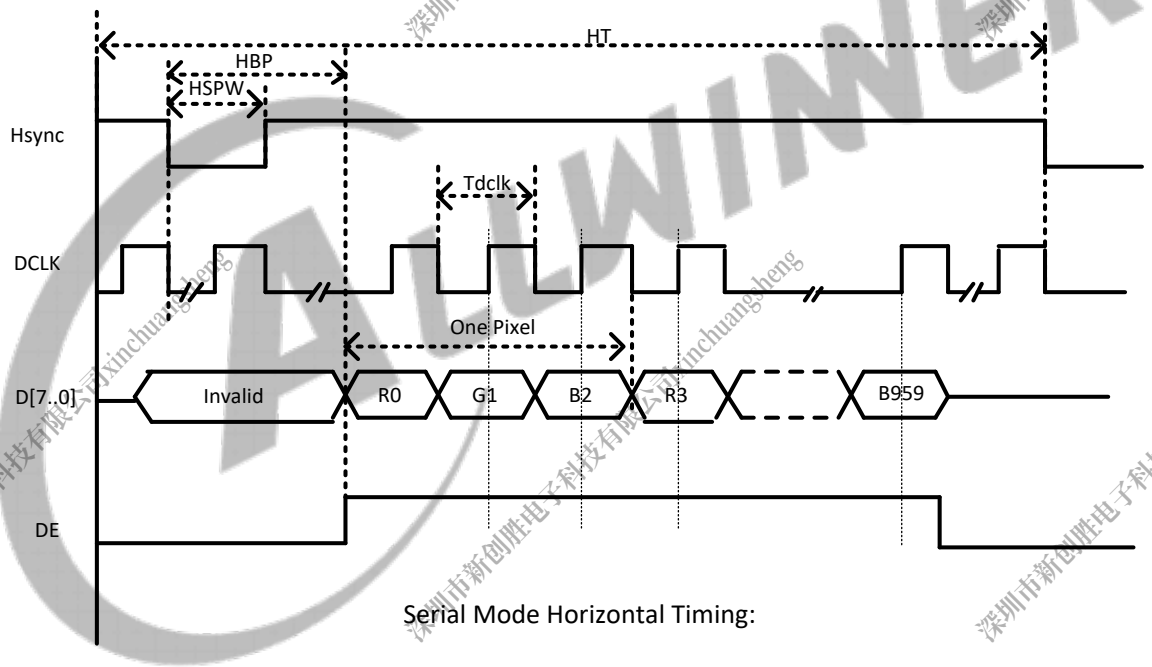


Figure 5-11 HV_IF Horizontal Timing



Parallel Mode Horizontal Timing:



Serial Mode Horizontal Timing:

Table 5-20 LCD HV_IF Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DCLK Cycle Time	tDCLK	5.9	-	-	ns
Hsync Period Time	tHT	-	HT+1	-	tDCLK
Hsync Width	tHSPW	-	HSPW+1	-	tDCLK
Hsync Back Porch	tHBP	-	HBP+1	-	tDCLK
Vsync Period Time	tVT	-	VT/2	-	tHT
Vsync Width	tVSPW	-	VSPW+1	-	tHT

Parameter	Symbol	Min	Typ	Max	Unit
Vsync Back Porch	tVBP	-	VBP+1	-	tHT

(1) Vsync: Vertical sync, indicates one new frame.
(2) Hsync: Horizontal sync, indicate one new scan line.
(3) DCLK: Dot clock, pixel data are sync by this clock.
(4) LDE: LCD data enable.
(5) LD[23..0]: 24Bit RGB/YUV output from input FIFO for panel.

5.10.3 Parallel CSI Interface Timing

Figure 5-12 Parallel CSI Data Sample Timing

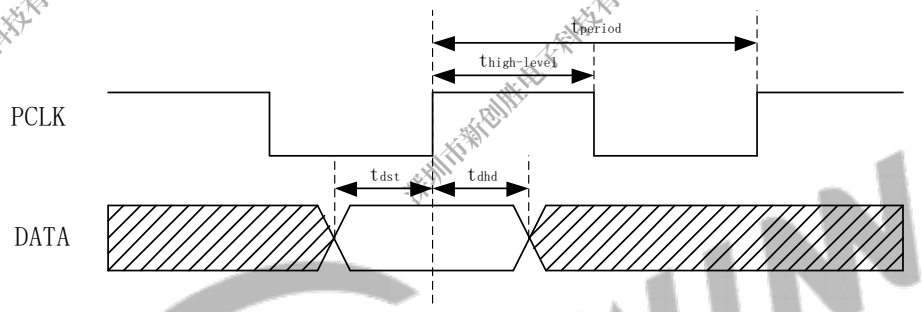


Table 5-21 Parallel CSI Interface Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
Pclk period	t_{period}	6.73	-	-	ns
Pclk frequency	$1/t_{period}$	-	-	148.5	MHz
Pclk duty	$t_{high-level}/t_{period}$	40	50	60	%
Data input setup time	t_{dst}	0.6	-	-	ns
Data input hold time	t_{dhd}	0.6	-	-	ns

5.10.4 MIPI CSI Interface Timing

Figure 5-13 MIPI CSI Interface Timing

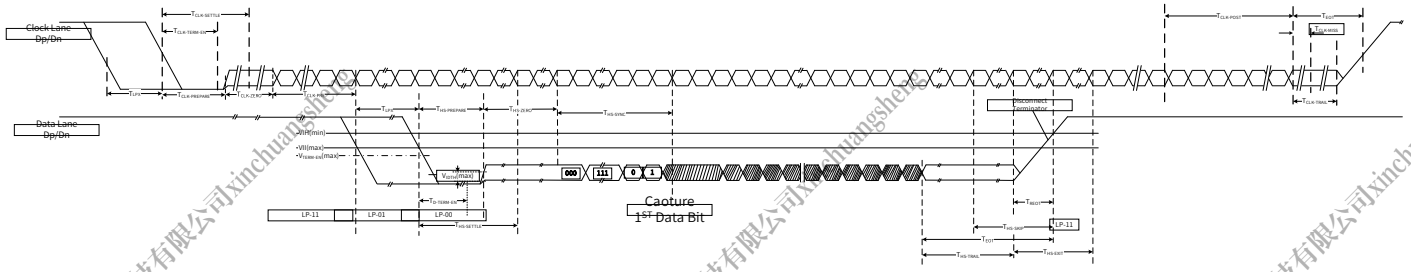


Table 5-22 MIPI CSI Interface Timing Constants

Parameter	Description	Min	Typ	Max	Unit	Notes
$T_{CLK-MISS}$	Timeout for receiver to detect absence of Clock transitions and disable the Clock Lane HS-RX.			60	ns	(1), (6)
$T_{CLK-POST}$	Time that the transmitter continues to send HS clock after the last associated Data Lane has transitioned to LP Mode. Interval is defined as the period from the end of THS-TRAIL to the beginning of $T_{CLK-TRAIL}$.	60ns + 52*UI			ns	(5)
$T_{CLK-PRE}$	Time that the HS clock shall be driven by the transmitter prior to any associated Data Lane beginning the transition from LP to HS mode.	8			UI	(5)
$T_{CLK-PREPARE}$	Time that the transmitter drives the Clock Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission.	38		95	ns	(5)
$T_{CLK-SETTLE}$	Time interval during which the HS receiver should ignore any Clock Lane HS transitions, starting from the beginning of TCLK-PREPARE.	95		300	ns	(6), (7)
$T_{CLK-TERM-EN}$	Time for the Clock Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		38	ns	(6)
$T_{CLK-TRAIL}$	Time that the transmitter drives the HS-0 state after the last payload clock bit of a HS transmission burst.	60			ns	(5)
$T_{CLK-PREPARE}$ + $T_{CLK-ZERO}$	TCLK-PREPARE + time that the transmitter drives the HS-0 state prior to starting the Clock.	300			ns	(5)
$T_{D-TERM-EN}$	Time for the Data Lane receiver to enable the HS line termination, starting from the time point when Dn crosses $V_{IL,MAX}$.	Time for Dn to reach $V_{TERM-EN}$		35ns + 4*UI		(6)

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{EOT}	Transmitted time interval from the start of $T_{HS-TRAIL}$ or $T_{CLK-TRAIL}$, to the start of the LP-11 state following a HS burst.			105ns + n*12*UI		(3), (5)
$T_{HS-EXIT}$	Time that the transmitter drives LP-11 following a HS burst.	100			ns	(5)
$T_{HS-PREPARE}$	Time that the transmitter drives the Data Lane LP-00 Line state immediately before the HS-0 Line state starting the HS transmission	40ns + 4*UI		85ns + 6*UI	ns	(5)
$T_{HS-PREPARE}$ + $T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time that the transmitter drives the HS-0 state prior to transmitting the Sync sequence.	145ns + 10*UI			ns	(5)
$T_{HS-SETTLE}$	Time interval during which the HS receiver shall ignore any Data Lane HS transitions, starting from the beginning of $T_{HS-PREPARE}$. The HS receiver shall ignore any Data Lane transitions before the minimum value, and the HS receiver shall respond to any Data Lane transitions after the maximum value.	85ns + 6*UI		145ns + 10*UI	ns	(6)
$T_{HS-SKIP}$	Time interval during which the HS-RX should ignore any transitions on the Data Lane, following a HS burst. The end point of the interval is defined as the beginning of the LP-11 state following the HS burst.	40			ns	(6)
$T_{HS-TRAIL}$	Time that the transmitter drives the flipped differential state after last payload data bit of a HS transmission burst	max(n*8*UI, 60ns + n*4*UI)			ns	(2), (3), (5)
T_{INIT}		100			ns	(5)
T_{LPX}	Transmitted length of any Low-Power state period	50			ns	(4), (5)
Ratio T_{LPX}	Ratio of $T_{LPX(MASTER)}/T_{LPX(SLAVE)}$ between Master and Slave side	2/3		3/2	ns	

Parameter	Description	Min	Typ	Max	Unit	Notes
T_{TA-GET}	Time that the new transmitter drives the Bridge state (LP-00) after accepting control during a Link Turnaround.	$5*T_{LPX}$			ns	(5)
T_{TA-GO}	Time that the transmitter drives the Bridge state (LP-00) before releasing control during a Link Turnaround.	$4*T_{LPX}$			ns	(5)
$T_{TA-SURE}$	Time that the new transmitter waits after the LP-10 state before transmitting the Bridge state (LP-00) during a Link Turnaround.	T_{LPX}		$2*T_{LPX}$	ns	(5)
T_{WAKEUP}	Time that a transmitter drives a Mark-1 state prior to a Stop state in order to initiate an exit from ULPS.	1			ms	(5)

NOTE

(1) The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

(2) If a > b then max (a, b) = a otherwise max (a, b) = b.

(3) Where n = 1 for Forward-direction HS mode and n = 4 for Reverse-direction HS mode.

(4) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

(5) Transmitter-specific parameter.

(6) Receiver-specific parameter.

(7) The stated values are considered informative guidelines rather than normative requirements since this parameter is untestable in typical applications.

5.10.5 MIPI DPHY Interface Timing

Figure 5-14 MIPI DPHY Timing

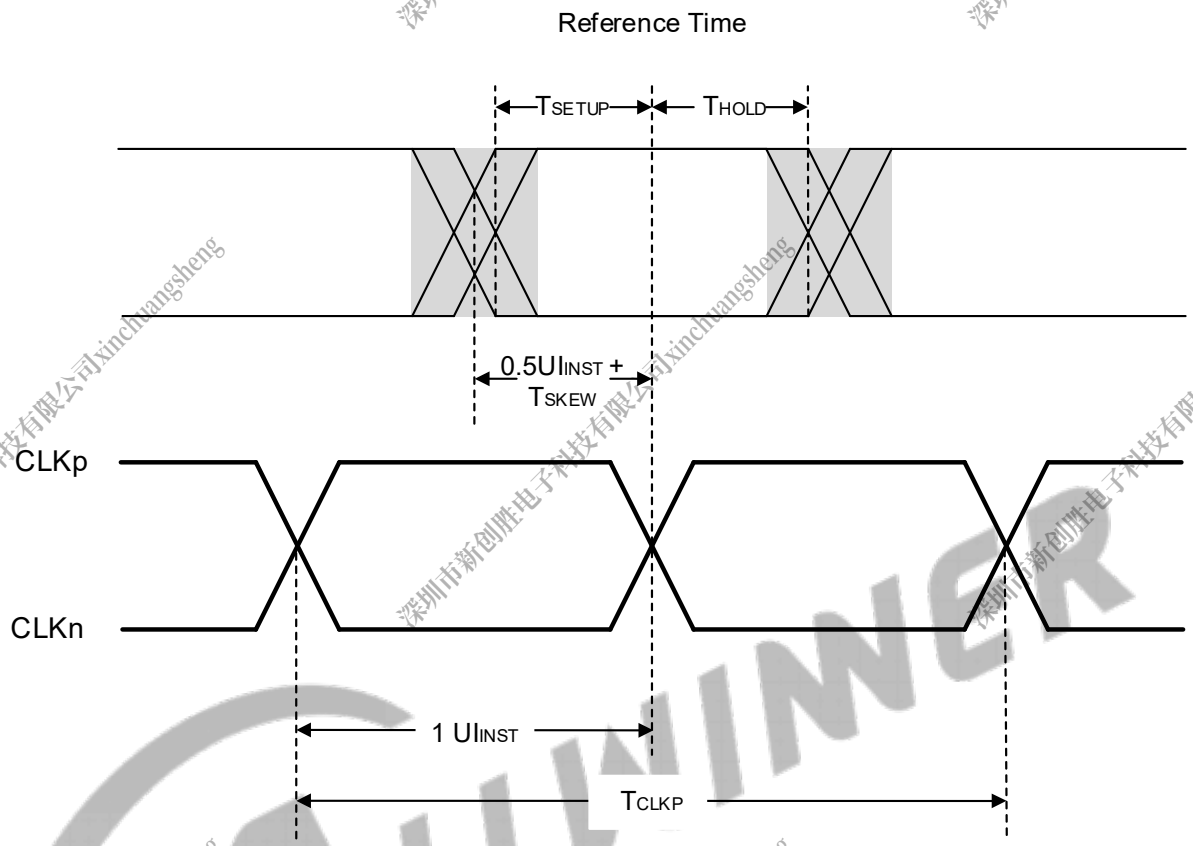


Table 5-23 MIPI DPHY Timing Constants

Parameter	Symbol	Units in Ulinst			Operational Frequency in Gbps	
		Min	Max	Total	Min	Max
Data to Clock Skew	$T_{skew[tx]}$	-0.15	0.15	0.3	0.08	1.0
		-0.20	0.20	0.4	>1.0	1.5
Data to Clock Setup Time	$T_{setup[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5
Clock to Data Hold Time	$T_{hold[rx]}$	0.15	-	-	0.08	1.0
		0.20			>1.0	1.5

5.10.6 GMAC Interface Timing

5.10.6.1 RGMII

Figure 5-15 RGMII Receive Timing

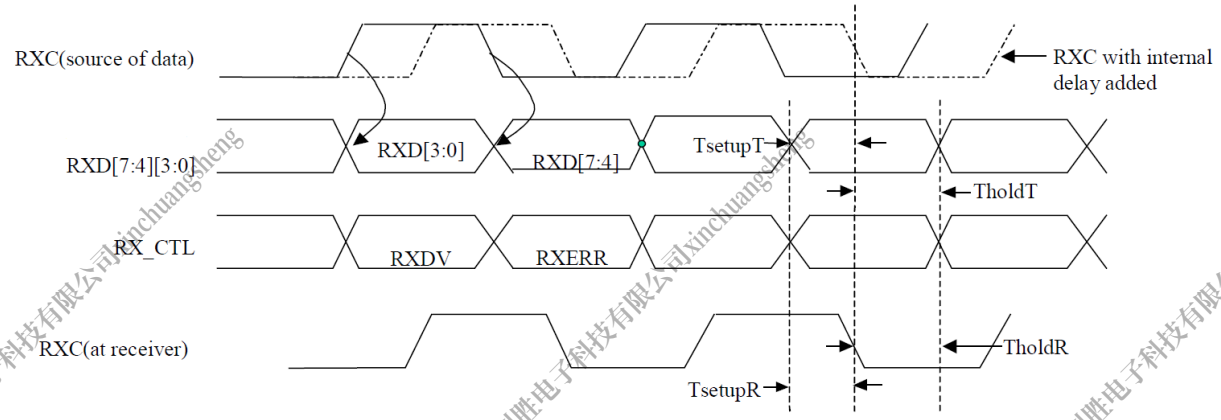


Figure 5-16 RGMII Transmit Timing

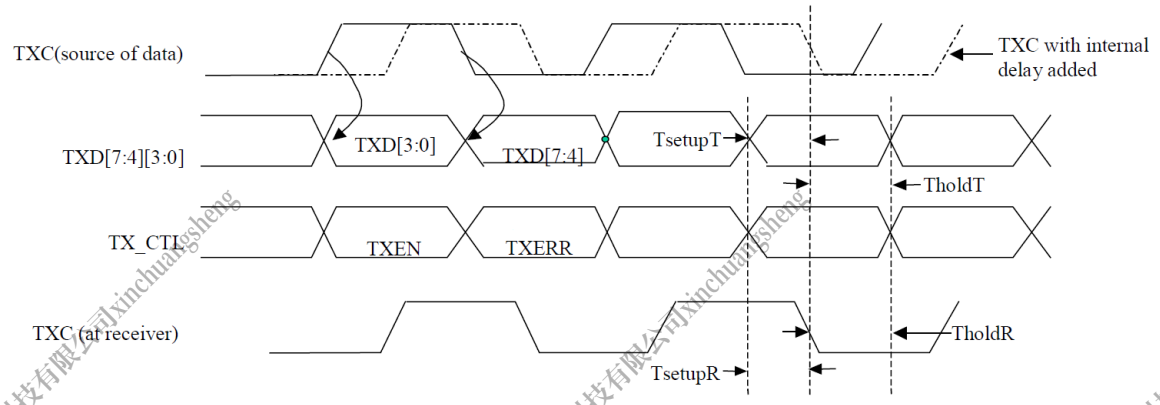


Table 5-24 RGMII Timing Parameters

Parameter	Description	Min	Typical	Max	Unit
Tcyc	Clock Cycle Duration *note1	7.2	8	8.8	ns
Duty_G	Duty Cycle Duration for Gigabit	45	50	55	%
Duty_T	Duty Cycle for 10/100T	40	50	60	%
TsetupT	Data to clock output setup(at Transmitter integrated delay)	1.2	2.0		ns
TholdT	Data to clock output hold(at Transmitter integrated delay)	1.2	2.0		ns
TsetupR	Data to clock input setup(at Receiver integrated delay)	1.0	2.0		ns

Parameter	Description	Min	Typical	Max	Unit
TholdR	Data to clock input hold(at Receiver integrated delay)	1.0	2.0		ns
For 10Mbps and 100Mbps, Tcyc will scale 400ns±40ns and 40ns±4ns.					

5.10.6.2 RMII

Figure 5-17 RMII Receive Timing

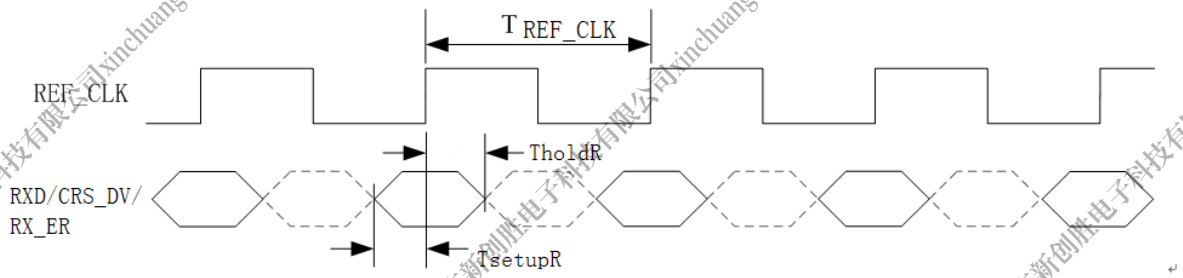


Figure 5-18 RMII Transmit Timing

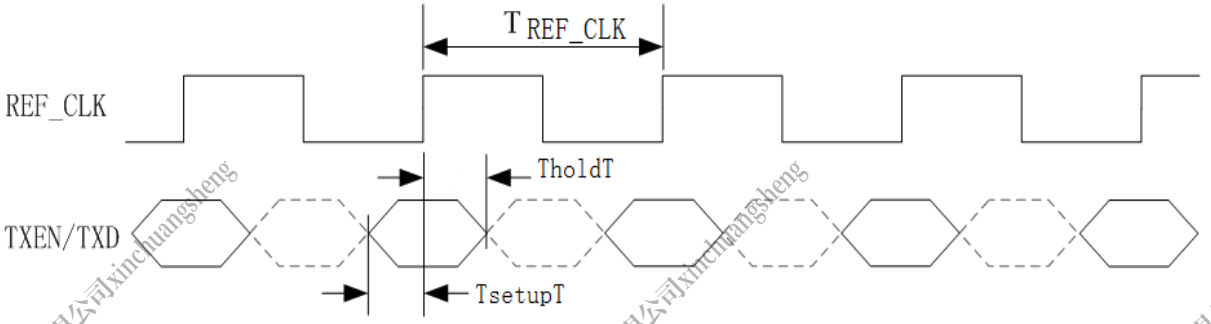


Table 5-25 RMII Timing Parameters

Parameter	Description	Min	Typ	Max	Unit
T_{REF_CLK}	Reference Clock Period	-	20	-	ns
Tduty	REF_CLK duty cycle	35		65	%
TsetupT	TXD/TXEN to REF_CLK setup time	4			ns
TholdT	TXD/TXEN to REF_CLK hold time	2			ns
TsetupR	RXD/CRS_DV/RX_ER to REF_CLK setup time	4			ns
TholdR	RXD/CRS_DV/RX_ER to REF_CLK hold time	2			ns

5.10.7 Local Bus Timing

Figure 5-19 Local Bus Timing

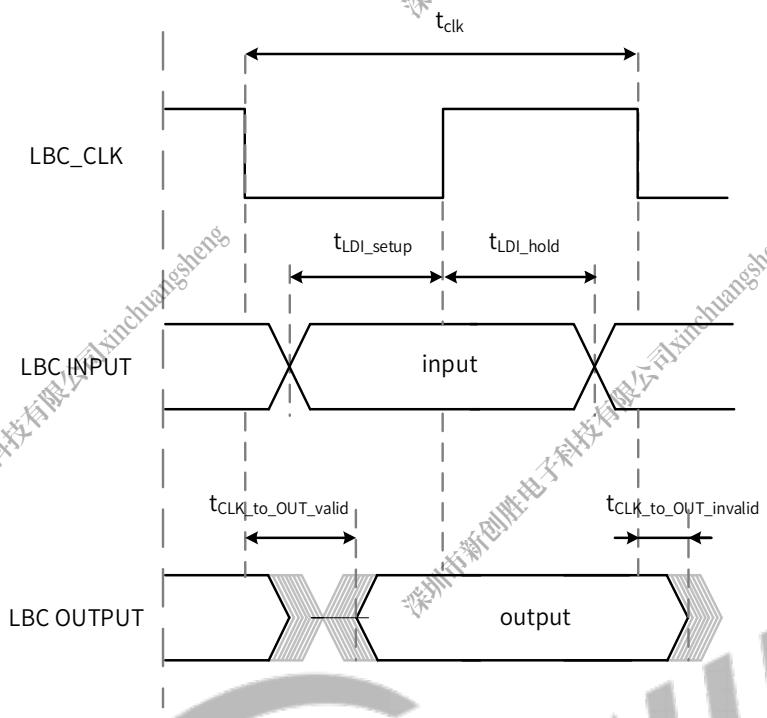


Table 5-26 Local Bus Timing Parameters

Parameter	Min	Max	Description
t_{clk}	5ns	-	LBC_CLK period (f_{clk}≤200M)
t_{LDI_setup}	1ns	-	Input signals valid before LBC_CLK edge
t_{LDI_hold}	1ns	-	Input signals valid after LBC_CLK edge
$t_{CLK\_to\_OUT\_valid}$	-	1ns	Output signals valid after LBC_CLK edge
$t_{CLK\_to\_OUT\_invalid}$	0ns	-	Output signals invalid after LBC_CLK edge

5.10.8 SPI Interface Timing

Figure 5-20 SPI Writing Timing

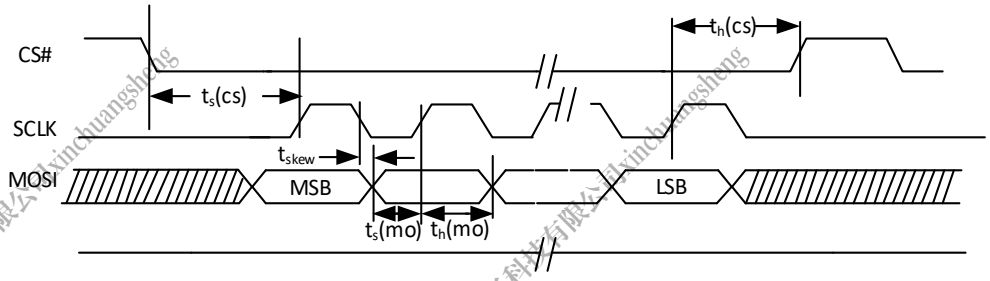


Figure 5-21 SPI Reading Timing

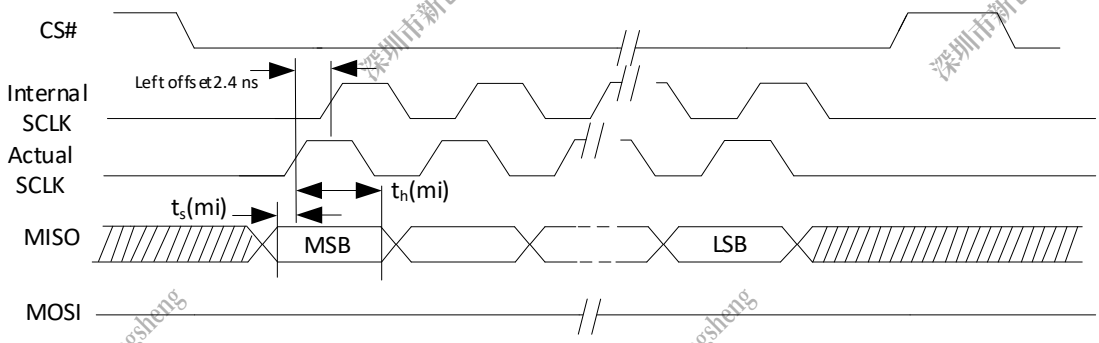


Table 5-27 SPI Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
CS# Active Setup Time	t_s(cs)	$2T^{(1)}$	-	-	ns
CS# Active Hold Time	t_h(cs)	$2T^{(1)}$	-	-	ns
CLK/Data output skew time	$t_{skew}^{(2)}$	-	-	1	ns
Data output Delay Time	T_s(mo)	$T^{(1)}/2 - t_{skew}$	-	$T^{(1)}/2 + t_{skew}$	ns
Data output Hold Time	t_h(mo)	$T^{(1)}/2 - t_{skew}$	-	$T^{(1)}/2 + t_{skew}$	ns
Data In Setup Time	t_s(mi)	0.2(master mode) 4.5(slave mode)	-	-	ns
Data In Hold Time	t_h(mi)	0.2(master mode) 2(slave mode)	-	-	ns

(1) T is the cycle of clock.

(2) t_{skew} is the output skew time between SCLK and MOSI. SCLK may be either faster or slower than MOSI.

5.10.9 SPI-DBI Interface Timing

Figure 5-22 DBI 3-line Serial Interface Timing

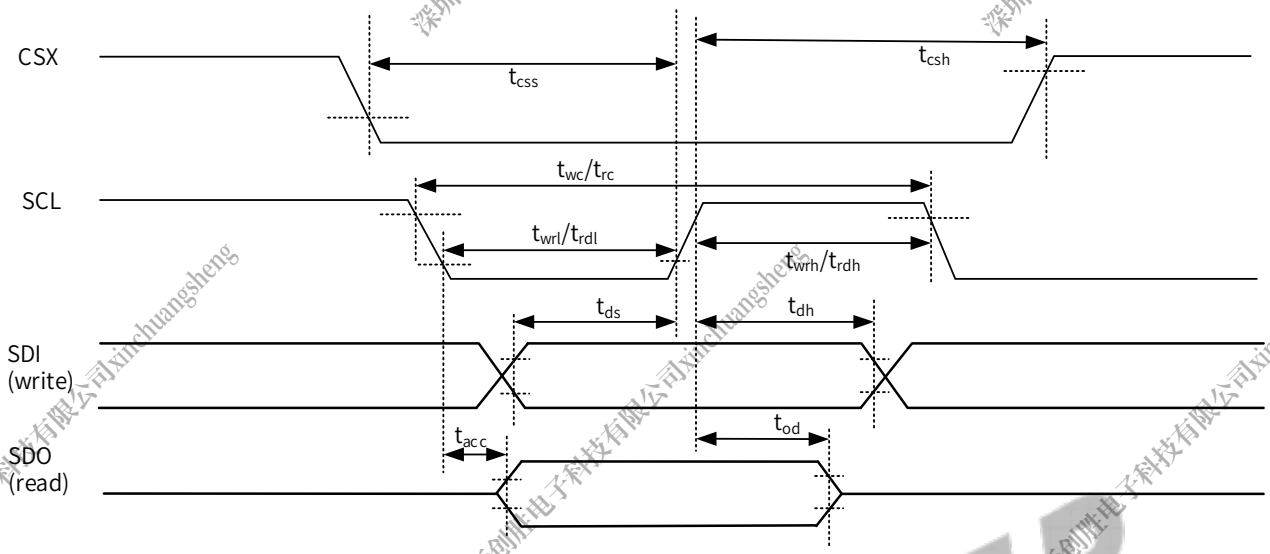


Table 5-28 DBI 3-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse "H" duration	t_{wrh}	7		ns
	Control pulse "L" duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-29 DBI 3-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse "H" duration	t_{rdh}	60		ns
	Control pulse "L" duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	10(1)	50	ns
	Output disable time	t_{od}	15(1)	50	ns

Signal	Parameter	Symbol	Min	Max	Unit
Note: Range of required clock frequency: 0-6.67 MHz.					

Figure 5-23 DBI 4-line Serial Interface Timing

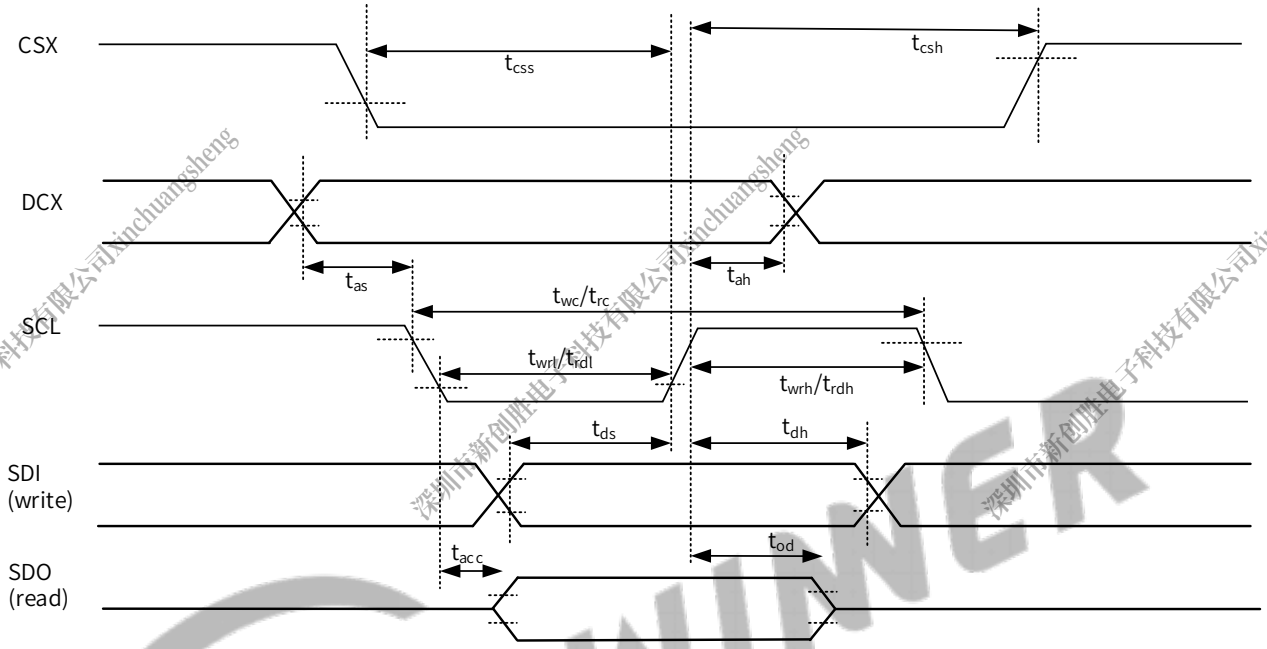


Table 5-30 DBI 4-line Serial Interface Write Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{css}	15		ns
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Write cycle	t_{wc}	16		ns
	Control pulse “H” duration	t_{wrh}	7		ns
	Control pulse “L” duration	t_{wrl}	7		ns
SDI/SDO	Data setup time	t_{ds}	7(1)		ns
	Data hold time	t_{dt}	7(1)		ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-60 MHz.					

Table 5-31 DBI 4-line Serial Interface Read Timing Parameters

Signal	Parameter	Symbol	Min	Max	Unit
CSX	Chip select setup time	t_{csh}	60		ns

Signal	Parameter	Symbol	Min	Max	Unit
DCX	Address setup time	t_{as}	10		ns
	Address hold time	t_{ah}	10		ns
SCL	Read cycle	t_{rc}	150		ns
	Control pulse “H” duration	t_{rdh}	60		ns
	Control pulse “L” duration	t_{rdl}	60		ns
SDI/SDO	Read access time	t_{racc}	-	50	ns
	Output disable time	t_{od}	15(1)	50	ns
Note: Range of required clock frequency: 0-6.67 MHz.					

5.10.10 SPI Flash Interface Timing

5.10.10.1 Controller Output to Target Input Timing

Figure 5-24 xSPI Target Data Input Timing

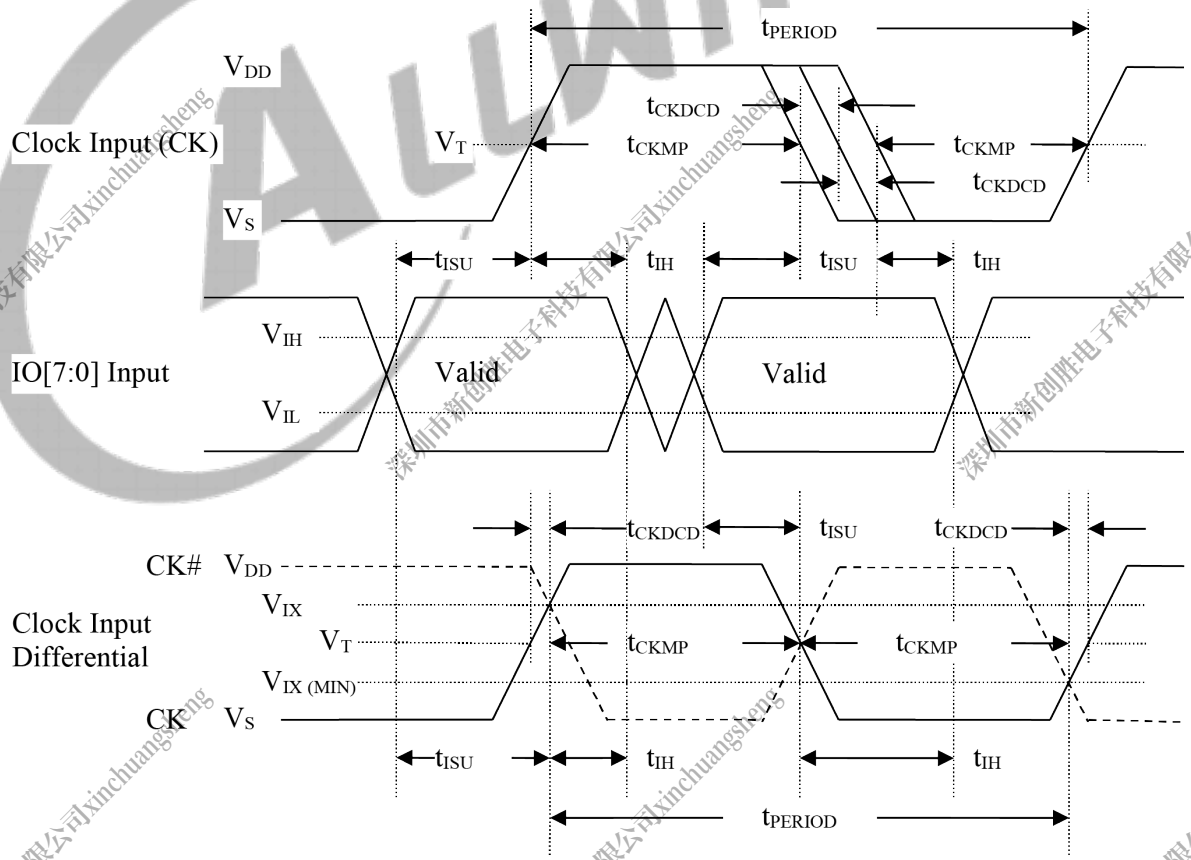


Table 5-32 Clock Input Threshold Levels

Parameter	Symbol	Min	Max	Unit
Clock Input Threshold (AC)	$V_{T\ (AC)}$	0.50 * V_{DD}	0.50 * V_{DD}	V
Input differential crossing (AC)	$V_{IX\ (AC)}$	0.4 * V_{DD}	0.60 * V_{DD}	V

Table 5-33 xSPI Device Input Timing

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		
Input CK									
Cycle Time Data Transfer Mode	t_{PERIOD}	6	-	7.5	-	10	-	ns	150 MHz (max) between the rising edges with respect to V_T.
Slew Rate	SR	0.94	-	0.75	-	0.56	-	V/ns	With respect to VIH/VIL.
Duty Cycle Distortion	t_{CKDCD}	0.0	0.3	0.0	0.375	0.0	0.5	ns	Allowable deviation from an ideal 50% duty cycle with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{CKMPW}	2.7	-	3.375	-	4.5	-	ns	With respect to V_T.
Input Signals (Referenced to CK)									
Input Setup Time (DTR)	t_{ISUddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (DTR)	t_{IHddr}	0.6	-	0.8	-	1.0	-	ns	With respect to V_{IH}/V_{IL}.
Input Setup Time (STR)	t_{ISU}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Input Hold Time (STR)	t_{IH}	1	-	2	-	2	-	ns	With respect to V_{IH}/V_{IL}.
Slew Rate @ 1.8 V	SR	0.94	--	0.75	-	0.56	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.
Slew Rate @ 3.0 V	SR	1.72	-	1.37	-	1.03	-	V/ns	With respect to V_{IH}/V_{IL} and xSPI reference load.

Parameter	Symbol	xSPI-333(1)		xSPI-266(2)		xSPI-200(3)		Unit	Comments
		Min	Max	Min	Max	Min	Max		

Note:

(1) xSPI-333: Up to 166 MHz; up to 333 MT/s.

(2) xSPI-266: Up to 133 MHz; up to 266 MT/s.

(3) xSPI-200: Up to 100 MHz; up to 200 MT/s.

5.10.10.2 Target Output to Controller Input Timing

Figure 5-25 xSPI Target Data Output Timing

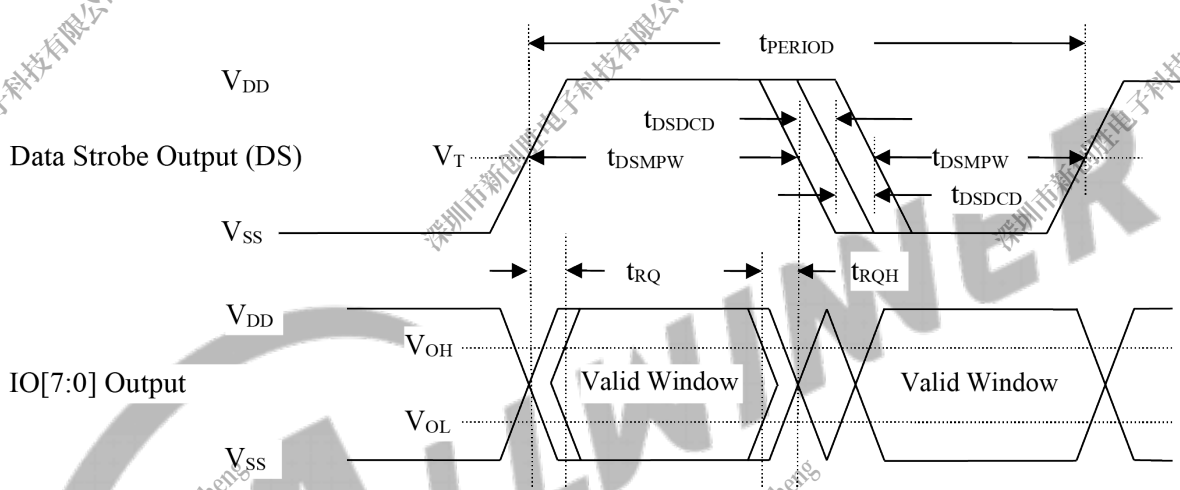


Table 5-34 xSPI Device Output Timing

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Data Strobe(2)					
Cycle Time Data Transfer Mode	t_{PERIOD}	10	-	ns	100 MHz (max) between the rising edges with respect to V_T.
Duty Cycle Distortion	t_{DSDCD}	0.0	0.4	ns	Allowable deviation from the input clock duty cycle distortion (tCKDCD) with respect to V_T. Includes jitter and phase noise.
Minimum Pulse Width	t_{DSMPW}	4.1	-	ns	Minimum Pulse Width of DS is smaller than that of CK since the target is allowed to add distortion when generating DS from CK. With respect to V_T.

Parameter	Symbol	xSPI-200(1)		Unit	Comments
		Min	Max		
Output DATA (Referenced to DS)					
Output skew	t_{RQ}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Output hold skew	t_{RQH}	-	0.8	ns	With respect to V_{OH}/V_{OL} and xSPI reference load.
Note: (1) xSPI-200: Up to 100 MHz; up to 200 MT/s. (2) Controller CK edges are the trigger for target IO and DS edges. IO and DS edges therefore always follow their related (triggering) CK edges.					

5.10.11 UART Interface Timing

Figure 5-26 UART RX Timing

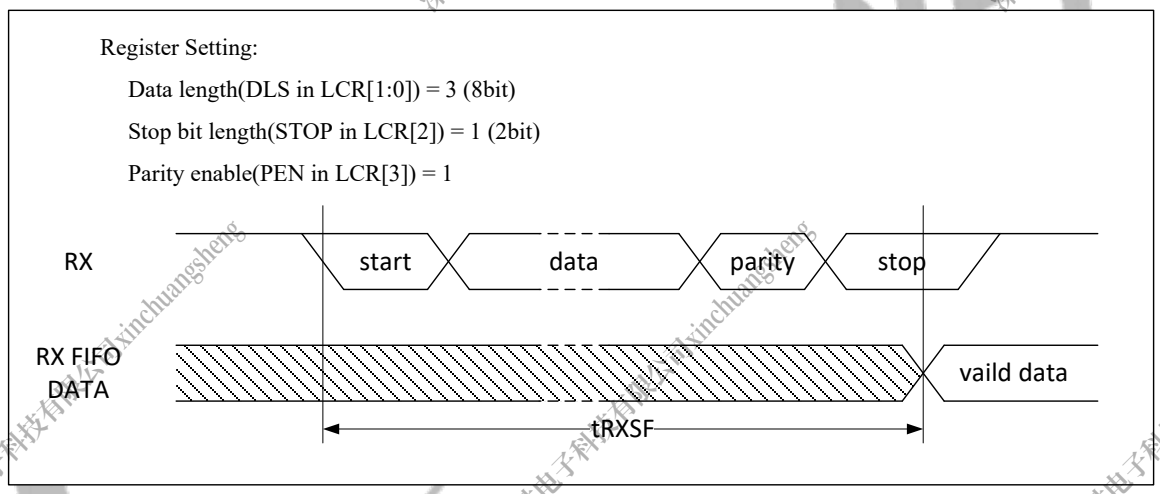


Figure 5-27 UART nCTS Timing

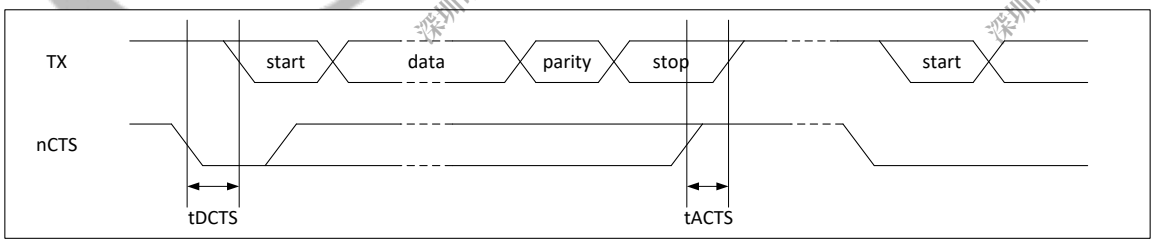


Figure 5-28 UART nRTS Timing

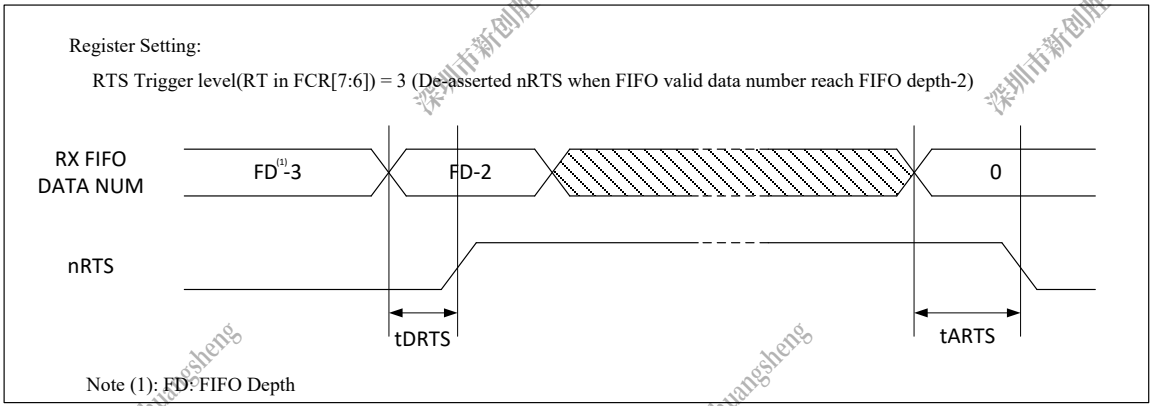


Table 5-35 UART Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
RX start to RX FIFO	tRXSF	10.5*BRP(1)	-	11*BRP(1)	ns
Delay time of de-asserted nCTS to TX strat	tDCTS	-	-	BRP(1)	ns
Step time of asserted nCTS to stop next transmission	tACTS	BRP(1) /4	-	-	ns
Delay time of de-asserted nRTS	tDRTS	-	-	BRP(1)	ns
Delay time of asserted nRTS	tARTS	-	-	BRP(1)	ns
(1) BRP: Baud-Rate Period.					

5.10.12 TWI Interface Timing

Figure 5-29 TWI Timing

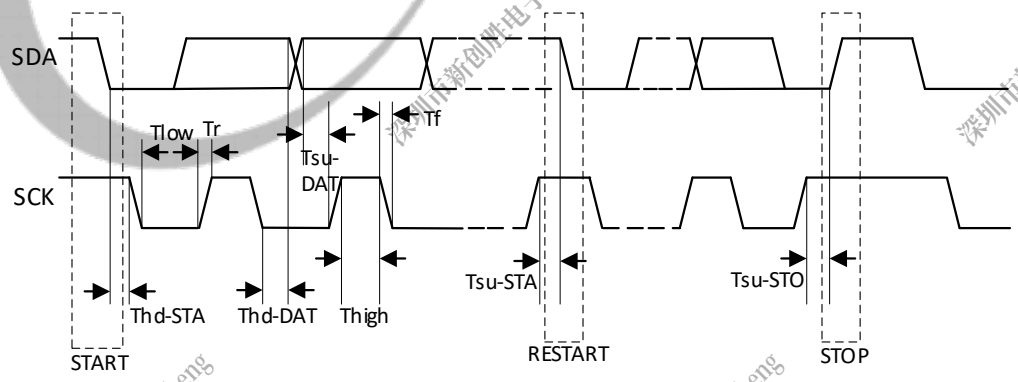


Table 5-36 TWI Timing Parameters

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
SCK clock frequency	Fsck	0	100	0	400	kHz

Parameter	Symbol	Standard mode		Fast mode		Unit
		Min	Max	Min	Max	
Setup Time In Start	Tsu-STA	4.7	-	0.6	-	us
Hold Time In Start	Thd-STA	4.0	-	0.6	-	us
Setup Time In Data	Tsu-DAT	250	-	100	-	ns
Hold Time In Data	Thd-DAT	0	-	0	-	us
Setup Time In Stop	Tsu-STO	4.0	-	0.6	-	us
SCK Low level Time	Tlow	4.7	-	1.3	-	us
SCK High level Time	Thigh	4.0	-	0.6	-	us
SCK/SDA Falling Time	Tf	-	300	20	300	ns
SCK/SDA Rising Time	Tr	-	1000	20	300	ns

5.10.13 I2S/PCM Interface Timing

Figure 5-30 I2S/PCM Timing in Master Mode

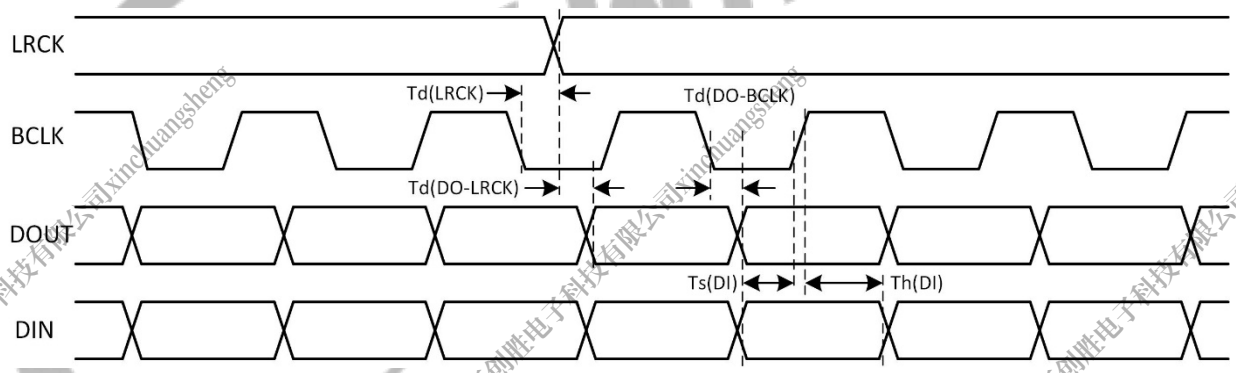


Table 5-37 I2S/PCM Timing Constants in Master Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK delay	T_d(LRCK)	-	-	10	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	8	ns
BCLK fall time	T_f	-	-	8	ns

Figure 5-31 I2S/PCM Timing in Slave Mode

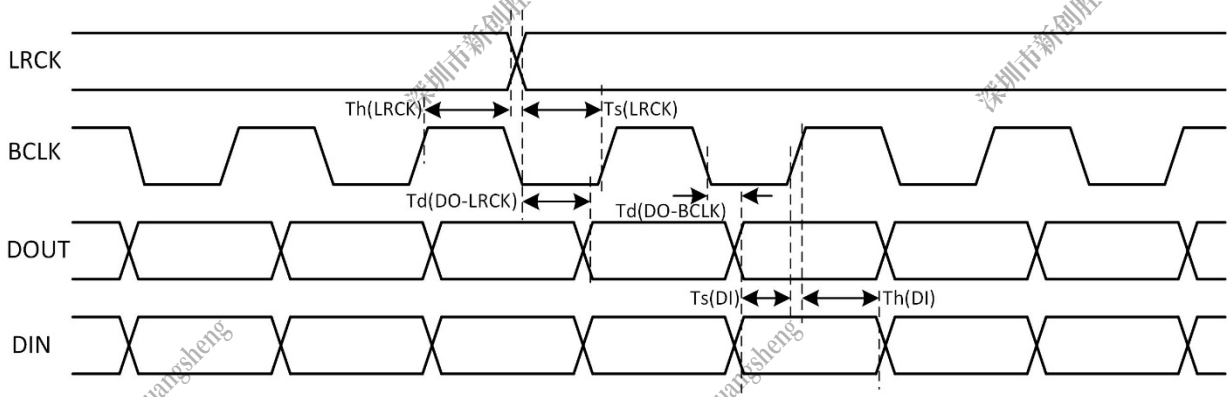


Table 5-38 Timing Constants in Slave Mode

Parameter	Symbol	Min	Typ	Max	Unit
LRCK setup	T_s(LRCK)	4	-	-	ns
LRCK hold	T_h(LRCK)	4	-	-	ns
LRCK to DOUT delay (For LJF)	T_d(DO-LRCK)	-	-	10	ns
BCLK to DOUT delay	T_d(DO-BCLK)	-	-	10	ns
DIN setup	T_s(DI)	4	-	-	ns
DIN hold	T_h(DI)	4	-	-	ns
BCLK rise time	T_r	-	-	4	ns
BCLK fall time	T_f	-	-	4	ns

5.10.14 DMIC Interface Timing

Figure 5-32 DMIC Timing

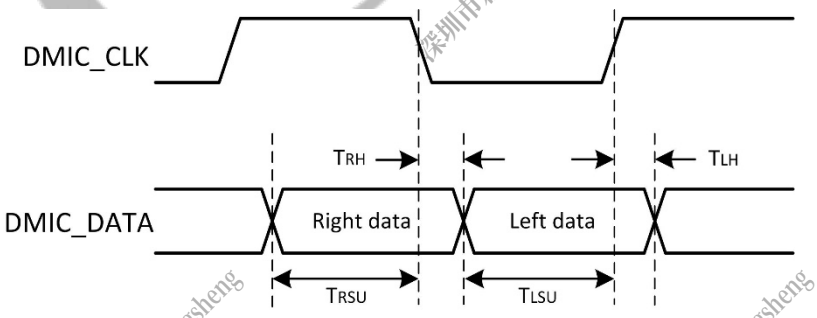


Table 5-39 DMIC Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
DMIC_DATA(Right) Setup Time to Falling Edge of DMIC_CLK	T_{RSU}	15	-	-	ns
DMIC_DATA(Right) Hold Time from Falling Edge of DMIC_CLK	T_{RH}	0	-	-	ns
DMIC_DATA(Left) Setup Time to Rising Edge of DMIC_CLK	T_{LSU}	15	-	-	ns
DMIC_DATA(Left) Hold Time From Rising edge of DMIC_CLK	T_{LH}	0	-	-	ns

5.10.15 OWA Interface Timing

Figure 5-33 OWA Timing

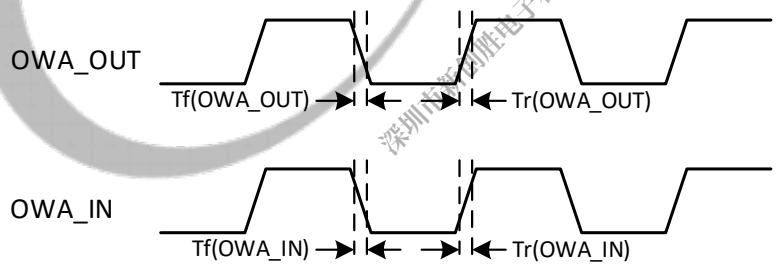


Table 5-40 OWA Timing Constants

Parameter	Symbol	Min	Typ	Max	Unit
OWA_OUT Rise Time	Tr(OWA_OUT)	-	-	8	ns
OWA_OUT Fall Time	Tf(OWA_OUT)	-	-	8	ns
OWA_IN Rise Time	Tr(OWA_IN)	-	-	4	ns
OWA_IN Fall Time	Tf(OWA_IN)	-	-	4	ns

5.11 Power-Up and Power-Down Sequence

NOTE

- All "Tn" markers represent different steps during power-on and power-off process and show the minimum time interval between current step and previous step.
- The consequent steps in power-on sequence should not start before the previous step supplies have been stabilized within 90%-110% of their nominal voltage, unless stated otherwise.
- Different power rails at the same Tn step should become stable within 1ms.
- VCC25-DRAM mentioned as below are external DRAM power supplies.

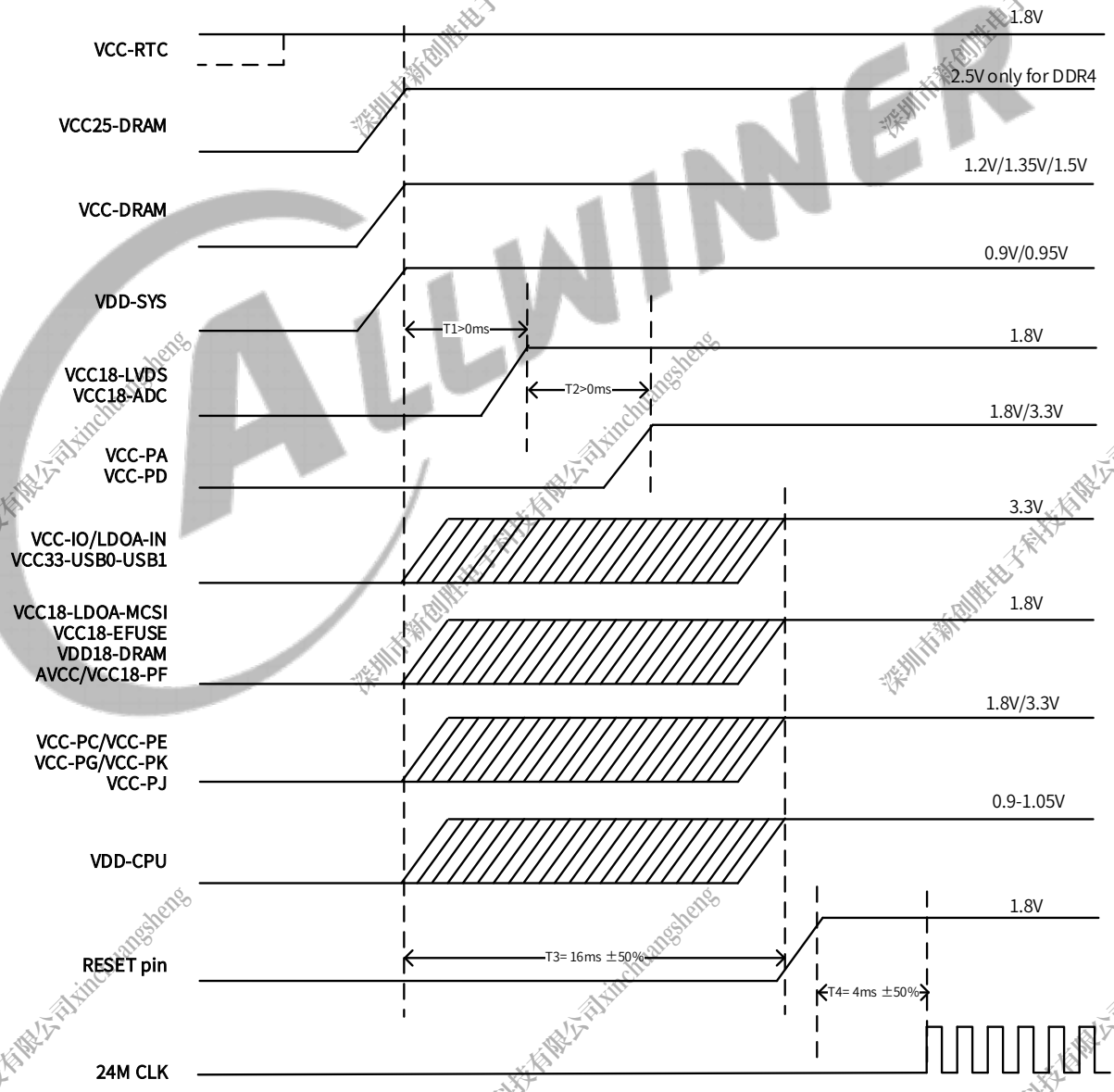
5.11.1 Power-Up Sequence

5.11.1.1 WBBGA Power-Up Sequence

The following figure shows an example of the power-up sequence. The description of the power-up sequence is as follows.

a. VCC-RTC is always-on.
b. VCC25-DRAM and VCC-DRAM, along with VDD-SYS, power on in the first step.
c. VCC-PD must power on after VCC18-LVDS, VCC-PA must power on after VCC18-ADC.
d. After VDD-SYS powers on, wait for a delay of 16ms ±50% before releasing the reset signal to initiate system boot.

Figure 5-34 Power-Up Sequence



5.11.1.2 eQFP Power-Up Sequence

The following figure shows an example of the power-up sequence. The description of the power-up sequence is as follows.

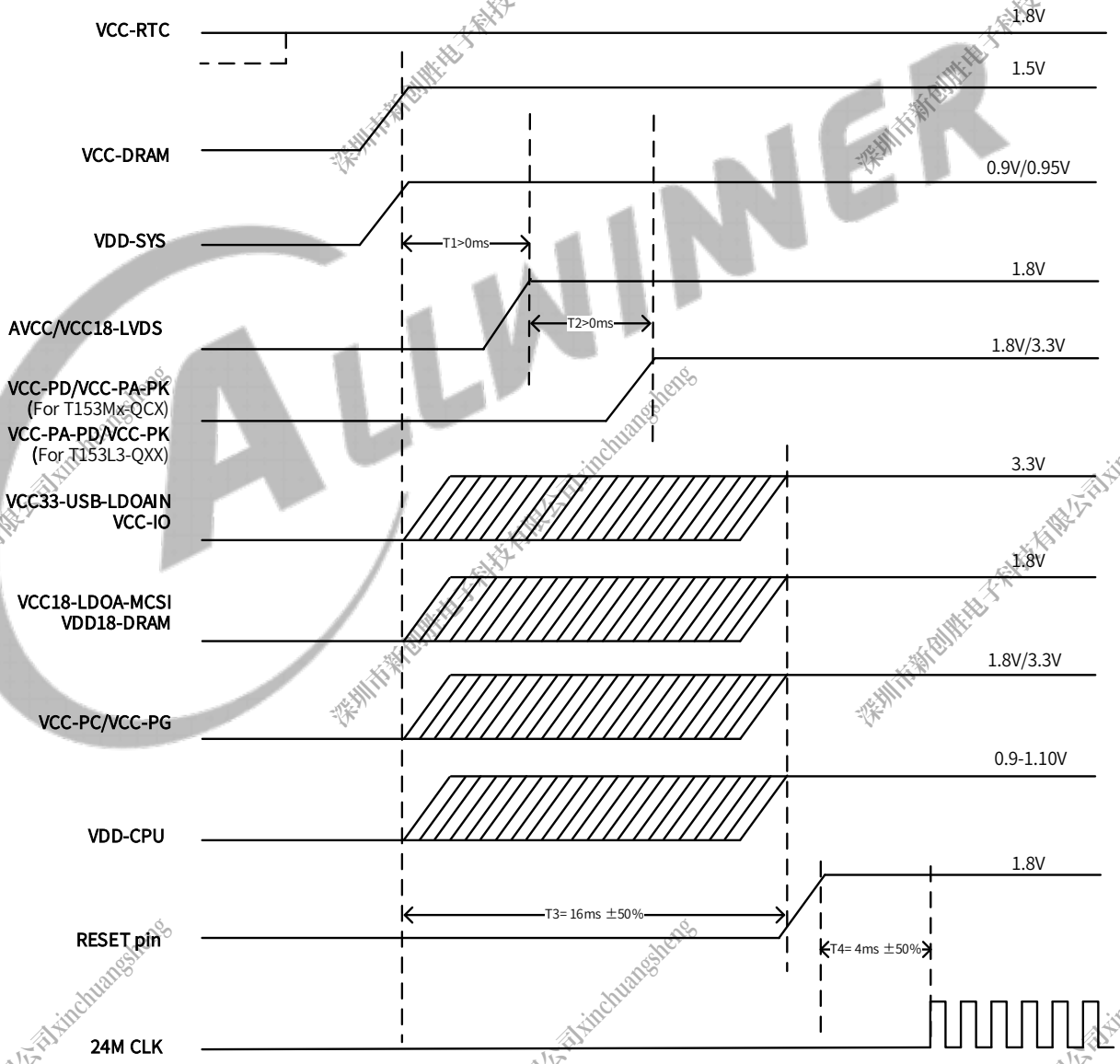
a. VCC-RTC is always-on.

b. VCC-DRAM, along with VDD-SYS, power on in the first step.

c. For T153Mx-QCX, VCC-PD&VCC-PA-PK must power on after AVCC&VCC18-LVDS. For T153L3-QXX, VCC-PA-PD&VCC-PK must power on after AVCC&VCC18-LVDS.

d. After VDD-SYS powers on, wait for a delay of 16ms ±50% before releasing the reset signal to initiate system boot.

Figure 5-35 Power-Up Sequence



5.11.2 Power-Down Sequence

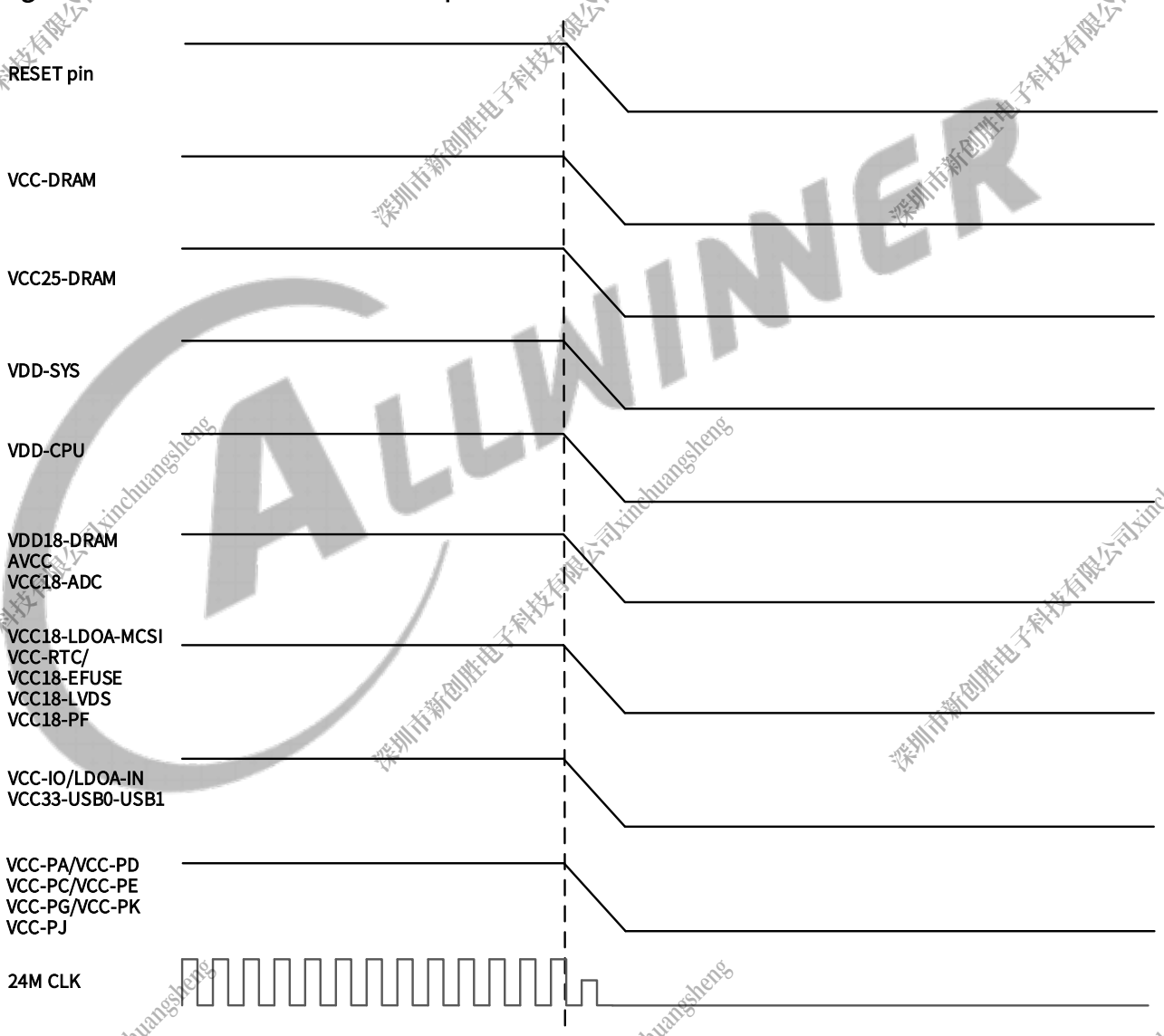
5.11.2.1 WBBGA Power-Down Sequence

The following figure shows an example of the power-down sequence. The description of the power-down sequence is as follows.

a. In the power-down process, there is no requirements on the power sequence. All the power can power down simultaneously.

b. The chip supports VCC-IO power-down detection by default. When VCC-IO powers down, the chip will power down the reset pin automatically.

Figure 5-36 WBBGA Power-Down Sequence



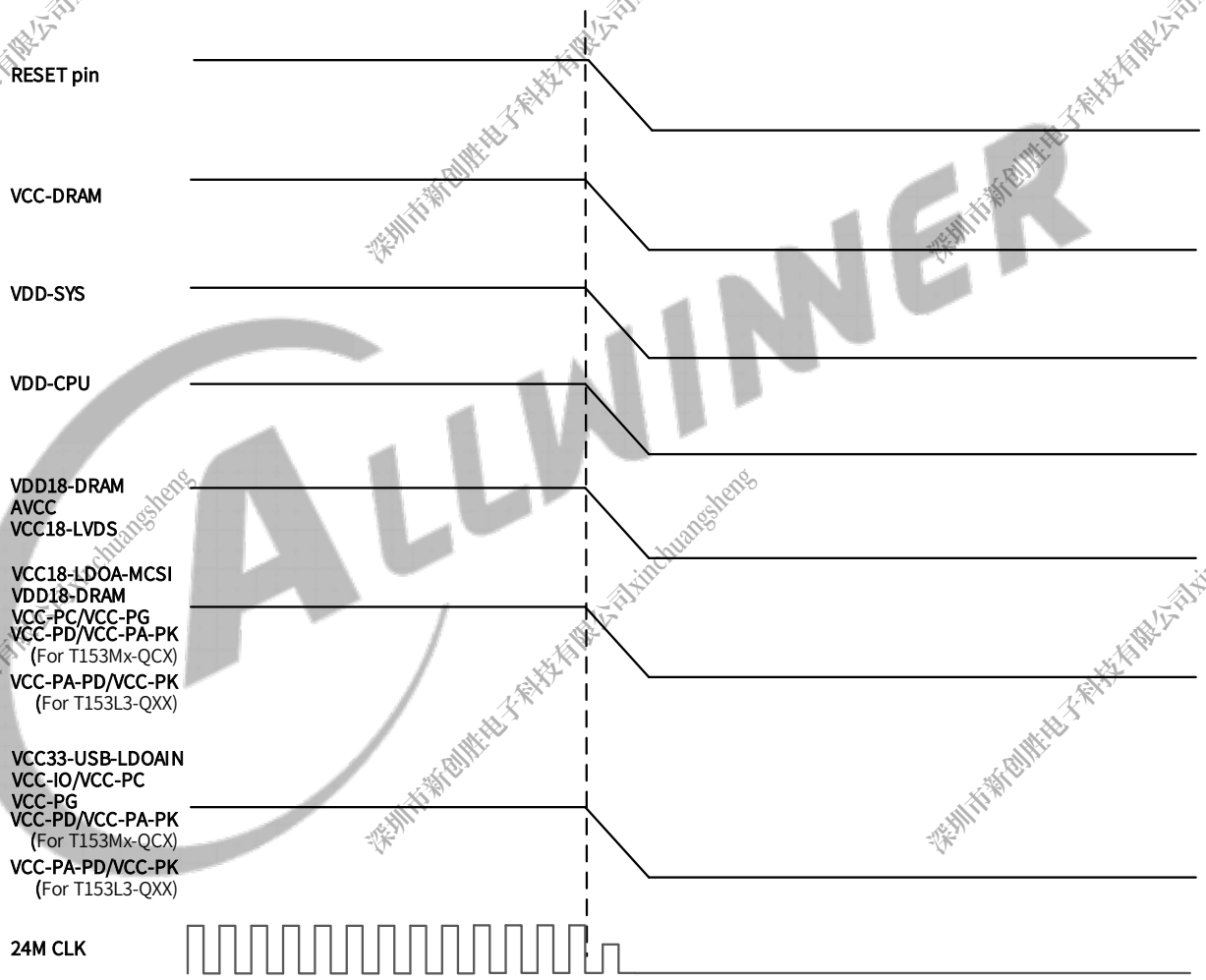
5.11.2.2 eQFP Power-Down Sequence

The following figure shows an example of the power-down sequence. The description of the power-down sequence is as follows.

a. In the power-down process, there is no requirements on the power sequence. All the power can power down simultaneously.

b. The chip supports VCC-IO power-down detection by default. When VCC-IO powers down, the chip will power down the reset pin automatically.

Figure 5-37 eQFP Power-Down Sequence



6 Temperature and Thermal Characteristics

6.1.1 Temperature

The following tables describe the temperature of the device

Table 6-1 Operating and Storage Temperature

Symbol	Parameter	Min	Max	Unit
T_a	Ambient Operating Temperature	-40	85	°C
T_{STG}	Storage Temperature	-40	150	°C

Table 6-2 Junction Temperature

Chip	Recommended Operating Temperature (T_j)		Absolute Maximum Junction Temperature	Unit
	Min	Max		
T153	-40	120	125	°C

6.1.2 Package Thermal Characteristics

The maximum chip junction temperature ($T_{J\,max}$) must never exceed the values given in Table 6-2 Junction Temperature.

Failure to maintain a junction temperature within the range specified reduces operating lifetime, reliability, and performance, and may cause irreversible damage to the system. It is useful to calculate the exact power consumption and junction temperature to determine which the temperature will be best suited to the application. Therefore, the product should include thermal analysis and thermal design to ensure the operating junction temperature of the device is within functional limits.

The following tables show the thermal resistance characteristics of the device. These data are based on JEDEC JESD51 standard, because the actual system design and temperature could be different from JEDEC JESD51, these simulating data are a reference only and may not represent actual use-case values, please prevail in the actual application condition test.

Table 6-3 WBBGA Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	25.1	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	14.37	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	1.74	-	°C/W

Table 6-4 eQFP Package Thermal Characteristics

Symbol	Parameter	Min	Typ(1)(2)	Max	Unit
θ_{JA}	Junction-to-Ambient Thermal Resistance	-	20.47	-	°C/W
θ_{JB}	Junction-to-Board Thermal Resistance	-	13.6	-	°C/W
θ_{JC}	Junction-to-Case Thermal Resistance	-	1.3	-	°C/W

(1) Reference document: JESD51-2 Integrated Circuits Thermal Test Method Environment Conditions – Natural Convection (Still Air). Available from www.jedec.org.

(2) The testing PCB is 4 layers, 114.5 mm x 76.2 mm body, and 1.6 mm thickness. Ambient temperature is 25 °C.

7 Pin Assignment

7.1.1 Pin Map

7.1.1.1 T153MX-BCX Pin Map

The following shows the WBBGA 327 balls, 13 mm x 13 mm size, 0.65&0.6 mm ball pitch, 0.3 mm ball size pin map.

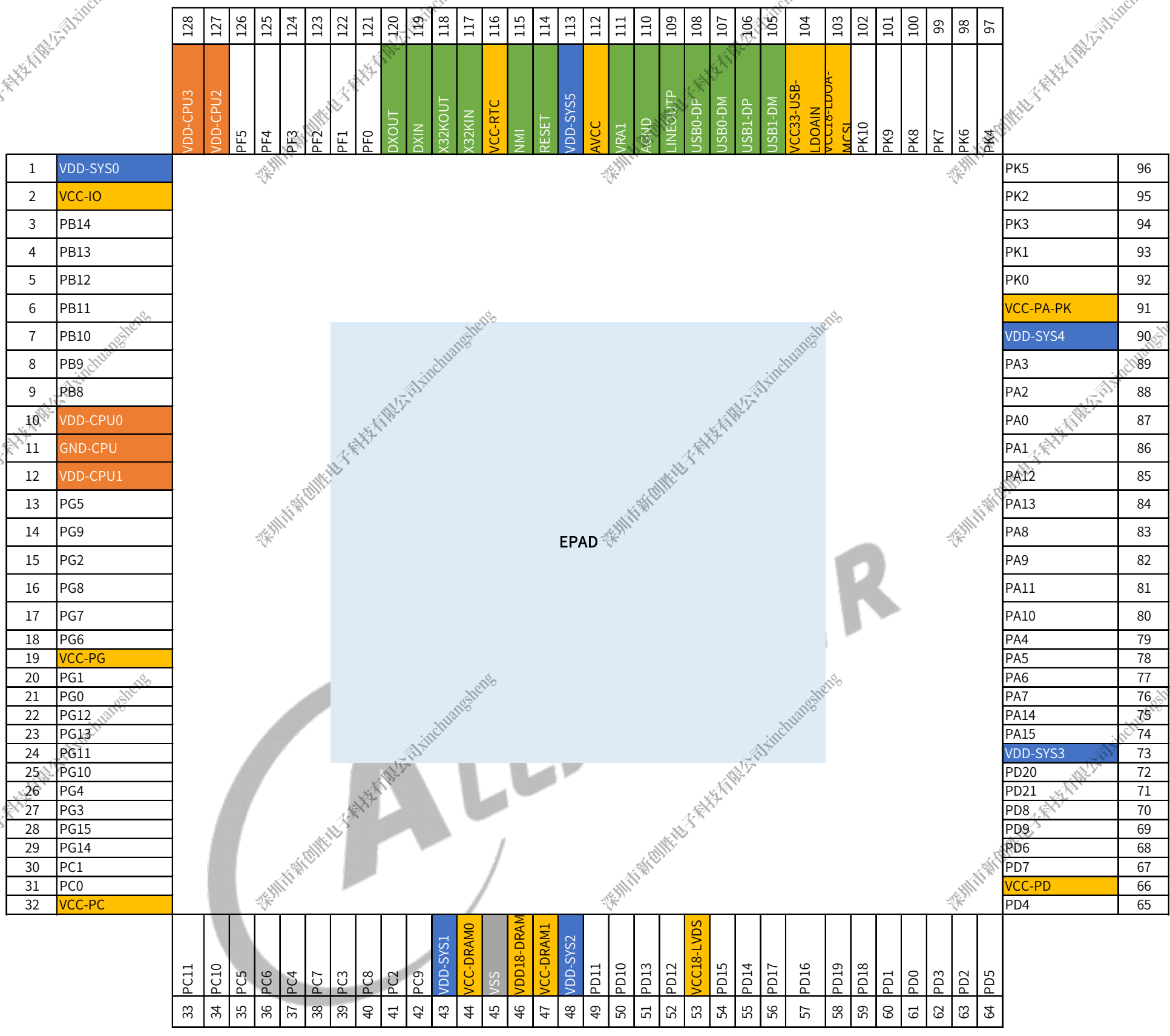
Figure 7-1 T153MX-BCX Pin Map

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	GND	PJ6	PJ4		PF4		PF6		DXIN		X32KFOUT		GND		PK9		PK7		PK1	PK5	GND	A
B	PJ3	PJ7	PJ5	PJ8	PF5	PF2	PF0	REFCLK-OUT	DXOUT	X32KOUT	GND	LINEOUTN	USB0-DM	USB1-DM	PK8	PK11	PK6	PK3	PK0	PK4	PE8	B
C	PJ1	PJ0	PJ2	PJ9	GND	PF3	PF1	GPIO0	GPIO4	X32KIN	RESET	LINEOUTP	USB0-DP	USB1-DP	GND	PK10	GND	PK2	PE9	PE0	PE5	C
D		PJ12	PJ13		1	2	3	4	5	6	7	8	9	10	11	12	13	14	PE1	PE7		D
E	PJ10	FEL	PJ11	1A	PJ15	PJ14	VCC-PJ	GPIO1		VCC18-PF	AVCC	TEST	VCC-RTC		AGND-ADC	VCC18-ADC	PE4	PE6	PE3	PA3	PE2	E
F		PB12	PB11	1B	PB13	PB14	GND	VCC-IO	GPIO2	PLLTEST	VRA1	VCC33-USB0-USB1	VCC-PK						PA18	PA19		F
G	PB3	PB2	PB1	1C				NMI	GND	GND	AGND	GND	VCC-PE	VCC18-EFUSE		PA2	PA0	PA1	PA8	PA11	PA9	G
H		PB0	PB6	1D	VDD-CPU	VDD-CPUFB	GND	GND	GND	GND	GND	GND	GND	LDOA-IN	VCC18-LDOA-MCSI	PA14	PA13	PA7	PA10	PA15		H
J	PB5	PB4	PB7	1E	VDD-CPU	VDD-CPU	VDD-CPU	VDD-CPU	GND	GND	GND	VDD-SYS	VDD-SYS	VCC-PA					PA16	PA5	PA4	J
K		PB8	PB9	1F				GND	GND	GND		VDD-SYS	GND	VCC-PD		PA23	PA12	PA21	PA6	PA17		K
L	PB10	GND	PG8	1G	PG15	PG14	PG12	GND	GND	GND	GND	VCC-DRAM	GND	GND	VCC18-LVDS	GND	PA22	PA20	GND	PD21	PD20	L
M		PG7	PG6	1H	VCC-PG	PG10	PG13		GND	GND		VCC-DRAM	GND	GND					PD9	PD8		M
N	PG3	PG2	PG0	1J	VCC-PC	PG9	PG11	GND	GND	GND	VCC-DRAM	VCC-DRAM	GND	GND		GND	PD23	PD22	PD4	PD7	PD6	N
P		PG1	PG5	1K			GND	GND			SZQ		GND	VDD18-DRAM		GND	GND	GND	PD2	PD5		P
R	PG4	GND	PC1	1L	GND		SDQM1	GND		SRAS	SCS1		SA6	SA15		SA3	GND	GND	PD1	PD0	PD3	R
T		PC0	PC11	1M	SDQ13		GND	SDQ3		GND	GND		SODT1	SA14		SA9	SVREF		PD18	GND		T
U	PC10	PC5	PC6	1N	SDQ14		SDQ5	SDQ1		SCAS	SA10			GND		GND	SA11		PD17	PD16	PD19	U
V		PC4	PC7	1P	GND		SDQ0	GND		SCS0	SODT0		GND	SRST		GND	SA13		PD15	PD14		V
W	PC3	PC8	GND	SDQ15	SDQS1P	SDQM0	GND	SDQS0N	SDQ2	SDQ4	SWE	GND	GND	SA4	GND	SA1	SA0	SA8	GND	PD13	PD12	W
Y	PC2	PC9	SDQ11	SDQ12	SDQS1N	GND	SDQ10	SDQS0P	SDQ7	GND	GND	SBA0	SCKN	SA12	SCKE0	SBA1	SA5	GND	SA7	PD11	PD10	Y
AA	GND	SDQ9	SDQ8		GND		GND		GND		SDQ6		SCKP		GND		GND		SA2	SBA2	GND	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

7.1.1.2 T153Mx-QCX Pin Map

The following shows the eQFP 128 pins, 14 mm x 14 mm size pin map.

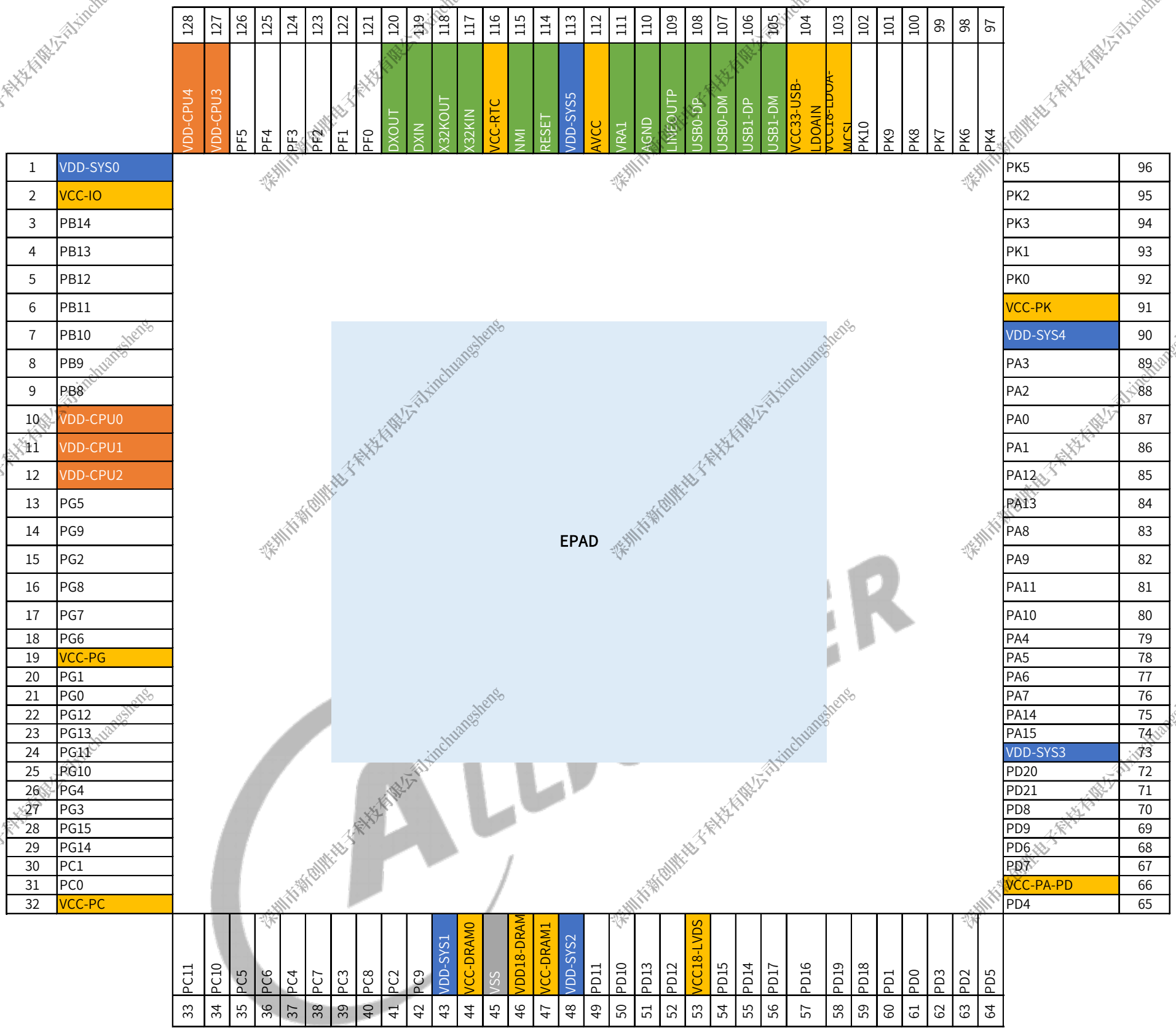
Figure 7-2 T153Mx-QCX Pin Map



7.1.1.3 T153L3-QCX Pin Map

The following shows the eQFP 128 pins, 14 mm x 14 mm size pin map.

Figure 7-3 T153L3-QCX Pin Map

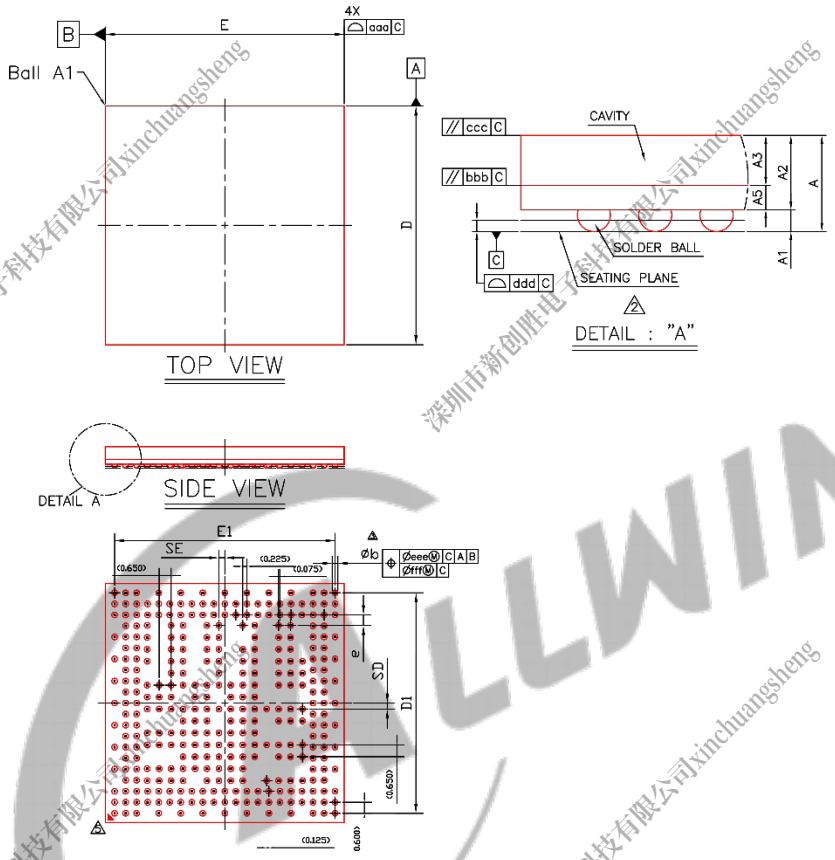


7.1.2 Package Dimension

7.1.2.1 T153MX-BCX Package Dimension

The following figure shows the top, bottom, and side views of the package.

Figure 7-4 T153MX-BCX Package Dimension



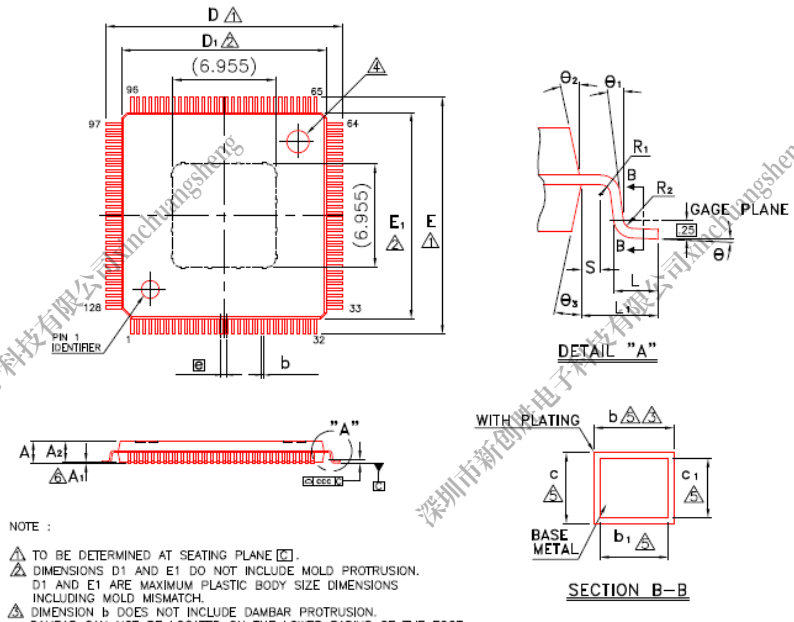
Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.099	1.170	1.241	0.043	0.046	0.049
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.910	0.960	1.010	0.036	0.038	0.040
A3	0.670	0.700	0.730	0.026	0.028	0.029
A5	0.220	0.260	0.300	0.009	0.010	0.012
E	12.900	13.000	13.100	0.508	0.512	0.516
D	12.900	13.000	13.100	0.508	0.512	0.516
E1	---	12.000	---	---	0.472	---
D1	---	12.000	---	---	0.472	---
e	---	0.575	---	---	0.023	---
b	0.260	0.310	0.360	0.010	0.012	0.014
aaa		0.150			0.006	
bbb		0.100			0.004	
ccc		0.100			0.004	
ddd		0.100			0.004	
eee		0.150			0.006	
fff		0.080			0.003	
MD/ME			21/21			
SE		0.325			0.013	
SD		0.325			0.013	

NOTE :
1. CONTROLLING DIMENSION : MILLIMETER.
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C.
4. SPECIAL CHARACTERISTICS C CLASS: ccc,ddd (SPIL STANDARD)
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY.
6. BALL PLACEMENT USE 0.300 mm SOLDER BALL. BGA PAD SOLDER MASK OPENING = 0.275 mm.

7.1.2.2 T153Mx-QCX Package Dimension

The following figure shows the top, bottom, and side views of the package.

Figure 7-5 T153Mx-QCX Package Dimension



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.009
b1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c1	0.09	—	0.16	0.004	—	0.006
D	15.85	16.00	16.15	0.624	0.630	0.636
D1	13.90	14.00	14.10	0.547	0.551	0.555
E	15.85	16.00	16.15	0.624	0.630	0.636
E1	13.90	14.00	14.10	0.547	0.551	0.555
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		
R1	0.08	—	—	0.003	—	—
R2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
θ1	0°	—	—	0°	—	—
θ2	11°	12°	13°	11°	12°	13°
θ3	11°	12°	13°	11°	12°	13°
ccc	0.08			0.003		

NOTE :

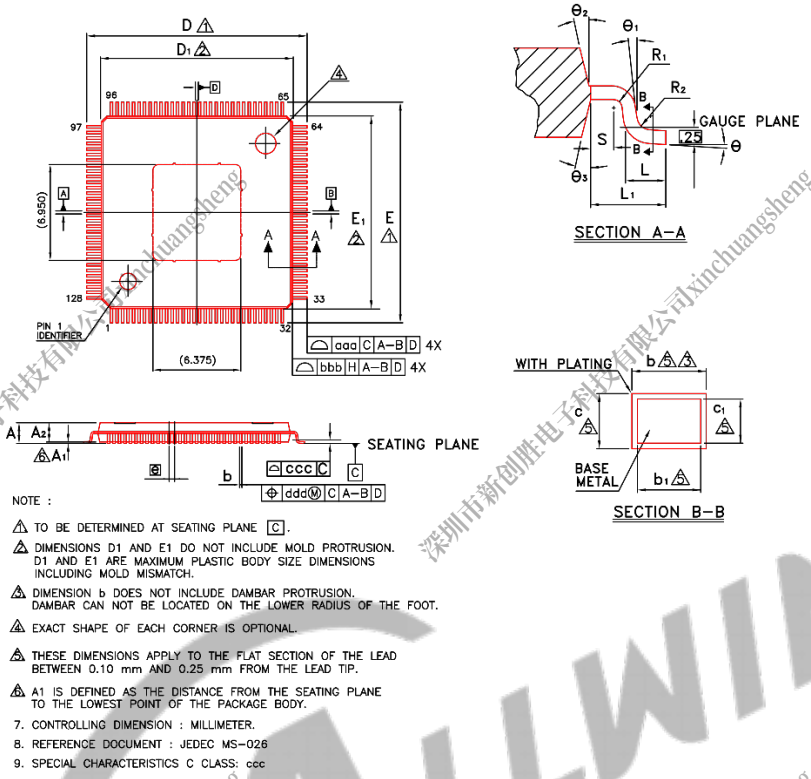
1. TO BE DETERMINED AT SEATING PLANE C.
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.
8. REFERENCE DOCUMENT : JEDEC MS-026.
9. SPECIAL CHARACTERISTICS C CLASS: ccc

TITLE : 128LD E-PAD LQFP (14x14x1.4 mm) PACKAGE OUTLINE-Cu L/F FOOTPRINT 2.0mm			
APPR.			
PE.		DWG NO.	PCO2035
PD.		REV NO.	A
QM.		DATE	05/22/'15
CHK.		DWG.	Leo Deng

7.1.2.3 T153L3-QCX Package Dimension

The following figure shows the top, bottom, and side views of the package.

Figure 7-6 T153L3-QCX Package Dimension



Item	Symbol	Dimension in mm		
		MIN	NOM	MAX
Total thickness	A	---	---	1.600
Lead stand off	A1	0.025	---	0.127
Mold thickness	A2	1.350	1.400	1.450
Lead thickness	b	0.130	0.180	0.230
Lead width	b1	0.130	0.160	0.190
Lead thickness with plating	c	0.090	0.140	0.200
Lead thickness	c1	0.090	0.120	0.160
Outer lead distance X	D	15.850	16.000	16.150
Outer lead distance Y	E	15.850	16.000	16.150
Package size X	D1	13.900	14.000	14.100
Package size Y	E1	13.900	14.000	14.100
E-PAD size X	D2	6.850	6.950	7.050
E-PAD size Y	E2	6.275	6.375	6.475
Lead pitch	e	0.400 BSC		
Lead length from gauge plane	L	0.450	0.600	0.750
Lead length from PKG edge	L1	1.000 REF		
Lead ARC	R1	0.080	---	---
Lead ARC	R2	0.080	---	0.200
Lead ARC distance from PKG edge	S	0.200	---	---
Angle	θ	0.000°	3.500°	7.000°
Angle	θ1	0.000°	---	---
Angle	θ2	11.000°	12.000°	13.000°
Angle	θ3	11.000°	12.000°	13.000°
PKG edge tolerance	aaa	0.200		
PKG profile of a surface	bbb	0.200		
Lead profile of a surface	ccc	0.080		
Lead position	ddd	0.070		

8 Carrier, Storage and Backing Information

8.1 Carrier

8.1.1 WBBGA Carrier

The following table shows matrix tray carrier information.

Table 8-1 WBBGA Matrix Tray Carrier Information

Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	119 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

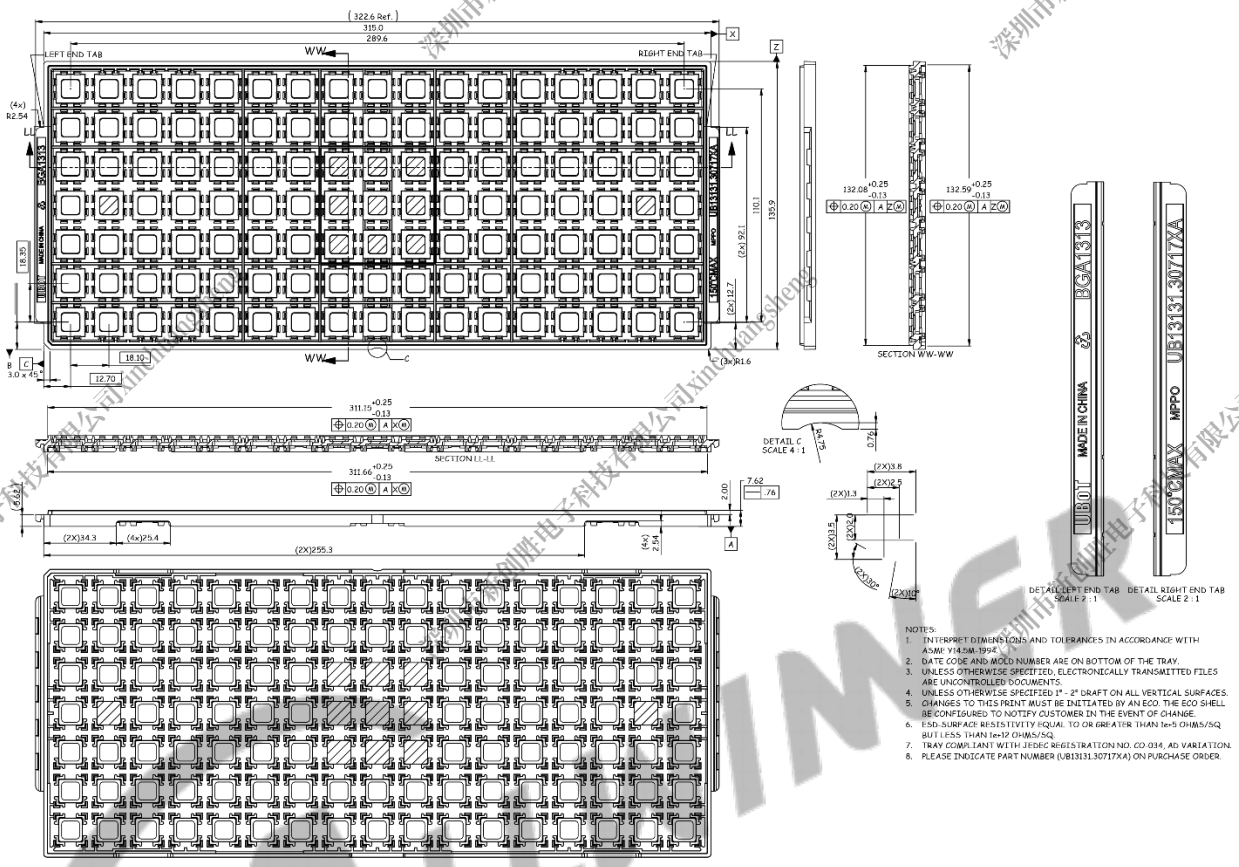
The following table shows packing quantity.

Table 8-2 WBBGA Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
T153MX-BCX	13 mm x 13 mm	119	10	1190	6	7140

The following figures show tray dimension drawing.

Figure 8-1 WBBGA Tray Dimension Drawing



8.1.2 eQFP Carrier

The following table shows matrix tray carrier information.

Table 8-3 eQFP Matrix Tray Carrier Information

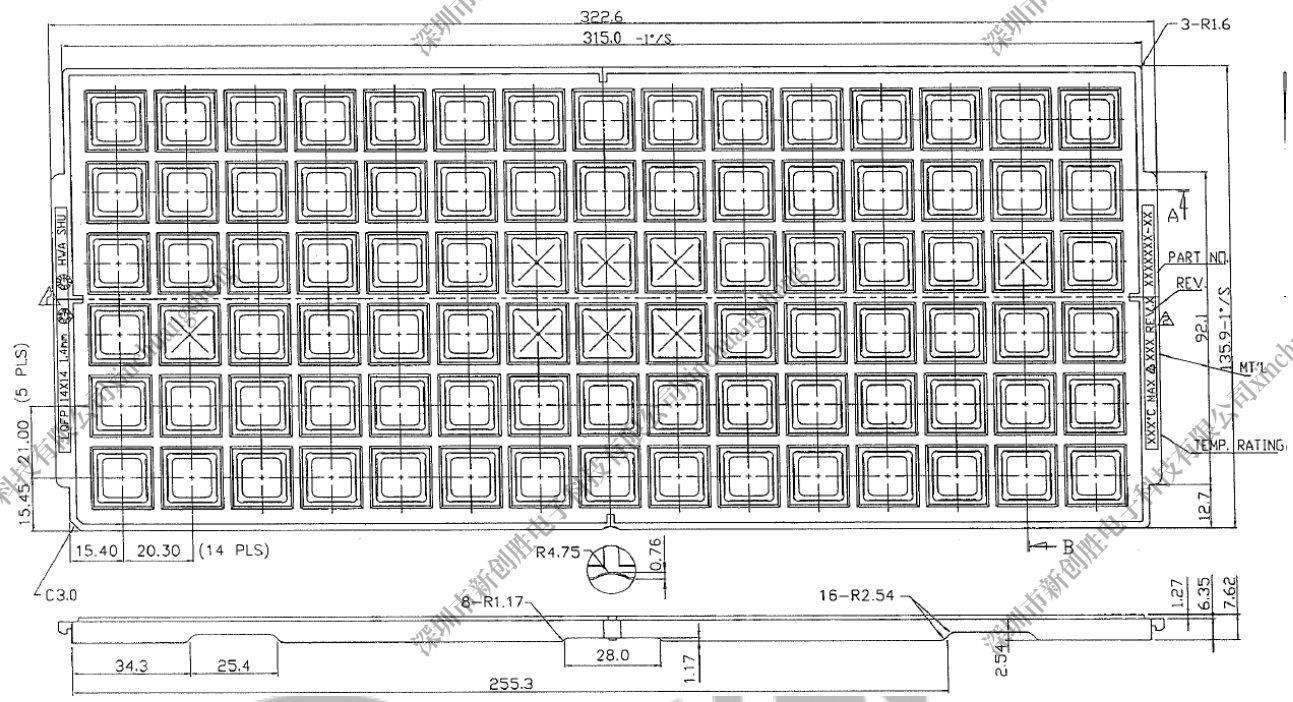
Item	Color	Size	Note
Tray	Black	322.6 mm x 135.9 mm x 7.62 mm	90 Qty/Tray
Aluminum foil bags	Silvery white	540 mm x 300 mm x 0.14 mm	Vacuum packing Including HIC and desiccant Printing: RoHS symbol
Pearl cotton cushion (Vacuum bag)	White	12 mm x 680 mm x 185 mm	
Pearl cotton cushion (The Gap between vacuum bag and inner box)	White	Left-Right: 12 mm x 180 mm x 85 mm Front-Back: 12 mm x 350 mm x 70 mm	
Inner Box	White	396 mm x 196 mm x 96 mm	Printing: RoHS symbol 10 Tray/Inner box
Carton	White	420 mm x 410 mm x 320 mm	6 Inner box/Carton

Table 8-4 eQFP Packing Quantity Information

Sample	Size	Qty/Tray	Tray/Inner Box	Full Inner Box Qty	Inner Box/Carton	Full Carton Qty
T153M4-QCX T153M3-QCX T153L3-QCX	14 mm x 14 mm	90	10	900	6	5400

The following figures show tray dimension drawing.

Figure 8-2 eQFP Tray Dimension Drawing



8.2 Storage

Reliability is affected if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

8.2.1 Moisture Sensitivity Level (MSL)

A package's MSL indicates its ability to withstand exposure after it is removed from its shipment bag, a low MSL device sample can be exposed on the factory floor longer than a high MSL device sample. Table 8-5 defines all MSL.

Table 8-5 MSL Summary

MSL	Out-of-bag floor life	Comments
1	Unlimited	≤30°C / 85%RH
2	1 year	≤30°C / 60%RH
2a	4 weeks	≤30°C / 60%RH
3	168 hours	≤30°C / 60%RH
4	72 hours	≤30°C / 60%RH
5	48 hours	≤30°C / 60%RH
5a	24 hours	≤30°C / 60%RH
6	Time on Label (TOL)	≤30°C / 60%RH

NOTE

The T153 device samples are classified as MSL3.

8.2.2 Bagged Storage Conditions

The following table defines the shelf life.

Table 8-6 Bagged Storage Conditions

Packing Mode	Vacuum packing
Storage Temperature	20-26°C
Storage Humidity	40%-60%RH
Shelf Life	12 months

8.2.3 Out-of-bag Duration

It is defined by the device MSL rating. The out-of-bag duration is as follows.

Table 8-7 Out-of-bag Duration

Storage Temperature	20-26°C
Storage Humidity	40%-60%RH
Moisture Sensitive Level (MSL)	3
Floor Life	168 hours

For no mention of storage rules in this document, refer to the latest *IPC/JEDEC J-STD-020C*.

8.3 Baking

It is not necessary to bake chips if the conditions specified in section 8.2.2 and section 8.2.3 have not been exceeded. It is necessary to bake chips if any condition specified in section 8.2.2 and section 8.2.3 has been exceeded.

It is necessary to bake chips if the storage humidity condition has been exceeded, we recommend that the device sample removed from its shipment bag for more than 2 days shall be baked to guarantee production.

Baking conditions: 125°C, 8 hours, nitrogen protection. Note that the baking should not exceed 1 times due to a risk of deformation.

9 Reflow Profile

All Allwinner chips provided for clients are lead-free RoHS-compliant products.

The reflow profile recommended in this document is a lead-free reflow profile that is suitable for pure lead-free technology of lead-free solder paste. If customers need to use lead solder paste, contact Allwinner FAE.

The following figure shows the appropriate reflow profile.

Figure 9-1 Lead-free Reflow Profile

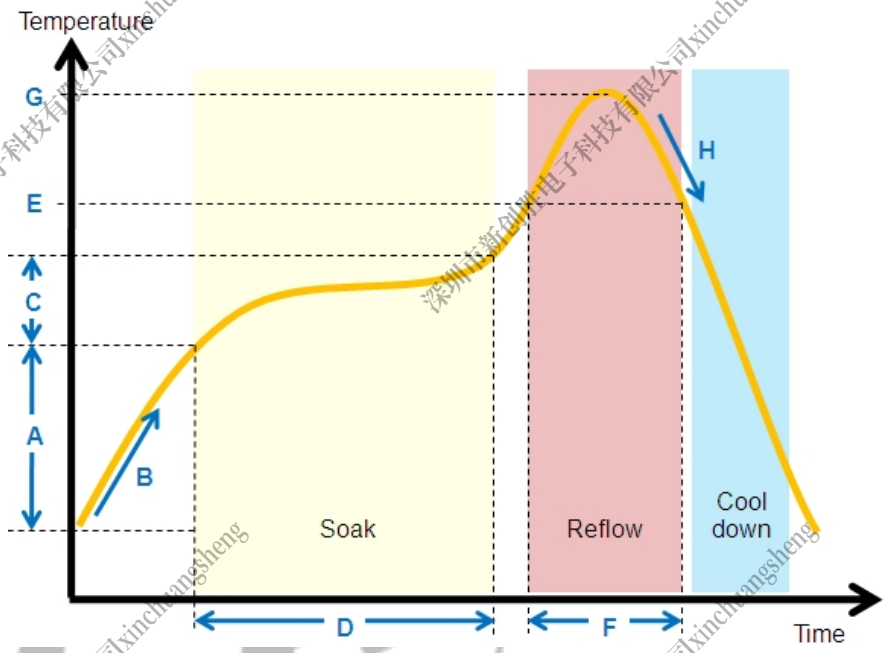


Table 9-1 Lead-free Reflow Profile Conditions

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	**Reflow condition**
Environment	N2 purge reflow usage (yes/no)	Yes, N2 purge used
	If yes, O2 ppm level	O2 < 1500 ppm
A	Preheat ramp up temperature range	25 °C -> 150 °C
B	Preheat ramp up rate	1.5–2.5 °C/s
C	Soak temperature range	150 °C -> 190 °C
D	Soak time	80–110 s
E	Liquidus temperature	217°C
F	Time above liquidus	60–90 s

	QTI typical SMT reflow profile conditions (for reference only)	
	Step	Reflow condition
G	Peak temperature	240–250 °C
H	Cool down temperature rate	⩽4°C/s

The method of measuring the reflow soldering process is as follows.

Fix the thermocouple probe of the temperature measuring line at the connection point between the pin (solderable end) of the packaged device and the pad by using high-temperature solder wire or high-temperature tape, fix the packaged device at the pad by using high-temperature tape or other methods, and cover over the thermocouple probe. See Figure 9-2.

Figure 9-2 Measuring the BGA Reflow Soldering Process

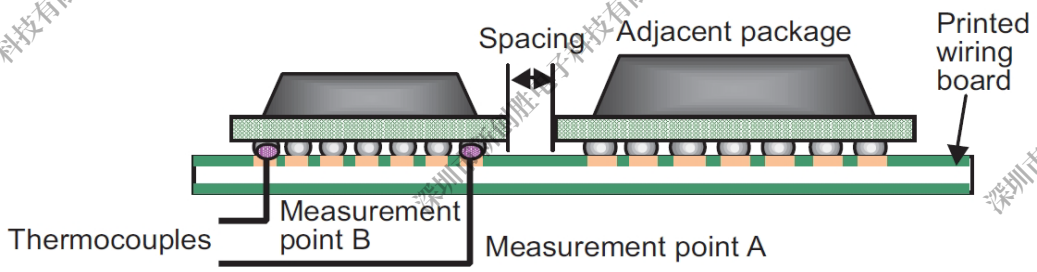
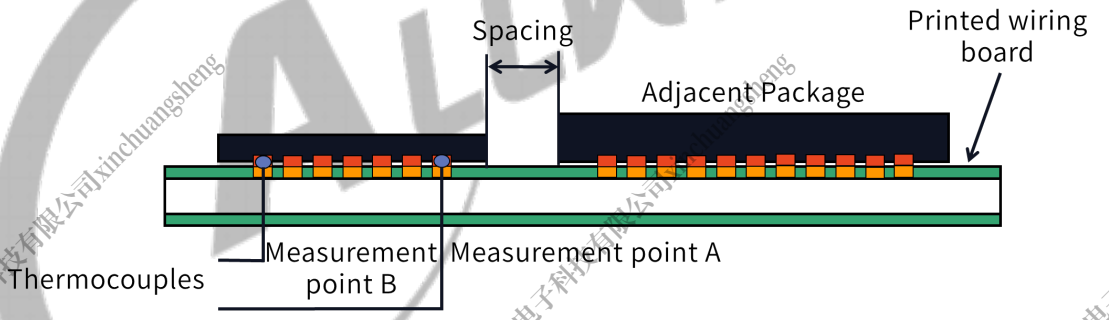


Figure 9-3 Measuring the QFP Reflow Soldering Process



If possible, the more accurate measuring way is to drill the packaged device, or drill the PCB, and fix the thermocouple probe through the drilled hole at the pad.

10 Part Marking

10.1 T153MX-BCX

The following figure shows the T153MX-BCX marking.

Figure 10-1 T153MX-BCX Marking

The following table describes the T153MX-BCX marking definitions.

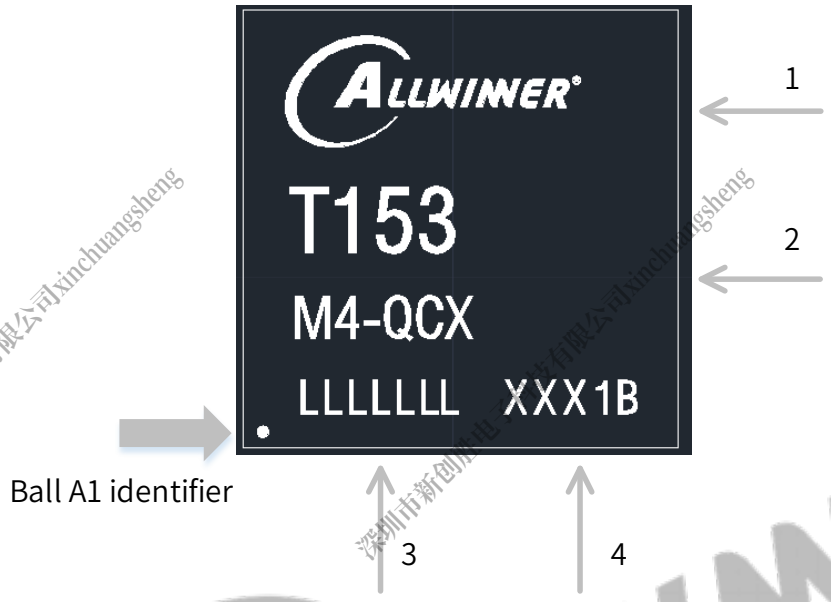
Table 10-1 T153MX-BCX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T153MX-BCX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

10.2 T153M4-QCX

The following figure shows the T153M4-QCX marking.

Figure 10-2 T153M4-QCX Marking



The following table describes the T153M4-QCX marking definitions.

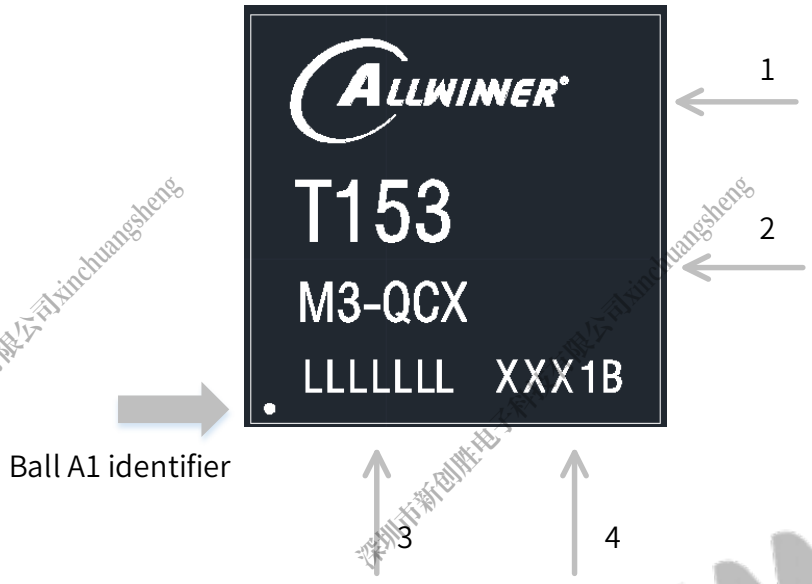
Table 10-2 T153M4-QCX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T153M4-QCX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXX1B	Date code	Dynamic

10.3 T153M3-QCX

The following figure shows the T153M3-QCX marking.

Figure 10-3 T153M3-QCX Marking



The following table describes the T153M3-QCX marking definitions.

Table 10-3 T153M3-QCX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T153M3-QCX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXX1B	Date code	Dynamic

10.4 T153L3-QXX

The following figure shows the T153L3-QXX marking.

Figure 10-4 T153L3-QXX Marking

The following table describes the T153L3-QXX marking definitions.

Table 10-4 T153L3-QXX Marking Definitions

No.	Marking	Description	Fixed/Dynamic
1	ALLWINNER	Allwinner logo or name	Fixed
2	T153L3-QXX	Product name	Fixed
3	LLLLLLL	Lot number	Dynamic
4	XXXXX	Date code	Dynamic

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