Specification

RS512M32LO4D1BDS-46IT

RS1G32LO4D2BDS-46IT

Industrial LPDDR4/4X

200-ball FBGA

Revision History

Rev	Date	Changes	Remark
V1.0	2021/10/15	Basic spec and architecture	Preliminary
V1.1	2022/6/25	Industrial Separate specifications	
V1.2	2022/12/25	Added 16Gb per Channel Refresh Requirement Parameters	
V1.3	2023/02/08	Added storage temperature	

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LPDDR4X/LPDDR4 SDRAM

RS512M32LO4D1BDS-46IT，RS1G32LO4D2BDS-46IT

Features

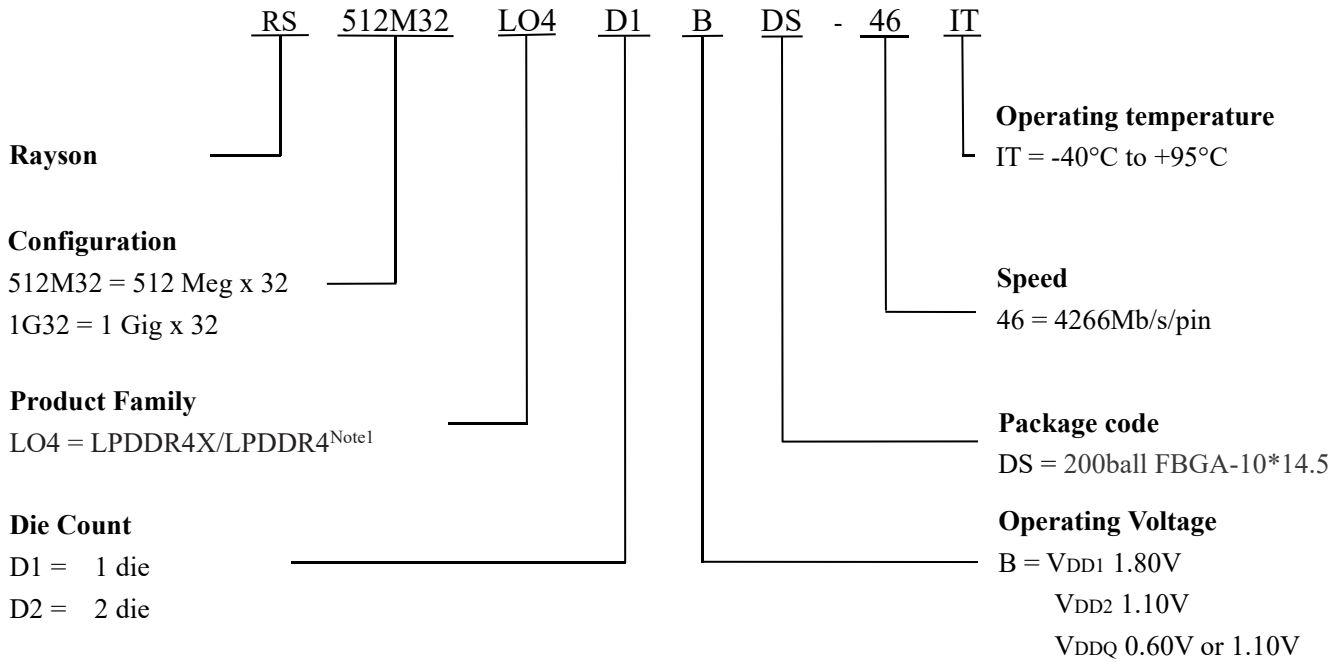
This data sheet is for LPDDR4X and LPDDR4 unified product based on LPDDR4X information. As for LPDDR4 setting, refer to General LPDDR4 Specification at the end of this datasheet.

- Ultra-low-voltage core and I/O power supplies
  - V_{DD1} = 1.70-1.95V; 1.80V nominal
  - V_{DD2} = 1.06-1.17V; 1.10V nominal
  - V_{DDQ} = 0.57-0.65V; 0.60V nominal
    Or V_{DDQ} = 1.06-1.17V; 1.10V nominal
- Frequency range
  - 2133-10 MHz (data rate range per pin:4266-20 Mb/s)
- 16 *n* prefetch DDR architecture
- 8 internal banks per channel for concurrent operation
- Single-data-rate CMD / ADR entry
- Bidirectional / differential data strobe per byte lane
- Programmable READ and WRITE latencies (RL / WL)
- Programmable and on-the-fly burst lengths (BL = 16, 32)
- Directed per-bank refresh for concurrent bank operation and ease of command scheduling
- Up to 8.53 GB / s per die x16 channel
- On-chip temperature sensor to control self refresh rate
- Partial-array self refresh (PASR)
- Selectable output drive strength (DS)
- Clock-stop capability
- RoHS-compliant, “green” packaging
- Programmable Vss(ODT) termination
- Single-ended CK and DQS support

Options	Marking
• V_{DD1}/V_{DD2}/V_{DDQ}: 1.80V/1.10V/0.60V or 1.10V	B
• Array configuration	
- 512Meg x 32 (2 channels x 16 I/O)	512M32
- 1 Gig x 32 (2 channels x 16 I/O)	1G32
• Device configuration	
- 512M32 x 1 die in package	D1
- 512M32 x 2 die in package	D2
• FBGA “green” package	
- 200-ball FBGA (10mm x14.5mm Seated height: 1.1mm MAX)	DS
• Speed grade, cycle time	
- 468ps@ RL = 36/40	-46
• Operating temperature range	
- -40°C to + 95°C	IT
• Storage temperature range	
- -55°C to + 125°C	

Part Number Ordering Information

Figure 1: Part Number Chart



Note1: LPDDR4X: V_{DDQ}=0.60V; LPDDR4: V_{DDQ}=1.10V;

Table 1:Key Timing Parameters

Speed Grade	Clock Rate (MHz)	Data Rate (Mb/s/pin)	WRITE Latency		READ Latency	
			Set A	Set B	DBI Disabled	DBI Enabled
-46	2133	4266	18	34	36	40

Table 2: Part Number List

Part Number	Total Density	Data Rate	Operating temperature
RS512M32LO4D1BDS-46IT	2GB(16Gb)	4266 Mb/s/pin	-40°C to + 95°C
RS1G32LO4D2BDS-46IT	4GB(32Gb)	4266 Mb/s/pin	-40°C to + 95°C

Contents

Product Specification

General Description

The 16Gb mobile low-power DDR4 SDRAM with low V_{DDQ} (LPDDR4X) is a high-speed,CMOS dynamic random-access memory device. This device is internally configured with 2 channels or 1 channel ×16 I/O, each channel having 8-banks.

General Notes

Throughout the data sheet, figures and text refer to DQs as DQ. DQ should be interpreted as any or all DQ collectively, unless stated otherwise.

DQS and CK should be interpreted as DQS_t, DQS_c and CK_t, CK_c respectively, unless stated otherwise. CA includes all CA pins used for a given density.

In timing diagrams, CMD is used as an indicator only. Actual signals occur on CA[5:0].

V_{REF} indicates V_{REFCA} and V_{REFDQ}.

Complete functionality may be described throughout the entire document. Any page or diagram may have been simplified to convey a topic and may not be inclusive of all requirements.

Any specific requirement takes precedence over a general statement.
Any functionality not specifically stated herein is considered undefined, illegal, not supported, and will result in unknown operation.

For single-ended CK and DQS features or specifications, refer to the LPDDR4X SingleEnded CK and DQS Addendum.

Device Configuration

Table 3: Device Configuration

		512M32 (16Gb/package)	1G32 (32Gb/package)
Die Organization in the package	Channel A, rank 0	x16 mode × 1 die (dual channel)	x16 mode × 1 die (dual channel)
	Channel B, rank 0		
	Channel A, rank 1	-	x16 mode × 1 die (dual channel)
	Channel B, rank 1		
Die addressing	Dual/single Die	16Gb dual-channel die	16Gb dual-channel die
	Memory density (per die)	16Gb	16Gb
	Memory density (per channel)	8Gb	8Gb
	Configuration	64Mb × 16 DQ × 8 banks × 2 channels	64Mb × 16 DQ × 8 banks × 2 channels
	Number of channels (per die)	2	2
	Number of banks (per channel)	8	8
	Array prefetch (bits, per channel)	256	256
	Number of rows (per channel)	65,336	65,336
	Number of columns (fetch boundaries)	64	64
	Page size (bytes)	2048	2048
	Channel density (bits per channel)	8,589,934,592	8,589,934,592
	Total density (bits per die)	17,179,869,184	17,179,869,184
	Bank address	BA[2:0]	BA[2:0]
	Row address	R[15:0]	R[15:0]
	Column address	C[9:0]	C[9:0]
	Burst starting address boundary	64-bit	64-bit

Note: 1.Refer to Package Block Diagram section in Product Specification and SDRAM Addressing section in General LPDDR4X specification.

Refresh Requirement Parameters

Table 4: Refresh Requirement Parameters

Parameter	Symbol	8Gb Per Channel	unit
REFRESH cycle time (all banks)	^{t}RFCab	280	ns
REFRESH cycle time (per bank)	^{t}RFCpb	140	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	ns

Note: 1. This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.

Table 5: Refresh Requirement Parameters – 16Gb per Channel

Parameter	Symbol	16Gb Per Channel	unit
REFRESH cycle time (all banks)	^{t}RFCab	380	ns
REFRESH cycle time (per bank)	^{t}RFCpb	190	ns
Per bank refresh to per bank refresh time (different bank)	^{t}PBR2PBR	90	ns

Note: 1. This table only describes refresh parameters which are density dependent. Refer to Refresh Requirement section in General LPDDR4X specification for all the refresh parameters.

Package Block Diagrams

Figure 2: Single-Die, Dual-Channel Package Block Diagram

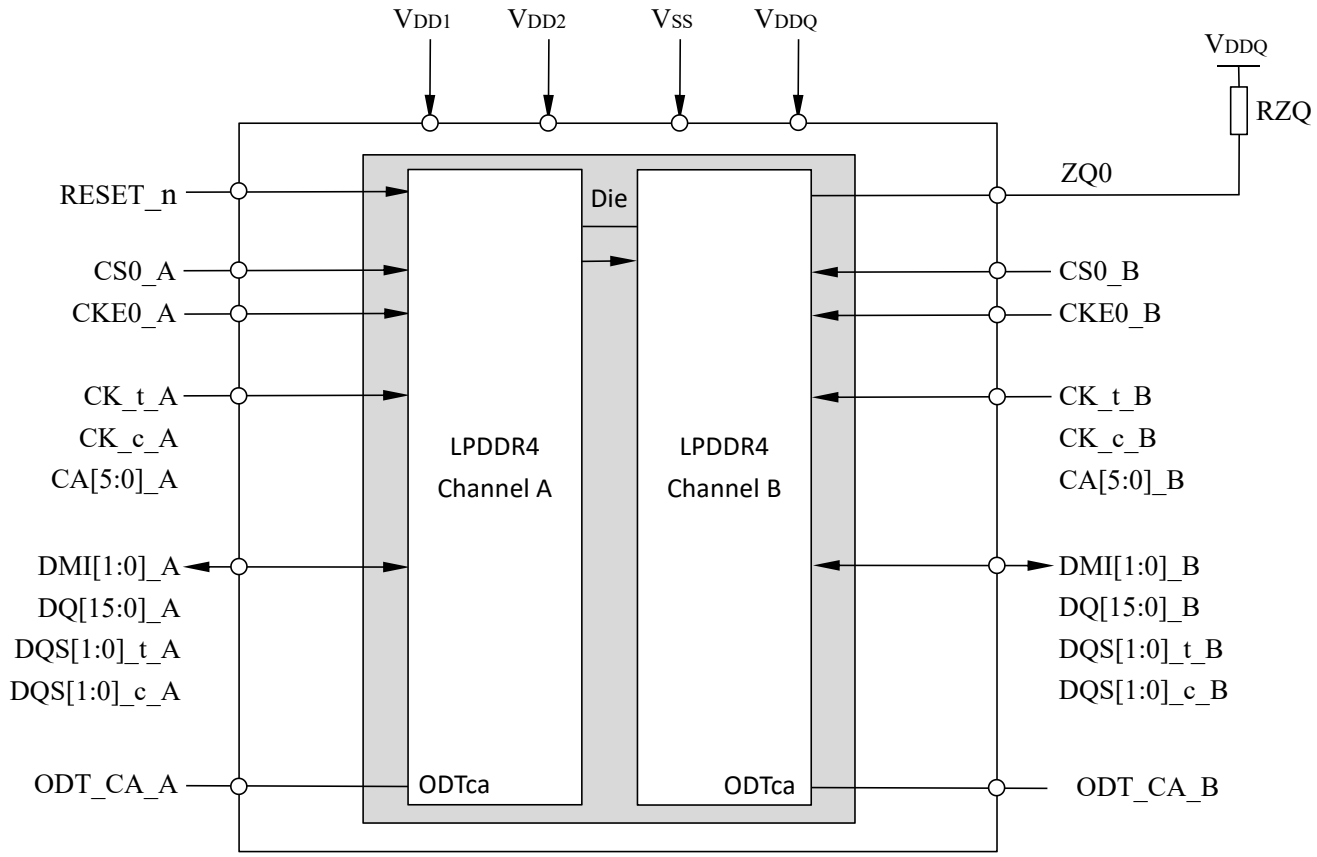
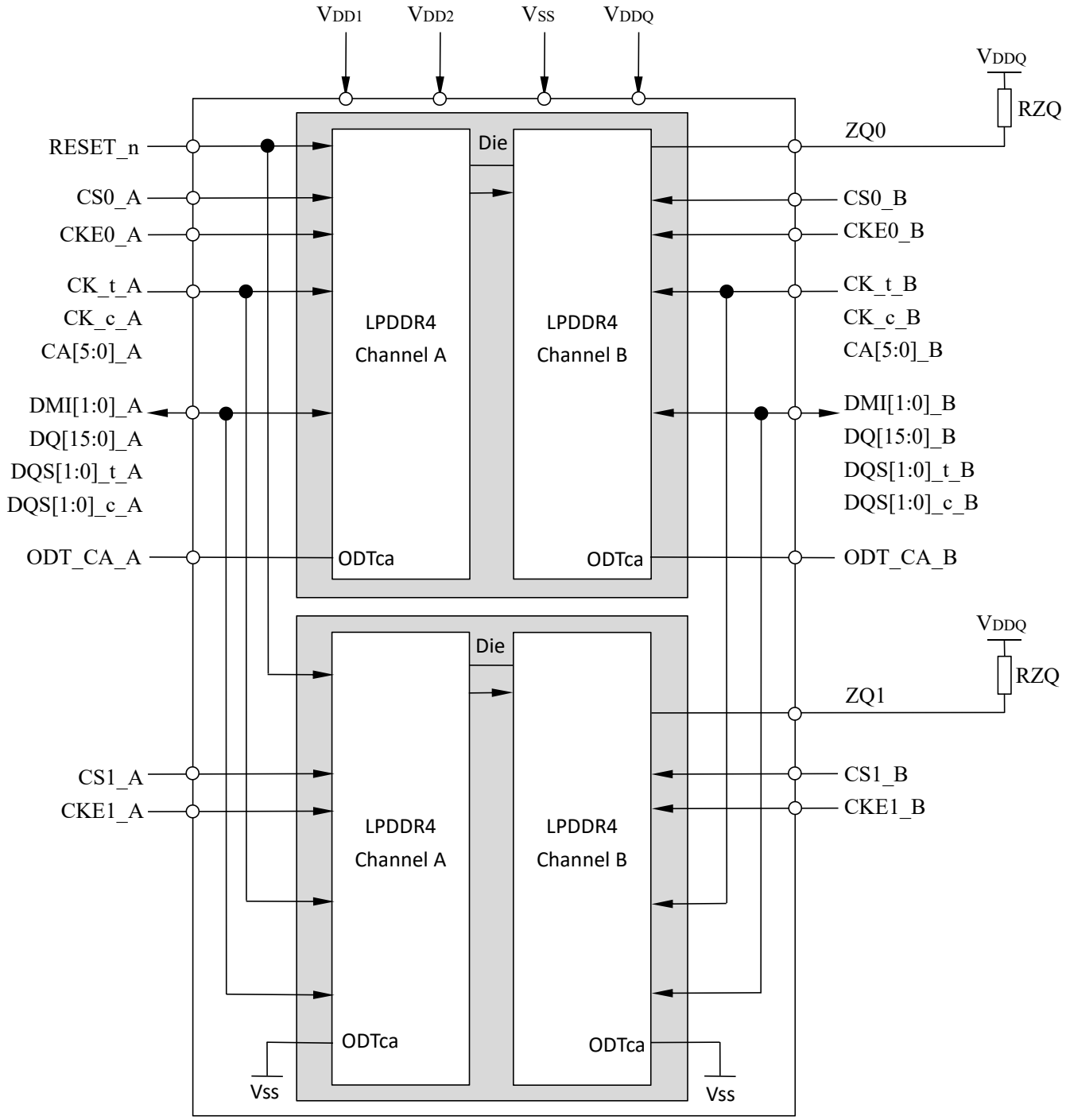


Figure 3:Dual-Die, Dual-Channel Package Block Diagram



Ball Assignments and Descriptions Single-Rank

Figure 4: 200-Ball Dual-Channel, Single-Rank Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			NC	VDD2	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMIO_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_A	NC	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	VSS	CKE0_A	NC			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	NC			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	NC	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_c_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_c_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_t_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	DNU	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

Top View (ball down)

LPDDR4_A(Channel A） LPDDR4_B(Channel B） ZQ,ODT_CA,RESET Supply Ground

Ball Assignments and Descriptions Dual-Rank

Figure 5: 200-Ball Dual-Channel, Dual-Rank Discrete FBGA

	1	2	3	4	5	6	7	8	9	10	11	12
A	DNU	DNU	V_{SS}	V_{DD2}	ZQ0			ZQ1	VDD2	V_{SS}	DNU	DNU
B	DNU	DQ0_A	V_{DDQ}	DQ7_A	V_{DDQ}			V_{DDQ}	DQ15_A	V_{DDQ}	DQ8_A	DNU
C	V_{SS}	DQ1_A	DMIO_A	DQ6_A	V_{SS}			V_{SS}	DQ14_A	DMI1_A	DQ9_A	V_{SS}
D	V_{DDQ}	V_{SS}	DQS0_t_A	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_A	V_{SS}	V_{DDQ}
E	V_{SS}	DQ2_A	DQS0_c_A	DQ5_A	V_{SS}			V_{SS}	DQ13_A	DQS1_c_A	DQ10_A	V_{SS}
F	V_{DD1}	DQ3_A	V_{DDQ}	DQ4_A	V_{DD2}			V_{DD2}	DQ12_A	V_{DDQ}	DQ11_A	V_{DD1}
G	V_{SS}	ODT_CA_A	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	NC	V_{SS}
H	V_{DD2}	CA0_A	CS1_A	CS0_A	V_{DD2}			V_{DD2}	CA2_A	CA3_A	CA4_A	V_{DD2}
J	V_{SS}	CA1_A	VSS	CKE0_A	CKE1_A			CK_t_A	CK_c_A	V_{SS}	CA5_A	V_{SS}
K	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
L												
M												
N	V_{DD2}	V_{SS}	V_{DD2}	V_{SS}	NC			NC	V_{SS}	V_{DD2}	V_{SS}	V_{DD2}
P	V_{SS}	CA1_B	V_{SS}	CKE0_B	CKE1_B			CK_t_B	CK_c_B	V_{SS}	CA5_B	V_{SS}
R	V_{DD2}	CA0_B	CS1_B	CS0_B	V_{DD2}			V_{DD2}	CA2_B	CA3_B	CA4_B	V_{DD2}
T	V_{SS}	ODT_CA_B	V_{SS}	V_{DD1}	V_{SS}			V_{SS}	V_{DD1}	V_{SS}	RESET_n	V_{SS}
U	V_{DD1}	DQ3_B	V_{DDQ}	DQ4_B	V_{DD2}			V_{DD2}	DQ12_B	V_{DDQ}	DQ11_B	V_{DD1}
V	V_{SS}	DQ2_B	DQS0_c_B	DQ5_B	V_{SS}			V_{SS}	DQ13_B	DQS1_c_B	DQ10_B	V_{SS}
W	V_{DDQ}	V_{SS}	DQS0_t_B	V_{SS}	V_{DDQ}			V_{DDQ}	V_{SS}	DQS1_t_B	V_{SS}	V_{DDQ}
Y	V_{SS}	DQ1_B	DMI0_B	DQ6_B	V_{SS}			V_{SS}	DQ14_B	DMI1_B	DQ9_B	V_{SS}
AA	DNU	DQ0_B	V_{DDQ}	DQ7_B	V_{DDQ}			V_{DDQ}	DQ15_B	V_{DDQ}	DQ8_B	DNU
AB	DNU	DNU	V_{SS}	V_{DD2}	V_{SS}			V_{SS}	V_{DD2}	V_{SS}	DNU	DNU
	1	2	3	4	5	6	7	8	9	10	11	12

Top View (ball down)

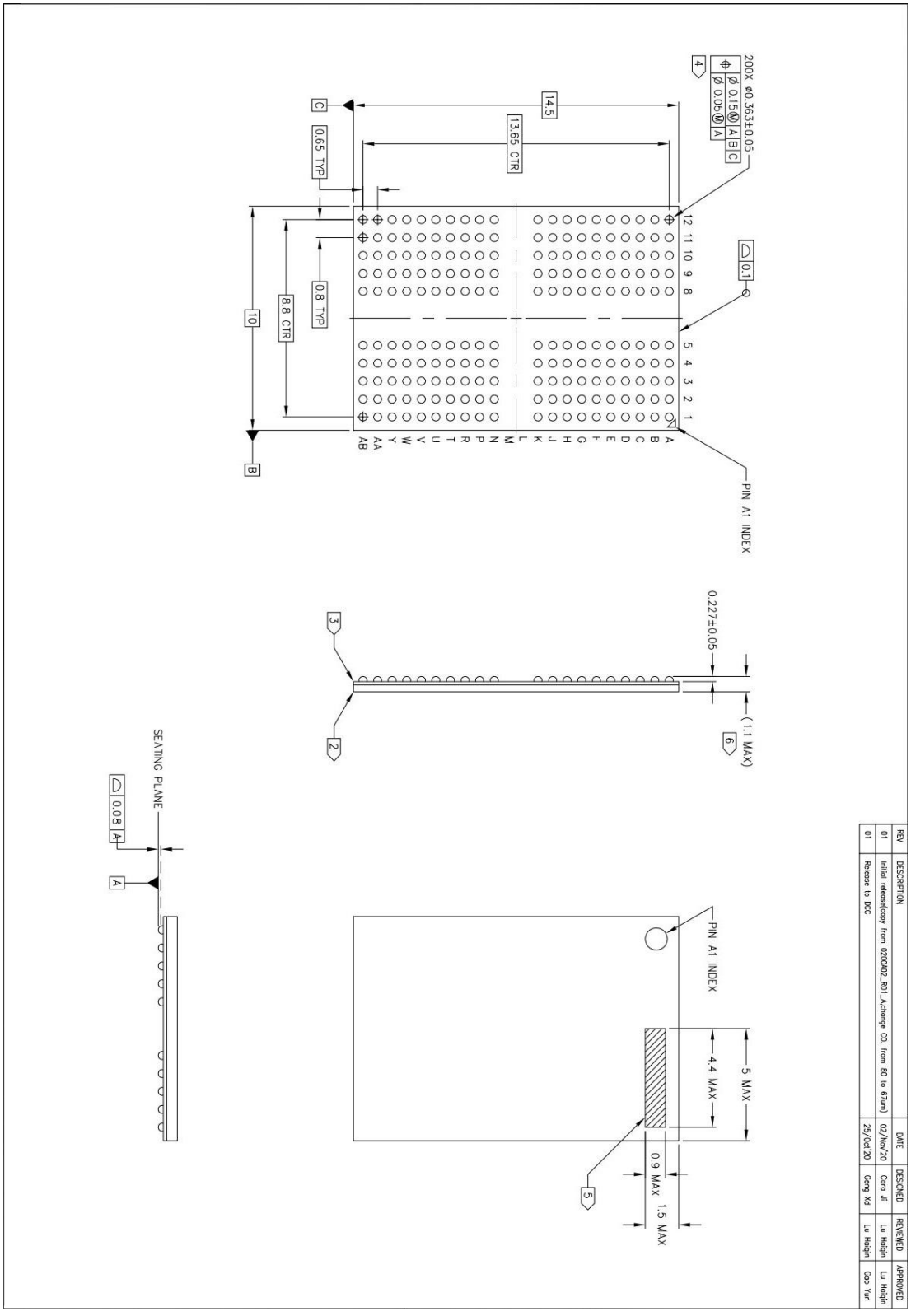
LPDDR4_A(Channel A） LPDDR4_B(Channel B） ZQ,ODT_CA,RESET Supply Ground

Table 5: Ball/Pad Descriptions

Symbol	Type	Description
CK_t_A, CK_c_A CK_t_B, CK_c_B	Input	**Clock:** CK_t and CK_c are differential clock inputs. All address, command and control input signals are sampled on positive edge of CK_t and the negative edge of CK_c.AC timings for CA parameters are referenced to clock. Each channel (A, B) has its own clock pair.
CKE0_A,CKE1_A CKE0_B,CKE1_B	Input	**Clock enable:** CKE HIGH activates and CKE LOW deactivates the internal clock signals, input buffers, and output drivers. Power-saving modes are entered and exited via CKE transitions. CKE is sampled at the rising edge of CK.
CS0_A, CS1_A CS0_B, CS1_B	Input	**Chip select:** Each channel (A, B) has its own CS signals.
CA[5:0]_A CA[5:0]_B	Input	**Command/address inputs:** Provide the command and address inputs according to the command truth table. Each channel (A, B) has its own CA signals.
ODT_CA_A ODT_CA_B	Input	**LPDDR4X CA ODT Control:** The ODT_CA pin is ignored by LPDDR4X devices. CA ODT is fully controlled through MR11 and MR22. The ODT_CA pin shall be connected to a valid logic level.
DQ[15:0]_A DQ[15:0]_B	I/O	**Data input/output:** Bidirectional data bus.
DQS[1:0]_t_A DQS[1:0]_c_A DQS[1:0]_t_B DQS[1:0]_c_B	I/O	**Data strobe:** DQS_t and DQS_c are bidirectional differential output clock signals used to strobe data during a READ or WRITE. The data strobe is generated by the DRAM for a READ and is edge-aligned with data. The data strobe is generated by the SoC memory controller for a WRITE and is trained to precede data. Each byte of data has a data strobe signal pair. Each channel (A, B) has its own DQS_t and DQS_c strobes.
DMI[1:0]_A DMI[1:0]_B	I/O	**Data mask/Data bus inversion:** DMI is a dual use bidirectional signal used to indicate data to be masked, and data which is inverted on the bus. For data bus inversion(DBI), the DMI signal is driven HIGH when the data on the data bus is inverted, or driven LOW when the data is in its normal state. DBI can be disabled via a mode register setting. For data mask, the DMI signal is used in combination with the data lines to indicate data to be masked in a MASK WRITE command (see the Data Mask (DM) and Data Bus Inversion (DBI) sections for details). The data mask function can be disabled via a mode register setting. Each byte of data has a DMI signal. Each channel has its own DMI signals.
ZQ0, ZQ1	Reference	**ZQ calibration reference:** Used to calibrate the output drive strength and the termination resistance. The ZQ pin shall be connected to V_{DDQ} through a 240Ω ±1% resistor.
VDDQ, VDD1, VDD2	Supply	**Power supplies:** Isolated on the die for improved noise immunity.
Vss	Supply	**Ground reference:** Power supply ground reference.
RESET_n	Input	**RESET:** When asserted LOW, the RESET pin resets all channels of the die.
DNU	–	**Do not use:** Must be grounded or left floating.
NC	–	**No connect:** Not internally connected.

Package Dimensions

Figure 6: 200-Ball FBGA – 10mm x 14.5mm (Package Code: DS)



Product Specific Mode Register definition

Table 6: Mode Register Contents

Notes 1 and 2 apply to entire table.

Mode Register	OP7	OP6	OP5	OP4	OP3	OP2	OP1	OP0
MR0			Single-ended mode			RFM support	Latency mode	REF
	OP[0] = 0b: Both legacy and modified refresh mode supported OP[1] = 0b: Device supports normal latency OP[2] = 0b: Device supports TRR OP[5] = 1b: Device supports single-ended mode							
MR3						PPRP[3]		
	OP[2] = 0b:PPR protection disabled (default); 1b: PPR protection enabled;							
MR5	Manufacturer ID							
	1111 1111b : Micron							
MR6	Revision ID1							
	0000 0111b							
MR8	I/O width		Density					
	OP[7:6] = 00b:x16/channel		OP[5:2] = 0100b: 16Gb dual-channel die OP[5:2] = 0110b: 16Gb single-channel die					
MR13						VRO		
	OP[2] = 0b: Normal operation (default); 1b: Output the $V_{REF(CA)}$ value on DQ7 and $V_{REF(DQ)}$ value on DQ6							
MR24	TRR mode				Unlimited MAC	MAC value		
	OP[3:0] = 1000b: Unlimited MAC; OP[7] = 0b: Disable (default); 1b: Reserved;							
MR25	PPR resources[4]							
	Bank7	Bank6	Bank5	Bank4	Bank3	Bank2	Bank1	Bank0
	0b: PPR resource is not available; 1b: PPR resource is available							

Notes: 1. The contents of Product Specific Mode Register definition will reflect information specific to each die in these packages.

2. Other bits not defined above and other mode registers are referred to Mode Register Assignments and Definitions section.

3. When not using PPR function, PPR protection should be enabled to prevent unintended PPR entry (MR3 OP[2] = 1b).

4.Before using PPR function, confirm the availability of PPR resource by reading MR25.

LPDDR4X I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section for detailed conditions.

Table 7-1: LPDDR4X I_{DD} Parameters – Single Die (16Gb Dual-Channel Die)

V_{DD2} = 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V;

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
IDD01	VDD1	8.40	mA	
IDD02	VDD2	59.00		
IDD0Q	VDDQ	1.50		
IDD2P1	VDD1	2.40	mA	
IDD2P2	VDD2	5.40		
IDD2PQ	VDDQ	1.50		
IDD2PS1	VDD1	2.40	mA	
IDD2PS2	VDD2	5.40		
IDD2PSQ	VDDQ	1.50		
IDD2N1	VDD1	2.40	mA	
IDD2N2	VDD2	33.00		
IDD2NQ	VDDQ	1.50		
IDD2NS1	VDD1	2.40	mA	
IDD2NS2	VDD2	25.00		
IDD2NSQ	VDDQ	1.50		
IDD3P1	VDD1	2.40	mA	
IDD3P2	VDD2	9.80		
IDD3PQ	VDDQ	1.50		
IDD3PS1	VDD1	2.40	mA	
IDD3PS2	VDD2	9.80		
IDD3PSQ	VDDQ	1.50		
IDD3N1	VDD1	3.40	mA	
IDD3N2	VDD2	44.00		
IDD3NQ	VDDQ	1.50		
IDD3NS1	VDD1	3.40	mA	
IDD3NS2	VDD2	36.00		
IDD3NSQ	VDDQ	1.50		

Table 7-2: LPDDR4X IDD Parameters – Single Die (16Gb Dual-Channel Die) (Continued)

V_{DD2} = 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V;

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
I_{DD4R1}	V_{DD1}	15.00	mA	2,3
I_{DD4R2}	V_{DD2}	400.00		
I_{DD4RQ}	V_{DDQ}	126.10		
I_{DD4W1}	V_{DD1}	15.00	mA	2
I_{DD4W2}	V_{DD2}	300.00		
I_{DD4WQ}	V_{DDQ}	1.50		
I_{DD51}	V_{DD1}	35.00	mA	
I_{DD52}	V_{DD2}	195.00		
I_{DD5Q}	V_{DDQ}	1.50		
I_{DD5AB1}	V_{DD1}	7.80	mA	
I_{DD5AB2}	V_{DD2}	41.00		
I_{DD5ABQ}	V_{DDQ}	1.50		
I_{DD5PB1}	V_{DD1}	6.70	mA	
I_{DD5PB2}	V_{DD2}	41.00		
I_{DD5PBQ}	V_{DDQ}	1.50		

Notes:

1. Published I_{DD} values except I_{DD4RQ} are the maximum I_{DD} values considering the worst-case conditions of process, temperature, and voltage.

2. BL = 16, DBI disabled.

3. I_{DD4RQ} value is reference only. Typical value. V_{OH} = 0.5 × V_{DDQ}; T_C = 25°C

4. I_{DD} values reflect dual-channel operation with the same pattern for each channel.

Table 8: I_{DD6} Full-Array Self Refresh Current – Single Die (16Gb Dual-Channel Die)

V_{DD2} = 1.06–1.17V; V_{DDQ} = 0.57–0.65V; V_{DD1} = 1.70–1.95V;

Temperature	Supply	Full-Array Self	Unit
25°C	V_{DD1}	0.65	mA
	V_{DD2}	1.33	
	V_{DDQ}	0.02	
95°C	V_{DD1}	6.50	mA
	V_{DD2}	18.00	
	V_{DDQ}	1.50	

Notes:

1. *I_{DD6} 25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6} 95°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.*
2. *I_{DD} values reflect dual-channel operation with the same pattern for each channel.*

LPDDR4 I_{DD} Parameters

Refer to I_{DD} Specification Parameters and Test Conditions section for detailed conditions.

Table 9-1: LPDDR4 I_{DD} Parameters – Single Die (16Gb Dual-Channel Die)

V_{DD2} = 1.06–1.17V; V_{DDQ} =1.06–1.17V; V_{DD1} = 1.70–1.95V;

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
I_{DD01}	V_{DD1}	8.40	mA	
I_{DD02}	V_{DD2}	59.00		
I_{DD0Q}	V_{DDQ}	1.50		
I_{DD2P1}	V_{DD1}	2.40	mA	
I_{DD2P2}	V_{DD2}	5.40		
I_{DD2PQ}	V_{DDQ}	1.50		
I_{DD2PS1}	V_{DD1}	2.40	mA	
I_{DD2PS2}	V_{DD2}	5.40		
I_{DD2PSQ}	V_{DDQ}	1.50		
I_{DD2N1}	V_{DD1}	2.40	mA	
I_{DD2N2}	V_{DD2}	33.00		
I_{DD2NQ}	V_{DDQ}	1.50		
I_{DD2NS1}	V_{DD1}	2.40	mA	
I_{DD2NS2}	V_{DD2}	25.00		
I_{DD2NSQ}	V_{DDQ}	1.50		
I_{DD3P1}	V_{DD1}	2.40	mA	
I_{DD3P2}	V_{DD2}	9.80		
I_{DD3PQ}	V_{DDQ}	1.50		
I_{DD3PS1}	V_{DD1}	2.40	mA	
I_{DD3PS2}	V_{DD2}	9.80		
I_{DD3PSQ}	V_{DDQ}	1.50		
I_{DD3N1}	V_{DD1}	3.40	mA	
I_{DD3N2}	V_{DD2}	44.00		
I_{DD3NQ}	V_{DDQ}	1.50		
I_{DD3NS1}	V_{DD1}	3.40	mA	
I_{DD3NS2}	V_{DD2}	36.00		
I_{DD3NSQ}	V_{DDQ}	1.50		

Table 9-2: LPDDR4 IDD Parameters – Single Die (16Gb Dual-Channel Die) (Continued)

V_{DD2} = 1.06–1.17V; V_{DDQ} =1.06–1.17V; V_{DD1} = 1.70–1.95V;

Symbol	Supply	Speed Grade	Unit	Note
		4266 Mb/s		
IDD4R1	VDD1	15.00	mA	2,3
IDD4R2	VDD2	400.00		
IDD4RQ	VDDQ	187.80		
IDD4W1	VDD1	15.00	mA	2
IDD4W2	VDD2	300.00		
IDD4WQ	VDDQ	1.50		
IDD51	VDD1	35.00	mA	
IDD52	VDD2	195.00		
IDD5Q	VDDQ	1.50		
IDD5AB1	VDD1	7.80	mA	
IDD5AB2	VDD2	41.00		
IDD5ABQ	VDDQ	1.50		
IDD5PB1	VDD1	6.70	mA	
IDD5PB2	VDD2	41.00		
IDD5PBQ	VDDQ	1.50		

Notes:

1. Published IDD values except IDD4RQ are the maximum IDD values considering the worst-case conditions of process, temperature, and voltage.

2. BL = 16, DBI disabled.

3. IDD4RQ value is reference only. Typical value. V_{OH} = 0.5 × V_{DDQ}; T_C = 25°C

4. IDD values reflect dual-channel operation with the same pattern for each channel.

Table 10: I_{DD6} Full-Array Self Refresh Current – Single Die (16Gb Dual-Channel Die)

V_{DD2} = 1.06–1.17V; V_{DDQ} =1.06–1.17V; V_{DD1} = 1.70–1.95V;

Temperature	Supply	Full-Array Self	Unit
25°C	V_{DD1}	0.65	mA
	V_{DD2}	1.33	
	V_{DDQ}	0.02	
95°C	V_{DD1}	6.50	mA
	V_{DD2}	18.00	
	V_{DDQ}	1.50	

Notes: 1.I_{DD6} 25°C is the typical value in the distribution with nominal V_{DD} and a reference-only value. I_{DD6} 95°C is the maximum I_{DD} guaranteed value considering the worst-case conditions of process, temperature, and voltage.

2.I_{DD} values reflect dual-channel operation with the same pattern for each channel.