16-Bit ADC with On-board Reference

PRODUCT DESCRIPTION

The MS1100 is a precision, continuously self-calibrating ADC up to 16 bits resolution. The on-board reference provides a differential input range of ±2.048V. The MS1100 uses an I²C serial interface.

The MS1100 operates from a single power supply ranging from 2.7V to 5.5V. The MS1100 can perform conversions at rates of 15, 30, 60 or 240 samples per second (SPS). In single-conversion mode, the MS1100 automatically powers down after a conversion, greatly reducing current consumption during idle periods.

The MS1100 is designed for applications requiring high resolution measurement, where space and power consumption are major considerations.

SOT23-6

FEATURES

- I²C Serial Interface
- On-board Reference: Accuracy: 2.048V ±0.5% ; Drift:10ppm/°C
- On-board PGA and OSC
- 16 bits Resolution
- INL: 0.01% of FSR Max
- I²C Address Number:8
- Programmable Data Rate: 15SPS to 240SPS
- Power Supply: 2.7V to 5.5V
- Low Current Consumption: 315μA

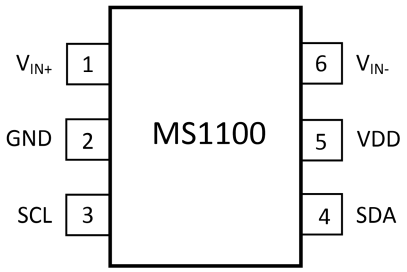
APPLICATIONS

- Portable Instrumentation
- Industrial Process Control
- Smart Transmitters
- Consumer Goods
- Factory Automation
- Temperature Measurement

PRODUCT SPECIFICATION

Part Number	I²C Address	Range	Package	Marking
MS1100	1001 000	00	SOT23-6	1100
MS1100	1001 001	01	SOT23-6	1100
MS1100	1001 010	02	SOT23-6	1100
MS1100	1001 011	03	SOT23-6	1100
MS1100	1001 100	04	SOT23-6	1100
MS1100	1001 101	05	SOT23-6	1100
MS1100	1001 110	06	SOT23-6	1100
MS1100	1001 111	07	SOT23-6	1100

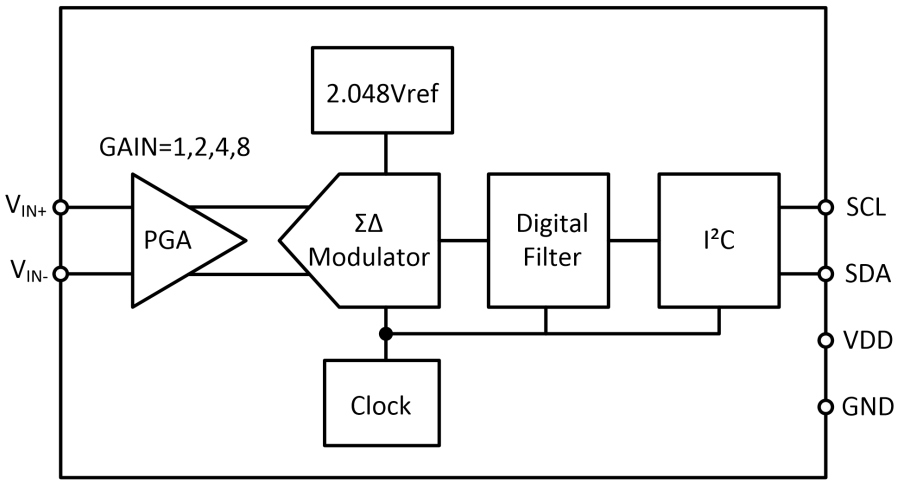
PIN CONFIGURATION



PIN DESCRIPTION

Pin	Symbol	Type	Description
1	VIN+	I	Differential Channel : Positive Input
2	GND	--	Ground
3	SCL	I	Serial Clock Input: Clocks Output Data on SDA
4	SDA	I/O	Serial Data: Transmits and Receives Data
5	VDD	--	Power Supply
6	VIN-	I	Differential Channel : Negative Input

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Any exceeding absolute maximum rating application causes permanent damage to device. Because long-time absolute operation state affects device reliability. Absolute ratings just conclude from a series of extreme tests. It doesn't represent chip can operate normally in these extreme conditions.

Symbol	Parameter	Ratings	Unit
Power Supply	VDD	-0.3 ~ 6	V
Input Current	IIN	100mA, Momentary	mA
Input Current	IIN	10mA, Continuous	mA
Analog Inputs (A0,A1 to GND)	VIN	-0.3 ~ VDD+0.3	V
SDA,SCL Voltage to GND	V	-0.5 ~ 6	V
Maximum Junction Temperature	T	150	°C
Operating Temperature Range	TA	-40 ~ 125	°C
Storage Temperature Range	Tstg	-60 ~ 150	°C
Lead Temperature (Soldering, 10s)	T	260	°C

ELECTRICAL CHARACTERISTICS

VDD=5.0V, TA = -40 to 85°C, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Unit
Analog Input					
Full-Scale Input Voltage	(VIN+)-(VIN-)		±2.048/PGA		V
Analog Input Voltage	VIN+ to GND, VIN- to GND	GND-0.2		VDD+0.2	V
Differential Input Impedance			2.8/PGA		MΩ
Common-Mode Input Impedance	PGA=1		3.5		MΩ
	PGA=2		3.5		MΩ
	PGA=4		1.8		MΩ
	PGA=8		0.9		MΩ
System Performance					
Resolution and No Missing Codes	DR=00	12		12	Bits
	DR=01	14		14	Bits
	DR=10	15		15	Bits
	DR=11	16		16	Bits
Data Rate	DR=00	180	240	308	SPS
	DR=01	45	60	77	SPS
	DR=10	22	30	39	SPS
	DR=11	11	15	20	SPS
Integral Nonlinearity	DR=11,PGA=1, End Point Fit [1]		±0.004	±0.010	% of FSR[2]
Offset Error	PGA=1		8	15	mV
	PGA=2		8	15	mV
	PGA=4		8	15	mV
	PGA=8		8	15	mV
Offset Drift	PGA=1		1.2		uV/°C
	PGA=2		0.6		uV/°C
	PGA=4		0.3		uV/°C
Offset vs VDD	PGA=8		0.3		uV/°C
	PGA=1		800		uV/V
	PGA=2		400		uV/V
	PGA=4		200		uV/V
	PGA=8		150		uV/V
Gain Error			0.05	0.4	%
Channel Offset Match [3]	Match between any two channels		0.02	0.1	%

Parameter	Condition	Min	Typ	Max	Unit
System Performance					
Gain Error Drift			10		ppm/°C
Gain vs VDD			80		ppm/V
Common-Mode Rejection	At DC and PGA=8	95	105		dB
	At DC and PGA=1		100		dB
Digital Input/Output					
VIH		0.7×VDD		6	V
VIL		GND-0.5		0.3×VDD	V
VOL	IOL=3mA	GND		0.4	V
Input Leakage,IH				10	uA
Input Leakage,IL		-10			uA
Power Supply Requirements					
Power-Supply Voltage	VDD	2.7		5.5	V
Supply Current	Power-Down		0.05	2	uA
	Active Mode		315	350	uA
Power Dissipation	VDD=5.0V		1.6	1.9	mW
	VDD=3.0V		0.96		mW

Note：

1. 99% of full-scale.
2. FSR = full-scale range = 2 × 2.048V/PGA = 4.096V/PGA.
3. Includes all errors from on-board PGA and reference.

FUNCTION DESCRIPTION

The MS1100 is a 16-bit, self-calibrating, delta-sigma A/D converter. The MS1100 consists of a delta-sigma A/D converter core with adjustable gain, a 2.048V reference, a clock oscillator, and an I^2C interface. Each of these blocks are described in detail in the sections that follow.

Analog-to-Digital Converter

The MS1100 A/D converter core consists of a differential switched-capacitor delta-sigma modulator followed by a digital filter. The modulator measures the voltage difference between the positive and negative analog inputs and compares it to a reference voltage, which, in the MS1100, is 2.048V. The digital filter receives a high-speed bit stream from the modulator and outputs a code, which is a number proportional to the input voltage.

Voltage Reference

The MS1100 contains an onboard 2.048V voltage reference. This reference is used as the ADC voltage reference; an external reference cannot be connected. The MS1100 voltage reference is internal only, and cannot be measured directly or used by external circuitry. The onboard reference specifications are part of the overall gain and drift specifications of the MS1100. The converter drift and gain error specifications reflect the performance of the onboard reference as well as the performance of the A/D converter core. There are no separate specifications for the on-board reference itself.

Output Code Calculation

The output code is a scaled value that is proportional, except for clipping, to the voltage difference between the two analog inputs. The output code is confined to a finite range of numbers; this range depends on the number of bits needed to represent the code. The number of bits needed to represent the output code for the MS1100 depends on the data rate, as shown in Table 1.

Table 1. Minimum and Maximum Codes

Data Rate	Number Of Bits	Minimum Code	Maximum Code
15SPS	16	-32768	32767
30SPS	15	-16384	16383
60SPS	14	-8192	8191
240SPS	12	-2048	2047

For a minimum output code of Min Code, gain setting of the PGA, and positive and negative input voltages of VIN+ and VIN−, the output code is given by the expression:

$$\text{Output Code} = -1 \times \text{Min Code} \times \text{PGA} \times \frac{(V_{IN+})-(V_{IN-})}{2.048V}$$

In the previous expression, it is important to note that the negated minimum output code is used. The MS1100 outputs codes in binary tw's complement format, so the absolute values of the minima and maxima are not the same; the maximum n-bit code is $2^{n-1}-1$, while the minimum n-bit code is $-1\times2^{n-1}$. For example, the ideal expression for output codes with a data rate of 30SPS and PGA=2 is:

$$\text{Output Code} = 16384 \times 2 \times \frac{(V_{IN+})-(V_{IN-})}{2.048V}$$

The MS1100 outputs all codes right-justified and sign-extended. This feature makes it possible to perform averaging on the higher data rate codes using only a 16-bit accumulator. Table 2 shows the output codes for various input levels.

Table 2. Output Codes for Different Input Signals

Data Rate	Differential Input Signal				
	-2.048V[1]	-1LSB	ZERO	+1LSB	+2.048V
15SPS	8000_H	$FFFF_H$	0000_H	0001_H	$7FFF_H$
30SPS	$C000_H$	$FFFF_H$	0000_H	0001_H	$3FFF_H$
60SPS	$E000_H$	$FFFF_H$	0000_H	0001_H	$1FFF_H$
240SPS	$F000_H$	$FFFF_H$	0000_H	0001_H	$0FFF_H$

Note 1: Differential input only; do not drive the MS1100 inputs below −200mV.

Self-Calibration

The previous expressions for the MS1100 output code do not account for the gain and offset errors in the modulator. To compensate for these, the MS1100 incorporates self-calibration circuitry. The self-calibration system operates continuously and requires no user intervention. No adjustments can be made to the self-calibration system, and none need to be made. The self-calibration system cannot be deactivated. The offset and gain error figures shown in the Electrical Characteristics include the effects of calibration.

Clock Oscillator

The MS1100 features an onboard clock oscillator, which drives the operation of the modulator and digital filter. The Typical Characteristics show variations in data rate over supply voltage and temperature.

It is not possible to operate the MS1100 with an external system clock.

Input Impedance

The MS1100 uses a switched-capacitor input stage. To external circuitry, it looks roughly like a resistance. The resistance value depends on the capacitor values and the rate at which they are switched. The switching frequency is the same as the modulator frequency; the capacitor values depend on the PGA setting. The switching clock is generated by the onboard clock oscillator, so its frequency (nominally 275kHz) is dependent on supply voltage and temperature.

The common-mode and differential input impedances are different. For a gain setting of the PGA, the differential input impedance is typically: 2.8MΩ/PGA

The common-mode impedance also depends on the PGA setting. The typical value of the input impedance often cannot be neglected. Unless the input source has a low impedance, the MS1100 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Bear in mind, however, that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications. Because the clock oscillator frequency drifts slightly with temperature, the input impedances will also drift. For many applications, this input impedance drift can be neglected, and the expression given above for typical input impedance can be used.

Aliasing

If frequencies are input to the MS1100 that exceed half the data rate, aliasing will occur. To prevent aliasing, the input signal must be bandlimited. The MS1100 digital filter provides some attenuation of high-frequency noise, but the digital filter Sinc1 frequency response cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be needed; in such instances, a simple RC filter will suffice. When designing an input filter circuit, remember to take into account the interaction between the filter network and the input impedance of the MS1100.

Operating Modes

The MS1100 operates in one of two modes: continuous conversion or single-conversion.

In continuous-conversion mode, Once a conversion has been completed, the MS1100 places the result in the output register and immediately begins another conversion.

In single-conversion mode, the MS1100 waits until the ST/DRDY bit in the conversion register is set to 1. When this happens, MS1100 powers up and performs a single conversion. After the conversion completes, the MS1100 places the result in the output register, resets the ST/DRDY bit to 0, and powers down. Writing a 1 to ST/DRDY while a conversion is in progress has no effect. When switched from continuous-conversion mode to single conversion mode, the MS1100 completes the current conversion, resets the ST/DRDY bit to 0, and powers down.

Reset and Power-Up

When the MS1100 powers up, it automatically performs a reset. As part of the reset process, the MS1100 sets all of the bits in the configuration register to their default settings.

The MS1100 responds to the I^2C General Call Reset command. When the MS1100 receives a General Call Reset, it performs an internal reset, exactly as though it had just been powered on.

I^2C Interface

The MS1100 communicates through an I^2C interface. Devices on the I^2C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pull-up resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^2C bus always takes place between two devices, one acting as the master and the other as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^2C devices can act as masters or slaves, but the MS1100 can only act as a slave device.

An I^2C bus consists of two lines, SDA and SCL. SDA carries data; SCL provides the clock. All data is transmitted across the I^2C bus in groups of eight bits. To send a bit on the I^2C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero; a HIGH indicates the bit is one). Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on SCL clocks the SDA bit into the receiver's shift register. The I^2C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line. The master always drives the clock line. The MS1100 never drives SCL, because it cannot act as a master. On the MS1100, SCL is an input only.

Most of the time the bus is idle; no communication occurs place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start a communication and initiate a START condition on the bus. Normally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or its counterpart, a STOP condition. A START condition occurs when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition occurs when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that indicates which slave device it wants to communicate with. This byte is called the address byte. Each device on an I^2C bus has a unique 7-bit address to which it responds. The master sends an address in the address byte, together with a bit that indicates whether it wishes to read from or write to the slave device.

Every byte transmitted on the I^2C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit.

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address it, it will receive a not-acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

A timing diagram for an MS1100 I^2C transaction is shown in Figure 1. The parameters for this diagram are given in Table 3.

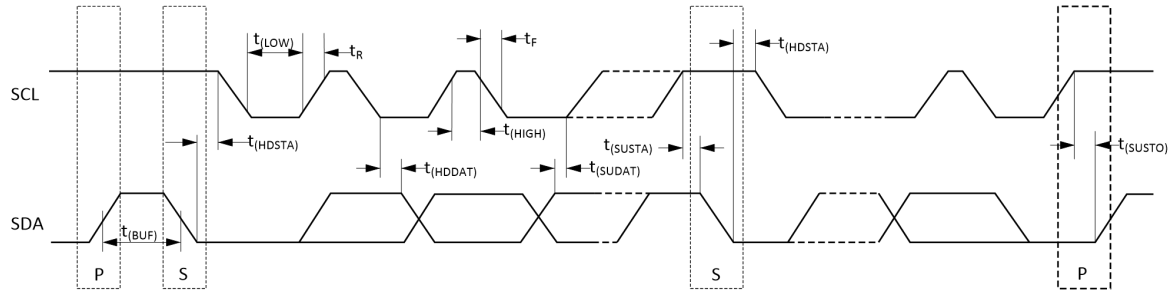


Figure 1. I^2C Timing Diagram

Table 3. Timing Diagram Definitions

Parameter	High-Speed Mode		Unit
	Min	Max	
SCLK operating frequency $t_{(SCLK)}$		0.4	MHz
Bus free time between START and STOP condition $t_{(BUF)}$	600		ns
Hold time after repeated START condition. After this period, the first clock is generated. $t_{(HDSTA)}$	600		ns
Repeated START condition setup time $t_{(SUSTA)}$	600		ns
Stop condition setup time $t_{(SUSTO)}$	600		ns
Data hold time $t_{(HDDAT)}$	0		ns
Data setup time $t_{(SUDAT)}$	100		ns
SCLK clock LOW period $t_{(LOW)}$	1300		ns
SCLK clock HIGH period $t_{(HIGH)}$	600		ns
Clock/data fall time t_F		300	ns
Clock/data rise time t_R		300	ns

Registers

The MS1100 has two registers that are accessible via its I^2C port. The output register contains the result of the last conversion; the configuration register allows the user to change the MS1100 operating mode and query the status of the device.

Output Register

The 16-bit output register contains the result of the last conversion in binary two's complement format. Following reset or power-up, the output register is cleared to zero, and remains zero until the first conversion is completed. The output register format is shown in Table 4.

Table 4. Output Register

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Configuration Register

The 8-bit configuration register can be used to control the MS1100 operating mode, input selection, data rate, and PGA settings. The configuration register format is shown in Table 5. The default setting is 8CH.

Table 5. Configuration Register

BIT	7	6	5	4	3	2	1	0
NAME	ST/DRDY	0	0	SC	DR1	DR0	PGA1	PGA0
DEFAULT	1	0	0	0	1	1	0	0

Bit 7: ST/DRDY

The meaning of the ST/DRDY bit depends on whether it is being written to or read from.

In single conversion mode, writing a 1 to the ST/DRDY bit causes a conversion to start, and writing a 0 has no effect. In continuous conversion mode, the MS1100 ignores the value written to ST/DRDY.

When read, ST/DRDY indicates whether the data in the output register is new data. If ST/DRDY is 0, the data just read from the output register is new, and has not been read before. If ST/DRDY is 1, the data just read from the output register has been read before.

The MS1100 sets ST/DRDY to 0 when it writes data into the output register. It sets ST/DRDY to 1 after any of the bits in the configuration register have been read. (Note that the read value of the bit is independent of the value written to this bit.)

In continuous-conversion mode, use ST/DRDY to determine when new conversion data is ready. If ST/DRDY is 1, the data in the output register has already been read, and is not new. If it is 0, the data in the output register is new, and has not yet been read.

In single-conversion mode, use ST/DRDY to determine when a conversion has completed. If ST/DRDY is 1, the output register data is old, and the conversion is still in process; if it is 0, the output register data is the result of the new conversion.

Note that the output register is returned from the MS1100 before the configuration register. The state of the ST/DRDY bit applies to the data just read from the output register, and not to the data from the next read operation.

Bit 4：SC

SC controls whether the MS1100 is in continuous or single conversion mode. When SC is 1, the MS1100 is in single conversion mode; when SC is 0, it is in continuous conversion mode. The default setting is 0.

Bits 3-2：DR

Bits 3 and 2 control the MS1100 data rate, as shown in Table 6.

Table 6. DR Bits

DR1	DR0	Data Rate	Resolution
0	0	240 SPS	12 Bit
0	1	60 SPS	14 Bit
1	0	30 SPS	15 Bit
1[1]	1[1]	15 SPS	16 Bit

Note 1: Default setting

bits1-0：PGA

Bits 1 and 0 control the MS1100 gain setting, as shown in Table 7.

Table 7. PGA Bits

PGA1	PGA0	Gain
0[1]	0[1]	1
0	1	2
1	0	4
1	1	8

Note 1: Default setting

Reading from the MS1100

To read the output register and the configuration register from the MS1100, first address the MS1100 for reading, then read three bytes. The first two bytes will be the output register's contents, and the third will be the configuration register's contents.

It is not required to read the configuration register byte. It is permissible to read fewer than three bytes during a read operation.

Reading more than three bytes from the MS1100 has no effect. All bytes following the third will be FFH. It is possible to ignore the ST/DRDY bit and read data from the MS1100 output register at any time, without regard to whether a new conversion is complete. If the output register is read more than once during a conversion cycle, it will return the same data each time. New data will be returned only when the output register has been updated. A timing diagram of a typical MS1100 read operation is shown in Figure 2.

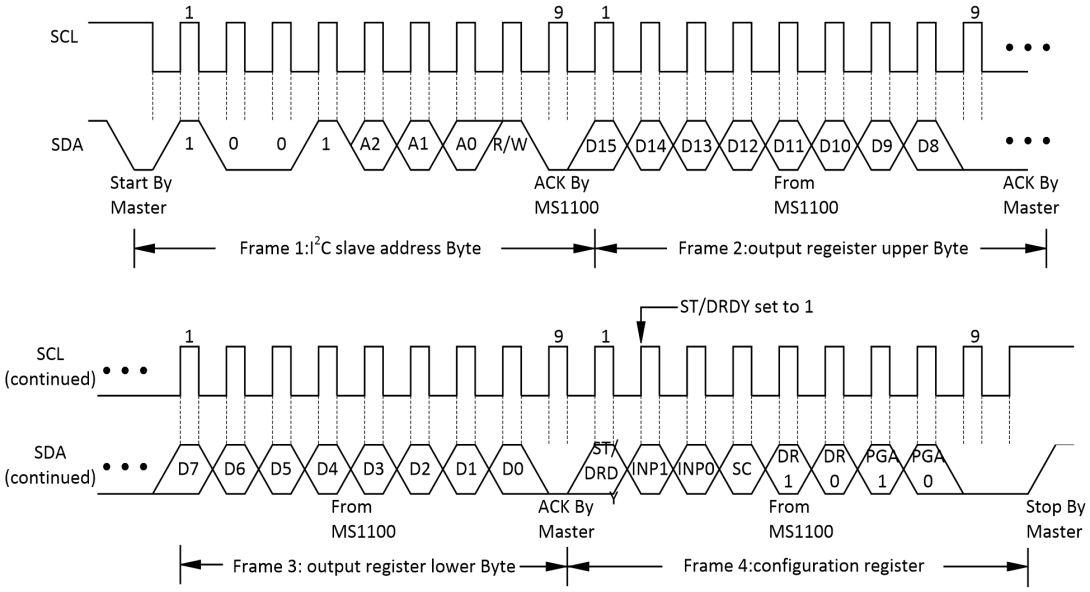


Figure 2. Timing Diagram for Reading From the MS1100

Writing to the MS1100

To write to the configuration register, first address the MS1100 for writing, and send one byte. The byte will be written to the configuration register. Note that data cannot be written to the output register.

Writing more than one byte to the MS1100 has no effect. The MS1100 will ignore any bytes sent to it after the first one, and it will only acknowledge the first byte. A timing diagram of a typical MS1100 write operation is shown in Figure 3.

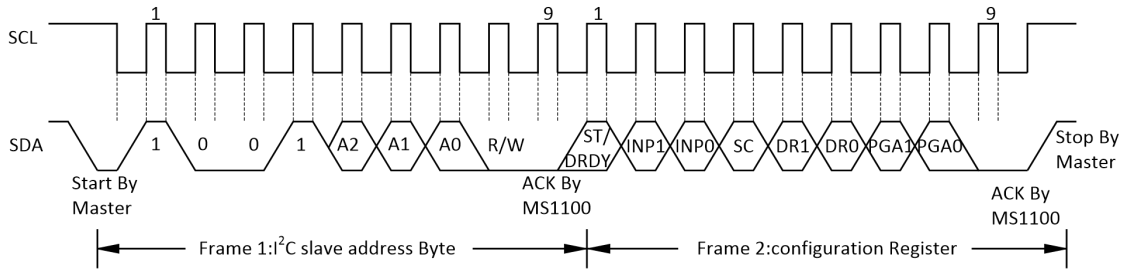


Figure 3. Timing Diagram for Writing to the MS1100

APPLICATIONS INFORMATION

For many applications, connecting the MS1100 is extremely simple. A basic connection diagram for the MS1100 is shown in Figure 4.

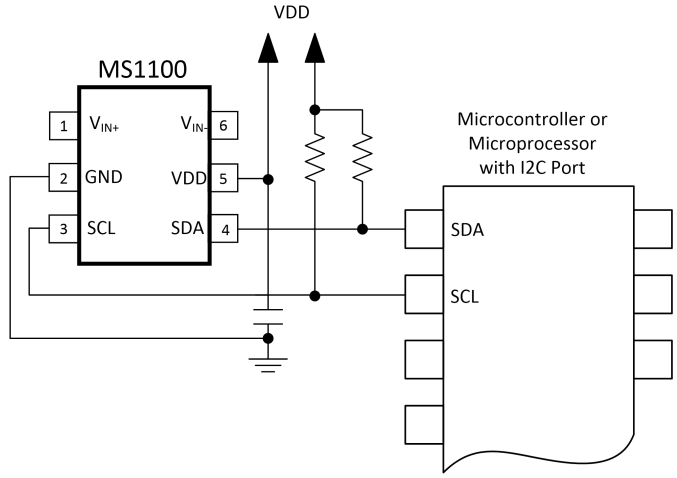


Figure 4. Typical Connections of the MS1100

The fully differential voltage input of the MS1100 is ideal for connection to differential sources with moderately low source impedance, such as bridge sensors and thermistors. Although the MS1100 can read bipolar differential signals, it cannot accept negative voltages on either input. It may be helpful to think of the MS1100 positive voltage input as noninverting, and of the negative input as inverting.

When the MS1100 is converting, it draws current in short spikes. The 0.1µF bypass capacitor supplies the momentary bursts of extra current needed from the supply. The MS1100 interfaces directly to standard mode, fast mode, and high-speed mode I^2C controllers. Any microcontroller's I^2C peripheral, including master-only and non-multiiple-master I^2C peripherals, will work with the MS1100. The MS1100 does not perform clock-stretching (i.e., it never pulls the clock line low), so it is not necessary to provide for this unless other devices are on the same I^2C bus.

Pull-up resistors are necessary on both the SDA and SCL lines because I^2C bus drivers are open-drain. The size of these resistors depends on the bus operating speed and capacitance of the bus lines. Higher-value resistors consume less power, but increase the transition times on the bus, limiting the bus speed. Lower-value resistors allow higher speed at the expense of higher power consumption. Long bus lines have higher capacitance and require smaller pullup resistors to compensate. The resistors should not be too small; if they are, the bus drivers may not be able to pull the bus lines low.

Connecting Multiple Devices

Connecting multiple MS1100s to a single bus is almost trivial. The MS1100 is available in eight different versions, each of which has a different I^2C address. An example showing three MS1100s connected on a single bus is shown in Figure 5. Up to eight MS1100s (provided their addresses are different) can be connected to a single bus.

Note that only one set of pull-up resistors is needed per bus. You might find that you need to lower the pull-up resistor values slightly to compensate for the additional bus capacitance presented by multiple devices and increased line length.

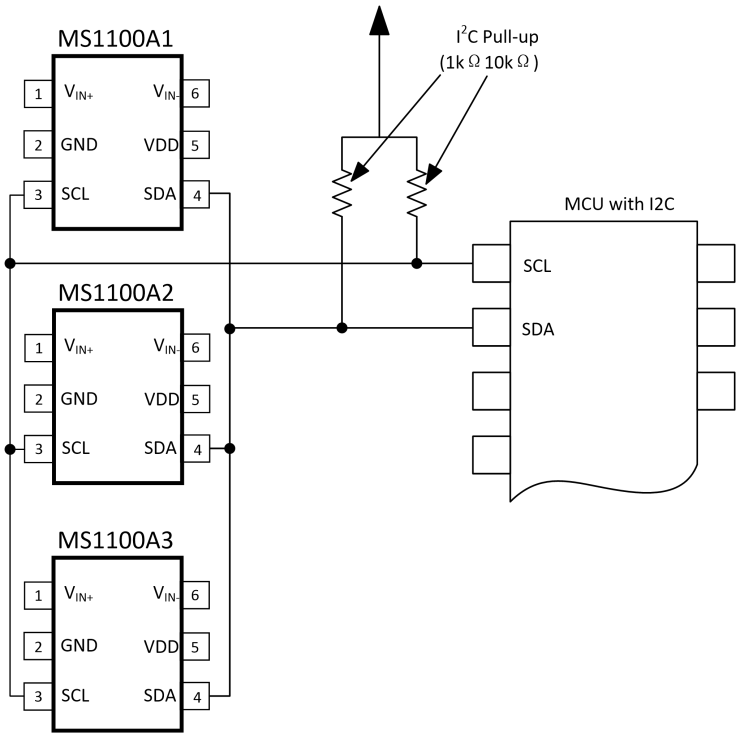


Figure 5. Connecting Multiple MS1100s

Using GPIO Ports For I²C

Most microcontrollers have programmable input/output pins that can be set in software to act as inputs or outputs. If an I²C controller is not available, the MS1100 can be connected to GPIO pins, and the I²C bus protocol simulated, or bit-banged, in software. An example of this for a single MS1100 is shown in Figure 6.

Note that no pull-up resistor is shown on the SCL line. In this simple case, the resistor is not needed; the microcontroller can simply leave the line on output, and set it to one or zero as appropriate. It can do this because the MS1100 never drives its clock line low. This technique can also be used with multiple devices, and has the advantage of lower current consumption due to the absence of a resistive pull-up.

If there are any devices on the bus that may drive their clock lines low, the above method should not be used; the SCL line should be high-Z or zero and a pull-up resistor provided as usual. Note also that this cannot be done on the SDA line in any case, because the MS1100 does drive the SDA line low from time to time, as all I²C devices do.

Some microcontrollers have selectable strong pull-up circuits built in to their GPIO ports. In some cases, these can be switched on and used in place of an external pull-up resistor. Weak pull-ups are also provided on some microcontrollers, but usually these are too weak for I²C communication. If there is any doubt about the matter, test the circuit before committing it to production.

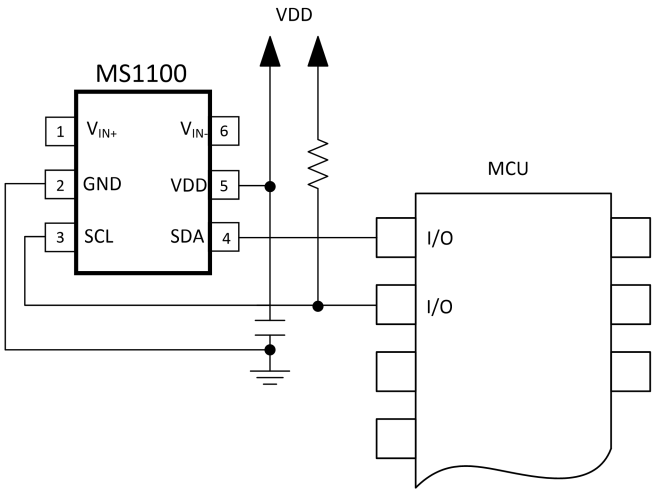


Figure 6. Using GPIO with a single MS1100

Single-Ended Inputs

Although the MS1100 has a fully differential input, it can easily measure single-ended signals. A simple single-ended connection scheme is shown in Figure 7. The MS1100 is configured for single-ended measurement by grounding either of its input pins, usually VIN–, and applying the input signal to VIN+. The single-ended signal can range from –0.2V to VDD + 0.3V. The MS1100 loses no linearity anywhere in its input range. Negative voltages cannot be applied to this circuit because the MS1100 inputs can only accept positive voltages.

The MS1100 input range is bipolar differential with respect to the reference, i.e. ±VDD. The single-ended circuit shown in Figure 7 covers only half the MS1100 input scale because it does not produce differentially negative inputs; therefore, one bit of resolution is lost.

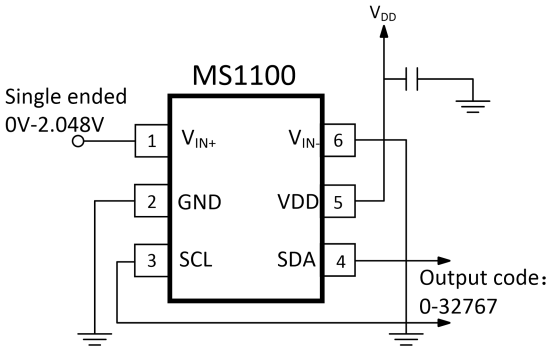


Figure 7. Measuring Single-Ended Inputs

Low-Side Current Monitor

Figure 8 shows a circuit for a low-side shunt-type current monitor. The circuit reads the voltage across a shunt resistor, which is sized as small as possible while still giving a readable output voltage. This voltage is amplified by MS8552, and the result is read by the MS1100.

It is suggested that the MS1100 be operated at a gain of 8. The gain of the MS8552 can then be set lower. For a gain of 8, the op amp should be set up to give a maximum output voltage of no greater than 0.256V. If the shunt resistor is sized to provide a maximum voltage drop of 64mV at full-scale current, the full-scale input to the MS1100 is 0.2V.

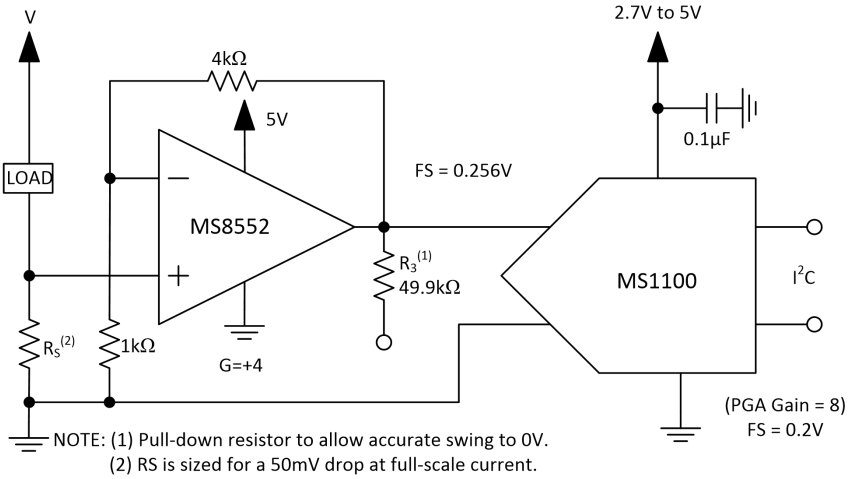
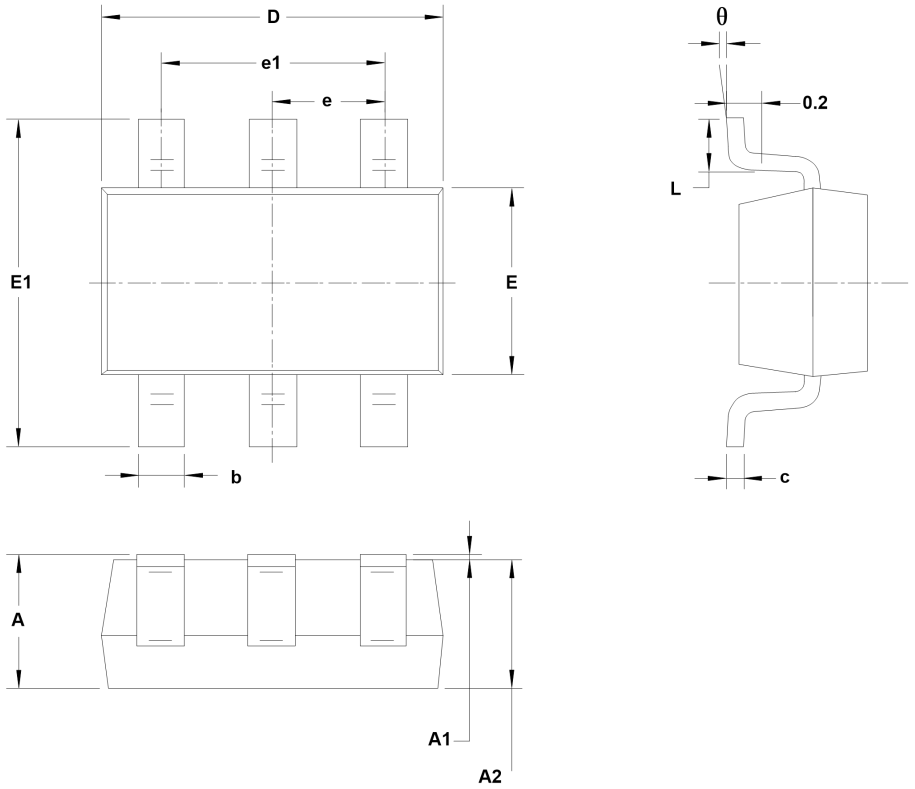


Figure 8. Low-Side Current Measurement

PACKAGE OUTLINE DIMENSIONS

SOT23-6



Symbol	Dimensions In Millimeters		Dimensions in Inches	
	MIN	MAX	MIN	MAX
A	1.050	1.250	0.041	0.049
A1	0.000	0.100	0.000	0.004
A2	1.050	1.150	0.041	0.045
b	0.300	0.500	0.012	0.020
c	0.100	0.200	0.004	0.008
D	2.820	3.20	0.111	0.119
E	1.500	1.700	0.059	0.067
E1	2.650	2.950	0.104	0.116
e	0.950BSC		0.037BSC	
e1	1.900BSC		0.075BSC	
L	0.300	0.600	0.012	0.024
θ	0º	8º	0º	8º

MARKING and PACKAGING SPECIFICATIONS

1. Marking Drawing Description

Product Name : 1100

Product Code : XXXXX

2. Marking Drawing Demand

Laser printing, contents in the middle, font type Arial.

3. Packaging Specifications

Device	Package	Piece/Reel	Reel/Box	Piece /Box	Box/Carton	Piece/Carton
MS1100	SOT23-6	3000	10	30000	4	120000

STATEMENT

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MOS CIRCUIT OPERATION PRECAUTIONS

Static electricity can be generated in many places. The following precautions can be taken to effectively prevent the damage of MOS circuit caused by electrostatic discharge:

1. The operator shall ground through the anti-static wristband.
2. The equipment shell must be grounded.
3. The tools used in the assembly process must be grounded.
4. Must use conductor packaging or anti-static materials packaging or transportation.

+86-571-89966911

Rm701, No.9 Building, No. 1 WeiYe Road, Puyan Street, Binjiang District, Hangzhou, Zhejiang

http:// www.relmon.com