SIM8950 Series Display Driver Development Guide

Smart Module

Shanghai SIMCom Wireless Solutions Ltd.
Floor 6, Building B, SIM Technology Building, No.633, Jinzhong Road
Changning District200335
Tel:86-21-31575100/31575200
support@simcom.com
www.simcom.com

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About Document

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1 Purpose of this document

This document describes how to bringup the display panel in kernel and Little Kernel (LK) with the Display Serial Interface (DSI) on the SIM8950 Android platform.

2 Kernel panel bringup

2.1 Prerequisites

Gather the following information from the panel specification and hardware schematic:

1) Panel parameters – Panel type, resolution, bpp, fps, porch values
2) Panel power-on sequence and signal duration for GPIO pins, for example RESET/IOVDD
3) Panel DSI initial command sequence and subsequent delay.
4) Bitclk needed to reach the target fps
5) GPIO connection between the host and panel including RESET, TE, and so on
6) Panel power supplies and voltages

2.2 DSI panel bringup

Bringup the Linux kernel first and then port it to the little kernel (LK) later. This chapter describes the Linux kernel bringup.

Follow these steps for Linux kernel panel bringup:

1) Disable continuous splash in LK and Kernel.
2) Verify that panel backlight is enabled or turn it always ON during bringup.
3) Prepare the panel dtsi file.

   Create the dtsi file in one of two ways:

   - ☐ Use QTI's GCDB parser
   - ☐ Refer to one of the dtsi files located under kernel/arch/arm/boot/dts/qcom folder.

4) Include the panel DTSI in the platform device tree and select the panel DTSI that should be picked up.

2.2.1 Disable continuous splash in LK and kernel

The continuous splash needs to be disabled in both LK and kernel at this point so that the kernel

begins settings from scratch.
1. Disable continuous splash in LK: Disable the Macro DISPLAY_SPLASH_SCREEN at bootable/bootloader/lk/target/$(project)/rules.mk. Use the chipset rules.mk file specific to the chipset that you are working on.
Example:
bootable/bootloader/lk/target/msm8953/rules.mk
-DEFINES += DISPLAY_SPLASH_SCREEN=1
+#DEFINES += DISPLAY_SPLASH_SCREEN=1
DEFINES += DISPLAY_TYPE_MIPI=1
DEFINES += DISPLAY_TYPE_DSI6G=1
2. Disable continuous splash in kernel: Make sure that panel node does not contain “qcom,cont-splash-enabled” element. For the new panels being created, this element may not be included, but be sure to check for it. Below is an example for reference.
Example:
--- kernel/msm-3.18/arch/arm/boot/dts/qcom/dsi-panel-nt35532-1080p-video-sim.dtsi
qcom,mdss-dsi-underflow-color = <0xff>;
qcom,mdss-dsi-border-color = <0>;
-qcom,cont-splash-enabled;
+//qcom,cont-splash-enabled;

2.2.2 Verify that the panel backlight is enabled

For bringup, to rule out backlight issues, it is recommended that the backlight be enabled all the time, if possible.
1. The node shown below in panel dtsi file refers to the backlight type to be used. Set it as shown below.
qcom,mdss-dsi-bl-pmic-control-type: A string that specifies the implementation of backlight control for this panel.
"bl_ctrl_pwm" = Backlight controlled by PWM gpio.
"bl_ctrl_wled" = Backlight controlled by WLED.
"bl_ctrl_dcs" = Backlight controlled by DCS commands.
other: Unknown backlight control. (default)
2. If backlight is PWM controlled, configure the PWM parameters also, as shown below.

qcom,mdss-dsi-bl-min-level = <1>;
qcom,mdss-dsi-bl-max-level = <255>;
qcom,mdss-dsi-bl-pmic-control-type = "bl_ctrl_pwm";
qcom,mdss-dsi-bl-pmic-pwm-frequency = <100>;
qcom,mdss-dsi-bl-pmic-bank-select = <0>;

2.2.3 Prepare the dtsi files with the mandatory elements and panel

Information:
It is important to hook in all the panel related information in this dtsi file so that the host will be configured according to the panel requirements.
All panel ".dtsi" files are placed under the kernel\ msm-3.18\arch\arm\boot\dts\qcom\ folder.
The detailed documentation is found in kernel\msm-3.18\Documentation\devicetree\bindings\fb\mdss-dsi-panel.txt file

The examples below show single dsi Video mode panel dtsi files. The steps for preparing the dtsi files start in Section 5.2.3.1.
Video mode panel .dtsi file example

```
&mdss_mdp {
    dsi_nt35532_1080p_video: qcom,mdss_dsi_nt35532_1080p_video {
        qcom,mdss-dsi-panel-name = "nt35532 1080p video mode dsi panel";
        qcom,mdss-dsi-panel-controller = <&mdss_dsi0>;
        qcom,mdss-dsi-panel-type = "dsi_video_mode";
        qcom,mdss-dsi-panel-destination = "display_1";
        qcom,mdss-dsi-panel-framerate = <60>;
        qcom,mdss-dsi-virtual-channel-id = <0>;
        qcom,mdss-dsi-stream = <0>;
        qcom,mdss-dsi-panel-width = <1080>;
        qcom,mdss-dsi-panel-height = <1920>;
        qcom,mdss-dsi-h-front-porch = <100>;
        qcom,mdss-dsi-h-back-porch = <80>;
        qcom,mdss-dsi-h-pulse-width = <20>;
        qcom,mdss-dsi-h-sync-skew = <0>;
        qcom,mdss-dsi-v-back-porch = <16>;
        qcom,mdss-dsi-v-front-porch = <16>;
        qcom,mdss-dsi-v-pulse-width = <5>;
        qcom,mdss-dsi-h-left-border = <0>;
        qcom,mdss-dsi-h-right-border = <0>;
        qcom,mdss-dsi-v-top-border = <0>;
        qcom,mdss-dsi-v-bottom-border = <0>;
        qcom,mdss-dsi-bpp = <24>;
        qcom,mdss-dsi-color-order = "rgb_swap_rgb";
        qcom,mdss-dsi-underflow-color = <0xff>;
        qcom,mdss-dsi-border-color = <0>;
        qcom,cont-splash-enabled;
        qcom,mdss-dsi-on-command = [15 01 00 00 00 00 02 FF 01
            15 01 00 00 00 00 02 FB 01
```

```
        15 01 00 00 00 00 02 00 01
        15 01 00 00 00 00 02 01 55
        15 01 00 00 00 00 02 02 59
        15 01 00 00 00 00 02 04 0C
        15 01 00 00 00 00 02 05 2B
        15 01 00 00 00 00 02 06 64
        15 01 00 00 00 00 02 07 C6
        15 01 00 00 00 00 02 0D 89
        15 01 00 00 00 00 02 0E 89
        15 01 00 00 00 00 02 0F E0
        15 01 00 00 00 00 02 10 03
        ......
        15 01 00 00 00 00 02 FB 01
        15 01 00 00 00 00 02 D3 15
        15 01 00 00 00 00 02 D4 10
        15 01 00 00 00 00 02 D5 18
        15 01 00 00 00 00 02 D6 B8
        15 01 00 00 00 00 02 D7 00
        15 01 00 00 00 00 02 55 80
        05 01 00 00 78 00 02 11 00
        05 01 00 00 32 00 02 29 00];
qcom,mdss-dsi-off-command = [05 01 00 00 32 00 02 28 00
                05 01 00 00 78 00 02 10 00];
qcom,mdss-dsi-on-command-state = "dsi_lp_mode";
qcom,mdss-dsi-off-command-state = "dsi_lp_mode";
qcom,mdss-dsi-h-sync-pulse = <1>;
qcom,mdss-dsi-traffic-mode = "burst_mode";
qcom,mdss-dsi-lane-map = "lane_map_0123";
qcom,mdss-dsi-bllp-eof-power-mode;
qcom,mdss-dsi-bllp-power-mode;
qcom,mdss-dsi-lane-0-state;
qcom,mdss-dsi-lane-1-state;
qcom,mdss-dsi-lane-2-state;
qcom,mdss-dsi-lane-3-state;
qcom,mdss-dsi-panel-timings = [ee 38 26 00 6a 6c 2c 3c 2c 03 04 00];
qcom,mdss-dsi-t-clk-post = <0x02>;
qcom,mdss-dsi-t-clk-pre = <0x2c>;
qcom,mdss-dsi-dma-trigger = "trigger_sw";
qcom,mdss-dsi-mdp-trigger = "none";
qcom,mdss-dsi-bl-min-level = <1>;
qcom,mdss-dsi-bl-max-level = <255>;
qcom,mdss-dsi-reset-sequence = <1 20>, <0 2>, <1 20>;
qcom,mdss-dsi-panel-timings-phy-v2 = [24 1f 08 09 05 03 04 a0
            24 1f 08 09 05 03 04 a0
```

```
                24 1f 08 09 05 03 04 a0
                24 1f 08 09 05 03 04 a0
                24 1b 08 09 05 03 04 a0];
        qcom,mdss-dsi-bl-pmic-control-type = "bl_ctrl_pwm";
        qcom,mdss-dsi-bl-pmic-pwm-frequency = <100>;
        qcom,mdss-dsi-bl-pmic-bank-select = <0>;
        qcom,mdss-dsi-pwm-gpio = <&pm8953_mpps 4 0>;
        qcom,panel-supply-entries = <&dsi_panel_pwr_supply>;
    };
};
```

2.2.3.1 Fill the panel LCD information

☐ Fill the panel LCD parameters either from the bridge IC vendor or the LCD vendor. You can check the panel spec or check with the panel vendor for this information.

DTSI node name	Description
qcom,mdss-dsi-panel-framerate	Specifies the frame rate for the panel 60 = 60 frames per second (default)
qcom,mdss-dsi-panel-width	Specifies panel width in pixels
qcom,mdss-dsi-panel-height	Specifies panel height in pixels
qcom,mdss-dsi-h-front-porch	Horizontal front porch value in pixel 6 = default value
qcom,mdss-dsi-h-back-porch	Horizontal back porch value in pixel 6 = default value
qcom,mdss-dsi-h-pulse-width	Horizontal pulse width 2 = default value
qcom,mdss-dsi-h-sync-skew	Horizontal sync skew value 0 = default value
qcom,mdss-dsi-v-back-porch	Vertical back porch value in pixel 6 = default value
qcom,mdss-dsi-v-front-porch	Vertical front porch value in pixel 6 = default value
qcom,mdss-dsi-v-pulse-width	Vertical pulse width 2 = default value

qcom,mdss-dsi-bpp	Specifies the panel bits per pixel 3 = for rgb111 8 = for rgb332 12 = for rgb444 16 = for rgb565 18 = for rgb666 24 = for rgb888
qcom,mdss-dsi-h-sync-pulse	Specifies the pulse mode option for the panel 0 = Don't send hsa/he following vs/ve packet(default) 1 = Send hsa/he following vs/ve packet
qcom,mdss-dsi-traffic-mode	Specifies the panel traffic mode "non_burst_sync_pulse" = non burst with sync pulses (default) "non_burst_sync_event" = non burst with sync start event "burst_mode" = burst mode

2.2.3.2 Pack the ON/OFF commands

Pack the panel ON commands and the state in which they need to be sent, high speed or low power.

Panel ON and OFF commands need to be packed in a specific format. Please find the details below for the below entries.

Command name	Description
qcom,mdss-dsi-on-command	A byte stream formed by multiple dcs packets based on qcom dsi controller protocol. byte 0: dcs data type byte 1: set to indicate this is an individual packet (no chain) byte 2: virtual channel number byte 3: expect ack from client (dcs read command) byte 4: wait number of specified ms after dcs command transmitted byte 5, 6: 16 bits length in network byte order byte 7 and beyond: number byte of payload
qcom,mdss-dsi-off-command	A byte stream formed by multiple dcs packets based on qcom dsi controller protocol. byte 0: dcs data type byte 1: set to indicate this is an individual packet (no chain) byte 2: virtual channel number byte 3: expect ack from client (dcs read command) byte 4: wait number of specified ms after dcs command transmitted byte 5, 6: 16 bits length in network byte order byte 7 and beyond: number byte of payload

Example.

qcom,mdss-dsi-on-command = [39 01 00 00 00 00 04 b9 ff 83 94

39 01 00 00 00 00 0b B1 48 0f 6f 09 33 54 51 51 30 43

39 01 00 00 00 00 07 BA 63 03 68 6B B2 C0

39 01 00 00 00 00 07 B2 00 80 64 0c 06 2F

39 01 00 00 00 00 15 B4 19 74 19 74 19 74 01 0C 86 75 00 3F 19 74 19 74 09 74 01 0c

39 01 00 00 00 00 22 D3 00 00 07 07 00 00 12 10 32 10 01 00 01 32 13 C0 00 00 32 10 08 00 00 37 04 03 03 37 04 00 47 0c 40

39 01 00 00 00 00 2D D5 18 18 18 18 00 01 02 03 04 05 06 07 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 19 19 19 19 20 21 22 23

39 01 00 00 00 00 2d D6 18 18 19 19 07 06 05 04 03 02 01 00 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 18 19 19 18 18 23 22 21 20

39 01 00 00 00 00 03 B6 2f 2f

39 01 00 00 00 00 3b E0 00 02 08 0c 0e 11 14 11 24 32 41 40 4a 5a 5f 62 72 77 77 8b a2 52 53 5a 60 66 6e 7f 7F 00 02 08 0c 0e 11 14 11 24 32 41 40 49 5a 5f 62 71 76 77 8b a1 52 54 5b 61 67 73 7f 7F

39 01 00 00 00 00 02 CC 0b

39 01 00 00 00 00 03 C0 1F 31

39 01 00 00 00 00 02 D4 02

39 01 00 00 00 00 02 BD 01

39 01 00 00 00 00 02 B1 60

39 01 00 00 00 00 02 BD 00

39 01 00 00 00 00 08 BF 40 81 50 00 1A FC 01

05 01 00 00 78 00 02 11 00

05 01 00 00 14 00 02 29 00

];

qcom,mdss-dsi-off-command = [05 01 00 00 00 00 02 28 00

05 01 00 00 00 00 02 10 00];

NOTE: The incorrect DCS command format may stop display bringup in kernel.

Panel ON and OFF commands can be sent in Low power state or High speed state. Select the state from the DTSI nodes shown in the table below.

Command name	Description
qcom,mdss-dsi-on-command-state	String that specifies the ctrl state for sending ON commands. "dsi_lp_mode" = dsi low power mode (default) "dsi_hs_mode" = dsi high speed mode
qcom,mdss-dsi-off-command-state	String that specifies the ctrl state for sending OFF commands. "dsi_lp_mode" = dsi low power mode (default) "dsi_hs_mode" = dsi high speed mode

Example:

qcom,mdss-dsi-on-command-state = "dsi_lp_mode";

qcom,mdss-dsi-off-command-state = "dsi_hs_mode";

2.2.3.3 Set the MDSS DSI host parameters

Update the panel name/dsi0 or dsi1/panel-type/lanes enabled using the guidelines in the table below.

The dsi host parameters needed to update the configuration properties are shown in the following table.

Property name	Description
qcom,mdss-dsi-panel-name	A string used as a descriptive name of the panel qcom,mdss-dsi-panel-name = "jdi 1080p video mode dsi panel";
qcom,mdss-dsi-panel-controller	Specifies the phandle for the dsi controller that this panel will be mapped to qcom,mdss-dsi-panel-controller = <&mdss_dsi0>;
qcom,mdss-dsi-panel-type	Specifies the panel operating mode qcom,mdss-dsi-panel-type = "dsi_video_mode";
qcom,mdss-dsi-panel-destination	A string that specifies the destination display for the panel qcom,mdss-dsi-panel-destination = "display_1"; This will be set to two only for second dtsi of dual-dsi panel.
qcom,mdss-dsi-virtual-channel-id	Specifies the virtual channel identifier qcom,mdss-dsi-virtual-channel-id = <0>;
qcom,mdss-dsi-stream	Specifies the packet stream to be used qcom,mdss-dsi-stream = <0>; This will be default stream 0 all the time.
qcom,mdss-dsi-lane-0-state; qcom,mdss-dsi-lane-1-state; qcom,mdss-dsi-lane-2-state; qcom,mdss-dsi-lane-3-state;	Boolean that specifies whether specified data lane is enabled If we use all four lanes, we need to specify all four nodes. If we use only lane0 and lane1, then we need to specify only "qcom,mdss-dsi-lane-0-state" and "qcom,mdss-dsi-lane-1-state" accordingly.
qcom,mdss-dsi-reset-sequence	An array that lists the sequence of reset gpio values and sleeps Each command will have the format defined as below: Reset GPIO value Sleep value (in ms)

2.2.3.4 Calculate the PHY timings

1. Calculate the DSI PHY timings and Tclk-post and Tclk-pre values from the timing calculator in the DSI Timing Parameters User Interactive Spreadsheet and update below entries.

PHY timing properties:

- qcom,mdss-dsi-panel-timings: An array of length 12 that specifies the PHY timing settings for the panel.
- qcom,mdss-dsi-t-clk-post: Specifies the byte clock cycles after mode switch.
  0x03 = default value.
- qcom,mdss-dsi-t-clk-pre: Specifies the byte clock cycles before mode switch.
  0x24 = default value.

- qcom,mdss-dsi-panel-timings-phy-v2: An array of length 40 char that specifies the PHY version 2 lane timing settings for the panel.

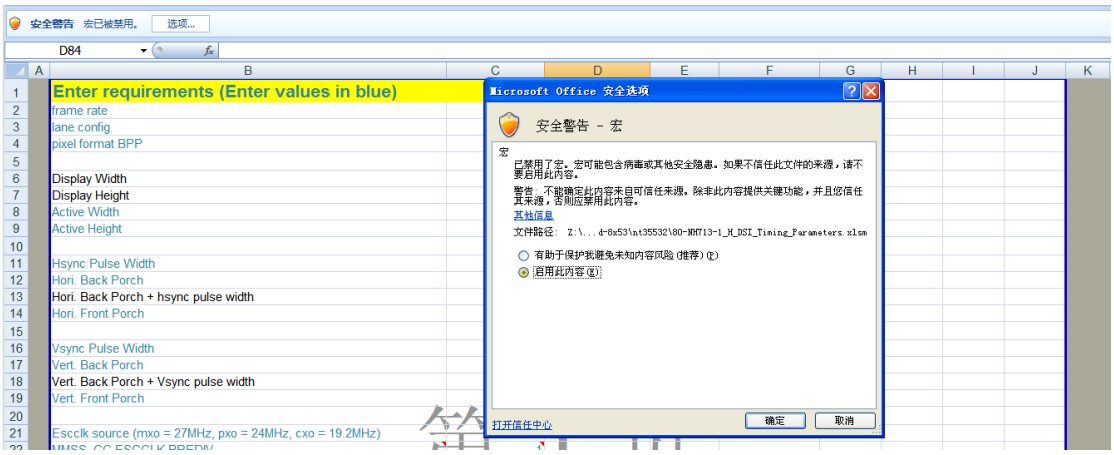
2. Check with the bridge IC vendor to obtain a bridge IC PHY timing specification. The following steps describe how to calculate the panel timings and fill in host registers. The interactive Excel spreadsheet features macros that will auto-calculate the PHY timings needed.

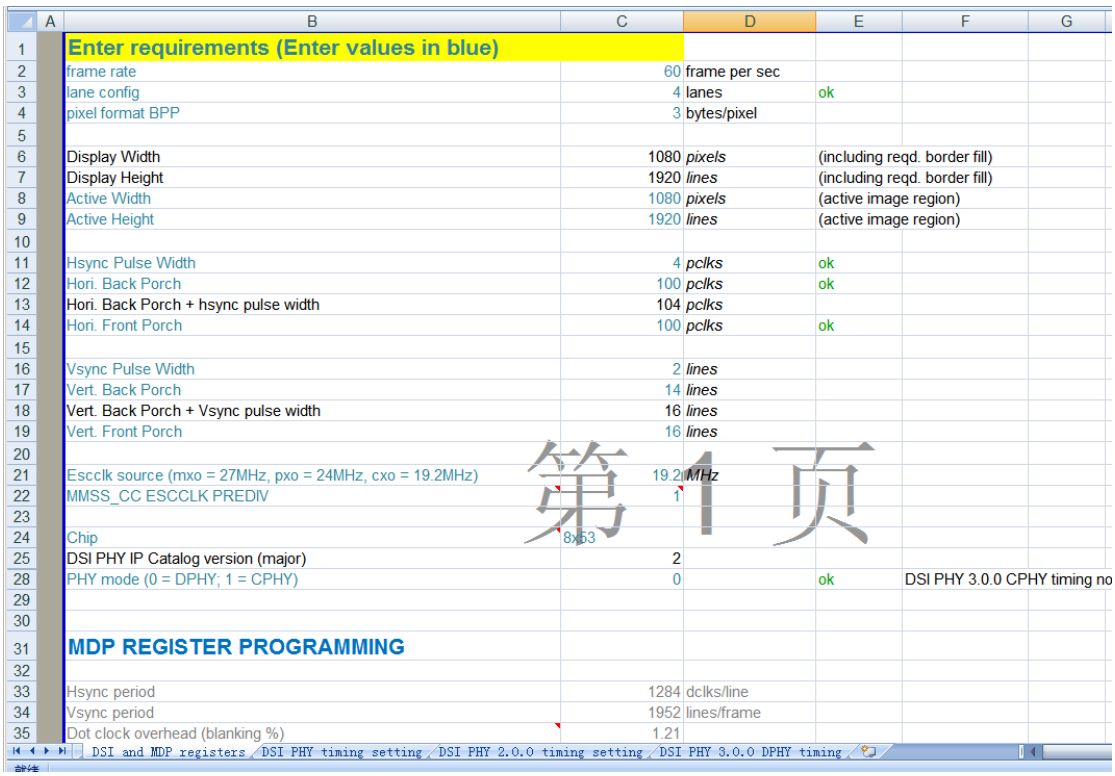
2.2.3.4.1 How to use the spreadsheet for DSI PHY timing calculation

The panel requires the PHY value setup for bitclk in the DSI PHY register. The DSI Timing Parameters User Interactive Spreadsheet (80-NH713-1) can be used to calculate the values automatically. Note that this can be used for only B-family chipsets that use the DSI6G DSI host design. You can download this from Docs and Downloads website.

To auto-calculate these values, follow the steps below.

1. Open the DSI and MDP Registers sheet. Enter panel resolution/porch values/fps/color depth/lane numbers into the area circled in red in the example below.



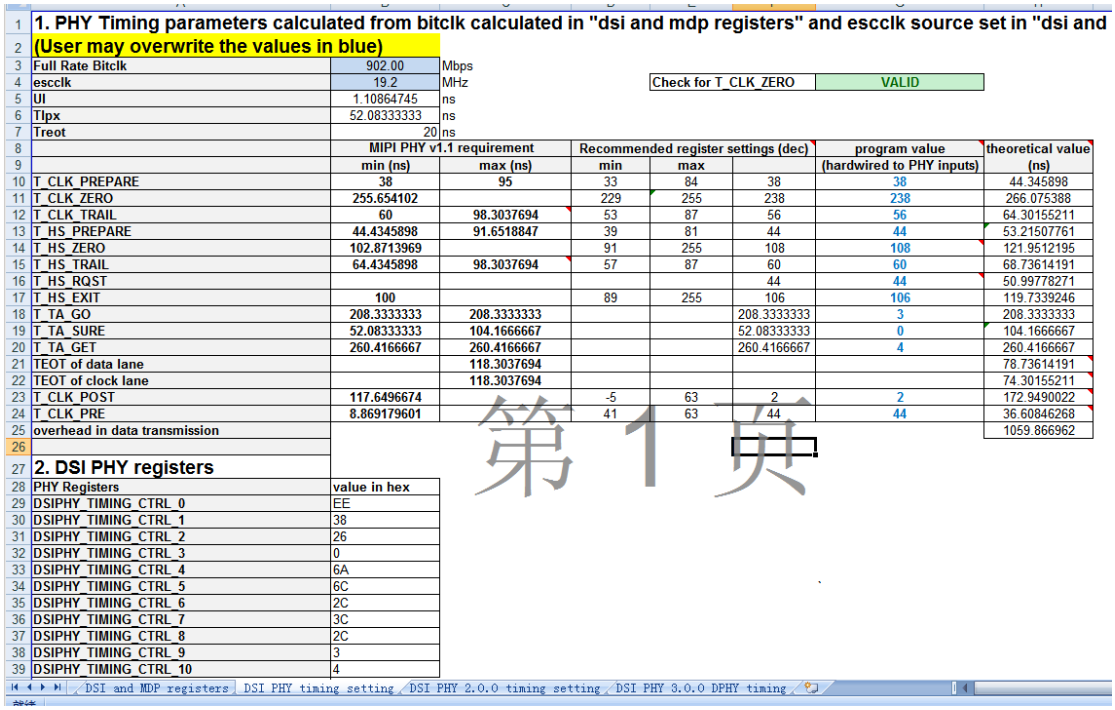


	A	B	C	D	E	F	G
1		**Enter requirements (Enter values in blue)**					
2		frame rate	60	frame per sec			
3		lane config	4	lanes	ok		
4		pixel format BPP	3	bytes/pixel			
5							
6		Display Width	1080	*pixels*	(including reqd. border fill)		
7		Display Height	1920	*lines*	(including reqd. border fill)		
8		Active Width	1080	*pixels*	(active image region)		
9		Active Height	1920	*lines*	(active image region)		
10							
11		Hsync Pulse Width	4	*pclks*	ok		
12		Hori. Back Porch	100	*pclks*	ok		
13		Hori. Back Porch + hsync pulse width	104	*pclks*			
14		Hori. Front Porch	100	*pclks*	ok		
15							
16		Vsync Pulse Width	2	*lines*			
17		Vert. Back Porch	14	*lines*			
18		Vert. Back Porch + Vsync pulse width	16	*lines*			
19		Vert. Front Porch	16	*lines*			
20							
21		Escclk source (mxo = 27MHz, pxo = 24MHz, cxo = 19.2MHz)	19.2	*MHz*			
22		MMSS_CC ESCCLK PREDIV	1				
23							
24		Chip	8x63				
25		DSI PHY IP Catalog version (major)	2				
28		PHY mode (0 = DPHY; 1 = CPHY)	0		ok	DSI PHY 3.0.0 CPHY timing no	
29							
30							
31		**MDP REGISTER PROGRAMMING**					
32							
33		Hsync period	1284	dclks/line			
34		Vsync period	1952	lines/frame			
35		Dot clock overhead (blanking %)	1.21				

DSI and MDP registers | DSI PHY timing setting | DSI PHY 2.0.0 timing setting | DSI PHY 3.0.0 DPHY timing

If spreadsheet says to change the porches to be multiple of 4 or make it even. Please change it accordingly and also update the panel porch node. You can refer to the user instructions in the excel sheet

2. Open the DSI PHY timing setting to see the calculated DSI-related clock rate in the blue fields. A value of INVALID will appear in the Check for T_CLK_ZERO field. Press CTRL+J and CTRL+K to recalculate T_CLK_ZERO to VALID.



1. PHY Timing parameters calculated from bitclk calculated in "dsi and mdp registers" and escclk source set in "dsi and (User may overwrite the values in blue)

Full Rate Bitclk	902.00	Mbps
escclk	19.2	MHz
UI	1.10864745	ns
Tlpx	52.08333333	ns
Treot	20	ns

Check for T_CLK_ZERO: VALID

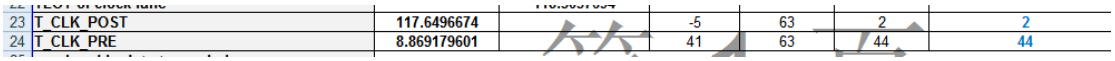
	MIPI PHY v1.1 requirement		Recommended register settings (dec)			program value	theoretical value
	min (ns)	max (ns)	min	max		(hardwired to PHY inputs)	(ns)
T_CLK_PREPARE	38	95	33	84	38	38	44.345898
T_CLK_ZERO	255.654102		229	255	238	238	266.075388
T_CLK_TRAIL	60	98.3037694	53	87	56	56	64.30155211
T_HS_PREPARE	44.4345898	91.6518847	39	81	44	44	53.21507761
T_HS_ZERO	102.8713969		91	255	108	108	121.9512195
T_HS_TRAIL	64.4345898	98.3037694	57	87	60	60	68.73614191
T_HS_RQST					44	44	50.99778271
T_HS_EXIT	100		89	255	106	106	119.7339246
T_TA_GO	208.3333333	208.3333333			208.3333333	3	208.3333333
T_TA_SURE	52.08333333	104.1666667			52.08333333	0	104.1666667
T_TA_GET	260.4166667	260.4166667			260.4166667	4	260.4166667
TEOT of data lane		118.3037694					78.73614191
TEOT of clock lane		118.3037694					74.30155211
T_CLK_POST	117.6496674		-5	63	2	2	172.9490022
T_CLK_PRE	8.869179601		41	63	44	44	36.60846268
overhead in data transmission							1059.866962

2. DSI PHY registers

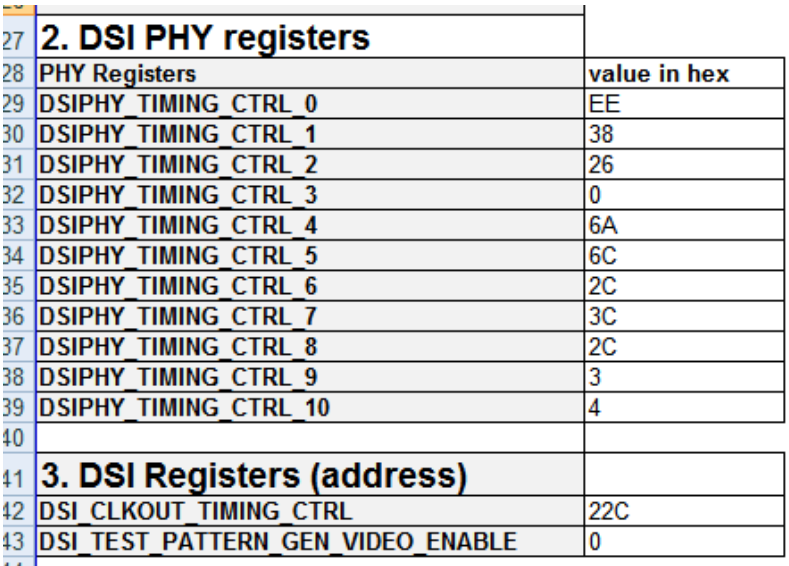
PHY Registers	value in hex
DSIPHY_TIMING_CTRL_0	EE
DSIPHY_TIMING_CTRL_1	38
DSIPHY_TIMING_CTRL_2	26
DSIPHY_TIMING_CTRL_3	0
DSIPHY_TIMING_CTRL_4	6A
DSIPHY_TIMING_CTRL_5	6C
DSIPHY_TIMING_CTRL_6	2C
DSIPHY_TIMING_CTRL_7	3C
DSIPHY_TIMING_CTRL_8	2C
DSIPHY_TIMING_CTRL_9	3
DSIPHY_TIMING_CTRL_10	4

DSI and MDP registers | DSI PHY timing setting | DSI PHY 2.0.0 timing setting | DSI PHY 3.0.0 DPHY timing

The spreadsheet will show the PHY value setup for bitclk, which the panel requires in the “DSI PHY register.” and “DSI and MDP registers”.



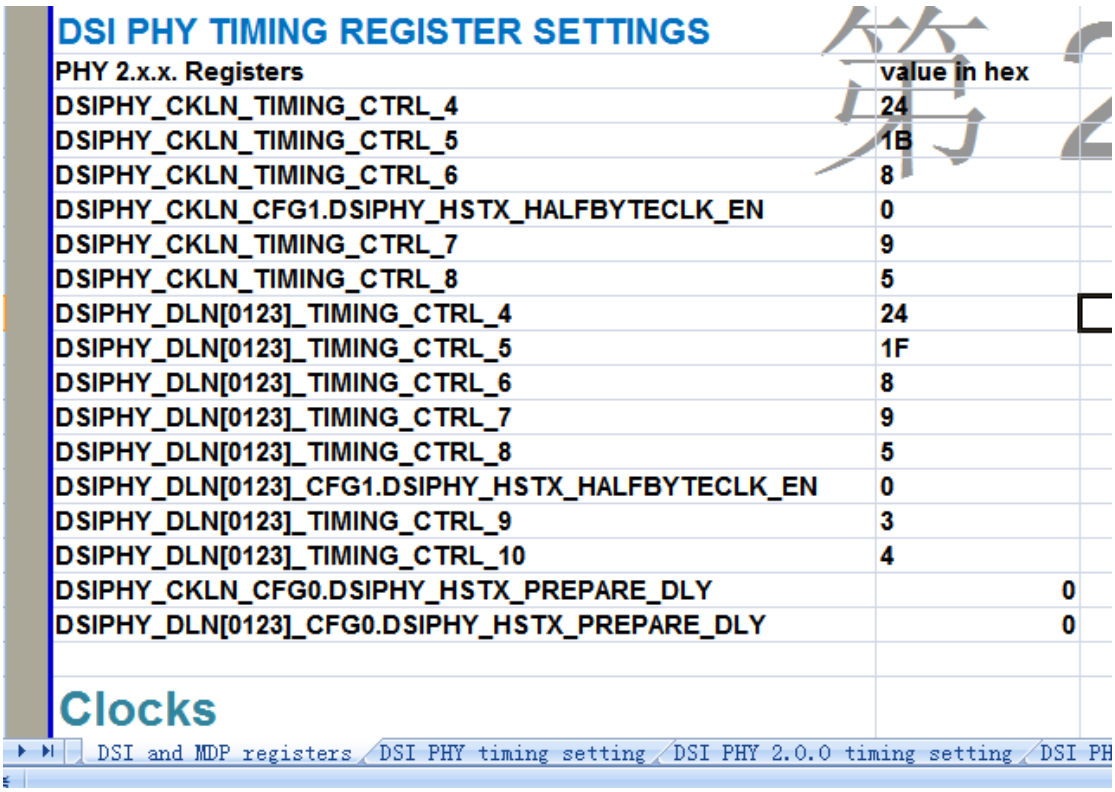
23	T_CLK_POST	117.6496674		-5	63	2	2
24	T_CLK_PRE	8.869179601		41	63	44	44



27	**2. DSI PHY registers**	
28	PHY Registers	value in hex
29	DSIPHY_TIMING_CTRL_0	EE
30	DSIPHY_TIMING_CTRL_1	38
31	DSIPHY_TIMING_CTRL_2	26
32	DSIPHY_TIMING_CTRL_3	0
33	DSIPHY_TIMING_CTRL_4	6A
34	DSIPHY_TIMING_CTRL_5	6C
35	DSIPHY_TIMING_CTRL_6	2C
36	DSIPHY_TIMING_CTRL_7	3C
37	DSIPHY_TIMING_CTRL_8	2C
38	DSIPHY_TIMING_CTRL_9	3
39	DSIPHY_TIMING_CTRL_10	4
40		
41	**3. DSI Registers (address)**	
42	DSI_CLKOUT_TIMING_CTRL	22C
43	DSI_TEST_PATTERN_GEN_VIDEO_ENABLE	0
44		
45		

DSI and MDP registers | DSI PHY timing setting | DSI PHY 2.0.0 timing setting

就绪



DSI PHY TIMING REGISTER SETTINGS	
PHY 2.x.x. Registers	**value in hex**
DSIPHY_CKLN_TIMING_CTRL_4	24
DSIPHY_CKLN_TIMING_CTRL_5	1B
DSIPHY_CKLN_TIMING_CTRL_6	8
DSIPHY_CKLN_CFG1.DSIPHY_HSTX_HALFBYTECLK_EN	0
DSIPHY_CKLN_TIMING_CTRL_7	9
DSIPHY_CKLN_TIMING_CTRL_8	5
DSIPHY_DLN[0123]_TIMING_CTRL_4	24
DSIPHY_DLN[0123]_TIMING_CTRL_5	1F
DSIPHY_DLN[0123]_TIMING_CTRL_6	8
DSIPHY_DLN[0123]_TIMING_CTRL_7	9
DSIPHY_DLN[0123]_TIMING_CTRL_8	5
DSIPHY_DLN[0123]_CFG1.DSIPHY_HSTX_HALFBYTECLK_EN	0
DSIPHY_DLN[0123]_TIMING_CTRL_9	3
DSIPHY_DLN[0123]_TIMING_CTRL_10	4
DSIPHY_CKLN_CFG0.DSIPHY_HSTX_PREPARE_DLY	0
DSIPHY_DLN[0123]_CFG0.DSIPHY_HSTX_PREPARE_DLY	0
Clocks	

DSI and MDP registers | DSI PHY timing setting | DSI PHY 2.0.0 timing setting | DSI PH

3. Update the Panel dtsi file “qcom,panel-phy-timingSettings” using the values listed above

obtained from the Excel worksheet.
Below is an example. Values are copied from above.

```
qcom,mdss-dsi-panel-timings = [ee 38 26 00 6a 6c 2c 3c 2c 03 04 00];
qcom,mdss-dsi-panel-timings-phy-v2 = [24 1f 08 09 05 03 04 a0
        24 1f 08 09 05 03 04 a0
        24 1f 08 09 05 03 04 a0
        24 1f 08 09 05 03 04 a0
        24 1b 08 09 05 03 04 a0];
```

Note:the last will always be “a0”.
The driver will then load those values at the D-PHY initial stage.
4. Copy the Program value for T_CLK_POST and T_CLK_PRE fields obtained from the Excel worksheet into the panel dtsi. The values in the Excel worksheet are in decimal. Make sure that they are converted to HEX before updating these two elements.

```
qcom,mdss-dsi-t-clk-post = <0x02>;
qcom,mdss-dsi-t-clk-pre = <0x2c>;
```

2.2.4 Select the panel
After creating the dtsi file, include that panel’s dtsi in the platform device tree and select the panel.
Example:
kernel/ msm-3.18/arch/arm/boot/dts/qcom/$(project).dtsi

```
#include "dsi-panel-nt35532-1080p-video-sim.dtsi"
```

Tell the DSI host to pick the panel. Point “qcom dsi-pref-prim-pan” to the name of the panel included in the panel’s dtsi file.
Example:

```
&mdss_dsi0 {
    qcom,dsi-pref-prim-pan = <&dsi_nt35532_1080p_video>;
    pinctrl-names = "mdss_default", "mdss_sleep";
    pinctrl-0 = <&mdss_dsi_active &mdss_te_active>;
    pinctrl-1 = <&mdss_dsi_suspend &mdss_te_suspend>;
```

3 Little Kernel (LK) Bringup

Once Kernel bringup is done, perform the following steps for little kernel (LK) bringup.
1. Create the panel header file. Do one of the following:
☐ Use the global component database (GCDB)
☐ Refer to one of the existing header files present in bootable/bootloader/lk/dev/gcdb/display/include/ and copy the new file to the same location.

2. After making the header file, include it in
bootable/bootloader/lk/target/msm8953/oem_panel.c and add
<Vendor>_<Resolution>_VIDEO/CMD_PANEL switch case on init_panel_data function.

3. We need to map the below data for your panel from the GCDB header file. Replace the below function pointers with your generated file pointers.

Example:

```
#include "include/panel_nt35532_1080p_video_sim.h"

enum {
	NT35532_1080P_VIDEO_PANEL,
}

static struct panel_list supp_panels[] = {
	{"nt35532_1080p_video", NT35532_1080P_VIDEO_PANEL},
};

		case NT35532_1080P_VIDEO_PANEL:
			panelstruct->paneldata	= &nt35532_1080p_video_panel_data;
			panelstruct->paneldata->panel_with_enable_gpio = 1;
			panelstruct->panelres	= &nt35532_1080p_video_panel_res;
			panelstruct->color	= &nt35532_1080p_video_color;
			panelstruct->videopanel	= &nt35532_1080p_video_video_panel;
			panelstruct->commandpanel = &nt35532_1080p_video_command_panel;
			panelstruct->state	= &nt35532_1080p_video_state;
			panelstruct->laneconfig	= &nt35532_1080p_video_lane_config;
			panelstruct->paneltiminginfo
				= &nt35532_1080p_video_timing_info;
			panelstruct->panelresetseq
					= &nt35532_1080p_video_reset_seq;
			panelstruct->backlightinfo = &nt35532_1080p_video_backlight;
			pinfo->mipi.panel_on_cmds
				= nt35532_1080p_video_on_command;
			pinfo->mipi.num_of_panel_on_cmds
				= NT35532_1080P_VIDEO_ON_COMMAND;
			pinfo->mipi.panel_off_cmds
				= nt35532_1080p_video_off_command;
			pinfo->mipi.num_of_panel_off_cmds
				= NT35532_1080P_VIDEO_OFF_COMMAND;
			memcpy(phy_db->timing,
				nt35532_1080p_14nm_video_timings,	MAX_TIMING_CONFIG	*
sizeof(uint32_t));
```

```
                break;

int lcd_select(void)
{
        //return HX8394F_720P_VIDEO_PANEL;
        return NT35532_1080P_VIDEO_PANEL;
}
```

Contact

Headquarters

Add: Floor 6, Building B, No.633 Jinzhong Road, Changning District, Shanghai P.R.China 200335
Tel: +86 21 3252 3424
Fax: +86 21 3252 3020
Email: simcom@sim.com

Technical Support

EMEA	APAC	America
West Europe we-support@sim.com	**ASEAN** asean-support@sim.com	**North America** us-support@sim.com
East Europe ee-support@sim.com	**Australia and New Zealand** anz-support@sim.com	**Central and South America** la-support@sim.com
Middle East me-support@sim.com	**Big China** China-support@sim.com	
Africa af-support@sim.com		