SIM8950 Series SPI Driver Development Guide Manual_V1.00.01

Smart Module

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Version History

Version	Date	Chapter	What is new
V1.00	2018-09-12		New version
V1.01	2018-09-19	2.1.1	1. SIM8950 Series SPI Driver Development Guide Manual

Contents

This document describes the Serial Peripheral Interface (SPI) and explains how to configure it in the kernel . Through these chapter , you can know to configure SPI.

1 Introduction

1.1 The Inter-Integrated Circuit(I2C) Overview

SPI allows full duplex / half duplex synchronous serial communication between main and slave ports. There is no explicit communication group frame, error checking, or defined data word length.

Main functions:

1. support up to up to 48MHz
2. support the transmission of 4-32 bit word length
3. at most support, there are four chip selection on each bus (CS).
4. support BAM.

2 SPI Configure Process

2.1 Dts Configure

Adding the new SPI bus is relatively simple. The main modification is DTS file, and the driver system is built without changing it.

Base address

BLSP Hardware ID	QUP core	Physical address
BLSP1	BLSP 1 QUP1	0x78B5000
BLSP1	BLSP 1 QUP2	0x78B6000
BLSP1	BLSP 1 QUP3	0x78B7000
BLSP1	BLSP 1 QUP4	0x78B8000
BLSP2	BLSP 2 QUP1	0x7AF5000
BLSP2	BLSP 2 QUP2	0x7AF6000
BLSP2	BLSP 2 QUP3	0x7AF7000
BLSP2	BLSP 2 QUP4	0x7AF8000

SPI core and QUP core shared base address or correct configuration value.

For example, adding a new SPI 3, first look at the hardware schematic diagram that SPI3_MOSI, SPI3_MISO, SPI3_CLK, SPI3_CS corresponding GPIO for GPIO8, GPIO9, GPIO11, GPIO10 are modified steps as follows:

The documents we have to modify：/kernel/msm-3.18/arch/arm/boot/dts/qcom/sim8950-msm8953.dtsi

```
spi_3: spi@78b7000 {    /* BLSP1 QUP3 */
    compatible = "qcom,spi-qup-v2";
    #address-cells = <1>;
    #size-cells = <0>;
    reg-names = "spi_physical", "spi_bam_physical";
    reg = <0x78b7000 0x600>,
          <0x7884000 0x1f000>;
    interrupt-names = "spi_irq", "spi_bam_irq";
    interrupts = <0 97 0>, <0 238 0>;
    spi-max-frequency = <19200000>;
    pinctrl-names = "default", "sleep", "cs_default";
    pinctrl-0 = <&spi3_default &spi3_cs0_active>;
    pinctrl-1 = <&spi3_sleep &spi3_cs0_sleep>;
    clocks = <&clock_gcc clk_gcc_blsp1_ahb_clk>,
             <&clock_gcc clk_gcc_blsp1_qup1_spi_apps_clk>;
    clock-names = "iface_clk", "core_clk";
    qcom,infinite-mode = <0>;
    qcom,use-bam;
    qcom,use-pinctrl;
    qcom,ver-reg-exists;
    qcom,bam-consumer-pipe-index = <8>;
    qcom,bam-producer-pipe-index = <9>;
    qcom,master-id = <86>;
    status = "ok";
  };
```

2.2 GPIO SPI Configure

The documents we have to modify :
/kernel/msm-3.18/arch/arm/boot/dts/qcom/sim8950-msm8953-pinctrl.dtsi

```
spi3 {
    spi3_default: spi3_default {
        /* active state */
        mux {
            /* MOSI, MISO, CLK */
            pins = “gpio8”, “gpio9”, “gpio11”;
            function = “blsp_spi3”;
        };
        config {
            pins=“gpio8”, “gpio9”, “gpio11”;
            drive-strength=<12>;
```

```
                bias-disable = <0>;
            };
        };
    spi3_sleep: spi3_sleep {
        /* suspended state */
        mux {
            /* MOSI, MISO, CLK */
            pins="gpio8", "gpio9", "gpio11";
            function = "gpio";
        };
        config {
            pins="gpio8", "gpio9", "gpio11";
            drive-strength=<2>;
            bias-pull-down;
        };
};

  spi3_cs0_active: cs0_active {
        /* CS */
        mux {
            pins= "gpio10";
            function = "gpio";
        };
        config {
            pins="gpio10";
            drive-strength= <2>;
            bias-disable = <0>;
        };
    };
};
```