256Mb N-die SDRAM Industrial

54TSOP(II) with Lead-Free & Halogen-Free (RoHS compliant)

datasheet

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Revision History

Revision No.	History	Draft Date	Remark	Editor
1.0	- First SPEC. Release	May. 2010	-	S.H.Kim

Table Of Contents

1. KEY FEATURES

- JEDEC standard 3.3V power supply
- LVTTL compatible with multiplexed address
- Four banks operation
- MRS cycle with address key programs
  - -. CAS latency (2 & 3)
  - -. Burst length (1, 2, 4, 8 & Full page)
  - -. Burst type (Sequential & Interleave)
- All inputs are sampled at the positive going edge of the system clock.
- Burst read single-bit write operation
- L(U)DQM (x16) for masking
- Auto & self refresh
- 64ms refresh period (8K Cycle)
- RoHS compliant for Lead-Free and Halogen-Free Package
- Support industrial Temp (-40 to 85 'C)

2. GENERAL DESCRIPTION

The K4S561632N is 268,435,456 bits synchronous high data rate Dynamic RAM organized as 4 x 4,196,304 words by 16bits, fabricated with SAMSUNG's high performance CMOS technology. Synchronous design allows precise cycle control with the use of system clock I/O transactions are possible on every clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

3. ORDERING INFORMATION

Part No.	Orgainization	Max Freq.	Interface	Package
K4S561632N-LI/P60	16M x 16	166MHz (CL=3)	LVTTL	54pin TSOP(II) Lead-Free & Halogen-Free
K4S561632N-LI/P75		133MHz (CL=3)		

[Table 1] Row & Column address configuration

Organization	Row Address	Column Address
16Mx16	A0~A12	A0-A8

4. PACKAGE PHYSICAL DIMENSION

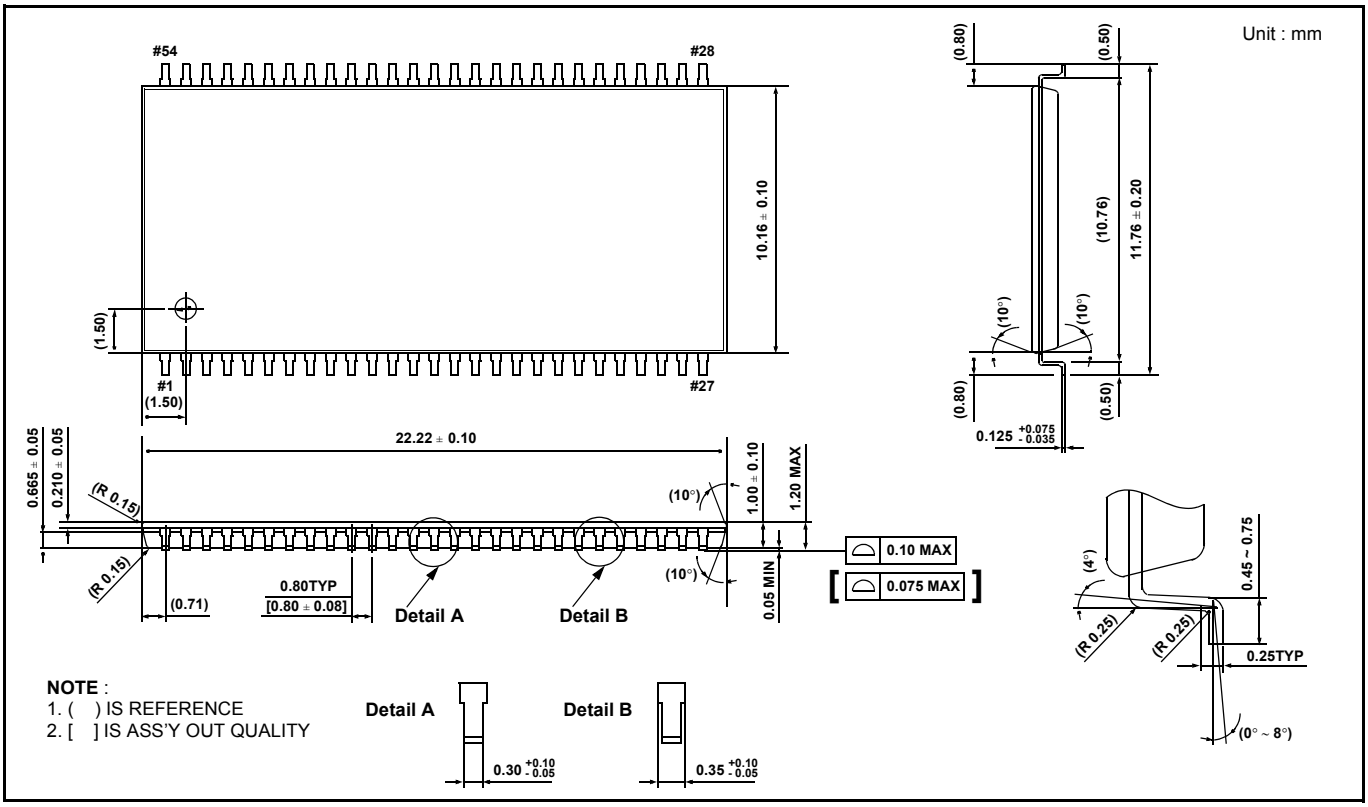
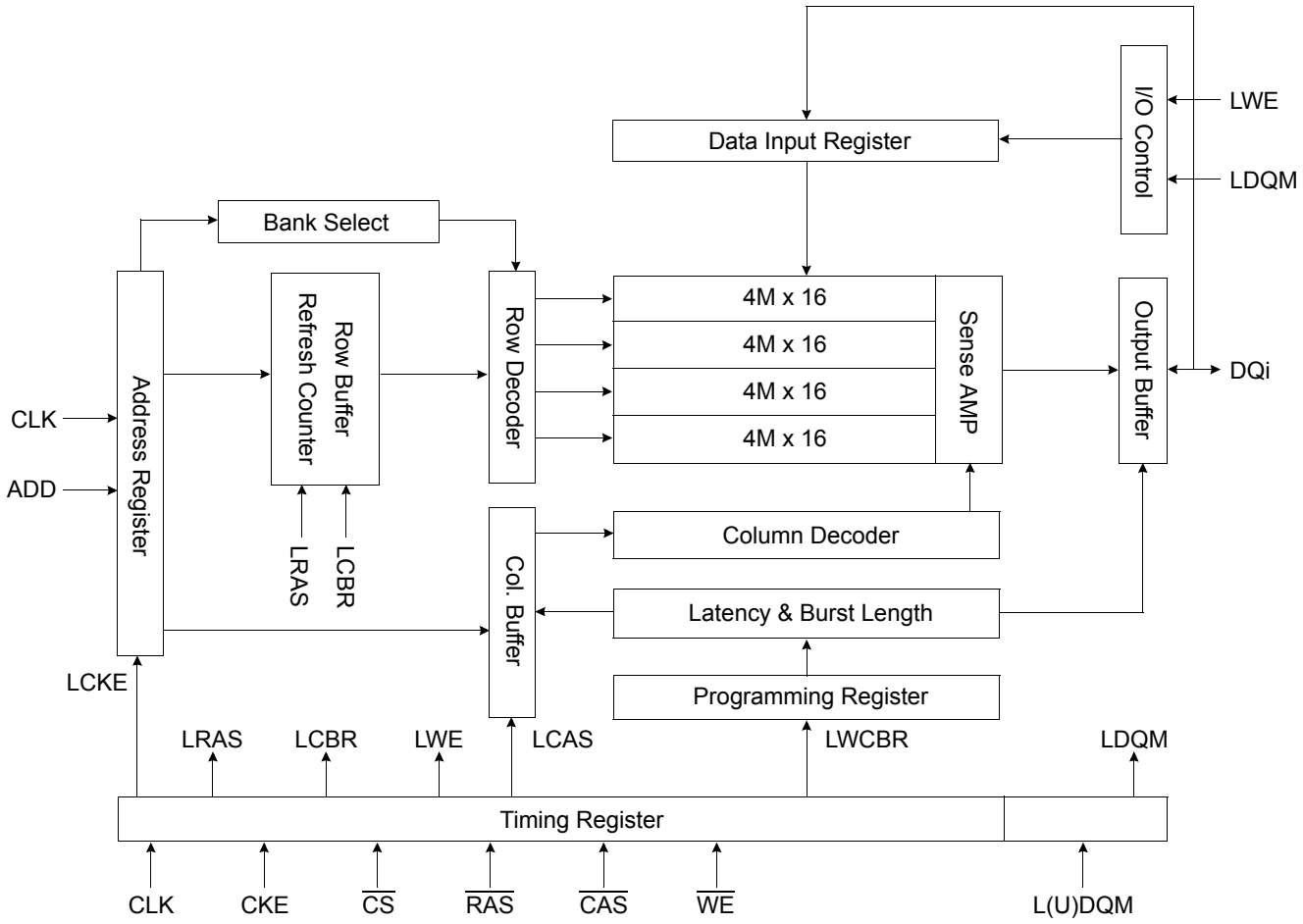


Figure 1. 54Pin TSOP(II) Package Dimension

5. FUNCTIONAL BLOCK DIAGRAM



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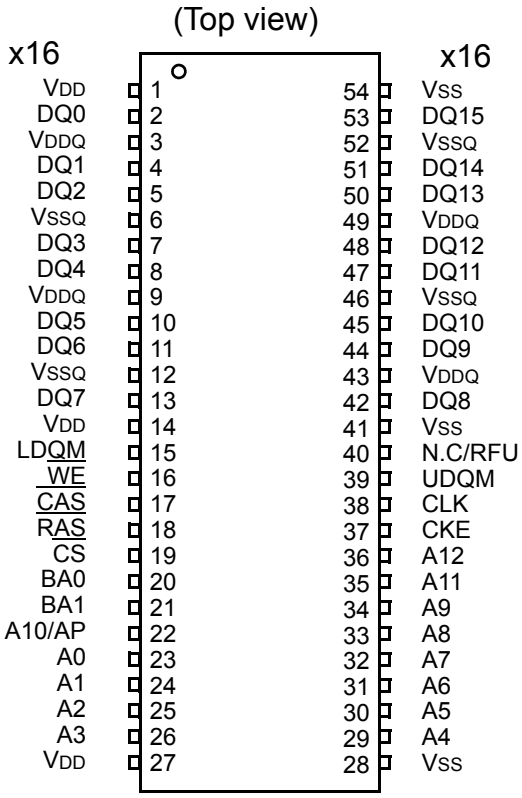
6. PIN CONFIGURATION



54Pin TSOP(II)
(400mil x 875mil)
(0.8 mm Pin pitch)

7. INPUT/OUTPUT FUNCTION DESCRIPTION

Pin	Name	Description
CLK	*System clock*	Active on the positive going edge to sample all inputs.
$\overline{CS}$	*Chip select*	Disables or enables device operation by masking or enabling all inputs except CLK, CKE and DQM
CKE	*Clock enable*	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior to new command. Disable input buffers for power down in standby.
A0 ~ A12	*Address*	Row/column addresses are multiplexed on the same pins. Row address : RA0 ~ RA12, Column address : (x16 : CA0 ~ CA8)
BA0 ~ BA1	*Bank select address*	Selects bank to be activated during row address latch time. Selects bank for read/write during column address latch time.
$\overline{RAS}$	*Row address strobe*	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	*Column address strobe*	Latches column addresses on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	*Write enable*	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQM	*Data input/output mask*	Makes data output Hi-Z, tSHZ after the clock and masks the output. Blocks data input when DQM active.
DQ0 ~ N	*Data input/output*	Data inputs/outputs are multiplexed on the same pins. (x16 : DQ0 ~ 15)
VDD/VSS	*Power supply/ground*	Power and ground for the input buffers and the core logic.
VDDQ/VSSQ	*Data output power/ground*	Isolated power supply and ground for the output buffers to provide improved noise immunity.
N.C/RFU	*No connection /reserved for future use*	This pin is recommended to be left No Connection on the device.

8. ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	VIN, VOUT	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	TSTG	-55 ~ +150	°C
Power dissipation	PD	1	W
Short circuit current	IOS	50	mA

NOTE : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

9. DC OPERATING CONDITIONS

Recommended operating conditions (Voltage referenced to VSS = 0V, TA = -40 to 85°C)

Parameter	Symbol	Min	Typ	Max	Unit	NOTE
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input logic high voltage	VIH	2.0	3.0	VDD+0.3	V	1
Input logic low voltage	VIL	-0.3	0	0.8	V	2
Output logic high voltage	VOH	2.4	-	-	V	IOH = -2mA
Output logic low voltage	VOL	-	-	0.4	V	IOL = 2mA
Input leakage current	ILI	-10	-	10	uA	3

NOTE :
1. VIH (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. VIL (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ VIN ≤ VDDQ.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

10. CAPACITANCE

(VDD = 3.3V, TA = 23°C, f = 1MHz, VREF =1.4V ± 200 mV)

Pin	Symbol	Min	Max	Unit
Clock	CCLK	2.5	3.5	pF
$\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM	CIN	2.5	3.8	pF
Address	CADD	2.5	3.8	pF
x16 : DQ0 ~ DQ15	COUT	4.0	6.0	pF

11. DC CHARACTERISTICS (x16)

(Recommended operating condition unless otherwise noted, TA = -40 to 85°C)

Parameter	Symbol	Test Condition		Version		Unit	NOTE
				60	75		
Operating current (One bank active)	ICC1	Burst length = 1 tRC ≥ tRC(min) IO = 0 mA		45	45	mA	1
Precharge standby current in power-down mode	ICC2P	CKE ≤ VIL(max), tCC = 10ns		2	2	mA	
	ICC2PS	CKE & CLK ≤ VIL(max), tCC = ∞		2	2		
Precharge standby current in non power-down mode	ICC2N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC = 10ns Input signals are changed one time during 20ns		15	15	mA	
Active standby current in power-down mode	ICC3P	CKE ≤ VIL(max), tCC = 10ns		5	5	mA	
	ICC3PS	CKE & CLK ≤ VIL(max), tCC = ∞		5	5		
Active standby current in non power-down mode (One bank active)	ICC3N	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), tCC = 10ns Input signals are changed one time during 20ns		25	25	mA	
	ICC3NS	CKE ≥ VIH(min), CLK ≤ VIL(max), tCC = ∞ Input signals are stable		20	20	mA	
Operating current (Burst mode)	ICC4	IO = 0 mA Page burst		50	50	mA	1
Refresh current	ICC5	tRC ≥ tRC(min)		80	80	mA	2
Self refresh current	ICC6	CKE ≤ 0.2V	I	3	3	mA	3
			P	1.5	1.5	uA	4

NOTE :

1. Measured with outputs open.
2. Refresh period is 64ms.
3. K4S561632N-LI
4. K4S561632N-LP
5. Unless otherwise noted, input swing level is CMOS(VIH /VIL=VDDQ/VSSQ)

12. AC OPERATING TEST CONDITIONS

(VDD = 3.3V ± 0.3V, TA = -40 to 85°C)

Parameter	Value	Unit
Input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	

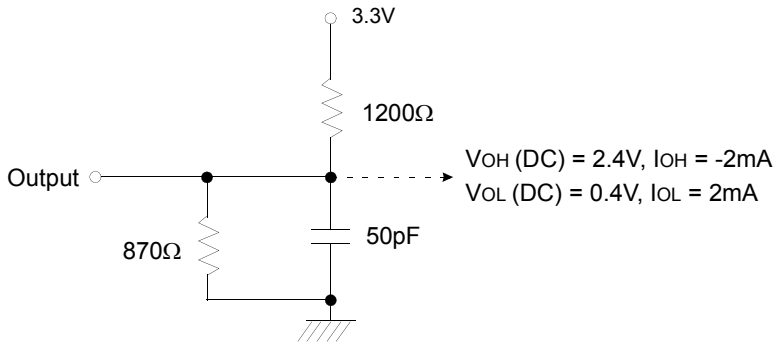


Figure 2. DC output load circuit

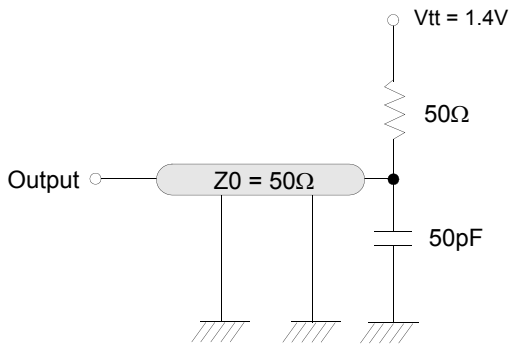


Figure 3. AC output load circuit

13. OPERATING AC PARAMETER

(AC operating conditions unless otherwise noted)

Parameter		Symbol	Version		Unit	NOTE
			60	75		
Row active to row active delay		tRRD(min)	12	15	ns	1
$\overline{RAS}$ to $\overline{CAS}$ delay		tRCD(min)	18	20	ns	1
Row precharge time		tRP(min)	18	20	ns	1
Row active time		tRAS(min)	42	45	ns	1
		tRAS(max)	100		us	
Row cycle time		tRC(min)	60	65	ns	1
Last data in to row precharge		tRDL(min)	2		CLK	2,5
Last data in to Active delay		tDAL(min)	2 CLK + tRP		-	5
Last data in to new col. address delay		tCDL(min)	1		CLK	2
Last data in to burst stop		tBDL(min)	1		CLK	2
Col. address to col. address delay		tCCD(min)	1		CLK	3
Number of valid output data	CAS latency=3		2		ea	4
	CAS latency=2		-	1		

NOTE : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.

2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. In 100MHz and below 100MHz operating conditions, tRDL=1CLK and tDAL=1CLK + 20ns is also supported. SAMSUNG recommends tRDL=2CLK and tDAL=2CLK + tRP.
6. $t_{RC} = t_{RFC}$, $t_{RDL} = t_{WR}$

14. AC CHARACTERISTICS

(AC operating conditions unless otherwise noted)

Parameter		Symbol	60 (x16 only)		75		Unit	NOTE
			Min	Max	Min	Max		
CLK cycle time	CAS latency=3	tCC	6	1000	7.5	1000	ns	1
	CAS latency=2		-		10			
CLK to valid output delay	CAS latency=3	tSAC		5		5.4	ns	1,2
	CAS latency=2			-		6		
Output data hold time	CAS latency=3	tOH	2.5		3		ns	2
	CAS latency=2		-		3			
CLK high pulse width		tCH	2.5		2.5		ns	3
CLK low pulse width		tCL	2.5		2.5		ns	3
Input setup time		tSS	1.5		1.5		ns	3
Input hold time		tSH	1		0.8		ns	3
CLK to output in Low-Z		tSLZ	1		1		ns	2
CLK to output in Hi-Z	CAS latency=3	tSHZ		5		5.4	ns	
	CAS latency=2			-		6		

NOTE : 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
If tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1]ns should be added to the parameter.
4. tSS applies for address setup tiem, clock enable setup time, commend setup tiem and data setup time.
tSH applies for address setup tiem, clock enable setup time, commend setup tiem and data setup time.

15. DQ BUFFER OUTPUT DRIVE CHARACTERISTICS

Parameter	Symbol	Condition	Min	Typ	Max	Unit	NOTE
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	1.37		4.37	Volts/ns	3
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	1.30		3.8	Volts/ns	3
Output rise time	trh	Measure in linear region : 1.2V ~ 1.8V	2.8	3.9	5.6	Volts/ns	1,2
Output fall time	tfh	Measure in linear region : 1.2V ~ 1.8V	2.0	2.9	5.0	Volts/ns	1,2

NOTE : 1. Rise time specification based on 0pF + 50 Ω to VSS, use these values to design to.
2. Fall time specification based on 0pF + 50 Ω to VDD, use these values to design to.
3. Measured into 50pF only, use these values to characterize to.
4. All measurements done with respect to VSS.

16. IBIS SPECIFICATION

[Table 2] IOH Characteristics (Pull-up)

Voltage	166MHz 133MHz Min	166MHz 133MHz Max
(V)	I (mA)	I (mA)
3.45		-2.4
3.3		-27.3
3.0	0.0	-74.1
2.6	-21.1	-129.2
2.4	-34.1	-153.3
2.0	-58.7	-197.0
1.8	-67.3	-226.2
1.65	-73.0	-248.0
1.5	-77.9	-269.7
1.4	-80.8	-284.3
1.0	-88.6	-344.5
0.0	-93.0	-502.4

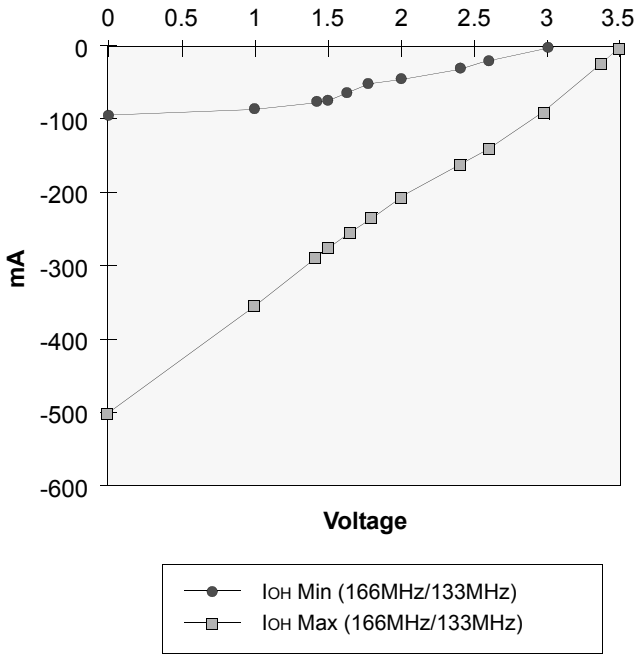


Figure 4. 166MHz/133MHz Pull-up

[Table 3] IOL Characteristics (Pull-down)

Voltage	166MHz 133MHz Min	166MHz 133MHz Max
(V)	I (mA)	I (mA)
0.0	0.0	0.0
0.4	27.5	70.2
0.65	41.8	107.5
0.85	51.6	133.8
1.0	58.0	151.2
1.4	70.7	187.7
1.5	72.9	194.4
1.65	75.4	202.5
1.8	77.0	208.6
1.95	77.6	212.0
3.0	80.3	219.6
3.45	81.4	222.6

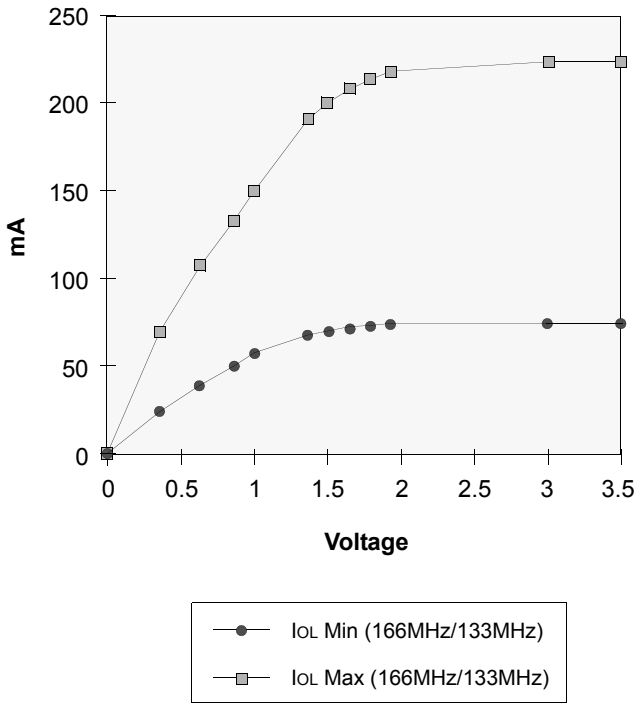


Figure 5. 166MHz/133MHz Pull-down

[Table 4] V_{DD} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

V_{DD} (V)	I (mA)
0.0	0.0
0.2	0.0
0.4	0.0
0.6	0.0
0.7	0.0
0.8	0.0
0.9	0.0
1.0	0.23
1.2	1.34
1.4	3.02
1.6	5.06
1.8	7.35
2.0	9.83
2.2	12.48
2.4	15.30
2.6	18.31

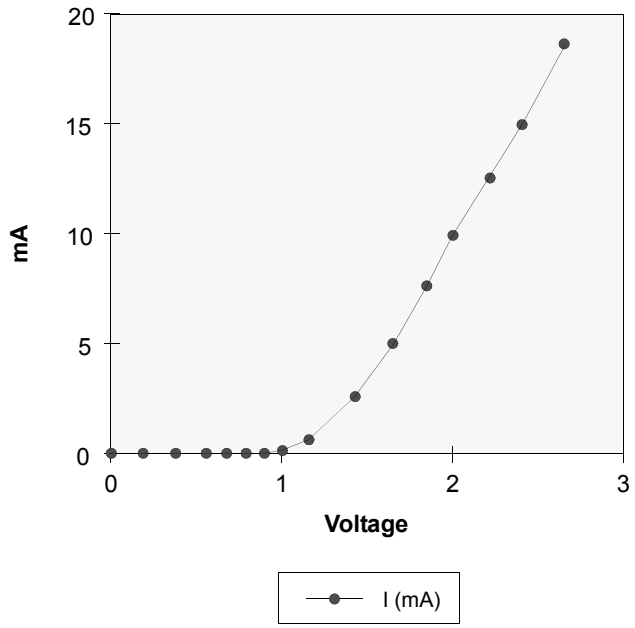


Figure 6. Minimum V_{DD} clamp current (Referenced to V_{DD})

[Table 5] V_{SS} Clamp @ CLK, CKE, $\overline{CS}$, DQM & DQ

V_{SS} (V)	I (mA)
-2.6	-57.23
-2.4	-45.77
-2.2	-38.26
-2.0	-31.22
-1.8	-24.58
-1.6	-18.37
-1.4	-12.56
-1.2	-7.57
-1.0	-3.37
-0.9	-1.75
-0.8	-0.58
-0.7	-0.05
-0.6	0.0
-0.4	0.0
-0.2	0.0
0.0	0.0

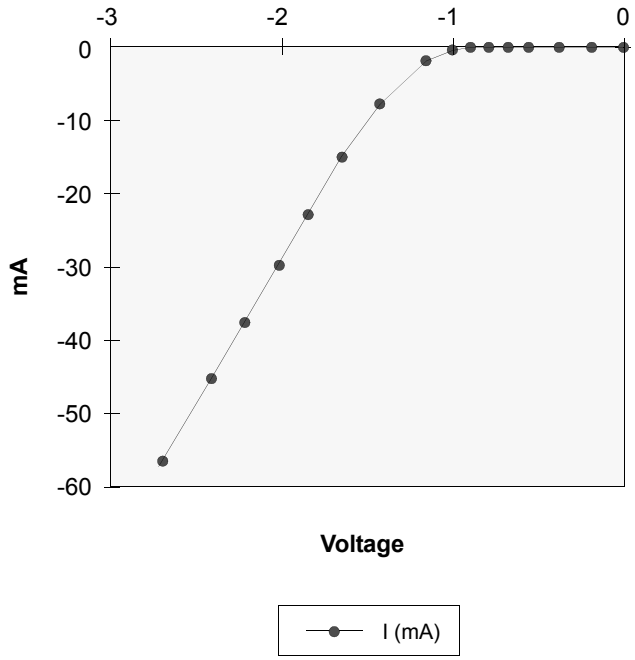


Figure 7. Minimum V_{SS} clamp current

17. SIMPLIFIED TRUTH TABLE

(V=Valid, X=Don't care, H=Logic high, L=Logic low)

Command			CKEn-1	CKEn	$\overline{CS}$	$\overline{RAS}$	$\overline{CAS}$	$\overline{WE}$	DQM	BA0,1	A10/AP	A0 ~ A9, A11,	NOTE
Register	Mode register set		H	X	L	L	L	L	X	OP code			1,2
Refresh	Auto refresh		H	H	L	L	L	H	X	X			3
	Self refresh	Entry		L									3
		Exit	L	H	L	H	H	H	X	X			3
					H	X	X	X					3
Bank active & row addr.			H	X	L	L	H	H	X	V	Row address		
Read & column address	Auto precharge disable		H	X	L	H	L	H	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Write & column address	Auto precharge disable		H	X	L	H	L	L	X	V	L	Column address	4
	Auto precharge enable										H		4,5
Burst stop			H	X	L	H	H	L	X	X			6
Precharge	Bank selection		H	X	L	L	H	L	X	V	L	X	
	All banks									X	H		
Clock suspend or active power down		Entry	H	L	H	X	X	X	X	X			
					L	V	V	V					
		Exit	L	H	X	X	X	X	X				
Precharge power down mode		Entry	H	L	H	X	X	X	X	X			
					L	H	H	H					
		Exit	L	H	H	X	X	X	X				
					L	V	V	V					
DQM			H	X					V	X			7
No operation command			H	X	H	X	X	X	X	X			
					L	H	H	H					

NOTE :

1. OP Code : Operand code
   A0 ~ A11 & BA0 ~ BA1 : Program keys. (@ MRS)
2. MRS can be issued only at all banks precharge state.
   A new command can be issued after 2 CLK cycles of MRS.
3. Auto refresh functions are as same as CBR refresh of DRAM.
   The automatical precharge without row precharge command is meant by "Auto".
   Auto/self refresh can be issued only at all banks precharge state.
4. BA0 ~ BA1 : Bank select addresses.
   If both BA0 and BA1 are "Low" at read, write, row active and precharge, bank A is selected.
   If BA0 is "High" and BA1 is "Low" at read, write, row active and precharge, bank B is selected.
   If BA0 is "Low" and BA1 is "High" at read, write, row active and precharge, bank C is selected.
   If both BA0 and BA1 are "High" at read, write, row active and precharge, bank D is selected.
   If A10/AP is "High" at row precharge, BA0 and BA1 is ignored and all banks are selected.
5. During burst read or write with auto precharge, new read/write command can not be issued.
   Another bank read/write command can be issued after the end of burst.
   New row active of the associated bank can be issued at tRP after the end of burst.
6. Burst stop command is valid at every burst length.
7. DQM sampled at positive going edge of a CLK and masks the data-in at the very CLK (Write DQM latency is 0),
   but makes Hi-Z state the data-out of 2 CLK cycles after. (Read DQM latency is 2)